DEPARTMENT OF COMPUTER SCIENCE
COLORADO SCHOOL OF MINES
EARTH • ENERGY • ENVIRONMENT

CSCI 341 Computer Organization
Final Exam Fall 2020

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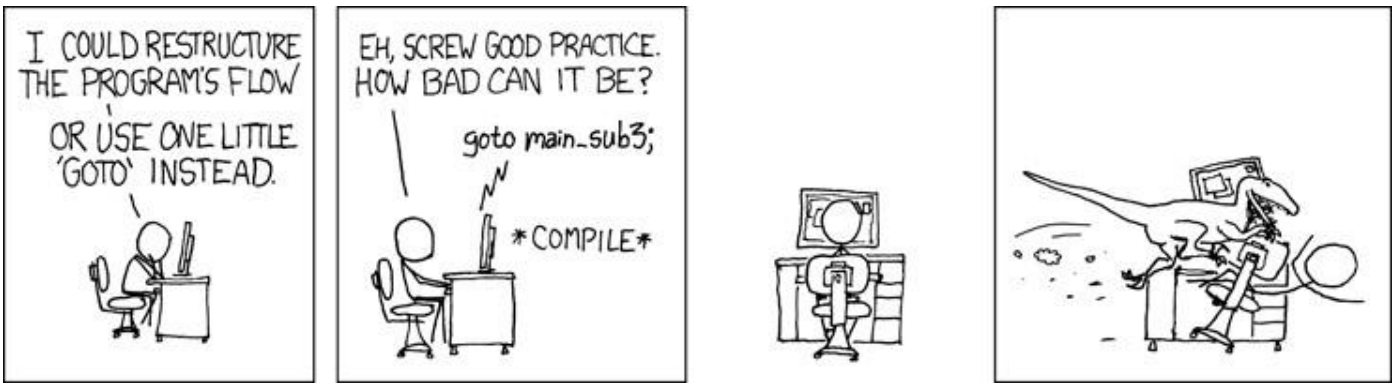
Print or type your name clearly on the line above, using your Canvas public name or gradebook name



Part 1: This part of the exam has 12 questions and each question is worth 4 points each. This section consists of **multiple-choice (MC)**. Answers to MC questions must be **supported with a concise, complete, and accurate justification to get full credit**. The file you upload should clearly indicate your selection. Do not expect us to draw conclusions. Loopholes will not get you credit; correct but low-quality/unexplained answers will get 1 point.

1. (12 points) Computer Arithmetic

   i. Convert the decimal value -53 to a 7-bit two's complement value. Show the conversion steps for credit.

   a. 0110101

   b. 1001011

   c. 1001010

   d. 1001100

   53 in binary = 0110101

   -53 = 1001010

   1001010 +1 = 1001011

   ii. If you were designing a 12-bit floating point representation using the IEEE 754 floating point standard as a model, and assigned 6 bits to the exponent, what would the bias value be? Explain your answer.

   a. -32

   b. 15

   c. 31

   d. -63

   Bias value = $2^6 - 1 = 63$

   iii. Explain your answer. Assume $t0 is loaded with 0XFFFF FF42.

   `addi $t0, $t0,0XA424` will result in an overflow (the value will not fit in $t0).

   a. True b. False

   This will result in overflow because the addition of the A to the F will make it take up one more value so it will no longer fit within 8 values.

2. (12 points) Assembly and Machine Language

i. If we have the instruction j Loop at PC 0xAB01 FFFF AB01 1044 and Loop is located at PC 0xAC00 FFFF AB02 AB00, what value is placed in the 26-bit immediate field of the instruction? Explain your answer/show your work.

a) A valid j instruction cannot be generated.

b) 0x300 3FFF EAc0 AAC0

c) 0xC00 FFFF AB01 1044

d) 0x0FF 0000 0001 9AB8

e) 0x0FF 0000 0001 9ABC

0xac00 -0xab01- = 0x0FF

FFFF – FFFF = 0000

AB02-AB01 = 0001

AB00-1044 = 9ABC

= 0x0FF 0000 0001 9ABC

ii. Explain your answer. The current address in $sp is 0x7546 FFB8. Once three 32-bit words are popped off the stack, the $sp should be adjusted to:

a. 0x7546 FFAC b. 0c7546 FFC0 c. 0x7546 FFA6 d. 0x7546 FFC4

Each word takes up 4 bits of address. Remove 12 from address when popping off 3 word from the stack.

0xF546 FFB8 – 12 = 0xF546 FFAC

iii. Explain your answer. Consider the instruction, `lbu $t0, 1($t1)`. Assume the value in register $t1 is 0x1000 0000. Assume that the data at stored at address 0x1000 0000 in memory is 0xAA22 BB44. What value is put in register $t0?

a. 0x0022 0000 b. 0xFFFF FFAA c. 0x0000 0022 d.0xFFFF FFBB e. 0x0000 00BB

0xAA22 BB44 stored as 0xAA 0x22 0xBB 0x44. Starting at address 0x1000 0000 0xAA is stored at 0x10000000 offset of 1 moves to 0x22.

3. (12 points) CPU Data Path

i. Show steps / explain your answer. A compiler generates two different sequences of instructions for the same program to be run on the same CPU. Sequence 1 uses 68 instructions with an average CPI of 2. Sequence 2 uses 51 instructions with an average CPI of 3. Which one of the following is most likely true?

a. Sequence 1 has a better performance

b. Sequence 2 has a better performance

c. Sequence 1 and 2 have the same performance

CPU = instruction count * CPI*clock cycle time

1 – 136*clock cycle time

2- 153*clock cycle time 1 has shorter time is clock cycle time is the same for both

ii. Explain your answer. Consider the following sequence of instruction: `lw $s3, 56($s0) add $t3, $t2, $t1 sw $t1, 72 ($t2)`

The status of "RegWrite" in CC6 from the MEM/WB pipeline register will be:

a. 0 b. 1 c. X (Don't care) d. RegWrite is 2 bits long

The status of RegWrite will be 1 since is writing back to the register.

iii. Explain your answer. Consider our final 5-cycle pipelined MIPS implementation. The operation times for the major functional units are given below; assume all other elements are 0ns. What should the clock cycle time be?

Reading instruction memory	210 ns
Reading register file / Control Unit	150 ns
ALU operation/Adders	100 ns
Data Memory Access	180 ns
Register write	120 ns

a. 210 ns b. 120 ns c. 150 ns d. 250 ns e. 760 ns

210 + 200+180+120+100 = 760

The clock cycle time is determined by the critical path and all of these functional units are critical, so their times are being added to find the clock cycle time.

4. (12 points) Memory Hierarchy

i. Explain your answer. If they have the same block size, which is larger, an 8-way associative cache with 16 sets, or a 16-way associative cache with 8 sets?

a. 8-way with 16 sets b. 16-way with 8 sets c. they are the same size

8-way with 16 sets = 8*16 = 128 blocks total

16-way with 8 sets = 16*8 = 128 blocks total

If the block are the same size they are just divided up in different ways so they will end up being the same size in the end.

ii. Explain your answer. With 32-bit addresses, byte addressing, and a 4KB page size, how many bits of an address are used for the virtual page number?

a. need more information b. 16 bits c. 20 bits d. 12 bits

32 total bits, 12 bits for the offset with 4KB page size

32-12 = 20

iii. If we have a base CPI of 1, a TLB hit & L1 cache hit together can resolve a memory reference in 1 CC, and we have the following miss rates and access times, what is the resulting effective CPI? Show your work/explain your selection.

Memory type	Miss rate	Access Time
TLB	1%	0.5 CC
Page Table	0.25%	10 CC
Disk		1000 CC
L1 Cache	10%	0.5CC
Main Memory		10CC

a. 27.1 CPI b. 4.6 CPI c. 5.5 CPI d. none of these

1 + 0.01*1000 + 0.1*10 = 12

Part 2 – Free Response Questions – work must be shown / partial credit may be assigned

1. (10 points) You are developing a 11-bit floating point representation so that it can be stored in 16 bits with SEC/DED coding to validate its correctness. You choose to have a 5 bit exponent and a 5 bit fraction, and to apply IEEE 754 to determine bias, normalized, denormalized, and special values.

   a. Given the value $-1.792*10^3$ what would the 11-bit floating point value be in binary?

   1792 = 11100000000 * 2^0

   = 1.11 *2^{10}

   Exponent = 10 + 5 = 15 = 01111

   Sign bit = 1

   1 01111 11000

   b. In binary, what is the 16-bit value with SEC/DED coding added to that value?

   c. What does the following 16-bit SEC/DED encoded 11-bit floating point value represent, in decimal? If it is invalid, correct it if possible and then convert it to decimal; if not possible to correct, explain why. Value: 0xDEC0

2. (10 points) You are testing the execution time of a program on three different MIPS implementations. The data segment of your program is 32800 bits in size while the program text segment is 5120 bits. Your program is comprised of 30% math/logic instructions, 35% of lw instructions and 35% of sw instructions. There are no data dependencies between instructions.

   This program is run on three different implementations: non-pipelined single cycle, nonpipelined multi-cycle, and pipelined. In a non-pipelined multi-cycle processor, instructions omit stages if they are not required to complete execution. So, instructions take only as many clock cycles as needed to complete the instruction.

   All processors have the same hardware with the following execution times for each stage:

IF	ID	EXE	MEM	WB
70 ns	100 ns	180 ns	250 ns	150 ns

   For each processor, calculate Tc and the average CPI for the program. Show all steps and complete the table below.

Processor Type	CPI	T_c
Single-Cycle		
Multi-Cycle		
Pipelined		

3. (12 points) Evaluate whether an 8-entry TLB would be better as fully associative vs. a 4-way associative on the given series of memory accesses, given the initial contents of the cache. Assume all entries are valid, and that they appear in LRU order, i.e. entry 0 is least recently used). The system uses byte addressing, 32-bit addresses and a 16KB page size.

   A TLB hit on the fully associative cache takes 2 clock cycles to resolve, while it can be resolved in 1 clock cycle on the 4-way associative cache; on the other hand, a TLB miss on either cache takes an average of 4 clock cycles to resolve.

   Assume that the page table and L1 cache performance remains the same in both scenarios.

Tag (FA)
0xA
0x8
0x1
0xD
0x4
0x3
0xE
0x7

Tag (4-way)
0x5
0x4
0x2
0x7
0x0
0x6
0x1
0x3

   Memory accesses: 0x0EDE2, 0x2AFF8, 0x3E75E, 0x1EA83, 0x074B4

   0x0EDE2 = 11~~10110111100010 =~~ 0x3

   0x2AFF8 = 1010~~10111111111000~~ = 0xA

   0x3E75E = 1111~~10011101011110 =~~ 0xF

   0x1EA83 = 111~~10101010000011~~ = 0x7

   0x074B4 = 1~~11010010110100 =~~ 0x1

FA = 2(Hit) +2(Hit) + 4(Miss) + 2(hit) + 2(Hit) = 12

4-way = 1(Hit) +4(Miss) + 4(Miss) + 1(hit) + 1(Hit) = 11

4-way associative TLB would be the better TLB since the number clock cycles to resolve for all memory accesses is shorter than for the fully associative TLB.