ST7703 Data Sheet

TFT Mobile Single Chip Driver
For 720RGB x 1600 dot, a-Si TFT LCD, 16.7M color
With MIPI Interface

Version 2.0 Preliminary
July 2020

List of Contents

List of Figures

List of Tables

Revision History

Version	Date	Description of Changes
1.0	2015/10/05	1. New setup
	2016/09/19	1. P189 Modify Using External Power IC Application
	2016/11/29	1. P62 Modify 04h Register ID1、ID2、ID3
	2017/04/20	1. P154 Add CBh Register.
	2017/07/18	1. Update C6h Register.
	2017/08/25	1. Update P154 VGH Detected Voltage
	2017/09/20	1. Update P13 DUMMY Pad Connection
	2018/01/03	1. Update EAh EQ_Delay Spec.
	2018/03/27	1. Update B2h Max. Gate Number
	2018/03/28	1. Update P181 Standby Mode Current Consumption
1.1	2018/03/30	1. Update B2h Max. Gate Number
1.2	2018/04/26	1. Update P197 Power On Timing of 3 Power Mode
1.3	2018/08/07	1. Update P146 BCh VDDD Voltage Selection
1.3	2018/08/27	1. Update P149 VBTLS[3:0] Voltage 2. Remove Temperature Sensor Function
2.0	2018/10/22	1. Update CABC 8bit~12bit Function (51h/52h/5Eh/5Fh/B1h)
	2018/11/28	1. Update P153 C6h (Default Value) 2. Updaty P161 E0h (Default Value)
	2018/12/04	1. Update P195 Power Off Timing of 3-Power Mode
	2018/12/27	1. Update P193 Power Off Timing (IOVCC T20) 2. Update P195 Power Off Timing (IOVCC T23)
	2019/02/20	1. Update P102 51h (Brightness Ratio) 2. Update P155 C7h (HOUT_OE)
	2019/04/09	1. Update Max. GIP Gate Number
	2019/05/13	1. Update P131 B1h 2. Update P132 B2h Gate Number Calculation
	2019/09/11	1. Update P14 BOM of 3 Power Mode
	2020/02/12	1. Update P194 Power On Timing of 3-Power Mode
	2020/07/02	1. Update P168 E9h PANELI_SEL[3:0]

1. General Description

The ST7703 is a single-chip solution for a-Si TFT LCD that combines a source driver, power supply circuit to drive a-Si TFT dot matrix LCD with 720RGBx1600 dots at maximum. The ST7703 supports MIPI Interface.

The ST7703 incorporates step-up and voltage follower circuits to generate drive voltage required for a-Si TFT and gate in panel (GIP) which including a dynamic backlight control function to control backlight brightness depending on image data, reducing power consumption at the backlight with the slightest influence on image quality.

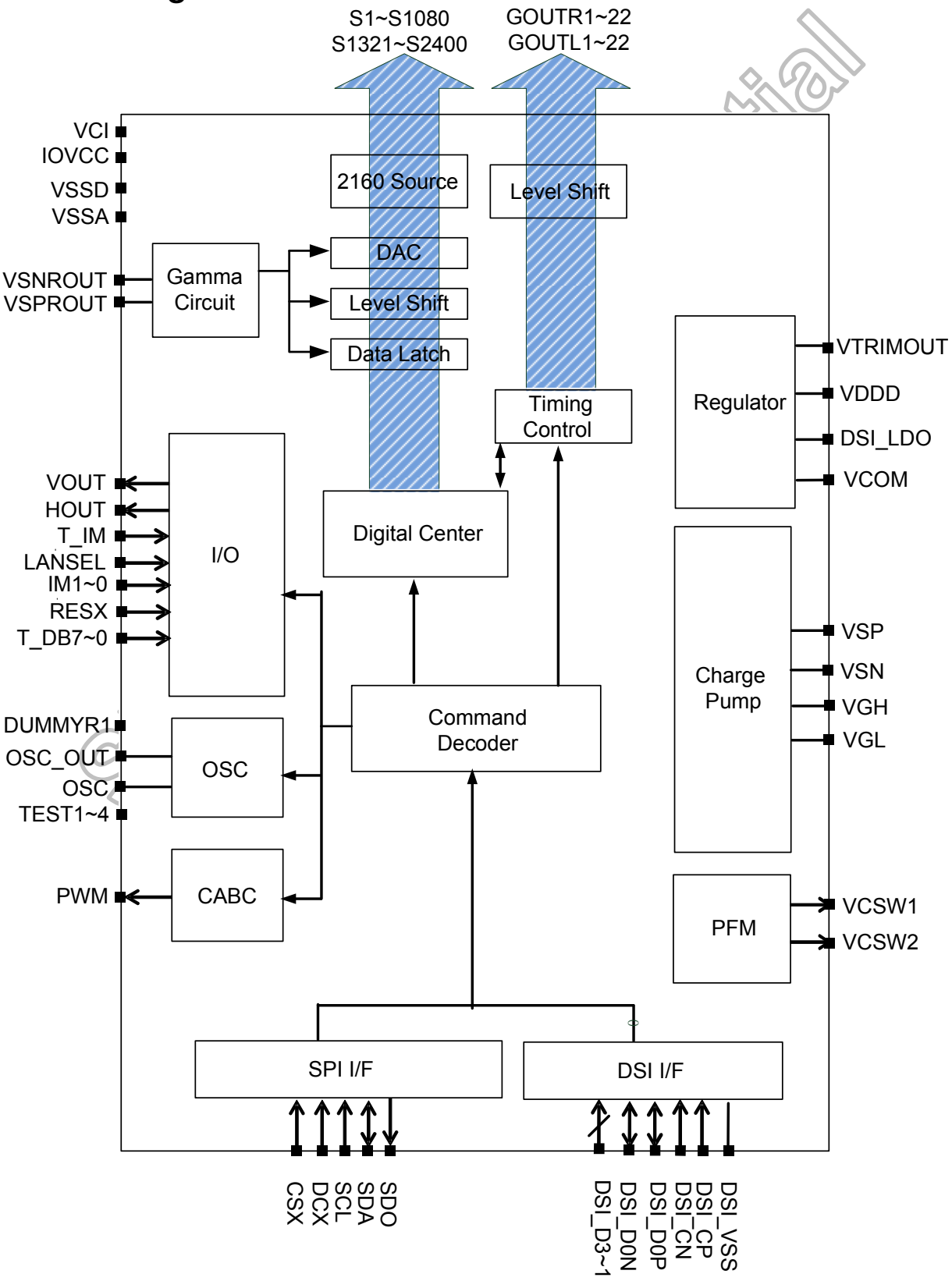
The ST7703 is suitable for small or medium-sized portable mobile solutions requiring long-term driving capabilities, such as digital mobile phones, PDAs and Smartphones.

2. Features

- Single chip solution for a HD720 GIP (Gate In Panel) type TFT LCD display
- Display Resolution：
  - 720RGB x (480 + 4xNL + RES_V_LSB)
  - 640RGB x (480 + 4xNL + RES_V_LSB)
  - 600RGB x (480 + 4xNL + RES_V_LSB)
  - 540RGB x (480 + 4xNL + RES_V_LSB)
- Display Color Modes：
  - Full color mode: 16.7M colors
  - Reduce color mode: 262k colors
  - Reduce color mode: 65k colors
  - Idle mode: 8 colors
- Display Interface：
  - MIPI Display Serial Interface (DSI V1.01)
- On chip：
  - VGH/VGL for GIP gate control
  - 1-dot / 1+2-dot / 2-dot / 3-dot / 4-dot / 8-dot / column / Zig-Zag inversion
  - Gamma correction function
  - Oscillator for display clock generation
  - Internal OTP programming voltage generator
  - 4 times MTP for VCOM setting、ID setting
  - CABC (Content Adaptive Brightness Control) function
  - DGC (Digital Gamma Correction) function
  - Color Enhancement function
- Input power：

  - External power IC and PFM：
    - I/O and interface power supply (IOVCC)：1.65V to 2.0V
    - Analog power supply (VCI)：2.5V to 3.3V
  - Three-Power Mode：
    - I/O and interface power supply (IOVCC)：1.65V to 2.0V
    - Analog power supply (VSP)：4.5V to 6.0V
    - Analog power supply (VSN)：-4.5V to -6.0V
- Output voltage：
  - Positive source output voltage level: VSPR=3.3V to 5.6V
  - Negative source output voltage level: VSNR=-5.6V to -3.3V
  - Positive gate driver output voltage level: VGH=+10V to +20V
  - Negative gate driver output voltage level: VGL=-7.5V to -15V
  - VCOM=-3.5V to 0V

3. Block Diagram



4. Pin Description

4.1 Power Supply Pins

Symbol	Name	Description	Connection when not used
IOVCC	I/O Power	Power supply for logic circuit.	-
VCI	Analog Power	Power supply for analog circuit.	-
VSSA	Analog GND	System ground for analog system.	-
VSSD	I/O GND	System ground for logic circuit.	-
DSI_VSS	MIPI GND	DSI interface analog ground.	-

4.2 Interface Logic Pins

Symbol	I/O	Description	Connection when not used
IM1~0 LANSEL	I	Interface mode select pins. IM1~IM0 and LANSEL are used for the combination of polarity swap and data lane swap of DSI.	GND
RESX	I	Reset pin. This signal will reset the device and must be applied to properly initialize the chip.	-
VOUT	O	Frame synchronization output signal pin.	OPEN
HOUT	O	Scan line synchronization output signal pin.	OPEN

IM1	IM0	LANSEL	D0P/N	D1P/N	CP/N	D2P/N	D3/PN
0	0	0	D3P/N	D2P/N	CP/N	D1P/N	D0P/N
0	1	0	D3N/P	D2N/P	CN/P	D1N/P	D0N/P
1	0	0	D0P/N	D1P/N	CP/N	D2P/N	D3P/N
1	1	0	D0N/P	D1N/P	CN/P	D2N/P	D3N/P
0	0	1	D2P/N	D1P/N	CP/N	D0P/N	D3P/N
0	1	1	D2N/P	D1N/P	CN/P	D0N/P	D3N/P
1	0	1	D3P/N	D0P/N	CP/N	D1P/N	D2P/N
1	1	1	D3N/P	D0N/P	CN/P	D1N/P	D2N/P

Note: "1" = IOVCC Level、"0" = VSSD Level.

4.3 MIPI Interface Pins

Symbol	I/O	Description	Connection when not used
DSI_D0P, DSI_D0P	I/O	High speed interface data differential signal input/output pins.	OPEN/GND
DSI_CP, DSI_CN	I	High speed interface clock differential signal input pins.	OPEN/GND
DSI_D3P~1P, DSI_D3N~1N	I	High speed interface data differential signal input pins.	OPEN/GND

4.4 Driver Output Pins

Symbol	I/O	Description	Connection when not used
S1 to S1080 S1321 to S2400	O	Pixel electrode driving output Display Resolution / Used Source Pins 720RGB: S1~S1080 and S1321~S2400 640RGB: S1~S960 and S1441~S2400 600RGB: S1~S900 and S1501~S2400 540RGB: S1~S810 and S1591~S2400	Open
CGOUTL_1~22 CGOUTR_1~22	O	Gate control signals for panel.	Open
VCOM	O	Regulator output for common voltage of panel	-

4.5 DC/DC Converter Pins

Symbol	I/O	Description	Connection when not used
VSP	I	Input voltage from the set-up circuit.	-
VSN	I	Input voltage from the set-up circuit.	-
VGH	O	Output voltage from the step-up circuit.	-
VGL	O	Output voltage from the step-up circuit.	-
DSI_LDO	O	High speed interface regulator output pin.	Open
VSPROUT	O	Output voltage generated from VSP. Output for positive gamma voltage generator.	-
VSNROUT	O	Output voltage generated from VSN. Output for negative gamma voltage generator.	-
VDDD	O	Reference voltage for internal logic.	-
VTRIMOUT	O	Reference voltage for internal voltage generating circuit.	-
VCSW1	O	PFM and Power IC control output for DC/DC converter to generate VSP.	-
VCSW2	O	PFM and Power IC control output for DC/DC converter to generate VSN.	-

4.6 CABC Control Pins

Symbol	I/O	Description	Connection when not used
PWM	O	This pin is connecting with the external LED driver.	Open

4.7 Test Pins

Symbol	I/O	Description	Connection when not used
OSC	I	Oscillator test pin	Open
CSX	I	Chip select input pin (“Low” enable) in RGB I/F test mode.	OPEN
DCX	I	Command/parameter selection in RGB I/F test mode. Low: Select command. High: Select data.	IOVCC/GND/ OPEN
SCL	I	A synchronous clock signals in RGB I/F test mode.	IOVCC/GND/ OPEN
SDA	I/O	Serial data input/output pin in RGB I/F test mode.	IOVCC/GND/ OPEN
SDO	O	A serial data output pin in RGB I/F test mode.	OPEN
T_DB7~0	I	8-bit input data bus in RGB I/F test mode.	IOVCC/GND/ OPEN
T_IM	I	Let driver IC into RGB I/F test mode if set T_IM= high.	Open
OSC_OUT	O	Test pin.	Open
NVDDDOUT	O	Test pin.	Open
NVTRIMOUT	O	Test pin.	Open
VREFOUT	O	Test pin.	Open
NVREFOUT	O	Test pin.	Open
VTESTOUTP	O	Test pin.	Open
VTESTOUTN	O	Test pin.	Open
DUMMYR1	-	Test pin for bonding quality test. They are short-circuited within the chip.	IOVCC/GND/ OPEN
DUMMY406~1	-	Not used.	IOVCC/GND/ OPEN
DUMMY_PM0 DUMMY_PM1	-	No use.	IOVCC/GND/ OPEN
DUMMY_RS0 DUMMY_RS1	-	No use.	IOVCC/GND/ OPEN
DUMMY_TEMP	-	No use.	IOVCC/GND/ OPEN

Note: “1” = IOVCC Level、“0” = VSSD Level.
Note: “X” = Don’t care.

4.8 BOM

Power IC Mode

NO.	IC Pin Name	Capacitance (uF)	Permissible Voltage (V)	Note
1	VCI	-	-	Don't need Capacitance
2	IOVCC	-	-	Don't need Capacitance
3	VSP	2.2	10	-
4	VSN	2.2	10	-
5	VGH	-	-	Don't need Capacitance
6	VGL	-	-	Don't need Capacitance
7	VSPROUT	-	-	Don't need Capacitance
8	VSNROUT	-	-	Don't need Capacitance
9	VTRIMOUT	-	-	Don't need Capacitance
10	VDDD	-	-	Don't need Capacitance
11	DSI_LDO	-	-	Don't need Capacitance
12	VCOM	-	-	Don't need Capacitance

Table 4-1: BOM of Power IC Mode

3 Power Mode

NO.	IC Pin Name	Capacitance (uF)	Permissible Voltage (V)	Note
1	VCI	-	-	Don't need Capacitance
2	IOVCC	-	-	Don't need Capacitance
3	VSP	-	-	FPC 建議預留
4	VSN	-	-	FPC 建議預留
5	VGH	-	-	Don't need Capacitance
6	VGL	-	-	Don't need Capacitance
7	VSPROUT	-	-	Don't need Capacitance
8	VSNROUT	-	-	Don't need Capacitance
9	VTRIMOUT	-	-	Don't need Capacitance
10	VDDD	-	-	Don't need Capacitance
11	DSI_LDO	-	-	Don't need Capacitance
12	VCOM	-	-	Don't need Capacitance

Table 4-2: BOM of 3 Power Mode

5. Function Description

5.1 SPI Interface

The selection of serial interface is by T_IM. ST7703 can support DPI/DBI type-C Option 1.

T_IM	Interface mode
0	MIPI Interface
1	DPI/DBI type-C Option 1 (9-bit SPI)

Table 5.1: DBI TYPE-C Serial Interface Selection Table

The serial interface is used to communication between the MPU and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDA (serial data input/output). Serial clock (SCL) can be stopped when no communication is necessary.

5.1.1 SPI Interface Write Mode

In SPI I/F Write Mode, the serial data packet contains a control bit DCX and a transmission byte If DCX is low, the transmission byte is command byte. If DCX is high, the transmission byte is stored in to command register. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or serial input/output data (SDA/SDO) have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

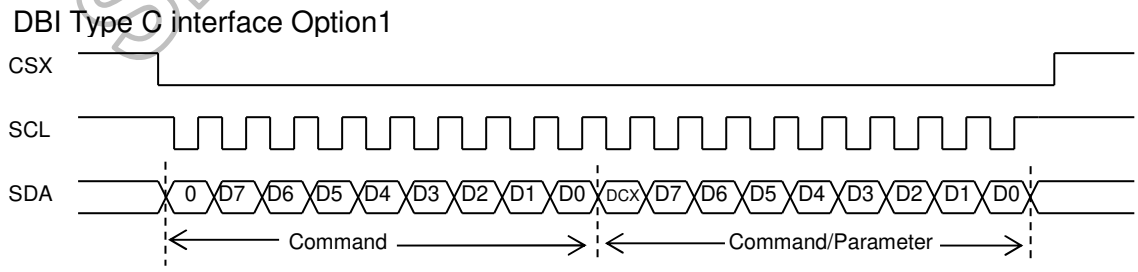


Figure 5.1: DBI Type C interface Option 1 write mode

5.1.2 SPI Interface Read Mode

In SPI I/F Read Mode, the host controller first has to send a command and then the following byte is transmitted to host controller in the SDA. The read mode has two type : one is command data 8-bits read and one is over 8-bits read.

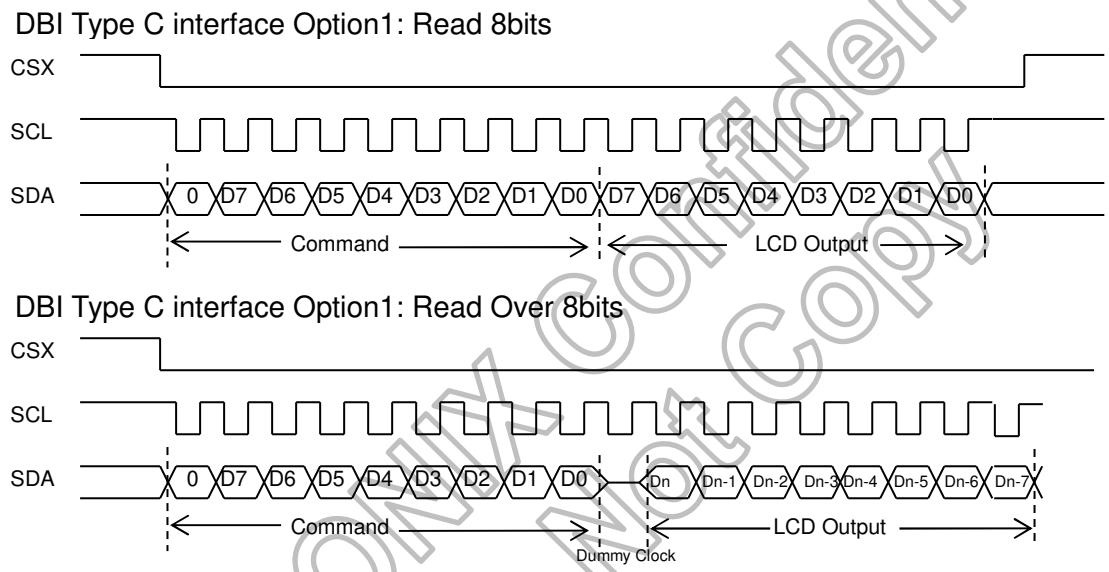


Figure 5.2: DBI Type C interface Option 1 read mode

5.1.3 Break and Pause Sequences

If there is a break on data transmission when transmit a command before a whole byte has been completed, then the driver IC will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following figure.

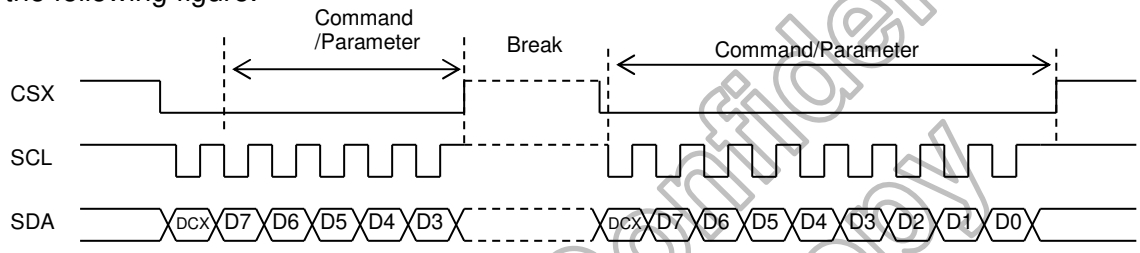


Figure 5.3: Driver IC data transfer recovery

If a one or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

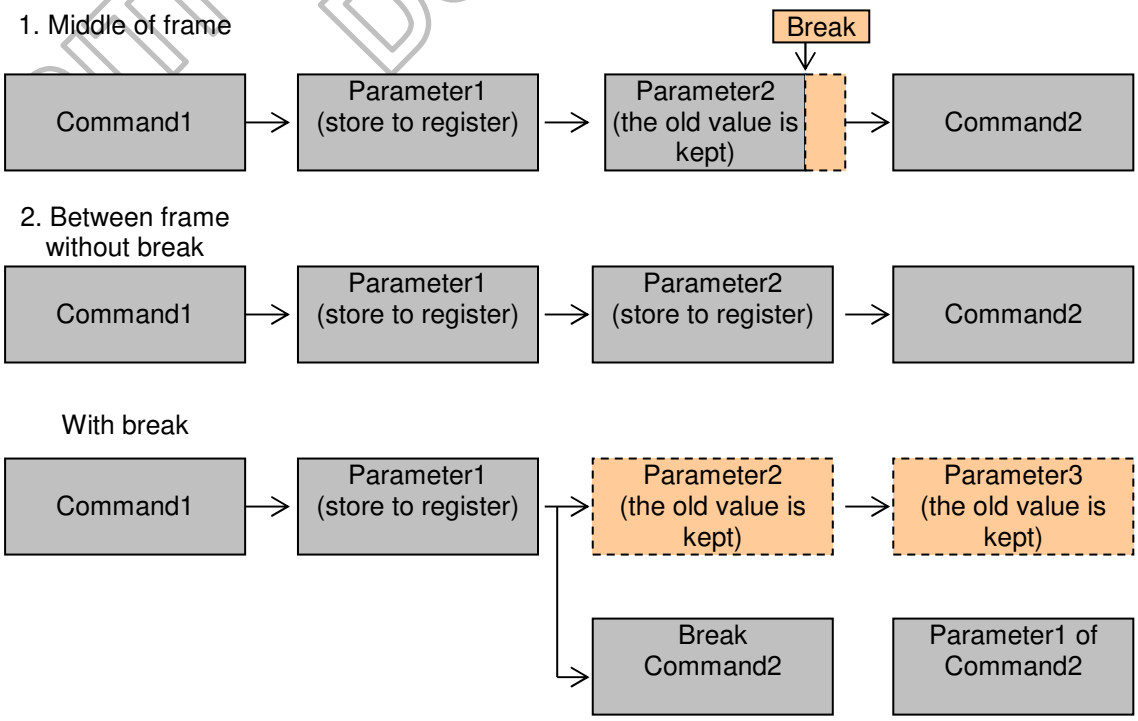


Figure 5.4: Break during parameter

The host processor can pause a write sequence by pulling the CSX signal high between command or data bytes. The driver IC shall wait for the host processor to drive CSX low before continuing the write sequence at the point where the sequence was paused.

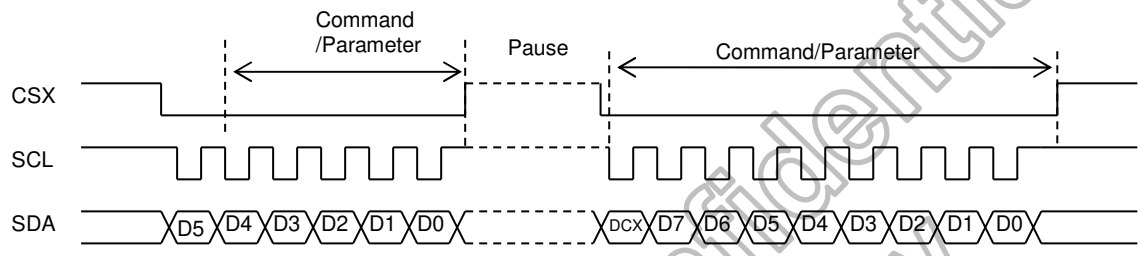


Figure 5.5: Driver IC data transfer pause

There are 4 cases where there is possible to see this kind of pause:

1. Command – Pause – Command
2. Command – Pause – Parameter
3. Parameter – Pause – Command
4. Parameter – Pause – Parameter

5.2 MIPI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The ST7703 only support Video mode.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the driver IC relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

Lane Pair	HOST(Master)/ Driver IC(Slave)
Clock Lane	- Unidirectional Lane - Clock Only - Escape mode (ULPS only)
Data Lane 0	- Bi-directional Lane - Forward High Speed - Bi-directional Escape Mode - Bi-directional LPDT
Data Lane 1 Data Lane 2 Data Lane 3	- Unidirectional Lane - Forward High Speed - Escape mode (ULPS only) - NO LPDT

Table 5.2: MIPI Interface Configuration

5.2.1 DSI General Interface Communication

The driver IC uses data and clock lane differential pairs for DSI. Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode. Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the HOST to the driver IC and vice versa.

State code	Line voltage Levels		High speed	Low power	
	DP	DN		Control mode	Escape mode
HS-0	HS Low	HS High	Differential-0	Note 1	Note 1
HS-1	HS High	HS Low	Differential-1	Note 1	Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	Note 2

Note 1 : During high-speed transmission, the low power receivers observe LP-00 on the lines.
Note 2 :If LP-11 occurs during Escape mode, the lane returns to Stop state (Control mode LP-11)

Table 5.3: Lane State Description

5.2.1.1 DSI Clock Lane

The principle flow chart of the different clock lanes power modes is illustrated below.

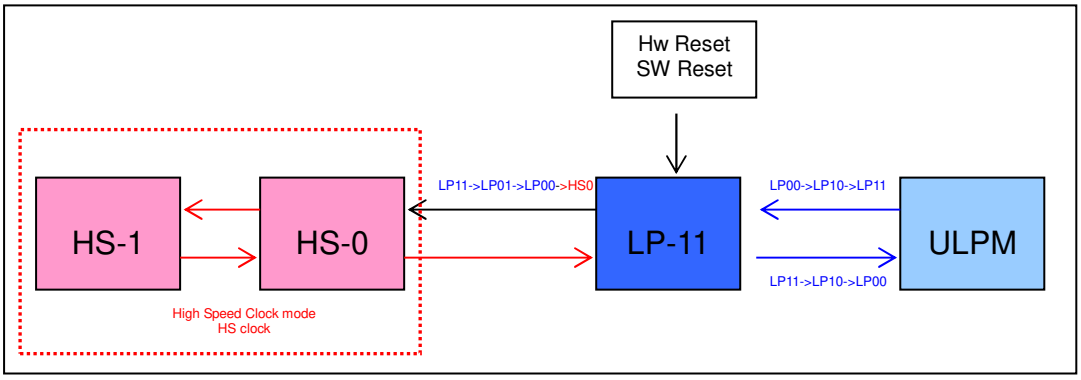


Figure 5.6: DSI Clock Lane State Diagram

LK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11:

1. After SW Reset, HW Reset or Power On Sequence =>LP-11
2. After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

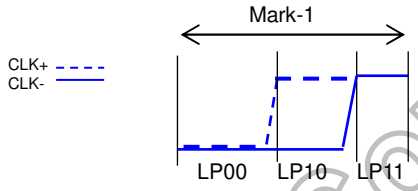


Figure 5.7: From ULPM to LPM

3. After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence and all three mode changes are illustrated below.

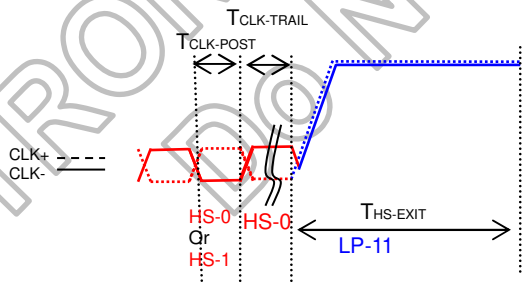


Figure 5.8: From High Speed Clock mode to LPM

Ultra Low Power Mode (LP-00: ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State. The entering way is from the Low Power Mode (LPM, LP-11 State) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below.

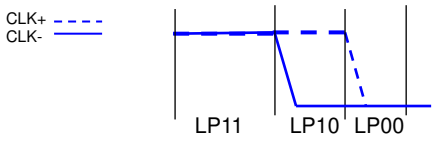


Figure 5.9: From LPM mode to ULPM

High Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State. The entering way is from the Low Power Mode (LPM, LP-11 State) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

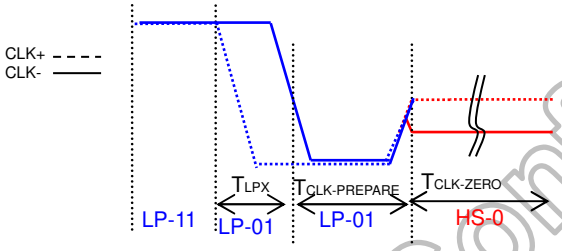


Figure 5.10: From LPM mode to HSCM

High Speed Clock Burst

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

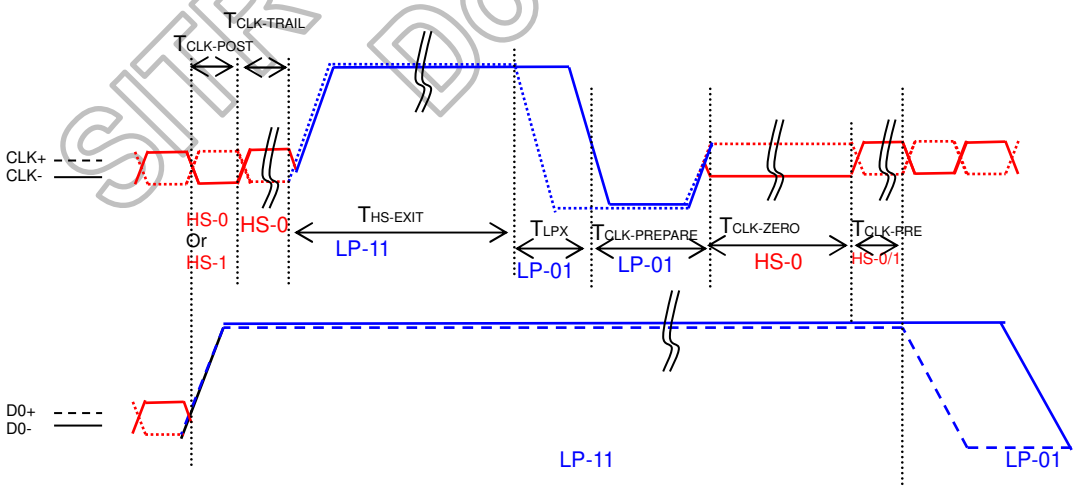


Figure 5.11: Switching the Clock Lane between HSCM and LPM

5.2.1.2 DSI-D0 Data Lane

DSI-D0+/- Data Lanes can be driven in different modes which are: Escape Mode, High-Speed Data Transmission and Bus Turnaround Request. The flow chart of the D0 data lanes is illustrated below.

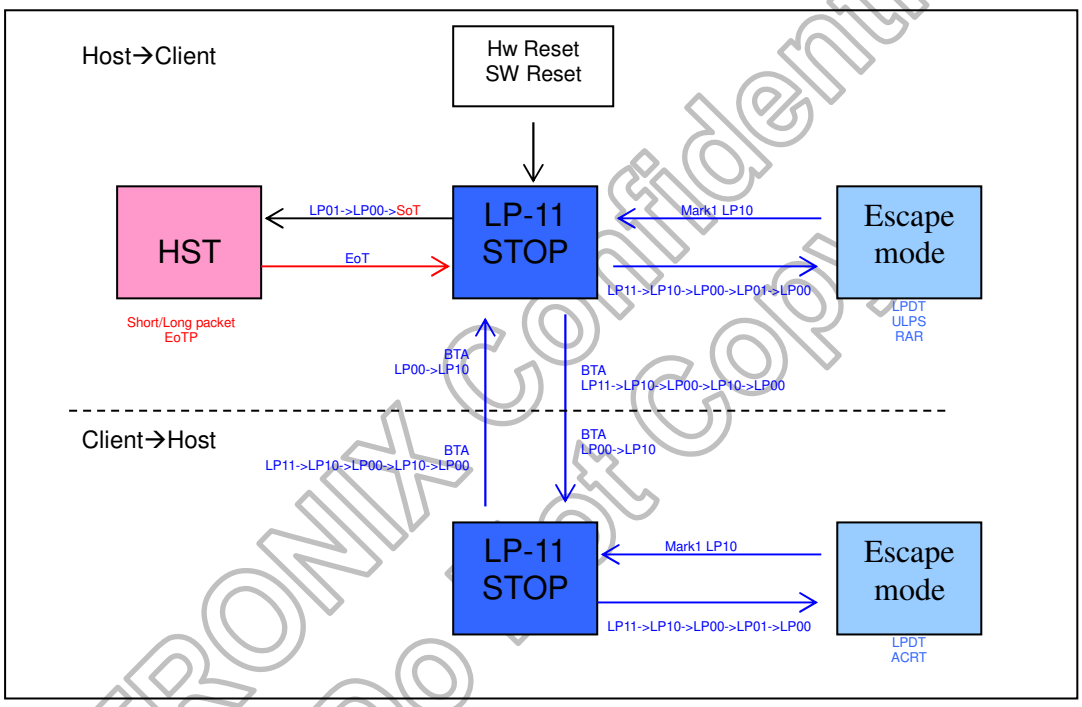


Figure 5.12: DSI Data Lane D0 State Diagram

Description	Operation Code
High Speed Data Transmission Burst	LP11->LP01->LP00
Escape mode entry	LP11->LP10->LP00->LP01->LP00
Bus turn around	LP11->LP10->LP00->LP10->LP00
Exit Escape mode (Mark-1)	LP00->LP10->LP11

Table 5.4: Data Lane D0 Operation Modes

ESCAPE MODE

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

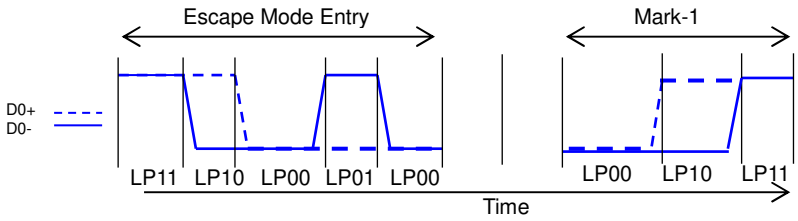


Figure 5.13: DSI Data Lane D0 general escape mode sequence

ST7703 can support three different Escape Commands. The commands (EC) can be divided 2 different groups: Mode or Trigger. The HOST is informing to the driver IC that it is controlling data lanes (DSI-D0+/-) with the mode. Escape commands are defined as below table.

Escape Command	Command Type	Entry Command Pattern (First Bit→Last Bit Transmitted)
Low Power Data Transmission	Mode	1110 0001
Ultra-Low Power mode	Mode	0001 1110
Remote Application Reset	Trigger	0110 0010
Tearing Effect	Trigger	0101 1101
Acknowledge	Trigger	0010 0001

Table 5.5: Escape Mode Commands

Low-Power Data Transmission (LPDT)

The HOST can send data to the driver IC in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command will been sent to this driver IC. The driver IC is also using the same sequence when it is sending data to the HOST. The Low Power Data Transmission (LPDT) is using a following sequence:

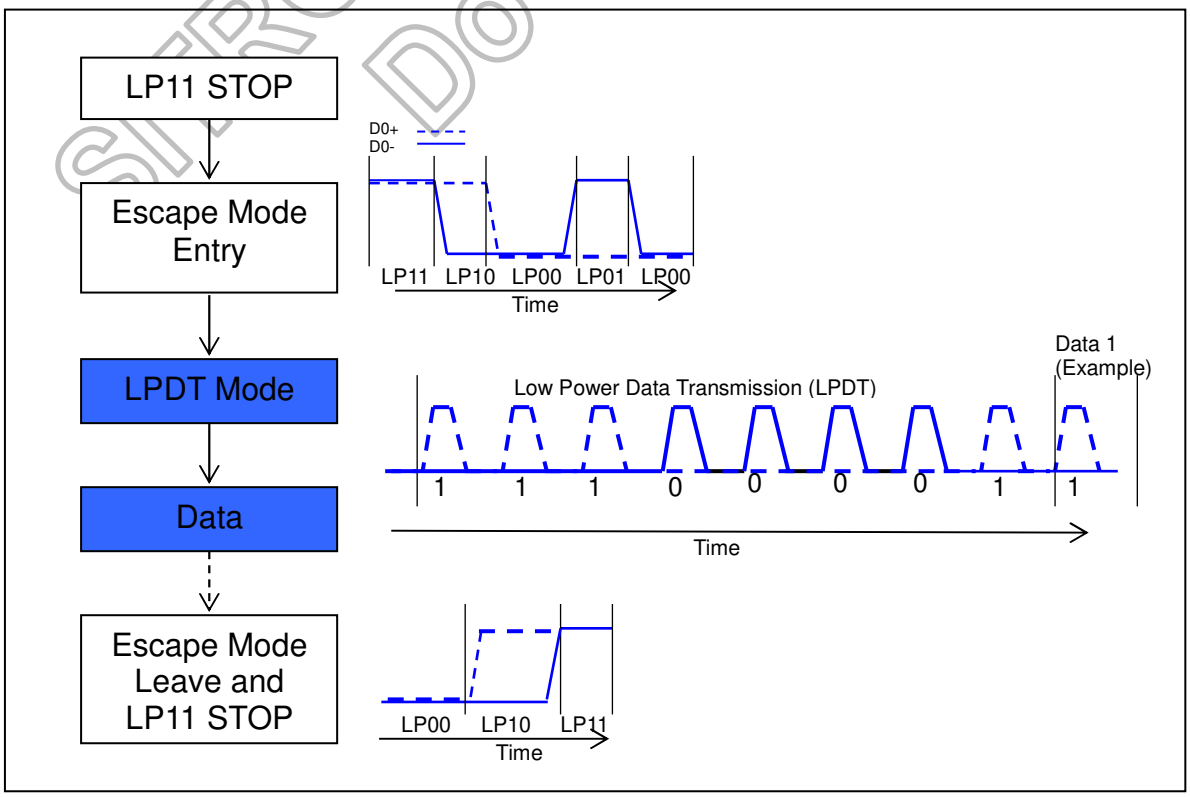


Figure 5.14: DSI Data Lane D0 LPDT sequence

Ultra Low Power State (ULPS)

The driver IC can enter this Ultra Low Power Sate to save power consumption when HOST send this ULPS command. Ultra Low Power State is using below sequence:

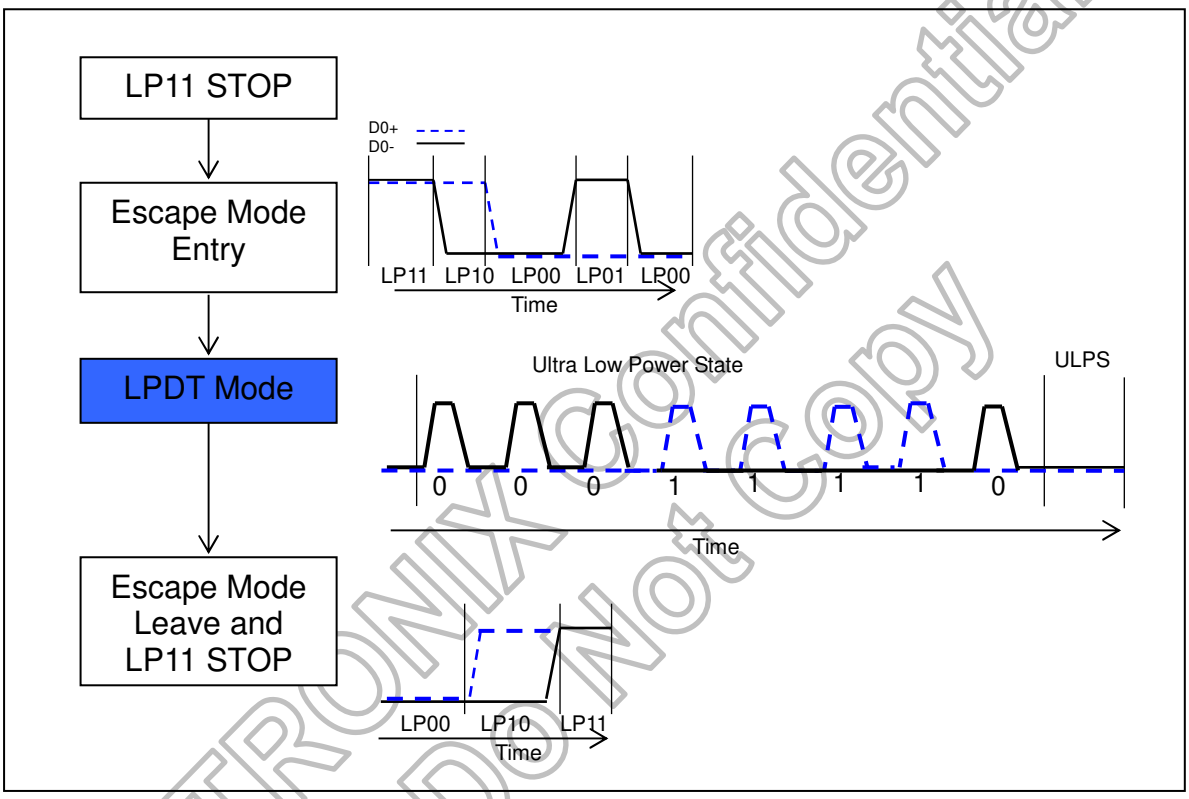


Figure 5.15: DSI Data Lane D0 ULPS sequence

Remote Application Reset (RAR)

The HOST can inform to the driver IC that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset (RAR) is using a following sequence:

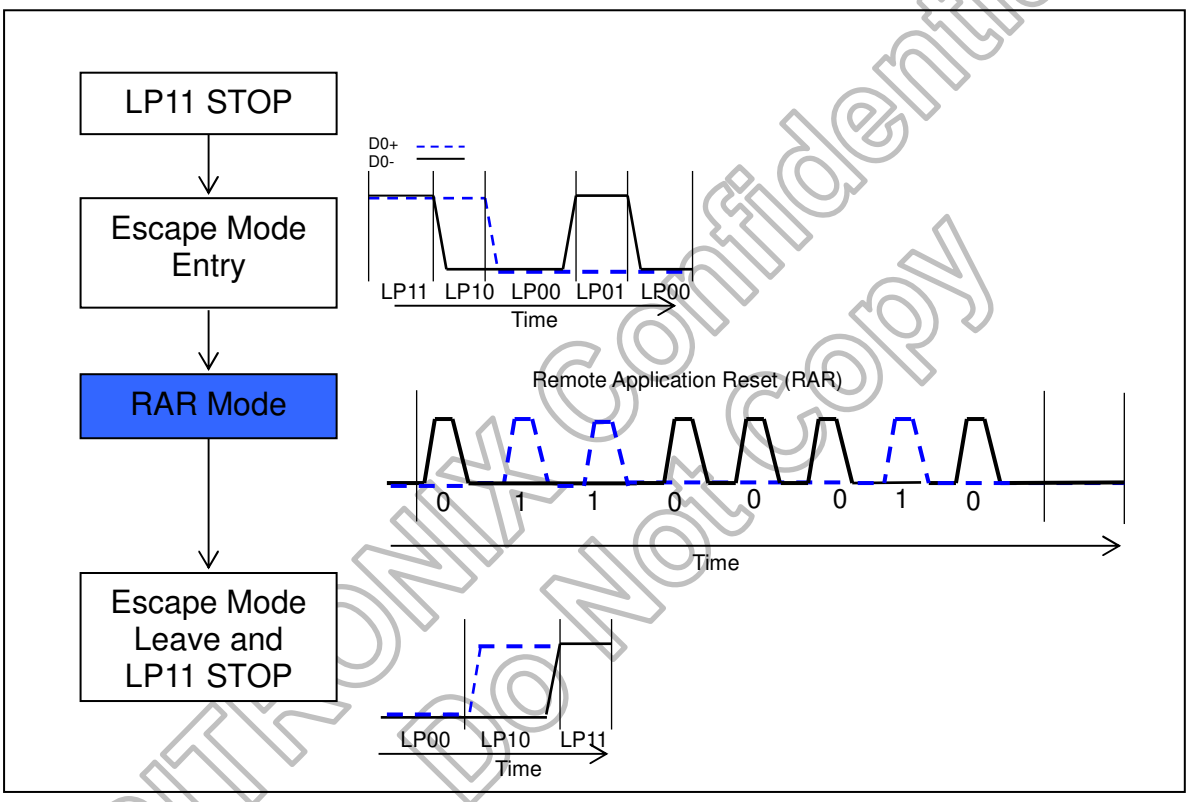


Figure 5.16: DSI Data Lane D0 RAR sequence

Tearing Effect (TEE)

The driver IC can inform to the HOST when a tearing effect event (New V-synch) has been happen on the driver IC by Tearing Effect (TEE). The Tearing Effect (TEE) is using a following sequence:

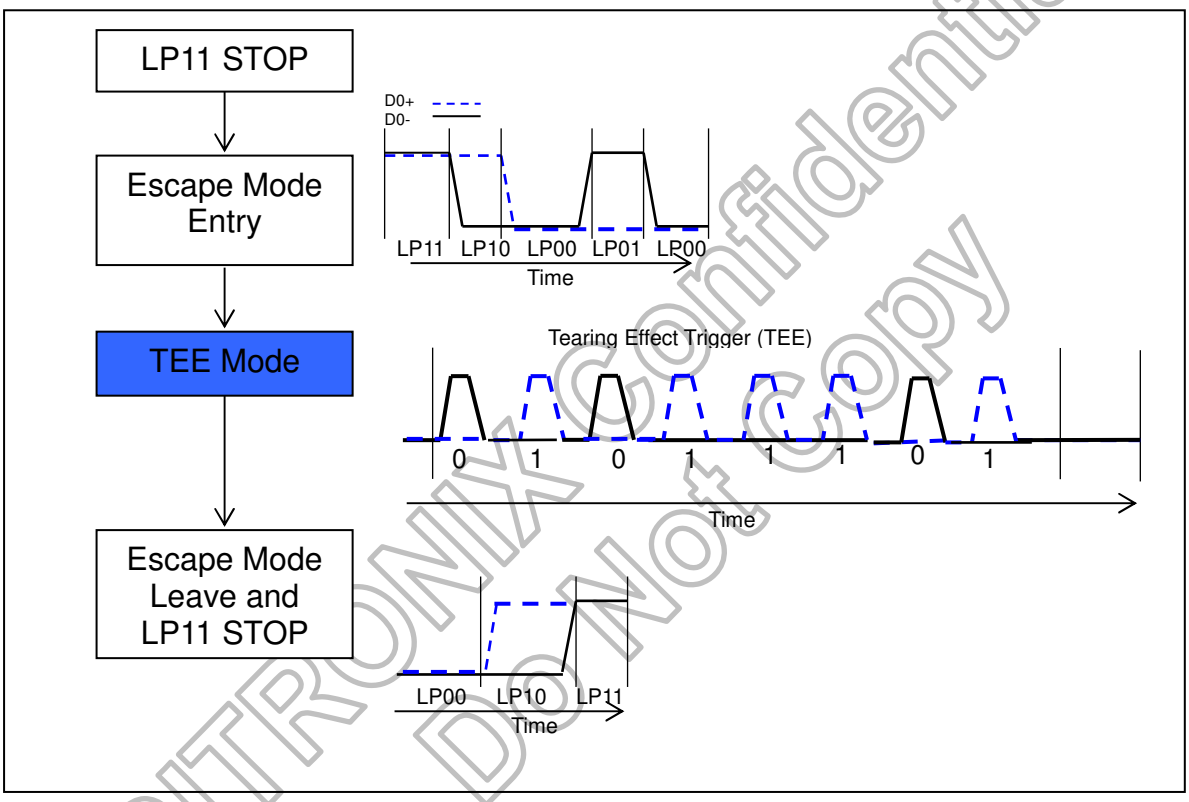


Figure 5.17: DSI Data Lane D0 TEE sequence

Acknowledge (ACK)

The driver IC can inform to the HOST when an error has not recognized on it by Acknowledge (ACK). The Acknowledge (ACK) is using a following sequence:

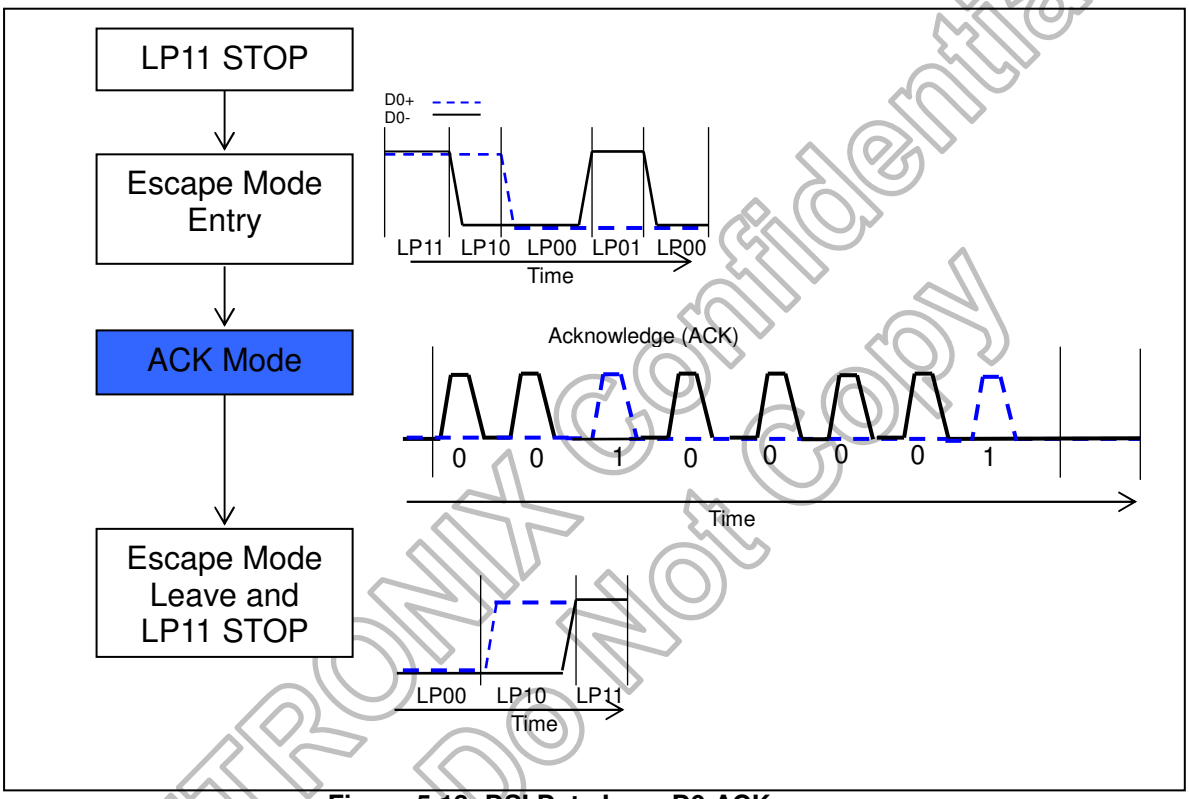


Figure 5.18: DSI Data Lane D0 ACK sequence

High Speed Data Transmission

The driver IC is entering High-Speed Data Transmission when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode by the HOST. Data lanes of the driver IC are entering (TSOT) in the High-Speed Data Transmission (HSDT) as below figure.

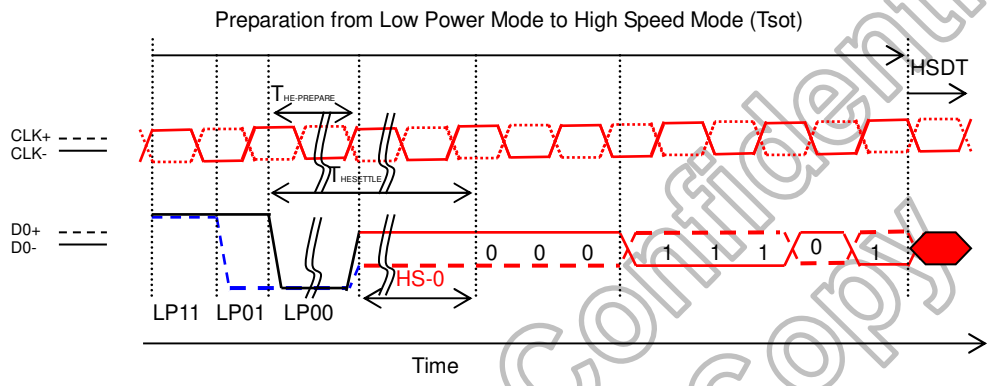
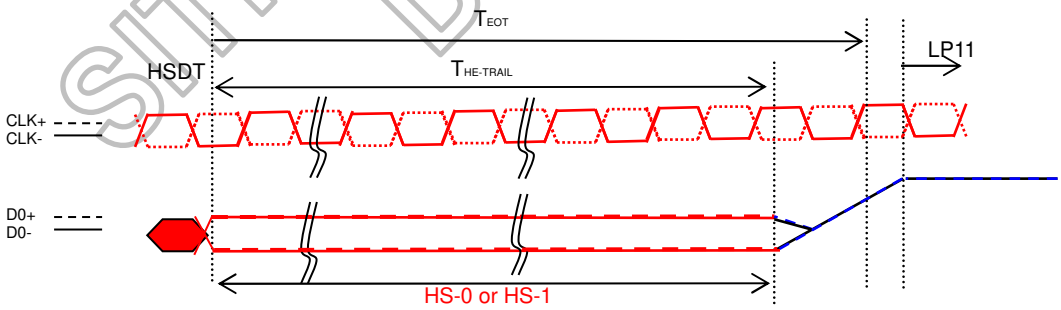


Figure 5.19: DSI Data Lane Entering High Speed Data Transmission

Leaving High Speed Data Transmission

The driver IC is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode by the HOST and it is kept until data lanes are in LP-11 mode.Data lanes of the driver IC are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Figure 5.20: DSI Data Lane Entering High Speed Data Transmission

Bus Turnaround (BTA)

The HOST or driver IC, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the HOST or driver IC. The HOST or driver IC is using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the HOST wants to do the bus turnaround procedure to the driver IC, as below.

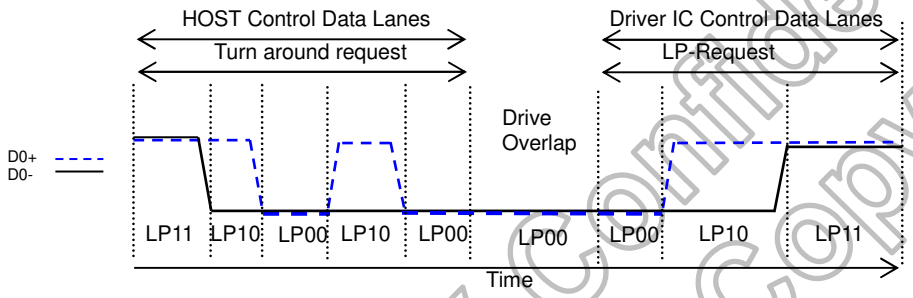
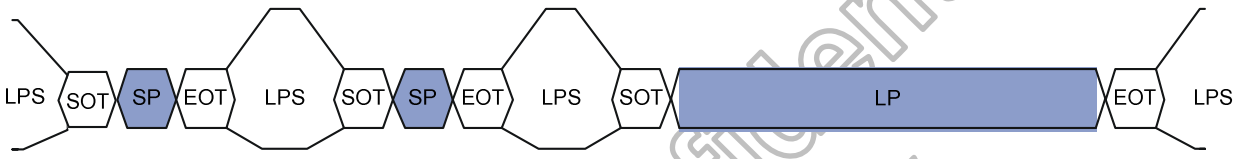


Figure 5.21: DSI Bus Turn Around Procedure

5.2.2 DSI Packet Level Communication

The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Below figure illustrates multiple HS Transmission packets.



LPS：Low power state
SOT：Start of Transmission
SP：Short Packet
LP：Long Packet
EOT：End of Transmission

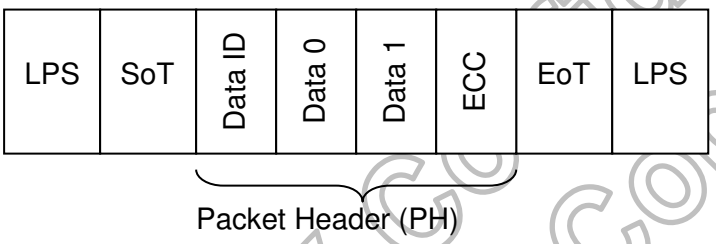
Figure 5.22: DSI multiple HS transmission packets

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the length of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

5.2.2.1 General Packet Structure

Short packets

Specify the payload length using the Data Type field and are from two to nine bytes in length. Short packet is used for most Command Mode commands and associated parameters. Where short packets format include an 8-bit Data ID followed by zero to seven bytes and an 8-bit ECC. Below figure shows the structure of the Short packet.

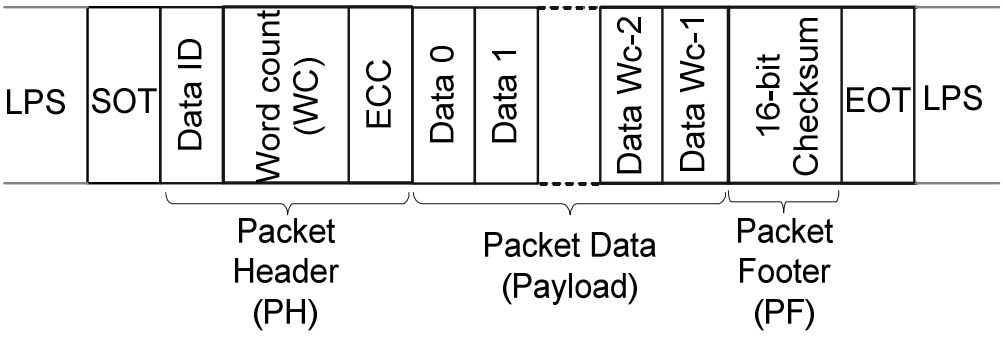


SOT: Start of Transmission
DI(Data ID): 8-bit Contain Virtual Channel Identifier and Data Type.
Data 0 and Data 1: Packet Data (8+8bit)
ECC(Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

Figure 5.23: Structure of the short packet

Long packets

Specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data. Below figure shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length. Where 65,541 bytes = (216-1) + 4 bytes PH + 2 bytes PF



DI (Data ID)：Contain Virtual Channel Identifier and Data Type.
WC (Word Count)：8+8 bits The receiver use WC to define packet end.
ECC (Error Correction Code)：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF(Packet Footer)：Mean 16-bit Checksum.

Figure 5.24: Structure of the long packet

According to packet form, basic elements include DI and ECC. Figure 4.44 the shows format of Data ID.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)		DT (Data Type)					

DI[7:6] ➔ These two bits identify the data as directed to one of four virtual channels.
DI[5:0]: These six bits specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

Figure 5.25: Format of data ID

Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the HOST. The ST7703 supports Virtual Channel only when VC = 00.

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Data type, hex	Data type, binary	Description packet	Size
05h	00 0101	DCS Write, no parameters	Short
15h	01 0101	DCS Write, 1 parameter	Short
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
13h	01 0011	Generic Short Write, 1 parameter	Short
23h	10 0011	Generic Short Write, 2 parameter	Short
14h	01 0100	Generic Read, 1 parameter	Short
29h	10 1001	Generic Long Write	Long
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	-

Table 5.6: Data Types from Host to the Driver IC

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge with Error Report	Short
21h	01 0001	Generic short READ Response, 1 byte returned	Short
22h	01 0010	Generic short READ Response, 2 byte returned	Short
1Ah	01 1010	Generic Read Long Response	Long
1Ch	01 1100	DCS Long READ Response	Long

Table 5.7: Data Types from the Driver IC to Host

Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH).

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function, as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

PACKET DATA (PD) ON THE LONG PACKET

Packet Data (PD) of the Long Packet is defined after Packet Header (PH) of the Long Packet. The number of the data bytes is defined on chapter "Word Count (WC) on the Long Packet".

PACKET FOOTER (PF) ON THE LONG PACKET

Packet Footer (PF) of the Long Packet is defined after the Packet Data (PD) of the Long Packet. The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet .The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X^{16}+X^{12}+X^5+X^0$.

5.2.2.2 Detail Format Description

Generic Write, 1 Parameter, Data Type = 01 0011 (13h)
Generic Write, 1 Parameter is always using a Short Packet from the HOST to the driver IC. The content of 2 payload bytes is “command” and “00h”.

Generic Write, 2 Parameter, Data Type = 10 0011 (23h)
Generic Write, 2 Parameter is always using a Short Packet from the HOST to the driver IC. The content of 2 payload bytes is “command” and “parameter”.

Generic Long Write, Data Type = 10 1001 (29h)
Generic Long Write is always using a Long Packet from the HOST to the driver IC. The content can include Command (No Parameters) or Command with 1 or more parameters.

Generic Read, 1 Parameter, Data Type = 01 0100 (14h)
Generic Read, 1 Parameter is always using a Short Packet from the HOST to the driver IC. The HOST has to define to the driver IC, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size”, which Data Type is 11 0111 and which is using Short Packet before the HOST can send “Generic Read, 1 Parameter” to the driver IC.

Display Command Set Write, No Parameter, Data Type = 00 0101 (05h)
Display Command Set (DCS) Write, No Parameter is always using a Short Packet from the HOST to the driver IC. The content of 2 payload bytes is “command” and “00h”.

Display Command Set Write, 1 Parameter, Data Type = 01 0101 (15h)
Display Command Set (DCS) Write, 1 Parameter is always using a Short Packet from the HOST to the driver IC. The content of 2 payload bytes is “command” and “parameter”.

Display Command Set Long Write, Data Type = 11 1001 (39h)
Display Command Set (DCS) Long Write is always using a Long Packet from the HOST to the driver IC. The content can include Command (No Parameters) or Command with 1 or more parameters.

Display Command Set (DCS) Read, No Parameter, Data Type = 00 0110 (06h)
Display Command Set (DCS) Read, No Parameter is always using a Short Packet, from the HOST to the driver IC. The HOST has to define to the driver IC, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size”, which Data Type is 11 0111 and which is using Short Packet before the HOST can send “Display Command Set (DCS) Read, No Parameter” to the driver IC.

Null Packet, No Data , Data Type = 00 1001 (09h)

Null Packet, No Data is always using a Long Packet, what is defined on Data Type from the HOST to the driver IC. The purpose of this command is keeping data lanes in the high speed mode, if it is needed. The driver IC is ignored Packet Data what the HOST is sending.

Set Maximum Return Packet Size, Data Type = 11 0011 (37h)

Set Maximum Return Packet Size is always using a Long Packet, what is defined on Data Type from the HOST to the driver IC. The purpose of this command is specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.

Sync Event (H Start, H End, V Start, V End), Data Type = XX 0001 (0xX1)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, The Sync Events are defined as follows:

- Data Type = 00 0001 (01h) V Sync Start
- Data Type = 01 0001 (11h) V Sync End
- Data Type = 10 0001 (21h) H Sync Start
- Data Type = 11 0001 (31h) H Sync End

Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode driver IC to 8-colors mode for power saving.

Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode driver IC from 8-colors mode to normal display operation.

Shutdown Peripheral Command, Data Type = 10 0010 (22h)

Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode driver IC for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up command.

Turn On Peripheral Command, Data Type = 11 0010 (32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode driver IC for normal display operation.

Blanking Packet (Long), Data Type = 01 1001 (19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the driver IC.

Packed Pixel Stream, 16-bit Format, Long packet, Data Type = 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode driver IC. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

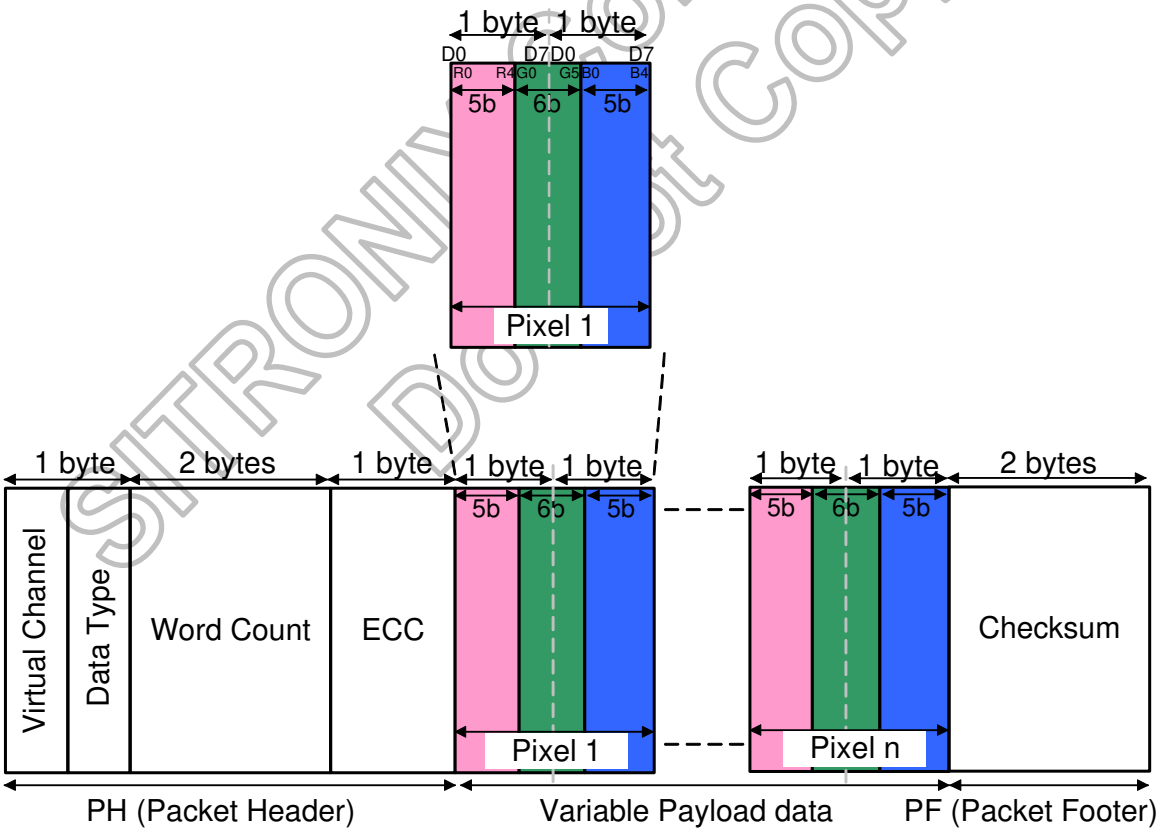
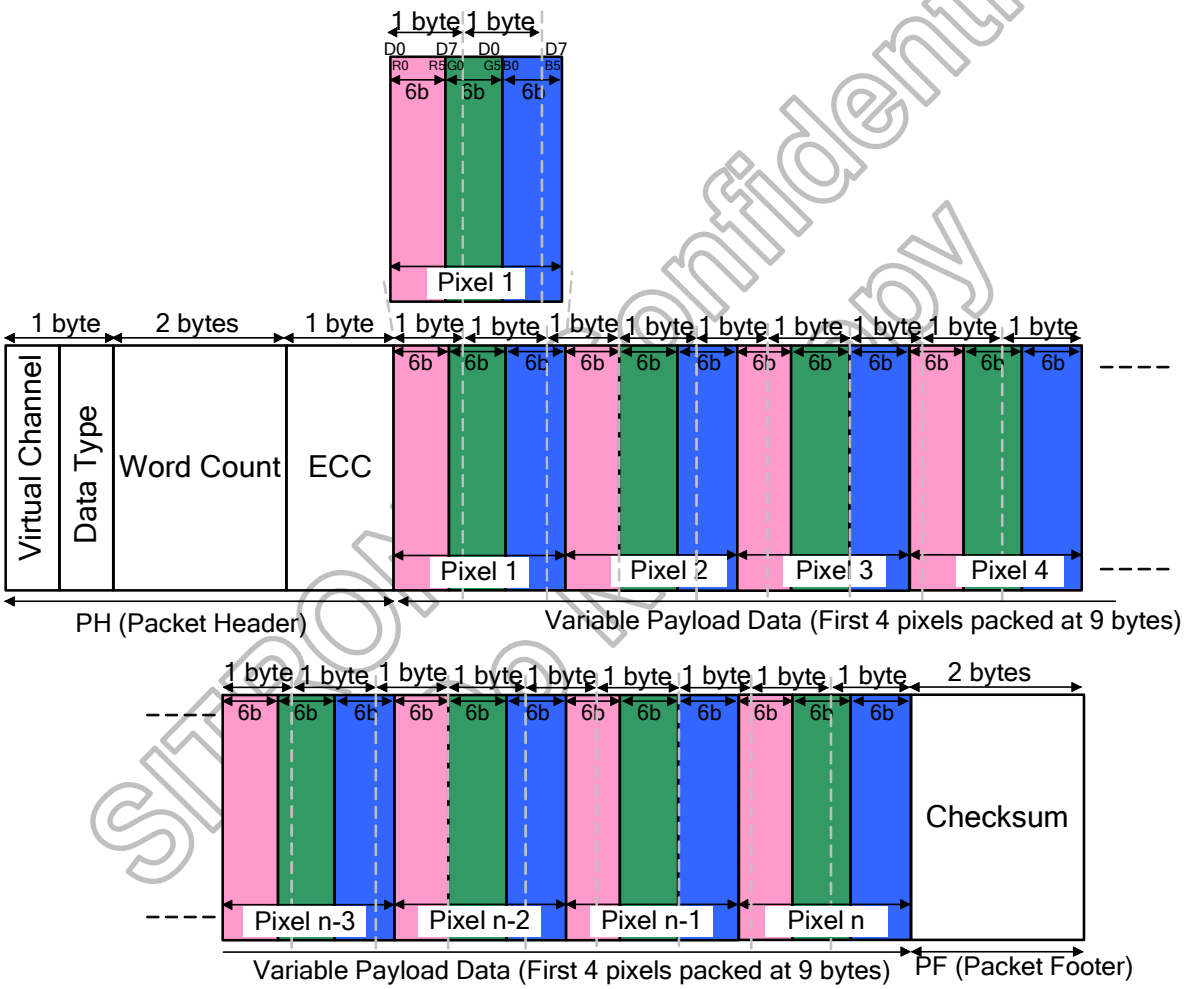


Figure 5.26: 16-bit RGB Color Format, Long packet

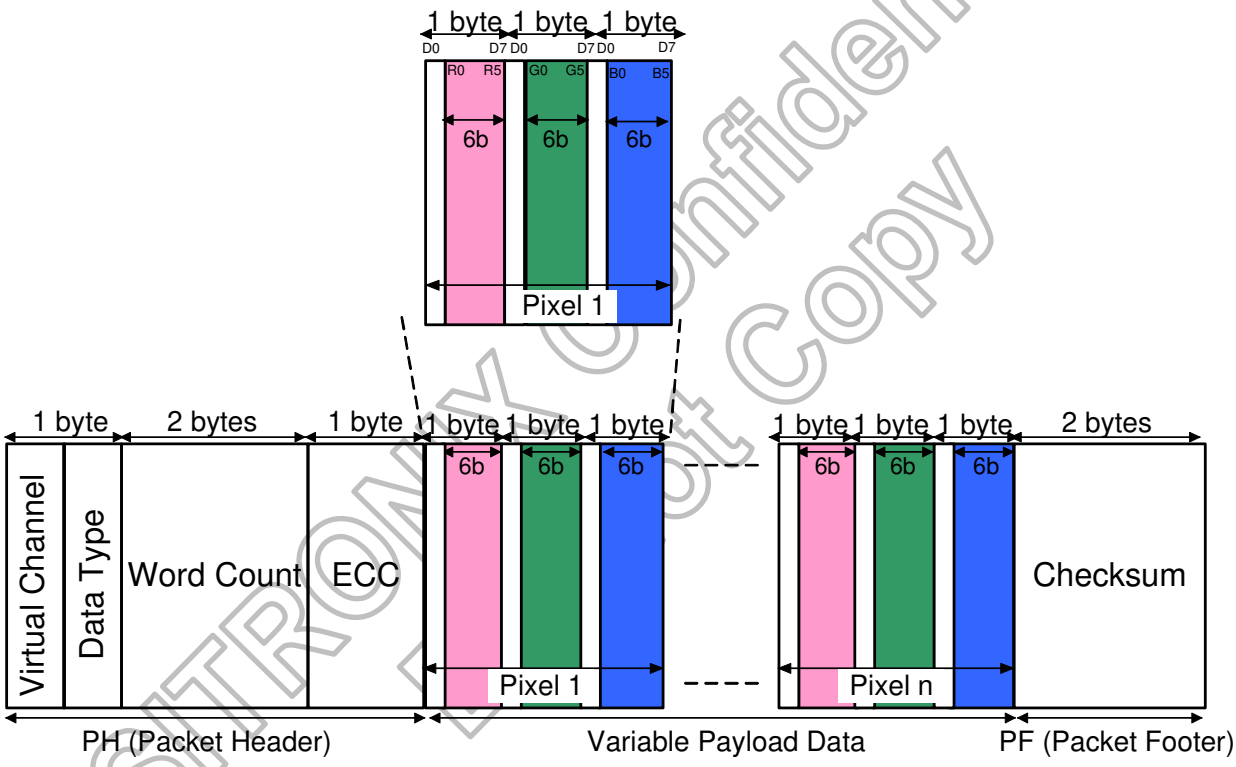
Packed Pixel Stream, 18-bit Format, Long packet, Data type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format is a Long packet used to transmit image data formatted as 18-bit pixels to a Video Mode driver IC. Pixel format is six bits red, six bits green, six bits blue, in that order.



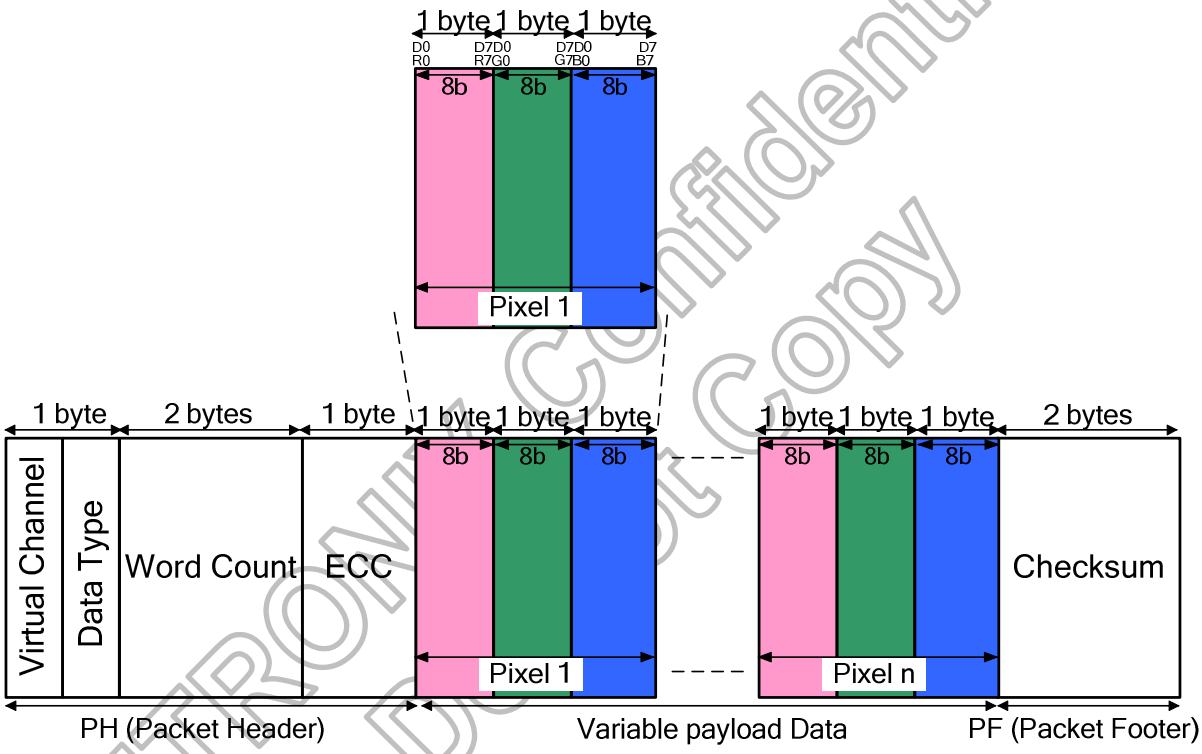
Pixel Stream, 18-bit Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)

Packed Pixel Stream 18-Bit Format is a Long packet used to transmit image data formatted as 18-bit pixels to a Video Mode driver IC. Each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored.



Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet used to transmit image data formatted as 18-bit pixels to a Video Mode driver IC. Pixel format is eight bits red, eight bits green, eight bits blue, in that order.



Acknowledge with Error Report, Data Type = 00 0010(02h)

"Acknowledge with Error Report" is always using a Short Packet, from the driver IC to the HOST. The Packet Data can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	Reserved
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Reserved
14	Reserved
15	Reserved

These errors of the previous packets can check "Read Display Signal Mode (0Eh)" and "Read Number of the Errors on DSI (05h)" commands. The bit D0 of the "Read Display Signal Mode (0Eh)" command has been set to '1' if a received packet includes an error.
The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read "Read Number of the Errors on DSI (05h)" command.

DCS Read Long Response, Data Type = 01 1100(1Ch)

DCS Read Long Response is always using a Long Packet, from the driver IC to the Host. "DCS Read Long Response" is used when the driver IC wants to response a DCS Read command, which the Host has sent to the driver IC.

DCS Read Short Response, 1 Byte Returned, Data Type = 10 0001(21h)

DCS Read Short Response, 1 Byte Returned is always using a Short Packet from the driver IC to the Host. "DCS Read Short Response, 1 Byte Returned" is used when the driver IC wants to response a DCS Read command, which the Host has sent to the driver IC.

DCS Read Short Response, 2 Bytes Returned, Data Type = 10 0010(22h)

DCS Read Short Response, 2 Bytes Returned is always using a Short Packet from the driver IC to the Host. "DCS Read Short Response, 2 Bytes Returned" is used when the driver IC wants to response a DCS Read command, which the Host has sent to the driver IC.

Generic Read Long Response, Data Type = 01 1010(1Ah)

Generic Read Long Response is always using a Long Packet from the driver IC to the HOST. "Generic Read Long Response" is used when the driver IC wants to response a Generic Read command.

Generic Read Short Response, 1 Byte Returned, Data Type = 01 0001(11h)

Generic Read Short Response, 1 Byte Returned is always using a Short Packet from the driver IC to the HOST. "Generic Read Short Response, 1 Byte Returned" is used when the driver IC wants to response a Generic Read command, which the HOST has sent to the driver IC.

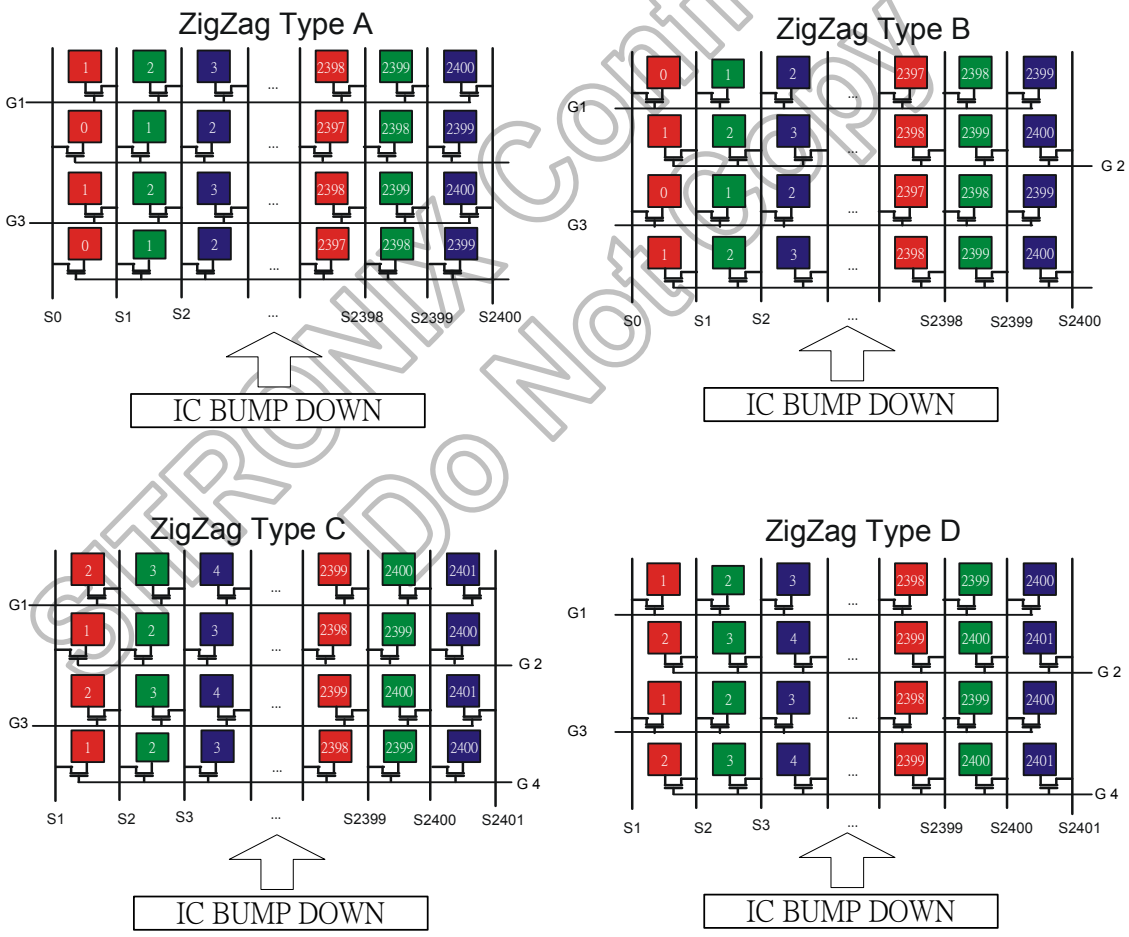
Generic Read Short Response, 2 Bytes Returned, Data Type = 01 0010(12h)

Generic Read Short Response, 2 Bytes Returned is always using a Short Packet from the driver IC to the HOST. "Generic Read Short Response, 2 Bytes Returned" is used when the driver IC wants to response a Generic Read command, which the HOST has sent to the driver IC.

5.3 Inversion

The ST7703 can support the column, 1-dot, 1+2-dot, 2-dot, 3-dot, 4-dot and 8-dot inversion of liquid crystal. These inversions can provide a solution for improving display quality. In determining the inversion drive for the inversion cycle, check the quality of display on the liquid crystal panel.

The ST7703 also can support the ZigZag inversion. Eight kinds of ZigZag inversion can be selected by software setting. These kinds are as below figure:



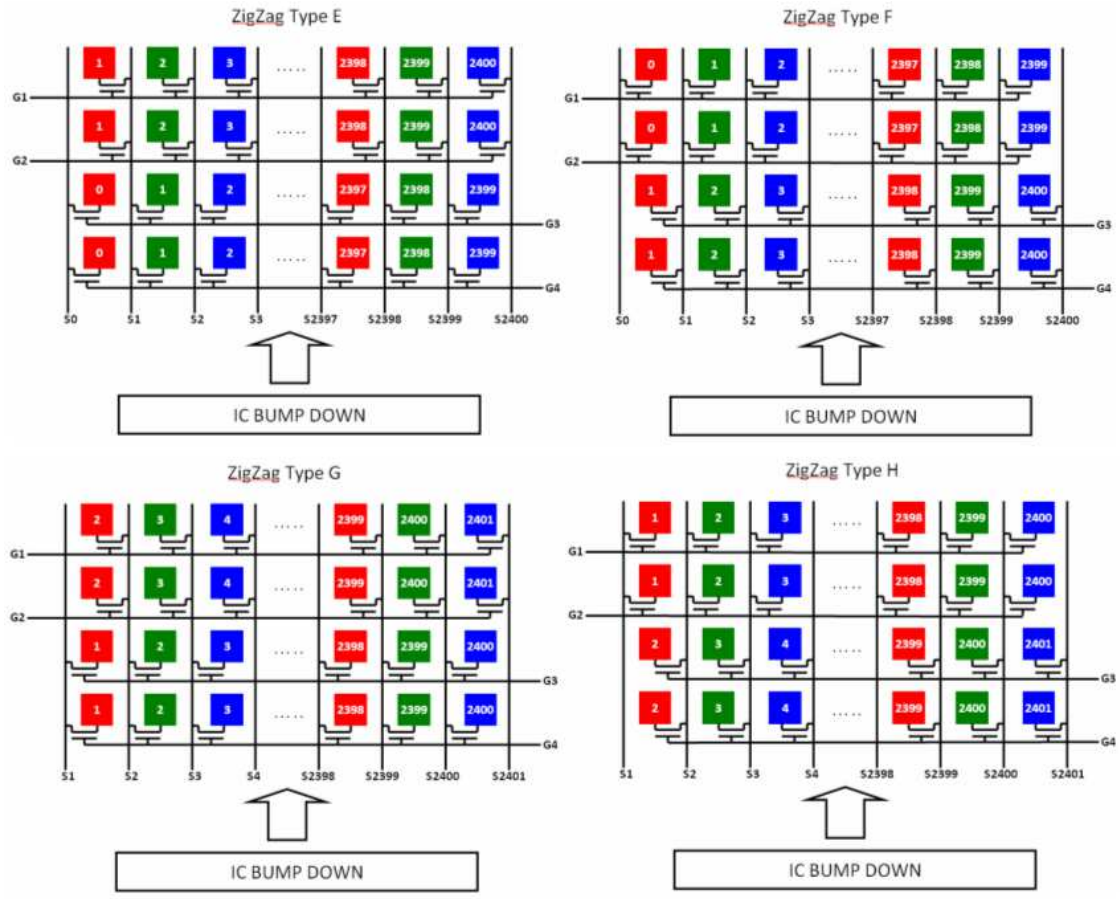


Figure 5.27: Source channels of ZigZag inversion mode

5.4 Gamma Function

The ST7703 offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The adjustment of digital gamma is selected by internal register DGC_EN bit.

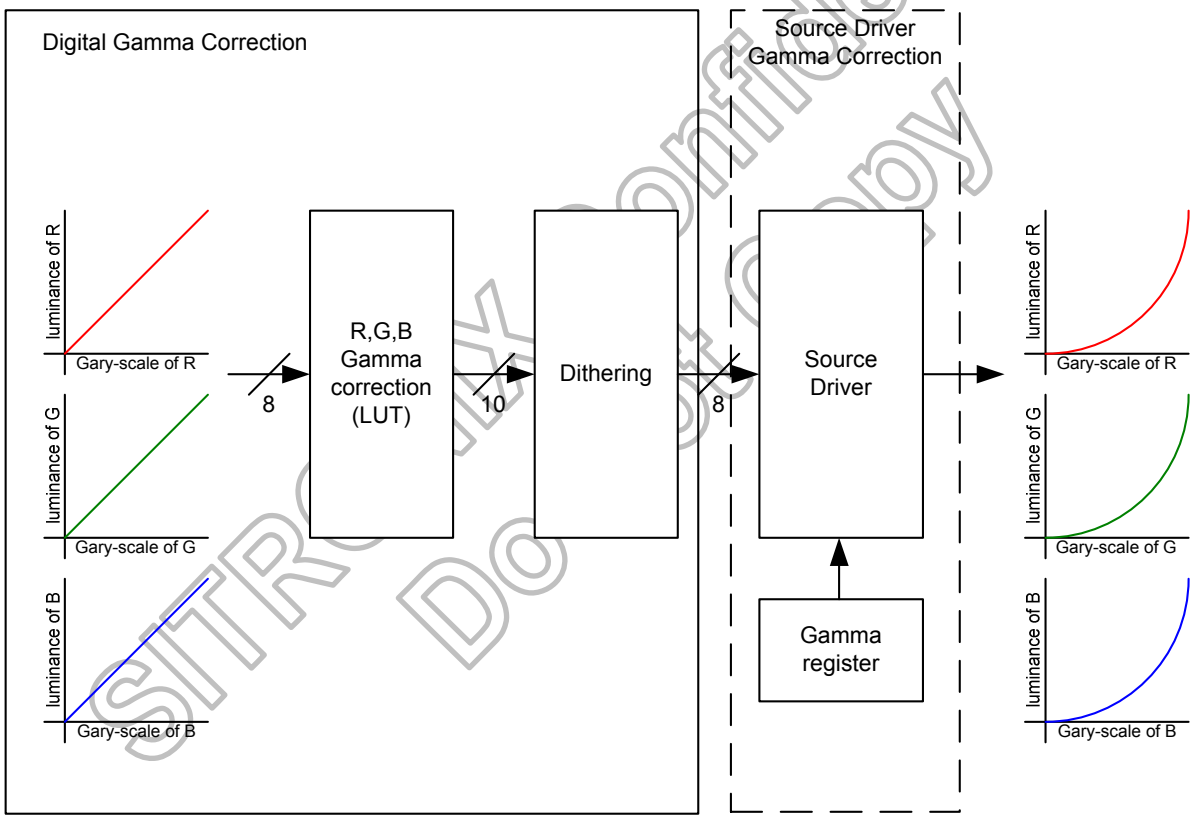
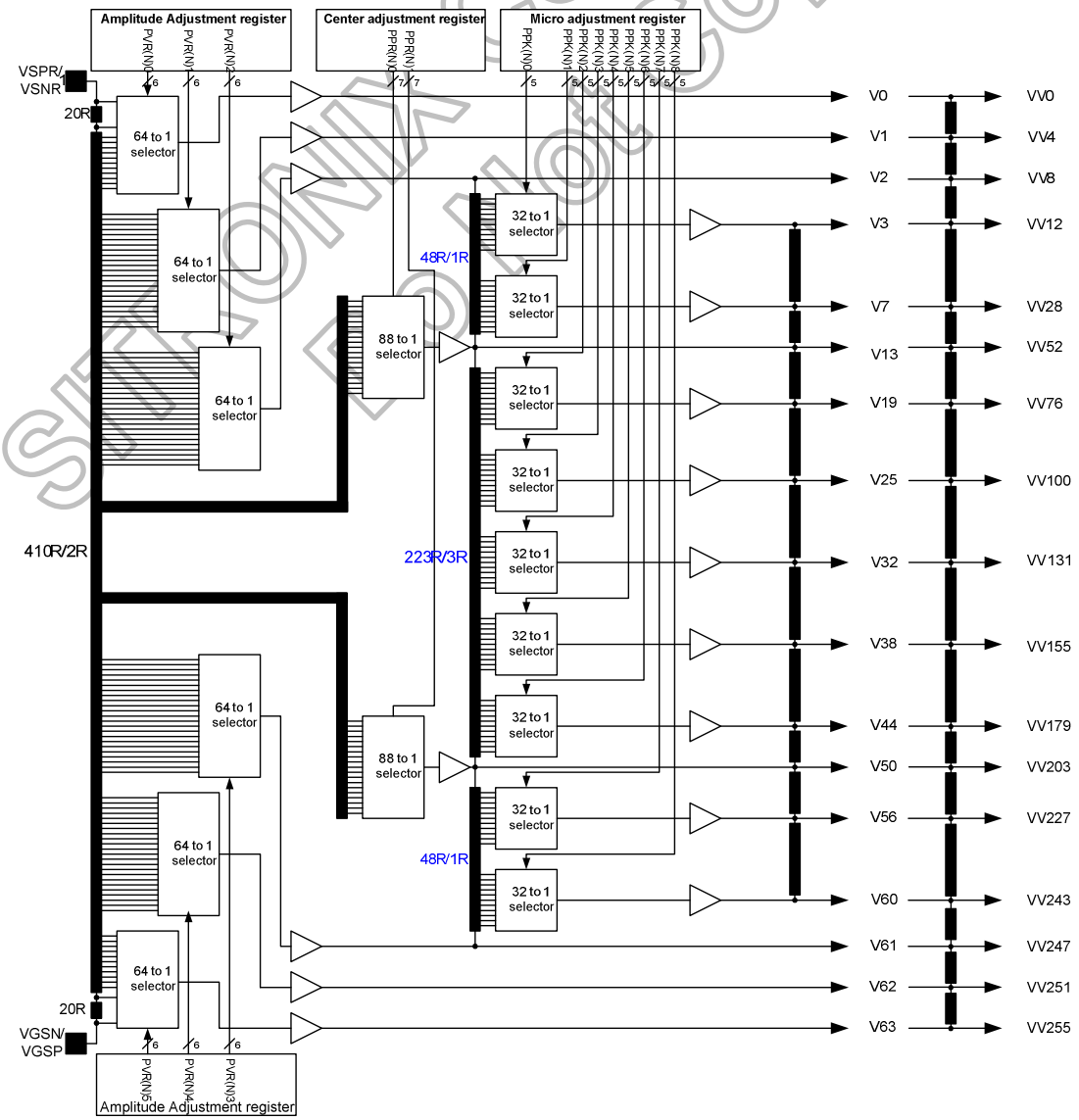


Figure 5.28: Gamma adjustments different of source driver with digital gamma correction

5.4.1 Gamma Characteristic Correction Function

The ST7703 incorporates gamma adjustment function for the 16.7m-color display. Gamma adjustment operation is implemented by deciding the 17 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including 17 gamma reference voltages. VgP/N (0, 4, 8, 12, 28, 52, 76, 100, 131, 155, 179, 203, 227, 273, 247, 251, 255).



5.4.2 Gray Voltage Generator for Digital Gamma Correction

The ST7703 digital gamma correction can reach the independent GAMMA curve of RGB. The ST7703 utilizes DGC_LUT (Digital Gamma Correction Look Up Table) to change input data from 8-bit into 10-bit and sends 10-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

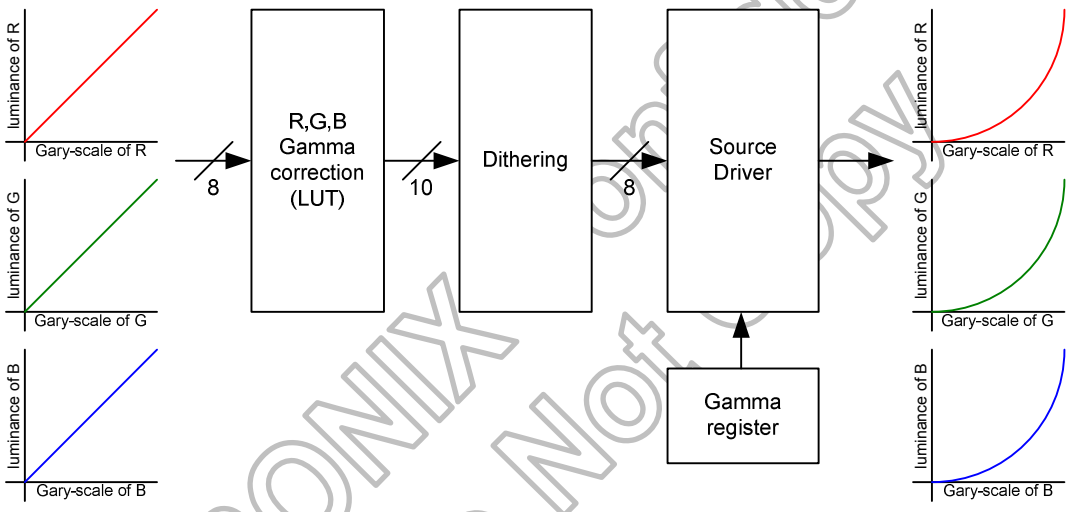


Figure 5.29: Block diagram of digital gamma correction

There are 99 bytes DGC LUT to set R, G, B gamma independently. When DGC_EN=1, R, G, B gamma will mapping V0, V8, V16, ..., V240, V248, V255 voltage to the LUT register setting gray level voltage.

CDh	DGC_R								
Parameter	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st	x	x	x	x	x	x	x	DGC_EN	00
2nd	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	80
3rd	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	80
:	:	:	:	:	:	:	:	:	:
33rd	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	80
34th	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	80

CEh	DGC_G								
Parameter	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	80
2nd	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	80
:	:	:	:	:	:	:	:	:	:
32rd	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	80
33th	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	80

CFh	DGC_B								
Parameter	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	80
2nd	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	80
:	:	:	:	:	:	:	:	:	:
32rd	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	80
33th	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	80

5.5 Sleep Out - command and Self-diagnostic Functions of the display module

5.5.1 Register Loading Detection

Sleep Out-command (11h) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (=increased by 1).

The flow chart for this internal function is following:

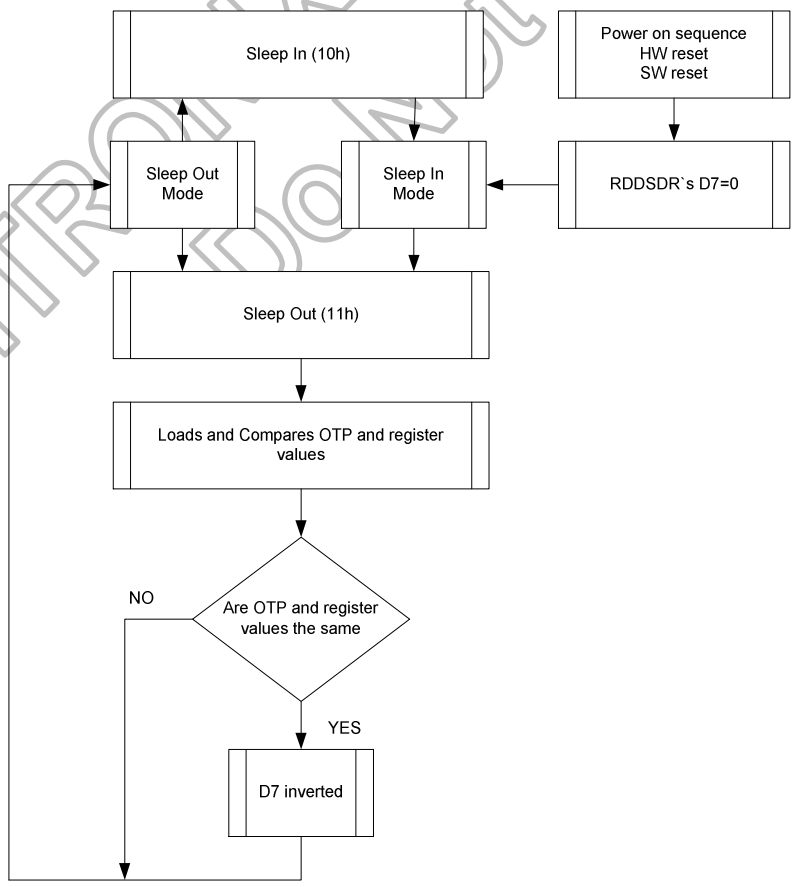


Figure 5.30: Sleep out flow chart–command and self-diagnostic functions

5.5.2 Functionality Detection

Sleep Out-command (11h) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (=increased by 1), which is defined in command "Read Display Self- Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (=increased by 1). The flow chart for this internal function is shown as below.

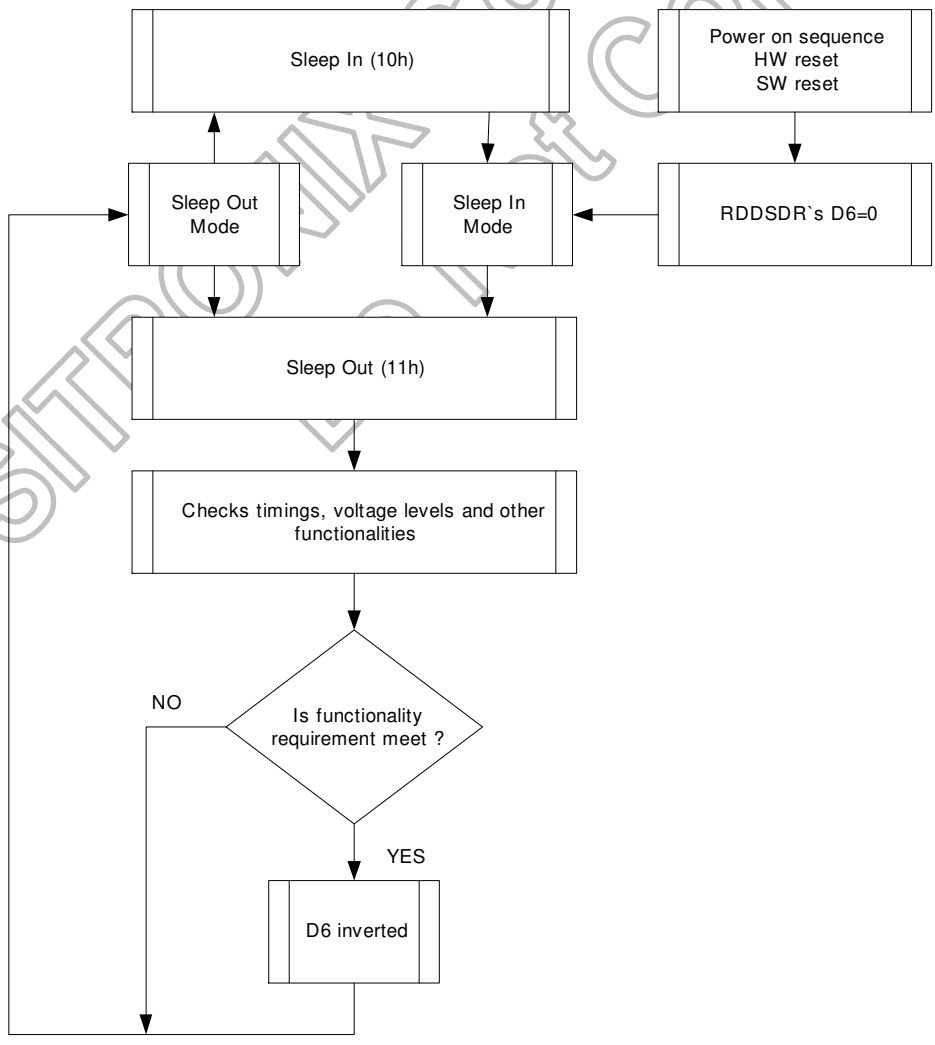


Figure 5.31: Sleep out flow chart internal function detection

5.6 Power on/off Sequence

Power source IOVCC, VCI can be applied and powered down in any order. IOVCC, VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.

During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.

NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

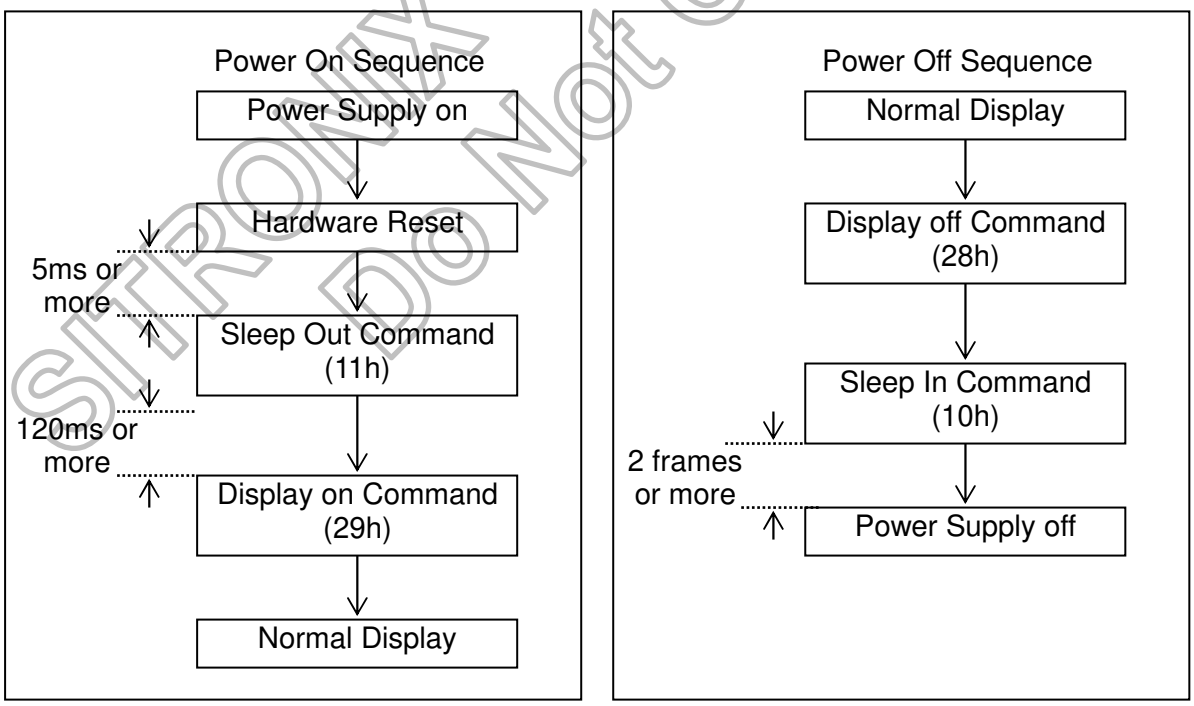


Figure 5.32: The power supply ON/OFF setting for Display ON/OFF and Sleep In/out

5.6.1 Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

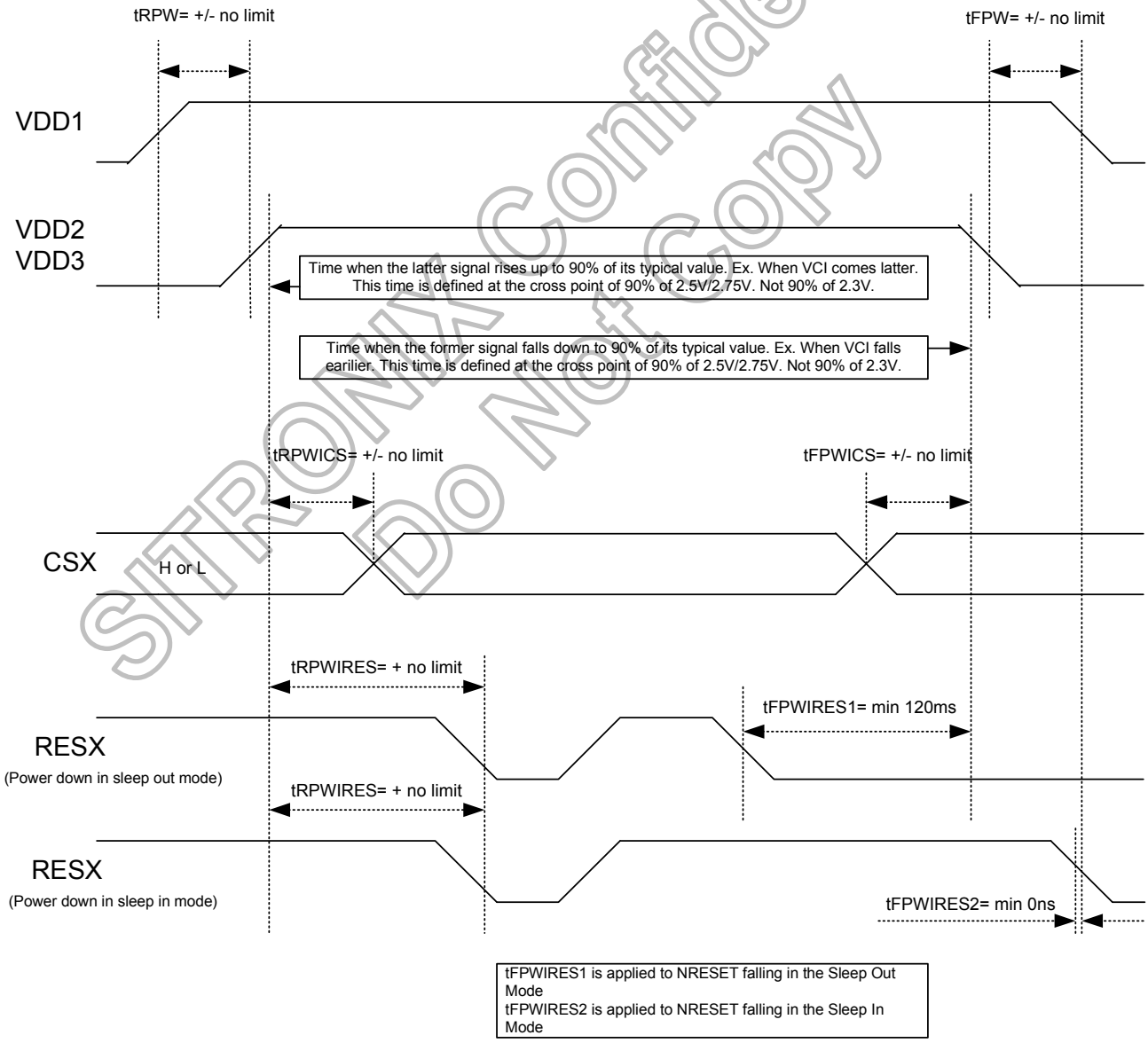
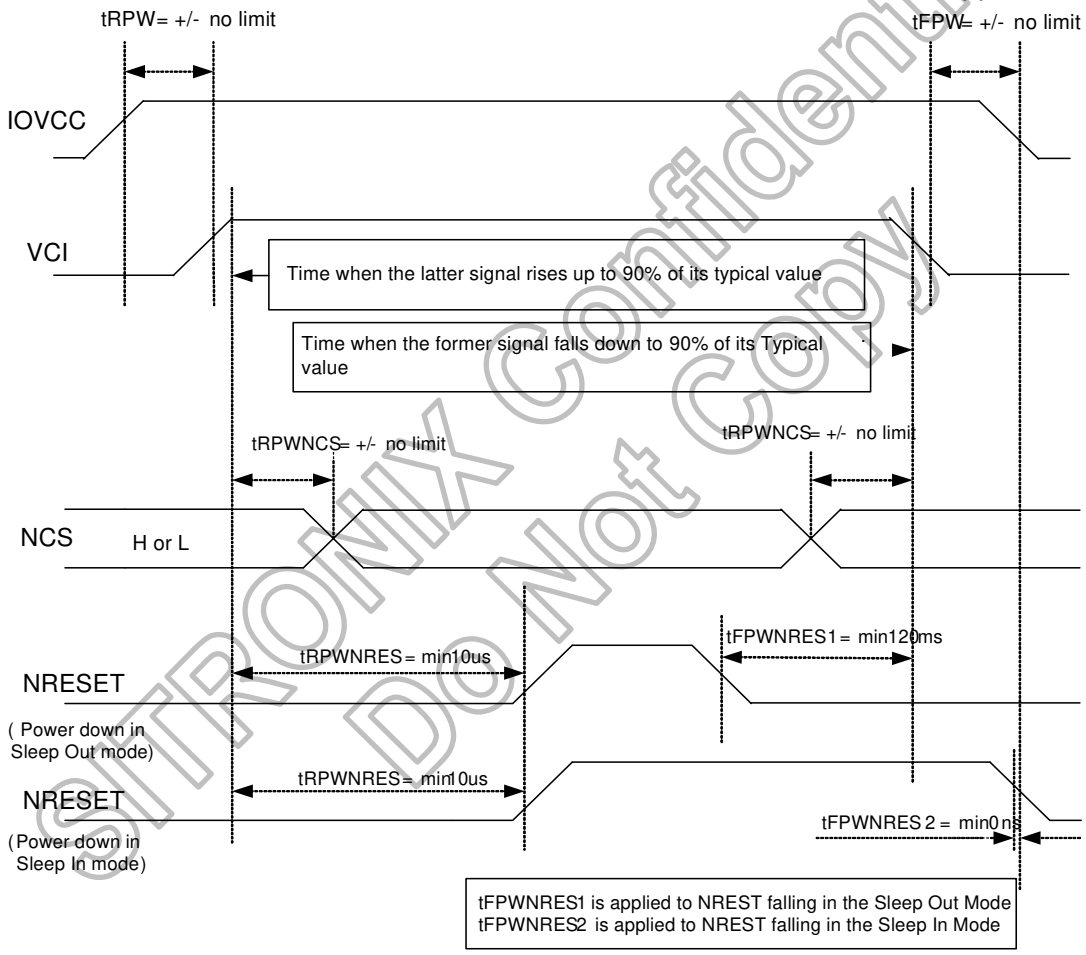


Figure 5.33: Case 1: RESX line is held high or unstable by host at power on

5.6.2 Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.



Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

Figure 5.34: Case 2: RESX line is held low by host at power on

5.7 Power Levels Definition

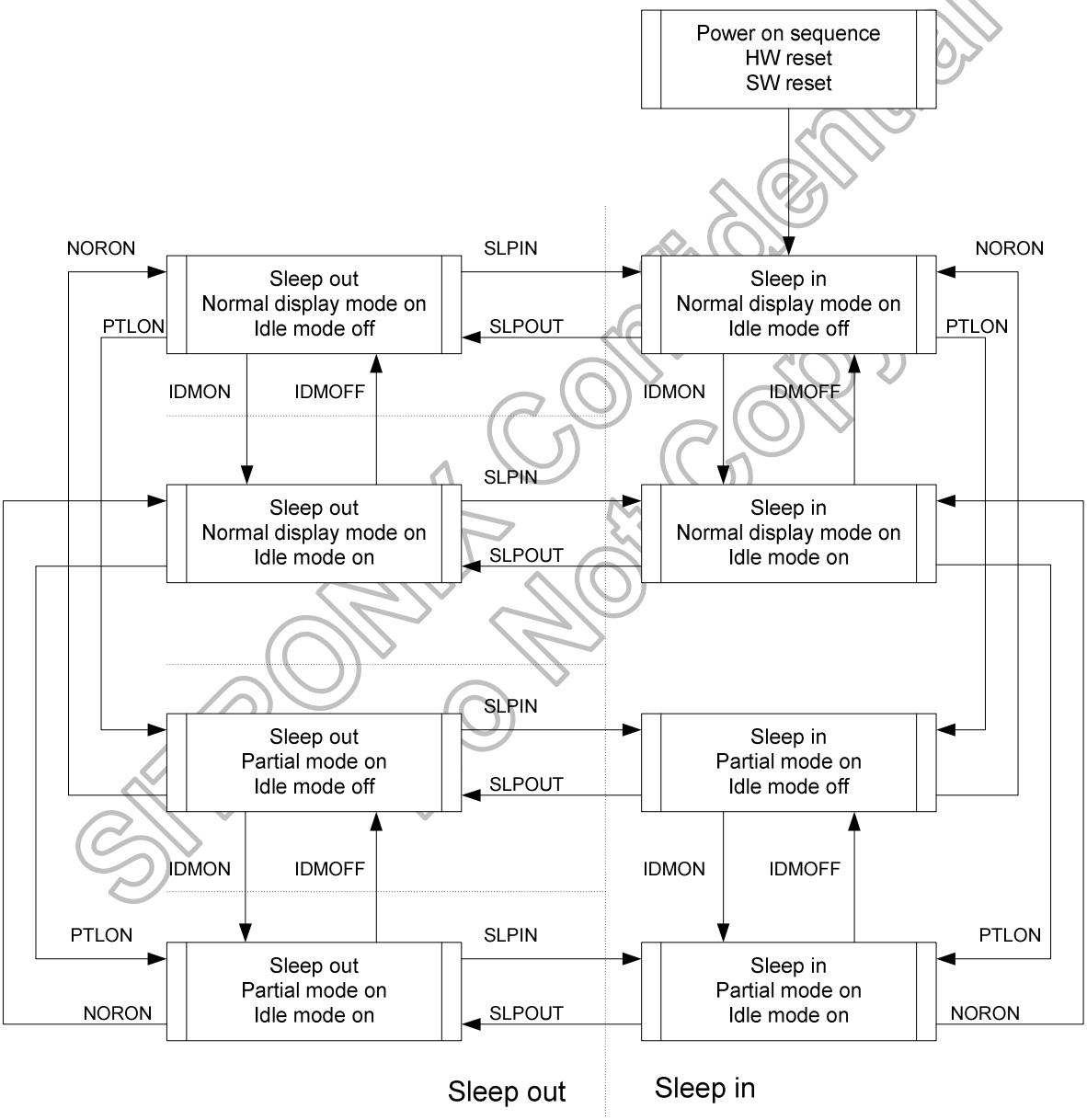


Figure 5.35: Power flow chart for different power modes

5.8 Reset function

5.8.1 Standard Command Default Value

Item	Register		After Power On	After Hardware Reset	After Software Reset
RDDPM	0Ah		08h	08h	08h
RDDMADCTR	0Bh		00h	00h	No Change
RDDCOLMOD	0Ch		70h	70h	No Change
RDDIM	0Dh		00h	00h	00h
RDDSM	0Eh		00h	00h	00h
RDDSDR	0Fh		00h	00h	00h
Sleep In/Out	10h/ 11h		In	In	In
Display On/Off	29h/ 28h		Off	Off	Off
Display mode (normal/partial)	13h/ 12h		Normal	Normal	Normal
Display Inversion On/Off	21h/ 20h		Off	Off	Off
All pixel On/Off	23/ 22h		Off	Off	Off
Display Idle Mode On/Off	39/ 38h		Off	Off	Off
Gamma setting	26H		GC0	GC0	GC0
Memory Data Access Control (MY/MX/RGB)	36H		0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	3AH		70h	70h	No Change
Display Brightness	51h/ 52h		00h	00h	00h
CTRL Display	53h/ 54h		00h	00h	00h
CABC Control	55h/ 56h		00h	00h	00h
ID1	DAH	NO OTP	38h	38h	38h
		OTPed	OTP Value	OTP Value	OTP Value
ID2	DBH	NO OTP	21h	21h	21h
		OTPed	OTP Value	OTP Value	OTP Value
ID3	DCH	NO OTP	1Fh	1Fh	1Fh
		OTPed	OTP Value	OTP Value	OTP Value

Table 5.8: Standard Command Default Value

5.8.2 Input Pins

Input pins	After Power On	After Hardware Reset	After Software Reset
RESX	Input valid	Input valid	Input valid
HS_DSI_D0P HS_DSI_D0P	Input valid	Input valid	Input valid
HS_DSI_D1P HS_DSI_D1P	Input valid	Input valid	Input valid
HS_DSI_D2P HS_DSI_D2P	Input valid	Input valid	Input valid
HS_DSI_D3P HS_DSI_D3N	Input valid	Input valid	Input valid
HS_DSI_CP HS_DSI_CN	Input valid	Input valid	Input valid

Table 5.9: Characteristics of Input Pins

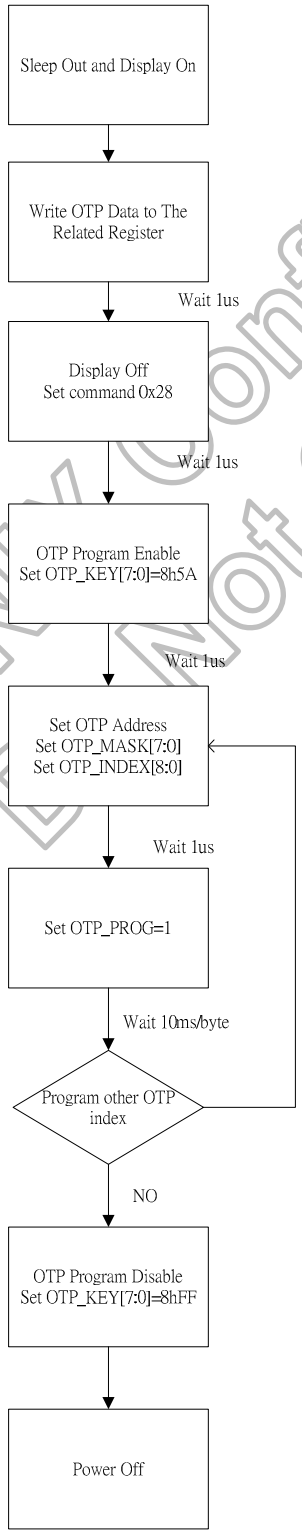
5.8.3 Output or Bi-directional Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
Source Output	VSSA	VSSA	VSSA
DSI_D0P DSI_D0P	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
CGOUTL1~22	VSSA	VSSA	VSSA
CGOUTR1~22	VSSA	VSSA	VSSA

Table 5.10: Characteristics of Output or Bi-direction Pins

5.9 OTP Sequence

5.9.1 OTP Sequence



5.9.2 OTP Standard Programming Table

Programming Index (Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Storage Index (Hex)
01	ID1_1[7:0]								01
	ID2_1[7:0]								02
	ID3_1[7:0]								03
	ID1_2[7:0]								04
	ID2_2[7:0]								05
	ID3_2[7:0]								06
	ID1_3[7:0]								07
	ID2_3[7:0]								08
	ID3_3[7:0]								09
	ID1_4[7:0]								0A
	ID2_4[7:0]								0B
	ID3_4[7:0]								0C
0D	VCOM_F1[7:0]								0D
	VCOM_B1[7:0]								0E
	VCOM_F2[7:0]								0F
	VCOM_B2[7:0]								10
	VCOM_F3[7:0]								11
	VCOM_B3[7:0]								12
	VCOM_F4[7:0]								13
	VCOM_B4[7:0]								14

5.10 CABC

This driver IC provides a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce the power consumption of the luminance source. There are two module architectures for CABC operation as below figure.

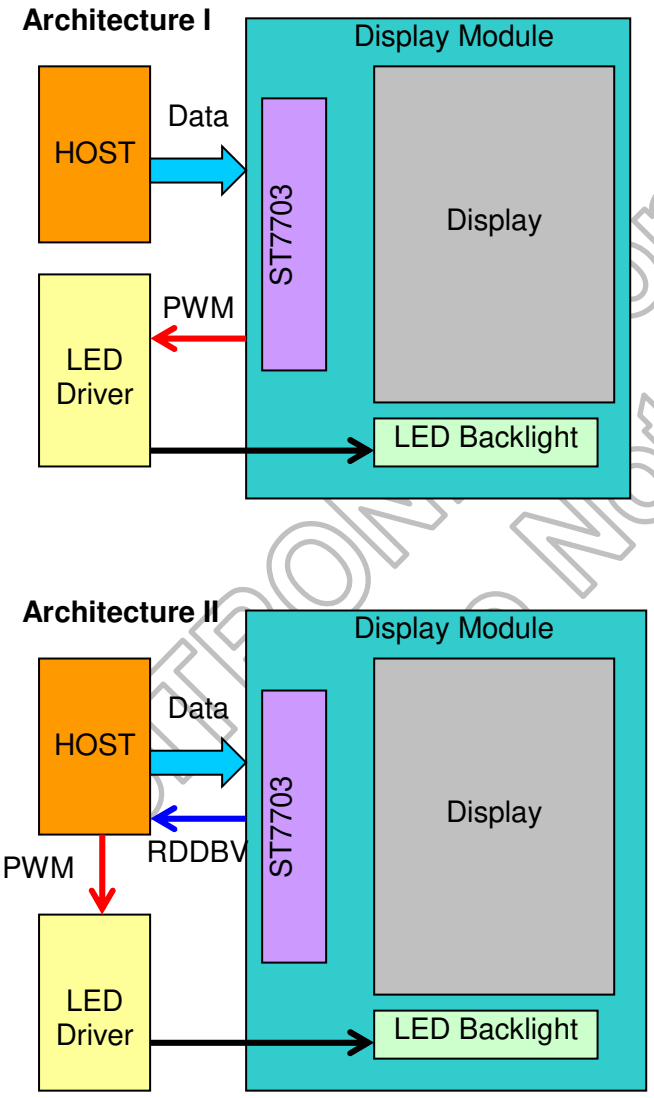
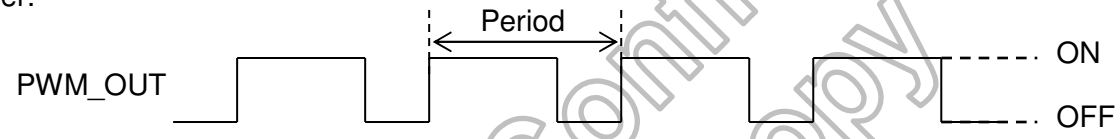


Figure 5.36: Two kinds of CABC Architecture

The driver IC will refer the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. The PWM frequency can be adjusted by PWM_DIV parameters and the calculating equation as below:

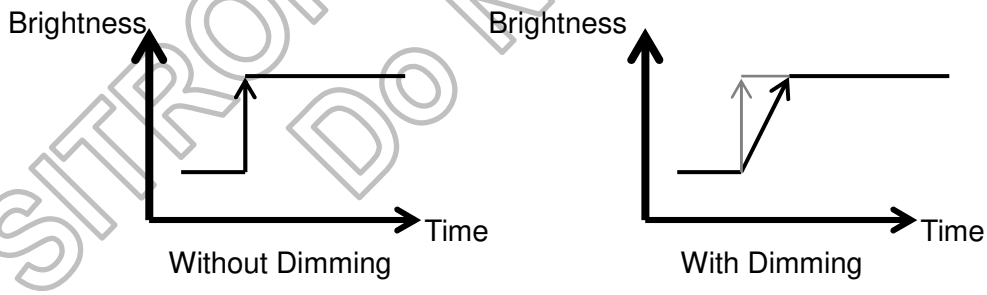
$$Fpwm\_out = \frac{36MHz / (2^{\wedge PWMDIV[2:0]})}{(PWM\_PERIOD[7:0]+1)x255}$$

The figure in the following is the basic timing diagram which is applied ST7703 to control LED driver.



Display Backlight Dimming Control

A dimming function is used when changing from brightness level to another. This dimming function curve is the same in increment and decrement directions. Dimming function can be enabled and disabled by software register. The basic idea is described below.



6. Command Description

6.1 Command Table

Standard Command

(Hex)	Operation code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
00h	NOP	W	0	0	0	0	0	0	0	0	No Operation	-
01h	SWRESET	W	0	0	0	0	0	0	0	1	Software Reset	-
04h	RDDIDIF	R	0	0	0	0	0	1	0	0	Read Display ID	-
			ID1[7:0]								ID1	38h
			ID2[7:0]								ID2	21h
			ID3[7:0]								ID3	1Fh
0Ah	RDDPM	R	0	0	0	0	1	0	1	0	Read display power mode	-
			D7	D6	D5	D4	D3	D2	0	0	-	08h
0Bh	RDDMADCTL	R	0	0	0	0	1	0	1	1	Read display MADCTL	-
			D7	D6	D5	D4	D3	D2	0	0	-	00h
0Ch	RDDCOLMOD	R	0	0	0	0	1	1	0	0	Read display pixel format	-
			-	D6	D5	D4	-	-	-	-	-	70h
0Dh	RDDIM	R	0	0	0	0	1	1	0	1	Read display image mode	-
			D7	D6	D5	0	0	D2	D1	D0	-	00h
0Eh	RDDSM	R	0	0	0	0	1	1	1	0	Read display signal mode	-
			D7	D6	0	0	0	0	0	D0	-	00h
0Fh	RDDSDR	R	0	0	0	0	1	1	1	1	Read display self-diagnostic result	-
			D7	D6	0	0	0	0	0	D0	-	00h
10h	SLPIN	W	0	0	0	1	0	0	0	0	Sleep In	-
11h	SLPOUT	W	0	0	0	1	0	0	0	1	Sleep Out	-

(Hex)	Operation code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
13h	NORON	W	0	0	0	1	0	0	1	1	Normal Display mode	-
20h	INVOFF	W	0	0	1	0	0	0	0	0	Display inversion off	-
21h	INVON	W	0	0	1	0	0	0	0	1	Display inversion on	-
22h	ALLPOFF	W	0	0	1	0	0	0	1	0	All pixel off	-
23h	ALLPON	W	0	0	1	0	0	0	1	1	All pixel on	-
28h	DISPOFF	W	0	0	1	0	1	0	0	0	Display off	-
29h	DISPON	W	0	0	1	0	1	0	0	1	Display on	-
36h	MADCTL	W	0	0	1	1	0	1	1	0	Memory Access Control	-
			MY	MX	x	x	RGB	x	x	x		00h
38h	IDMOFF	W	0	0	1	1	1	0	0	0	Idle mode off	-
39h	IDMON	W	0	0	1	1	1	0	0	1	Idle mode on	-
51h	WRDISBV	W	0	1	0	1	0	0	0	1	Write display brightness value	-
			DBV1[7]	DBV1[6]	DBV1[5]	DBV1[4]	DBV1[3]	DBV1[2]	DBV1[1]	DBV1[0]		00h
			DBV2[7]	DBV2[6]	DBV2[5]	DBV2[4]	DBV2[3]	DBV2[2]	DBV2[1]	DBV2[0]		00h
52h	RDRDISBV	R	0	1	0	1	0	0	1	0	Read display brightness value	-
			DBV1[7]	DBV1[6]	DBV1[5]	DBV1[4]	DBV1[3]	DBV1[2]	DBV1[1]	DBV1[0]		00h
			DBV2[7]	DBV2[6]	DBV2[5]	DBV2[4]	DBV2[3]	DBV2[2]	DBV2[1]	DBV2[0]		00h
53h	WRCTRLD	W	0	1	0	1	0	0	1	1	Write CTRL display	-
			x	x	BCTRL	x	x	DD	BL	x		00h
54h	RDCTRLD	R	0	1	0	1	0	1	0	0	Read CTRL display	-
			x	x	BCTRL	x	x	DD	BL	x		00h
55h	WRCABC	W	0	1	0	1	0	1	0	1	Write CABC mode	-
			x	x	x	x	x	x	C1	C0		00h
56h	RDCABC	R	0	1	0	1	0	1	1	0	Read CABC mode	-
			x	x	x	x	x	x	C1	C0		00h
5Eh	WRCABCMB	W	0	1	0	1	1	1	1	0	Write CABC minimum brightness	-
			CMB1[7]	CMB1[6]	CMB1[5]	CMB1[4]	CMB1[3]	CMB1[2]	CMB1[1]	CMB1[0]		00h
			CMB2[7]	CMB2[6]	CMB2[5]	CMB2[4]	CMB2[3]	CMB2[2]	CMB2[1]	CMB2[0]		00h
5Fh	RDCABCMB	R	0	1	0	1	1	1	1	1	Read CABC minimum brightness	-
			CMB1[7]	CMB1[6]	CMB1[5]	CMB1[4]	CMB1[3]	CMB1[2]	CMB1[1]	CMB1[0]		00h
			CMB2[7]	CMB2[6]	CMB2[5]	CMB2[4]	CMB2[3]	CMB2[2]	CMB2[1]	CMB2[0]		00h
68h	RDABCSDR	R	0	1	0	1	0	1	1	0	Read ABC Self-diagnostic result	-
			D7	D6	x	x	x	x	x	x		00h
70	RDBWLB	R	0	1	1	1	0	0	0	0	Read Black/White Low Bits	-
			Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0		-
71	RDBkx	R	0	1	1	1	0	0	0	1	Read Bkx	-
			Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2		-
72	RDBky	R	0	1	1	1	0	0	1	0	Read Bky	-
			Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2		-
73	RDWx	R	0	1	1	1	0	0	1	1	Read Wx	-
			Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2		-
74	RDWy	R	0	1	1	1	0	1	0	0	Read Wy	-
			Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2		-
75	RDRGLB	R	0	1	1	1	0	1	0	1	Read Red/Green Low Bits	-
			Rx1	Rx0	Ry1	Rx0	Gx1	Gx0	Gy1	Gy0		-
76	RDRx	R	0	1	1	1	0	1	1	0	Read Rx	-
			Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2		-

(Hex)	Operation code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
77	RDRy	R	0	1	1	1	0	1	1	1	Read Ry	-
			Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2		-
78	RDGx	R	0	1	1	1	1	0	0	0	Read Gx	-
			Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2		-
79	RDRy	R	0	1	1	1	1	0	0	1	Read Gy	-
			Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2		-
7A	RDBALB	R	0	1	1	1	1	0	1	0	Read Biue/AColour Low Bits	-
			Bx1	Bx0	By1	Bx0	Ax1	Ax0	Ay1	Ay0		-
7B	RDBx	R	0	1	1	1	1	0	1	1	Read Bx	-
			Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2		-
7C	RDBy	R	0	1	1	1	1	1	0	0	Read By	-
			By9	By8	By7	By6	By5	By4	By3	By2		-
7D	RDAx	R	0	1	1	1	1	1	0	1	Read Ax	-
			Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2		-
7E	RDAy	R	0	1	1	1	1	1	1	0	Read Ay	-
			Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2		-
A1	Read_DDB_start	R	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	-
			x	x	x	x	x	x	x	x		-
			x	x	x	x	x	x	x	x		00h
			x	x	x	x	x	x	x	x		00h
			x	x	x	x	x	x	x	x		00h
			x	x	x	x	x	x	x	x		00h
			1	1	1	1	1	1	1	1		FFh
A8	Read_DDB_continue	R	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.	-
			x	x	x	x	x	x	x	x		00h
			x	x	x	x	x	x	x	x		00h
			x	x	x	x	x	x	x	x		00h
			x	x	x	x	x	x	x	x		00h
DA	RDID1	R	1	1	0	1	1	0	1	0	Read ID1	-
			module's manufacturer[7:0]									38h
DB	RDID2	R	1	1	0	1	1	0	1	1	Read ID2	-
			LCD module/driver version [7:0]									21h
DC	RDID3	R	1	1	0	1	1	1	0	0	Read ID3	-
			LCD module/driver ID[7:0]									1Fh

User Command

(Hex)	Operation code	Para.	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
B9h	SETEXTC		1	0	1	1	1	0	0	1	-
		1	EXTC1[7]	EXTC1[6]	EXTC1[5]	EXTC1[4]	EXTC1[3]	EXTC1[2]	EXTC1[1]	EXTC1[0]	00
		2	EXTC2[7]	EXTC2[6]	EXTC2[5]	EXTC2[4]	EXTC2[3]	EXTC2[2]	EXTC2[1]	EXTC2[0]	00
		3	EXTC3[7]	EXTC3[6]	EXTC3[5]	EXTC3[4]	EXTC3[3]	EXTC3[2]	EXTC3[1]	EXTC3[0]	00
B1h	SETAPID		1	0	1	1	0	0	0	1	-
		1	RES_V_SEL	x	x	x	x	RES_V_[10]	RES_V_[9]	RES_V_[8]	00
		2	x	x	x	x	PWM_DUTY_RESO[2]	PWM_DUTY_RESO[1]	PWM_DUTY_RESO[0]	DBV_TYPE	00
B2h	SETDISP		1	0	1	1	0	0	1	0	
		1	NL[7]	NL[6]	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	C8
		2	RES_V_LSB[1]	RES_V_LSB[0]	BLK_CON[1]	BLK_CON[0]	x	RESO_SEL[2]	RESO_SEL[1]	RESO_SEL[0]	12
		3	WHITE_GND_EN	WHITE_FRAME_SEL[2]	WHITE_FRAME_SEL[1]	WHITE_FRAME_SEL[0]	x	ISC[2]	ISC[1]	ISC[0]	A0
B3h	SETRGBIF		1	0	1	1	0	0	1	1	
		1	VBP_RGB_GEN[7]	VBP_RGB_GEN[6]	VBP_RGB_GEN[5]	VBP_RGB_GEN[4]	VBP_RGB_GEN[3]	VBP_RGB_GEN[2]	VBP_RGB_GEN[1]	VBP_RGB_GEN[0]	28
		2	VFP_RGB_GEN[7]	VFP_RGB_GEN[6]	VFP_RGB_GEN[5]	VFP_RGB_GEN[4]	VFP_RGB_GEN[3]	VFP_RGB_GEN[2]	VFP_RGB_GEN[1]	VFP_RGB_GEN[0]	28
		3	DE_BP_RGB_GEN[7]	DE_BP_RGB_GEN[6]	DE_BP_RGB_GEN[5]	DE_BP_RGB_GEN[4]	DE_BP_RGB_GEN[3]	DE_BP_RGB_GEN[2]	DE_BP_RGB_GEN[1]	DE_BP_RGB_GEN[0]	28
		4	DE_FP_RGB_GEN[7]	DE_FP_RGB_GEN[6]	DE_FP_RGB_GEN[5]	DE_FP_RGB_GEN[4]	DE_FP_RGB_GEN[3]	DE_FP_RGB_GEN[2]	DE_FP_RGB_GEN[1]	DE_FP_RGB_GEN[0]	28
B4h	SETCYC		1	0	1	1	0	1	0	0	
		1	ZINV_S2401_EN	ZINV_G_EVEN_EN	ZINV_EN	ZINV2_EN	x	N_NW[2]	N_NW[1]	N_NW[0]	80
		2	x	x	x	x	x	I_NW[2]	I_NW[1]	I_NW[0]	00

(Hex)	Operation code	Para.	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
B5h	SETBGP		1	0	1	1	0	1	0	1	
		1	x	x	x	VREF_SEL[4]	VREF_SEL[3]	VREF_SEL[2]	VREF_SEL[1]	VREF_SEL[0]	09
		2	x	x	x	NVREF_SEL[4]	NVREF_SEL[3]	NVREF_SEL[2]	NVREF_SEL[1]	NVREF_SEL[0]	09
B6h	SETCOM		1	0	1	1	0	1	1	0	
		1	VCOMDC_F[7]	VCOMDC_F[6]	VCOMDC_F[5]	VCOMDC_F[4]	VCOMDC_F[3]	VCOMDC_F[2]	VCOMDC_F[1]	VCOMDC_F[0]	4D
		2	VCOMDC_B[7]	VCOMDC_B[6]	VCOMDC_B[5]	VCOMDC_B[4]	VCOMDC_B[3]	VCOMDC_B[2]	VCOMDC_B[1]	VCOMDC_B[0]	4D
		3	x	x	x	x	x	VCOM_OTP_TIME[2]	VCOM_OTP_TIME[1]	VCOM_OTP_TIME[0]	00
B7h	SETOTP		1	0	1	1	0	1	1	1	-
		1	OTP_KEY[7]	OTP_KEY[6]	OTP_KEY[5]	OTP_KEY[4]	OTP_KEY[3]	OTP_KEY[2]	OTP_KEY[1]	OTP_KEY[0]	FF
		2	OTP_MASK[7]	OTP_MASK[6]	OTP_MASK[5]	OTP_MASK[4]	OTP_MASK[3]	OTP_MASK[2]	OTP_MASK[1]	OTP_MASK[0]	00
		3	x	VPP_SEL[2]	VPP_SEL[1]	VPP_SEL[0]	x	x	x	OTP_INDEX[8]	30
		4	OTP_INDEX[7]	OTP_INDEX[6]	OTP_INDEX[5]	OTP_INDEX[4]	OTP_INDEX[3]	OTP_INDEX[2]	OTP_INDEX[1]	OTP_INDEX[0]	00
		5	Load_DIS	VPP_EN	OTP_SEL	OTP_PWE	OTP_PTM[1]	OTP_PTM[0]	OTP_POR	OTP_PORG	00
		6	OTP_DATA[7]	OTP_DATA[6]	OTP_DATA[5]	OTP_DATA[4]	OTP_DATA[3]	OTP_DATA[2]	OTP_DATA[1]	OTP_DATA[0]	00
B8h	SET POWER_EXT		1	0	1	1	1	0	0	0	
		1	x	PCCS[2]	PCCS[1]	PCCS[0]	ECP_DC_DIV[3]	ECP_DC_DIV[2]	ECP_DC_DIV[1]	ECP_DC_DIV[0]	34
		2	x	SINGLE_PUMP	DT[1]	DT[0]	SYNC_STB	XDK_ECP[1]	XDK_ECP[0]	x	22
		3	x	x	x	x	x	PFM_DC_DIV[2]	PFM_DC_DIV[1]	PFM_DC_DIV[0]	00
		4	x	x	x	x	x	x	ECP_SYNC_EN	VGX_SYNC_EN	03
		5	A_DC[1]	A_DC[0]	A_DTP[2]	A_DTP[1]	A_DTP[0]	A_DTN[2]	A_DTN[1]	A_DTN[0]	ED
		6	DCS[1]	DCS[0]	DTPS[2]	DTPS[1]	DTPS[0]	DTNS[2]	DTNS[1]	DTNS[0]	00
BAh	SETMIPI		1	0	1	1	1	0	1	0	
		1	x	x	x	x	VC_Main[1]	VC_Main[0]	Lane_Number[1]	Lane_Number[0]	33
		2	DSI_LDO_SEL[2]	DSI_LDO_SEL[1]	DSI_LDO_SEL[0]	x	x	x	RTERM[1]	RTERM[0]	61
		3	x	x	x	x	IHSRX[3]	IHSRX[2]	IHSRX[1]	IHSRX[0]	06
		4	x	x	x	x	Tx_clk_sel[1]	Tx_clk_sel[0]	x	x	F9
		5	HFP_OSC[7]	HFP_OSC[6]	HFP_OSC[5]	HFP_OSC[4]	HFP_OSC[3]	HFP_OSC[2]	HFP_OSC[1]	HFP_OSC[0]	FF
		6	HBP_OSC[7]	HBP_OSC[6]	HBP_OSC[5]	HBP_OSC[4]	HBP_OSC[3]	HBP_OSC[2]	HBP_OSC[1]	HBP_OSC[0]	0A

(Hex)	Operation code	Para.	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
BCh	SET VDC		1	0	1	1	1	1	0	0	
		1	x	NVDDD_SEL[2]	NVDDD_SEL[1]	NVDDD_SEL[0]	x	VDDD_SEL[2]	VDDD_SEL[1]	VDDD_SEL[0]	47
C0h	SETSCR		1	1	0	0	0	0	0	0	-
		1	N_POPON[7]	N_POPON[6]	N_POPON[5]	N_POPON[4]	N_POPON[3]	N_POPON[2]	N_POPON[1]	N_POPON[0]	73
		2	N_NOPON[7]	N_NOPON[6]	N_NOPON[5]	N_NOPON[4]	N_NOPON[3]	N_NOPON[2]	N_NOPON[1]	N_NOPON[0]	73
		3	I_POPON[7]	I_POPON[6]	I_POPON[5]	I_POPON[4]	I_POPON[3]	I_POPON[2]	I_POPON[1]	I_POPON[0]	50
		4	I_NOPON[7]	I_NOPON[6]	I_NOPON[5]	I_NOPON[4]	I_NOPON[3]	I_NOPON[2]	I_NOPON[1]	I_NOPON[0]	50
		5	SCR[31]	SCR[30]	SCR[29]	SCR[28]	SCR[27]	SCR[26]	SCR[25]	SCR[24]	C0
		6	SCR[23]	SCR[22]	SCR[21]	SCR[20]	SCR[19]	SCR[18]	SCR[17]	SCR[16]	00
		7	SCR[15]	SCR[14]	SCR[13]	SCR[12]	SCR[11]	SCR[10]	SCR[9]	SCR[8]	08
		8	SCR[7]	SCR[6]	SCR[5]	SCR[4]	SCR[3]	SCR[2]	SCR[1]	SCR[0]	70
C1h	SETPOWER		1	1	0	0	0	0	0	1	-
		1	VBTHS[3]	VBTHS[2]	VBTHS[1]	VBTHS[0]	VBTLS[3]	VBTLS[2]	VBTLS[1]	VBTLS[0]	53
		2	FBOFF_VGH	FBOFF_VGL	x	x	x	x	x	x	53
		3	x	x	VRP[5]	VRP[4]	VRP[3]	VRP[2]	VRP[1]	VRP[0]	C0
		4	x	x	VRN[5]	VRN[4]	VRN[3]	VRN[2]	VRN[1]	VRN[0]	16
		5	x	x	x	x	x	x	x	x	00
		6	VGL_DET_EN	VGH_DET_EN	VGL_TURBO	VGH_TURBO	x	APS[2]	APS[1]	APS[0]	77
		7	VGH1_L_DIV[3]	VGH1_L_DIV[2]	VGH1_L_DIV[1]	VGH1_L_DIV[0]	VGL1_L_DIV[3]	VGL1_L_DIV[2]	VGL1_L_DIV[1]	VGL1_L_DIV[0]	D1
		8	VGH1_R_DIV[3]	VGH1_R_DIV[2]	VGH1_R_DIV[1]	VGH1_R_DIV[0]	VGL1_R_DIV[3]	VGL1_R_DIV[2]	VGL1_R_DIV[1]	VGL1_R_DIV[0]	CC
		9	VGH2_L_DIV[3]	VGH2_L_DIV[2]	VGH2_L_DIV[1]	VGH2_L_DIV[0]	VGL2_L_DIV[3]	VGL2_L_DIV[2]	VGL2_L_DIV[1]	VGL2_L_DIV[0]	DD
		10	VGH2_R_DIV[3]	VGH2_R_DIV[2]	VGH2_R_DIV[1]	VGH2_R_DIV[0]	VGL2_R_DIV[3]	VGL2_R_DIV[2]	VGL2_R_DIV[1]	VGL2_R_DIV[0]	67
		11	VGH3_L_DIV[3]	VGH3_L_DIV[2]	VGH3_L_DIV[1]	VGH3_L_DIV[0]	VGL3_L_DIV[3]	VGL3_L_DIV[2]	VGL3_L_DIV[1]	VGL3_L_DIV[0]	77
		12	VGH3_R_DIV[3]	VGH3_R_DIV[2]	VGH3_R_DIV[1]	VGH3_R_DIV[0]	VGL3_R_DIV[3]	VGL3_R_DIV[2]	VGL3_R_DIV[1]	VGL3_R_DIV[0]	33
		13	VGH4_L_DIV[3]	VGH4_L_DIV[2]	VGH4_L_DIV[1]	VGH4_L_DIV[0]	VGL4_L_DIV[3]	VGL4_L_DIV[2]	VGL4_L_DIV[1]	VGL4_L_DIV[0]	33
		14	VGH4_R_DIV[3]	VGH4_R_DIV[2]	VGH4_R_DIV[1]	VGH4_R_DIV[0]	VGL4_R_DIV[3]	VGL4_R_DIV[2]	VGL4_R_DIV[1]	VGL4_R_DIV[0]	11
		15	VGH5_L_DIV[3]	VGH5_L_DIV[2]	VGH5_L_DIV[1]	VGH5_L_DIV[0]	VGL5_L_DIV[3]	VGL5_L_DIV[2]	VGL5_L_DIV[1]	VGL5_L_DIV[0]	11
		16	VGH5_R_DIV[3]	VGH5_R_DIV[2]	VGH5_R_DIV[1]	VGH5_R_DIV[0]	VGL5_R_DIV[3]	VGL5_R_DIV[2]	VGL5_R_DIV[1]	VGL5_R_DIV[0]	00
C3h	SETID		1	1	0	0	0	0	1	1	-
		1	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	38h
		2	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	21h
		3	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	1Fh
		4						ID_TIMES2	ID_TIMES1	ID_TIMES0	
C4h	SETDDB		1	1	0	0	0	1	0	0	-
		1	DDB1[7]	DDB1[6]	DDB1[5]	DDB1[4]	DDB1[3]	DDB1[2]	DDB1[1]	DDB1[0]	00h
		2	DDB2[7]	DDB2[6]	DDB2[5]	DDB2[4]	DDB2[3]	DDB2[2]	DDB2[1]	DDB2[0]	00h
		3	DDB3[7]	DDB3[6]	DDB3[5]	DDB3[4]	DDB3[3]	DDB3[2]	DDB3[1]	DDB3[0]	00h
		4	DDB4[7]	DDB4[6]	DDB4[5]	DDB4[4]	DDB4[3]	DDB4[2]	DDB4[1]	DDB4[0]	00h
C6h	SETECO		1	1	0	0	0	1	1	0	-
		1	ECO0[7]	ECO0[6]	ECO0[5]	ECO0[4]	ECO0[3]	ECO0[2]	ECO0[1]	ECO0[0]	01
		2	ECO1[7]	ECO1[6]	ECO1[5]	ECO1[4]	ECO1[3]	ECO1[2]	ECO1[1]	ECO1[0]	00
		3	ECO2[7]	ECO2[6]	ECO2[5]	ECO2[4]	ECO2[3]	ECO2[2]	ECO2[1]	ECO2[0]	CF
		4	ECO3[7]	ECO3[6]	ECO3[5]	ECO3[4]	ECO3[3]	ECO3[2]	ECO3[1]	ECO3[0]	FF
		5	ECO4[7]	ECO4[6]	ECO4[5]	ECO4[4]	ECO4[3]	ECO4[2]	ECO4[1]	ECO4[0]	00
		6	ECO5[7]	ECO5[6]	ECO5[5]	ECO5[4]	ECO5[3]	ECO5[2]	ECO5[1]	ECO5[0]	FF

(Hex)	Operation code	Para.	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
C7h	SETIO		1	1	0	0	0	1	1	1	-
		1	PWM_OE	x	INVPWM	VOUT_OE	HOUT_OE	x	x	x	00
		2	x	V_DELAY[2]	V_DELAY[1]	V_DELAY[0]	x	H_DELAY[2]	H_DELAY[1]	H_DELAY[0]	00
C8h	SETCABC		1	1	0	0	1	0	0	0	-
		1	x	PWMDIV[2]	PWMDIV[1]	PWMDIV[0]	x	x	x	x	10
		2	PWM_PERIOD[7]	PWM_PERIOD[6]	PWM_PERIOD[5]	PWM_PERIOD[4]	PWM_PERIOD[3]	PWM_PERIOD[2]	PWM_PERIOD[1]	PWM_PERIOD[0]	40
CBh	SETCLOCK		1	1	0	0	1	0	1	1	-
		1	OSC_DIV2	FORCE_ULP[2]	FORCE_ULP[1]	FORCE_ULP[0]	x	FRADJ[2]	FRADJ[1]	FRADJ[0]	03
CCh	SETPANEL		1	1	0	0	1	1	0	0	-
		1	x	x	x	x	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	00h
CDh	DGC_R		1	1	0	0	1	1	0	1	-
		1	x	x	x	x	x	DITH_EN	DITH_OPT	DGC_EN	00
		2	DGC_LUT_R00[7]	DGC_LUT_R00[6]	DGC_LUT_R00[5]	DGC_LUT_R00[4]	DGC_LUT_R00[3]	DGC_LUT_R00[2]	DGC_LUT_R00[1]	DGC_LUT_R00[0]	80
		3	DGC_LUT_R01[7]	DGC_LUT_R01[6]	DGC_LUT_R01[5]	DGC_LUT_R01[4]	DGC_LUT_R01[3]	DGC_LUT_R01[2]	DGC_LUT_R01[1]	DGC_LUT_R01[0]	80
		4	DGC_LUT_R02[7]	DGC_LUT_R02[6]	DGC_LUT_R02[5]	DGC_LUT_R02[4]	DGC_LUT_R02[3]	DGC_LUT_R02[2]	DGC_LUT_R02[1]	DGC_LUT_R02[0]	80
		:	:	:	:	:	:	:	:	:	
		10	DGC_LUT_R08[7]	DGC_LUT_R08[6]	DGC_LUT_R08[5]	DGC_LUT_R08[4]	DGC_LUT_R08[3]	DGC_LUT_R08[2]	DGC_LUT_R08[1]	DGC_LUT_R08[0]	80
		11	DGC_LUT_R09[7]	DGC_LUT_R09[6]	DGC_LUT_R09[5]	DGC_LUT_R09[4]	DGC_LUT_R09[3]	DGC_LUT_R09[2]	DGC_LUT_R09[1]	DGC_LUT_R09[0]	80
		12	DGC_LUT_R10[7]	DGC_LUT_R10[6]	DGC_LUT_R10[5]	DGC_LUT_R10[4]	DGC_LUT_R10[3]	DGC_LUT_R10[2]	DGC_LUT_R10[1]	DGC_LUT_R10[0]	80
		13	DGC_LUT_R11[7]	DGC_LUT_R11[6]	DGC_LUT_R11[5]	DGC_LUT_R11[4]	DGC_LUT_R11[3]	DGC_LUT_R11[2]	DGC_LUT_R11[1]	DGC_LUT_R11[0]	80
		:	:	:	:	:	:	:	:	:	
		20	DGC_LUT_R18[7]	DGC_LUT_R18[6]	DGC_LUT_R18[5]	DGC_LUT_R18[4]	DGC_LUT_R18[3]	DGC_LUT_R18[2]	DGC_LUT_R18[1]	DGC_LUT_R18[0]	80
		21	DGC_LUT_R19[7]	DGC_LUT_R19[6]	DGC_LUT_R19[5]	DGC_LUT_R19[4]	DGC_LUT_R19[3]	DGC_LUT_R19[2]	DGC_LUT_R19[1]	DGC_LUT_R19[0]	80
		22	DGC_LUT_R20[7]	DGC_LUT_R20[6]	DGC_LUT_R20[5]	DGC_LUT_R20[4]	DGC_LUT_R20[3]	DGC_LUT_R20[2]	DGC_LUT_R20[1]	DGC_LUT_R20[0]	80
		23	DGC_LUT_R21[7]	DGC_LUT_R21[6]	DGC_LUT_R21[5]	DGC_LUT_R21[4]	DGC_LUT_R21[3]	DGC_LUT_R21[2]	DGC_LUT_R21[1]	DGC_LUT_R21[0]	80
		:	:	:	:	:	:	:	:	:	
		31	DGC_LUT_R29[7]	DGC_LUT_R29[6]	DGC_LUT_R29[5]	DGC_LUT_R29[4]	DGC_LUT_R29[3]	DGC_LUT_R29[2]	DGC_LUT_R29[1]	DGC_LUT_R29[0]	80
		32	DGC_LUT_R30[7]	DGC_LUT_R30[6]	DGC_LUT_R30[5]	DGC_LUT_R30[4]	DGC_LUT_R30[3]	DGC_LUT_R30[2]	DGC_LUT_R30[1]	DGC_LUT_R30[0]	80
		33	DGC_LUT_R31[7]	DGC_LUT_R31[6	DGC_LUT_R31[5]	DGC_LUT_R31[4]	DGC_LUT_R31[3]	DGC_LUT_R31[2]	DGC_LUT_R31[1]	DGC_LUT_R31[0]	80
		34	DGC_LUT_R32[7]	DGC_LUT_R32[6	DGC_LUT_R32[5]	DGC_LUT_R32[4]	DGC_LUT_R32[3]	DGC_LUT_R32[2]	DGC_LUT_R32[1]	DGC_LUT_R32[0]	80

(Hex)	Operation code	Para.	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
CEh	DGC_G		1	1	0	0	1	1	1	0	
		1	DGC_LUT_G00[7]	DGC_LUT_G00[6]	DGC_LUT_G00[5]	DGC_LUT_G00[4]	DGC_LUT_G00[3]	DGC_LUT_G00[2]	DGC_LUT_G00[1]	DGC_LUT_G00[0]	80
		2	DGC_LUT_G01[7]	DGC_LUT_G01[6]	DGC_LUT_G01[5]	DGC_LUT_G01[4]	DGC_LUT_G01[3]	DGC_LUT_G01[2]	DGC_LUT_G01[1]	DGC_LUT_G01[0]	80
		3	DGC_LUT_G02[7]	DGC_LUT_G02[6]	DGC_LUT_G02[5]	DGC_LUT_G02[4]	DGC_LUT_G02[3]	DGC_LUT_G02[2]	DGC_LUT_G02[1]	DGC_LUT_G02[0]	80
		4	DGC_LUT_G03[7]	DGC_LUT_G03[6]	DGC_LUT_G03[5]	DGC_LUT_G03[4]	DGC_LUT_G03[3]	DGC_LUT_G03[2]	DGC_LUT_G03[1]	DGC_LUT_G03[0]	80
		:	:	:	:	:	:	:	:	:	
		10	DGC_LUT_G09[7]	DGC_LUT_G09[6]	DGC_LUT_G09[5]	DGC_LUT_G09[4]	DGC_LUT_G09[3]	DGC_LUT_G09[2]	DGC_LUT_G09[1]	DGC_LUT_G09[0]	80
		11	DGC_LUT_G10[7]	DGC_LUT_G10[6]	DGC_LUT_G10[5]	DGC_LUT_G10[4]	DGC_LUT_G10[3]	DGC_LUT_G10[2]	DGC_LUT_G10[1]	DGC_LUT_G10[0]	80
		12	DGC_LUT_G11[7]	DGC_LUT_G11[6]	DGC_LUT_G11[5]	DGC_LUT_G11[4]	DGC_LUT_G11[3]	DGC_LUT_G11[2]	DGC_LUT_G11[1]	DGC_LUT_G11[0]	80
		13	DGC_LUT_G12[7]	DGC_LUT_G12[6]	DGC_LUT_G12[5]	DGC_LUT_G12[4]	DGC_LUT_G12[3]	DGC_LUT_G12[2]	DGC_LUT_G12[1]	DGC_LUT_G12[0]	80
		:	:	:	:	:	:	:	:	:	
		19	DGC_LUT_G18[7]	DGC_LUT_G18[6]	DGC_LUT_G18[5]	DGC_LUT_G18[4]	DGC_LUT_G18[3]	DGC_LUT_G18[2]	DGC_LUT_G18[1]	DGC_LUT_G18[0]	80
		20	DGC_LUT_G19[7]	DGC_LUT_G19[6]	DGC_LUT_G19[5]	DGC_LUT_G19[4]	DGC_LUT_G19[3]	DGC_LUT_G19[2]	DGC_LUT_G19[1]	DGC_LUT_G19[0]	80
		21	DGC_LUT_G20[7]	DGC_LUT_G20[6]	DGC_LUT_G20[5]	DGC_LUT_G20[4]	DGC_LUT_G20[3]	DGC_LUT_G20[2]	DGC_LUT_G20[1]	DGC_LUT_G20[0]	80
		22	DGC_LUT_G21[7]	DGC_LUT_G21[6]	DGC_LUT_G21[5]	DGC_LUT_G21[4]	DGC_LUT_G21[3]	DGC_LUT_G21[2]	DGC_LUT_G21[1]	DGC_LUT_G21[0]	80
		:	:	:	:	:	:	:	:	:	
		30	DGC_LUT_G29[7]	DGC_LUT_G29[6]	DGC_LUT_G29[5]	DGC_LUT_G29[4]	DGC_LUT_G29[3]	DGC_LUT_G29[2]	DGC_LUT_G29[1]	DGC_LUT_G29[0]	80
		31	DGC_LUT_G30[7]	DGC_LUT_G30[6]	DGC_LUT_G30[5]	DGC_LUT_G30[4]	DGC_LUT_G30[3]	DGC_LUT_G30[2]	DGC_LUT_G30[1]	DGC_LUT_G30[0]	80
		32	DGC_LUT_G31[7]	DGC_LUT_G31[6]	DGC_LUT_G31[5]	DGC_LUT_G31[4]	DGC_LUT_G31[3]	DGC_LUT_G31[2]	DGC_LUT_G31[1]	DGC_LUT_G31[0]	80
		33	DGC_LUT_G32[7]	DGC_LUT_G32[6	DGC_LUT_G32[5]	DGC_LUT_G32[4]	DGC_LUT_G32[3]	DGC_LUT_G32[2]	DGC_LUT_G32[1]	DGC_LUT_G32[0]	80
CFh	DGC_B		1	1	0	0	1	1	1	1	
		1	DGC_LUT_B00[7]	DGC_LUT_B00[6]	DGC_LUT_B00[5]	DGC_LUT_B00[4]	DGC_LUT_B00[3]	DGC_LUT_B00[2]	DGC_LUT_B00[1]	DGC_LUT_B00[0]	80
		2	DGC_LUT_B01[7]	DGC_LUT_B01[6]	DGC_LUT_B01[5]	DGC_LUT_B01[4]	DGC_LUT_B01[3]	DGC_LUT_B01[2]	DGC_LUT_B01[1]	DGC_LUT_B01[0]	80
		3	DGC_LUT_B02[7]	DGC_LUT_B02[6]	DGC_LUT_B02[5]	DGC_LUT_B02[4]	DGC_LUT_B02[3]	DGC_LUT_B02[2]	DGC_LUT_B02[1]	DGC_LUT_B02[0]	80
		4	DGC_LUT_B03[7]	DGC_LUT_B03[6]	DGC_LUT_B03[5]	DGC_LUT_B03[4]	DGC_LUT_B03[3]	DGC_LUT_B03[2]	DGC_LUT_B03[1]	DGC_LUT_B03[0]	80
		:	:	:	:	:	:	:	:	:	
		10	DGC_LUT_B09[7]	DGC_LUT_B09[6]	DGC_LUT_B09[5]	DGC_LUT_B09[4]	DGC_LUT_B09[3]	DGC_LUT_B09[2]	DGC_LUT_B09[1]	DGC_LUT_B09[0]	80
		11	DGC_LUT_B10[7]	DGC_LUT_B10[6]	DGC_LUT_B10[5]	DGC_LUT_B10[4]	DGC_LUT_B10[3]	DGC_LUT_B10[2]	DGC_LUT_B10[1]	DGC_LUT_B10[0]	80
		12	DGC_LUT_B11[7]	DGC_LUT_B11[6]	DGC_LUT_B11[5]	DGC_LUT_B11[4]	DGC_LUT_B11[3]	DGC_LUT_B11[2]	DGC_LUT_B11[1]	DGC_LUT_B11[0]	80
		13	DGC_LUT_B12[7]	DGC_LUT_B12[6]	DGC_LUT_B12[5]	DGC_LUT_B12[4]	DGC_LUT_B12[3]	DGC_LUT_B12[2]	DGC_LUT_B12[1]	DGC_LUT_B12[0]	80
		:	:	:	:	:	:	:	:	:	
		19	DGC_LUT_B18[7]	DGC_LUT_B18[6]	DGC_LUT_B18[5]	DGC_LUT_B18[4]	DGC_LUT_B18[3]	DGC_LUT_B18[2]	DGC_LUT_B18[1]	DGC_LUT_B18[0]	80
		20	DGC_LUT_B19[7]	DGC_LUT_B19[6]	DGC_LUT_B19[5]	DGC_LUT_B19[4]	DGC_LUT_B19[3]	DGC_LUT_B19[2]	DGC_LUT_B19[1]	DGC_LUT_B19[0]	80
		21	DGC_LUT_B20[7]	DGC_LUT_B20[6]	DGC_LUT_B20[5]	DGC_LUT_B20[4]	DGC_LUT_B20[3]	DGC_LUT_B20[2]	DGC_LUT_B20[1]	DGC_LUT_B20[0]	80
		:	:	:	:	:	:	:	:	:	
		30	DGC_LUT_B29[7]	DGC_LUT_B29[6]	DGC_LUT_B29[5]	DGC_LUT_B29[4]	DGC_LUT_B29[3]	DGC_LUT_B29[2]	DGC_LUT_B29[1]	DGC_LUT_B29[0]	80
		31	DGC_LUT_B30[7]	DGC_LUT_B30[6]	DGC_LUT_B30[5]	DGC_LUT_B30[4]	DGC_LUT_B30[3]	DGC_LUT_B30[2]	DGC_LUT_B30[1]	DGC_LUT_B30[0]	80

		32	DGC_LUT _B31[7]	DGC_LUT _B31[6]	DGC_LUT _B31[5]	DGC_LUT _B31[4]	DGC_LUT _B31[3]	DGC_LUT _B31[2]	DGC_LUT _B31[1]	DGC_LUT _B31[0]	80
		33	DGC_LUT _B32[7]	DGC_LUT _B32[6	DGC_LUT _B32[5]	DGC_LUT _B32[4]	DGC_LUT _B32[3]	DGC_LUT _B32[2]	DGC_LUT _B32[1]	DGC_LUT _B32[0]	80

(Hex)	Operation code	Para.	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
			1	1	0	0	0	0	0	1	
		1	x	x	PVR0[5]	PVR0[4]	PVR0[3]	PVR0[2]	PVR0[1]	PVR0[0]	00
		2	x	x	PVR1[5]	PVR1[4]	PVR1[3]	PVR1[2]	PVR1[1]	PVR1[0]	11
		3	x	x	PVR2[5]	PVR2[4]	PVR2[3]	PVR2[2]	PVR2[1]	PVR2[0]	17
		4	x	x	PVR3[5]	PVR3[4]	PVR3[3]	PVR3[2]	PVR3[1]	PVR3[0]	2C
		5	x	x	PVR4[5]	PVR4[4]	PVR4[3]	PVR4[2]	PVR4[1]	PVR4[0]	32
		6	x	x	PVR5[5]	PVR5[4]	PVR5[3]	PVR5[2]	PVR5[1]	PVR5[0]	3F
		7	x	PPR0[6]	PPR0[5]	PPR0[4]	PPR0[3]	PPR0[2]	PPR0[1]	PPR0[0]	49
		8	x	PPR1[6]	PPR1[5]	PPR1[4]	PPR1[3]	PPR1[2]	PPR1[1]	PPR1[0]	3E
		9	x	x	x	PPK0[4]	PPK0[3]	PPK0[2]	PPK0[1]	PPK0[0]	07
		10	x	x	x	PPK1[4]	PPK1[3]	PPK1[2]	PPK1[1]	PPK1[0]	0D
		11	x	x	x	PPK2[4]	PPK2[3]	PPK2[2]	PPK2[1]	PPK2[0]	0E
		12	x	x	x	PPK3[4]	PPK3[3]	PPK3[2]	PPK3[1]	PPK3[0]	12
		13	x	x	x	PPK4[4]	PPK4[3]	PPK4[2]	PPK4[1]	PPK4[0]	13
		14	x	x	x	PPK5[4]	PPK5[3]	PPK5[2]	PPK5[1]	PPK5[0]	11
		15	x	x	x	PPK6[4]	PPK6[3]	PPK6[2]	PPK6[1]	PPK6[0]	13
		16	x	x	x	PPK7[4]	PPK7[3]	PPK7[2]	PPK7[1]	PPK7[0]	10
E0h	SETGAMMA	17	x	x	x	PPK8[4]	PPK8[3]	PPK8[2]	PPK8[1]	PPK8[0]	17
		18	x	x	NVR0[5]	NVR0[4]	NVR0[3]	NVR0[2]	NVR0[1]	NVR0[0]	00
		19	x	x	NVR1[5]	NVR1[4]	NVR1[3]	NVR1[2]	NVR1[1]	NVR1[0]	11
		20	x	x	NVR2[5]	NVR2[4]	NVR2[3]	NVR2[2]	NVR2[1]	NVR2[0]	17
		21	x	x	NVR3[5]	NVR3[4]	NVR3[3]	NVR3[2]	NVR3[1]	NVR3[0]	2C
		22	x	x	NVR4[5]	NVR4[4]	NVR4[3]	NVR4[2]	NVR4[1]	NVR4[0]	32
		23	x	x	NVR5[5]	NVR5[4]	NVR5[3]	NVR5[2]	NVR5[1]	NVR5[0]	3F
		24	x	NPR0[6]	NPR0[5]	NPR0[4]	NPR0[3]	NPR0[2]	NPR0[1]	NPR0[0]	49
		25	x	NPR1[6]	NPR1[5]	NPR1[4]	NPR1[3]	NPR1[2]	NPR1[1]	NPR1[0]	3E
		26	x	x	x	NPK0[4]	NPK0[3]	NPK0[2]	NPK0[1]	NPK0[0]	07
		27	x	x	x	NPK1[4]	NPK1[3]	NPK1[2]	NPK1[1]	NPK1[0]	0D
		28	x	x	x	NPK2[4]	NPK2[3]	NPK2[2]	NPK2[1]	NPK2[0]	0E
		29	x	x	x	NPK3[4]	NPK3[3]	NPK3[2]	NPK3[1]	NPK3[0]	12
		30	x	x	x	NPK4[4]	NPK4[3]	NPK4[2]	NPK4[1]	NPK4[0]	13
		31	x	x	x	NPK5[4]	NPK5[3]	NPK5[2]	NPK5[1]	NPK5[0]	11
		32	x	x	x	NPK6[4]	NPK6[3]	NPK6[2]	NPK6[1]	NPK6[0]	13
		33	x	x	x	NPK7[4]	NPK7[3]	NPK7[2]	NPK7[1]	NPK7[0]	10
		34	x	x	x	NPK8[4]	NPK8[3]	NPK8[2]	NPK8[1]	NPK8[0]	17

(Hex)	Operation code	Para.	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
E3h	SETEQ		1	1	1	0	0	0	1	1	-
		1	PNOEQ[7]	PNOEQ[6]	PNOEQ[5]	PNOEQ[4]	PNOEQ[3]	PNOEQ[2]	PNOEQ[1]	PNOEQ[0]	00
		2	NNOEQ[7]	NNOEQ[6]	PEOEQ[5]	NNOEQ[4]	NNOEQ[3]	NNOEQ[2]	NNOEQ[1]	NNOEQ[0]	00
		3	PEQGND[7]	PEQGND[6]	PEQGND[5]	PEQGND[4]	PEQGND[3]	PEQGND[2]	PEQGND[1]	PEQGND[0]	03
		4	NEQGND[7]	NEQGND[6]	NEQGND[5]	NEQGND[4]	NEQGND[3]	NEQGND[2]	NEQGND[1]	NEQGND[0]	03
		5	PEQVCI[7]	PEQVCI[6]	PEQVCI[5]	PEQVCI[4]	PEQVCI[3]	PEQVCI[2]	PEQVCI[1]	PEQVCI[0]	03
		6	NEQVCI[7]	NEQVCI[6]	NEQVCI[5]	NEQVCI[4]	NEQVCI[3]	NEQVCI[2]	NEQVCI[1]	NEQVCI[0]	03
		7	PEQVCI1[7]	PEQVCI1[6]	PEQVCI1[5]	PEQVCI1[4]	PEQVCI1[3]	PEQVCI1[2]	PEQVCI1[1]	PEQVCI1[0]	03
		8	NEQVCI1[7]	NEQVCI1[6]	NEQVCI1[5]	NEQVCI1[4]	NEQVCI1[3]	NEQVCI1[2]	NEQVCI1[1]	NEQVCI1[0]	03
		9	x	x	x	x	x	x	x	x	00
		10	x	x	x	x	x	x	x	x	00
		11	x	x	x	x	x	x	x	x	00
		12	x	x	x	x	x	x	x	x	00
		13	ESD_DET_DATA_WHITE	ESD_WHITE_EN	ESD_OPT_P[1]	ESD_OPT_P[0]	ESD_OPT_G[1]	ESD_OPT_G[0]	ESD_OPT_S[1]	ESD_OPT_S[0]	C0
		14	x	x	x	SLPIN_OPTION	VEDIO_NO_CHECK_EN	ESD_WHITE_GND_EN	ESD_DET_TIME_SEL[1]	ESD_DET_TIME_SEL[0]	14
E4h	SET_ROI		1	1	1	0	0	1	0	0	-
		1	x	x	x	x	x	x	x	CE_MASK	01
E5h	SETCOLOR_EN		1	1	1	0	0	1	0	1	-
		1	SP_LEVEL[1]	SP_LEVEL[0]	CE_EN	x	x	x	x	x	00
		2	x	x	x	x	X	x	x	x	00
		3	x	x	x	Blue_3[12]	Blue_3[11]	Blue_3[10]	Blue_3[9]	Blue_3[8]	08
		4	Blue_3[7]	Blue_3[6]	Blue_3[5]	Blue_3[4]	Blue_3[3]	Blue_3[2]	Blue_3[1]	Blue_3[0]	32
		5	x	x	x	Blue_2[12]	Blue_2[11]	Blue_2[10]	Blue_2[9]	Blue_2[8]	1c
		6	Blue_2[7]	Blue_2[6]	Blue_2[5]	Blue_2[4]	Blue_2[3]	Blue_2[2]	Blue_2[1]	Blue_2[0]	71
		7	x	x	x	Blue_1[12]	Blue_1[11]	Blue_1[10]	Blue_1[9]	Blue_1[8]	1F
		8	Blue_1[7]	Blue_1[6]	Blue_1[5]	Blue_1[4]	Blue_1[3]	Blue_1[2]	Blue_1[1]	Blue_1[0]	90
		9	x	x	x	Green_3[12]	Green_3[11]	Green_3[10]	Green_3[9]	Green_3[8]	1E
		10	Green_3[7]	Green_3[6]	Green_3[5]	Green_3[4]	Green_3[3]	Green_3[2]	Green_3[1]	Green_3[0]	CD
		11	x	x	x	Green_2[12]	Green_2[11]	Green_2[10]	Green_2[9]	Green_2[8]	07
		12	Green_2[7]	Green_2[6]	Green_2[5]	Green_2[4]	Green_2[3]	Green_2[2]	Green_2[1]	Green_2[0]	4C
		13	x	x	x	Green_1[12]	Green_1[11]	Green_1[10]	Green_1[9]	Green_1[8]	1E
		14	Green_1[7]	Green_1[6]	Green_1[5]	Green_1[4]	Green_1[3]	Green_1[2]	Green_1[1]	Green_1[0]	06
		15	x	x	x	Red_3[12]	Red _3[11]	Red _3[10]	Red _3[9]	Red _3[8]	1F
		16	Red _3[7]	Red _3[6]	Red _3[5]	Red _3[4]	Red _3[3]	Red _3[2]	Red _3[1]	Red _3[0]	66
		17	x	x	x	Red _2[12]	Red _2[11]	Red _2[10]	Red _2[9]	Red _2[8]	1E
		18	Red _2[7]	Red _2[6]	Red _2[5]	Red _2[4]	Red _2[3]	Red _2[2]	Red _2[1]	Red _2[0]	2A
		19	x	x	x	Red _1[12]	Red _1[11]	Red _1[10]	Red _1[9]	Red _1[8]	06

		20	Red _1[7]	Red _1[6]	Red _1[5]	Red _1[4]	Red _1[3]	Red _1[2]	Red _1[1]	Red _1[0]	70

(Hex)	Operation code	Para.	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
E9h	SETGIP1		1	1	1	0	1	0	0	1	-
		1	REF_EN	x	x	x	PANEL_SEL[3]	PANEL_SEL[2]	PANEL_SEL[1]	PANEL_SEL[0]	24
		2	x	x	x	SHR0[12]	SHR0[11]	SHR0[10]	SHR0[9]	SHR0[8]	00
		3	SHR0[7]	SHR0[6]	SHR0[5]	SHR0[4]	SHR0[3]	SHR0[2]	SHR0[1]	SHR0[0]	00
		4	x	x	x	SHR1[12]	SHR1[11]	SHR1[10]	SHR1[9]	SHR1[8]	00
		5	SHR1[7]	SHR1[6]	SHR1[5]	SHR1[4]	SHR1[3]	SHR1[2]	SHR1[1]	SHR1[0]	00
		6	SPON[7]	SPON[6]	SPON[5]	SPON[4]	SPON[3]	SPON[2]	SPON[1]	SPON[0]	00
		7	SPOFF[7]	SPOFF[6]	SPOFF[5]	SPOFF[4]	SPOFF[3]	SPOFF[2]	SPOFF[1]	SPOFF[0]	00
		8	SHR0_1[3]	SHR0_1[2]	SHR0_1[1]	SHR0_1[0]	SHR0_2[3]	SHR0_2[2]	SHR0_2[1]	SHR0_2[0]	00
		9	SHR0_3[3]	SHR0_3[2]	SHR0_3[1]	SHR0_3[0]	SHR1_1[3]	SHR1_1[2]	SHR1_1[1]	SHR1_1[0]	00
		10	SHR1_2[3]	SHR1_2[2]	SHR1_2[1]	SHR1_2[0]	SHR1_3[3]	SHR1_3[2]	SHR1_3[1]	SHR1_3[0]	00
		11	SHP[3]	SHP[2]	SHP[1]	SHP[0]	SCP[3]	SCP[2]	SCP[1]	SCP[0]	00
		12	CHR [7]	CHR [6]	CHR [5]	CHR [4]	CHR [3]	CHR [2]	CHR [1]	CHR [0]	02
		13	CON [7]	CON [6]	CON [5]	CON [4]	CON [3]	CON [2]	CON [1]	CON [0]	02
		14	COF [7]	COF [6]	COF [5]	COF [4]	COF [3]	COF [2]	COF [1]	COF [0]	00
		15	CHP[3]	CHP[2]	CHP[1]	CHP[0]	CCP[3]	CCP[2]	CCP[1]	CCP[0]	00
		16	USER_GIP_GATE[7]	USER_GIP_GATE[6]	USER_GIP_GATE[5]	USER_GIP_GATE[4]	USER_GIP_GATE[3]	USER_GIP_GATE[2]	USER_GIP_GATE[1]	USER_GIP_GATE[0]	00
		17	x	x	CGTS_L[21]	CGTS_L[20]	CGTS_L[19]	CGTS_L[18]	CGTS_L[17]	CGTS_L[16]	00
		18	CGTS_L[15]	CGTS_L[14]	CGTS_L[13]	CGTS_L[12]	CGTS_L[11]	CGTS_L[10]	CGTS_L[9]	CGTS_L[8]	00
		19	CGTS_L[7]	CGTS_L[6]	CGTS_L[5]	CGTS_L[4]	CGTS_L[3]	CGTS_L[2]	CGTS_L[1]	CGTS_L[0]	00
		20	x	x	CGTS_INV_L[21]	CGTS_INV_L[20]	CGTS_INV_L[19]	CGTS_INV_L[18]	CGTS_INV_L[17]	CGTS_INV_L[16]	00
		21	CGTS_INV_L[15]	CGTS_INV_L[14]	CGTS_INV_L[13]	CGTS_INV_L[12]	CGTS_INV_L[11]	CGTS_INV_L10]	CGTS_INV_L[9]	CGTS_INV_L[8]	00
		22	CGTS_INV_L[7]	CGTS_INV_L[6]	CGTS_INV_L[5]	CGTS_INV_L[4]	CGTS_INV_L[3]	CGTS_INV_L[2]	CGTS_INV_L[1]	CGTS_INV_L[0]	00
		23	x	x	CGTS_R[21]	CGTS_R[20]	CGTS_R[19]	CGTS_R[18]	CGTS_R[17]	CGTS_R[16]	00
		24	CGTS_R[15]	CGTS_R[14]	CGTS_R[13]	CGTS_R[12]	CGTS_R[11]	CGTS_R[10]	CGTS_R[9]	CGTS_R[8]	00
		25	CGTS_R[7]	CGTS_R[6]	CGTS_R[5]	CGTS_R[4]	CGTS_R[3]	CGTS_R[2]	CGTS_R[1]	CGTS_R[0]	00
		26	x	x	CGTS_INV_R[21]	CGTS_INV_R[20]	CGTS_INV_R[19]	CGTS_INV_R[18]	CGTS_INV_R[17]	CGTS_INV_R[16]	00
		27	CGTS_INV_R[15]	CGTS_INV_R[14]	CGTS_INV_R[13]	CGTS_INV_R[12]	CGTS_INV_R[11]	CGTS_INV_R10]	CGTS_INV_R[9]	CGTS_INV_R[8]	00
		28	CGTS_INV_R[7]	CGTS_INV_R[6]	CGTS_INV_R[5]	CGTS_INV_R[4]	CGTS_INV_R[3]	CGTS_INV_R[2]	CGTS_INV_R[1]	CGTS_INV_R[0]	00
		29	COS1_L[3]	COS1_L[2]	COS1_L[1]	COS1_L[0]	COS2_L[3]	COS2_L[2]	COS2_L[1]	COS2_L[0]	00
		30	COS3_L[3]	COS3_L[2]	COS3_L[1]	COS3_L[0]	COS4_L[3]	COS4_L[2]	COS4_L[1]	COS4_L[0]	00
		31	COS5_L[3]	COS5_L[2]	COS5_L[1]	COS5_L[0]	COS6_L[3]	COS6_L[2]	COS6_L[1]	COS6_L[0]	00
		:	:	:	:	:	:	:	:	:	
		37	COS17_L[3]	COS17_L[2]	COS17_L[1]	COS17_L[0]	COS18_L[3]	COS18_L[2]	COS18_L[1]	COS18_L[0]	00
		38	COS19_L[3]	COS19_L[2]	COS19_L[1]	COS19_L[0]	COS20_L[3]	COS20_L[2]	COS20_L[1]	COS20_L[0]	00
		39	COS21_L[3]	COS21_L[2]	COS21_L[1]	COS21_L[0]	COS22_L[3]	COS22_L[2]	COS22_L[1]	COS22_L[0]	00
		40	COS1_R[3]	COS1_R[2]	COS1_R[1]	COS1_R[0]	COS2_R[3]	COS2_R[2]	COS2_R[1]	COS2_R[0]	00

E9h	SETGIP1	41	COS3_R[3]	COS3_R[2]	COS3_R[1]	COS3_R[0]	COS4_R[3]	COS4_R[2]	COS4_R[1]	COS4_R[0]	00
		42	COS5_R[3]	COS5_R[2]	COS5_R[1]	COS5_R[0]	COS6_R[3]	COS6_R[2]	COS6_R[1]	COS6_R[0]	00
		:	:	:	:	:	:	:	:	:	
		48	COS17_R[3]	COS17_R[2]	COS17_R[1]	COS17_R[0]	COS18_R[3]	COS18_R[2]	COS18_R[1]	COS18_R[0]	00
		49h	COS19_R[3]	COS19_R[2]	COS19_R[1]	COS19_R[0]	COS20_R[3]	COS20_R[2]	COS20_R[1]	COS20_R[0]	00
		50	COS21_R[3]	COS21_R[2]	COS21_R[1]	COS21_R[0]	COS22_R[3]	COS22_R[2]	COS22_R[1]	COS22_R[0]	00
		51	TCON_OPT[7]	TCON_OPT[6]	TCON_OPT[5]	TCON_OPT[4]	TCON_OPT[3]	TCON_OPT[2]	TCON_OPT[1]	TCON_OPT[0]	00
		52	x	GIP_OPT[22]	GIP_OPT[21]	GIP_OPT[20]	GIP_OPT[19]	GIP_OPT[18]	GIP_OPT[17]	GIP_OPT[16]	00
		53	GIP_OPT[15]	GIP_OPT[14]	GIP_OPT[13]	GIP_OPT[12]	GIP_OPT[11]	GIP_OPT[10]	GIP_OPT[9]	GIP_OPT[8]	00
		54	GIP_OPT[7]	GIP_OPT[6]	GIP_OPT[5]	GIP_OPT[4]	GIP_OPT[3]	GIP_OPT[2]	GIP_OPT[1]	GIP_OPT[0]	00
		55	CHR2[7]	CHR2[6]	CHR2[5]	CHR2[4]	CHR2[3]	CHR2[2]	CHR2[1]	CHR2[0]	00
		56	CON2[7]	CON2[6]	CON2[5]	CON2[4]	CON2[3]	CON2[2]	CON2[1]	CON2[0]	02
		57	COFF2[7]	COFF2[6]	COFF2[5]	COFF2[4]	COFF2[3]	COFF2[2]	COFF2[1]	COFF2[0]	02
		58	CHP2[3]	CHP2[2]	CHP2[1]	CHP2[0]	CCP2[3]	CCP2[2]	CCP2[1]	CCP2[0]	00
		59	x	x	CKS[21]	CKS[20]	CKS[19]	CKS[18]	CKS[17]	CKS[16]	00
		60	CKS[15]	CKS[14]	CKS[13]	CKS[12]	CKS[11]	CKS[10]	CKS[9]	CKS[8]	00
		61	CKS[7]	CKS[6]	CKS[5]	CKS[4]	CKS[3]	CKS[2]	CKS[1]	CKS[0]	00
		62	COFF[9]	COFF[8]	CON[9]	CON[8]	SPOFF[9]	SPOFF[8]	SPON[9]	SPON[8]	00
		63	COFF2[9]	COFF2[8]	CON2[9]	CON2[8]	x	x	x	x	00

(Hex)	Operation code	Para.	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
EAh	SETGIP2		1	1	1	0	1	0	1	0	-
		1	YS2_SEL[1]	YS2_SEL[0]	YS1_SEL[1]	YS1_SEL[0]	YS2_XOR	YS1_XOR	YS_FLAG_EN	ALL_ON_EN	94
		2	GATE[7]	GATE[6]	GATE[5]	GATE[4]	GATE[3]	GATE[2]	GATE[1]	GATE[0]	00
		3	CK_ALL_ON_EN	STV_ALL_ON_EN	CK_ALL_ON_WIDTH1[5]	CK_ALL_ON_WIDTH1[4]	CK_ALL_ON_WIDTH1[3]	CK_ALL_ON_WIDTH1[2]	CK_ALL_ON_WIDTH1[1]	CK_ALL_ON_WIDTH1[0]	00
		4	x	x	CK_ALL_ON_WIDTH2[5]	CK_ALL_ON_WIDTH2[4]	CK_ALL_ON_WIDTH2[3]	CK_ALL_ON_WIDTH2[2]	CK_ALL_ON_WIDTH2[1]	CK_ALL_ON_WIDTH2[0]	00
		5	x	x	CK_ALL_ON_WIDTH3[5]	CK_ALL_ON_WIDTH3[4]	CK_ALL_ON_WIDTH3[3]	CK_ALL_ON_WIDTH3[2]	CK_ALL_ON_WIDTH3[1]	CK_ALL_ON_WIDTH3[0]	00
		6	YS_FLAG_PERIOD[7]	YS_FLAG_PERIOD[6]	YS_FLAG_PERIOD[5]	YS_FLAG_PERIOD[4]	YS_FLAG_PERIOD[3]	YS_FLAG_PERIOD[2]	YS_FLAG_PERIOD[1]	YS_FLAG_PERIOD[0]	00
		7	YS2_SEL_2[1]	YS2_SEL_2[0]	YS1_SEL_2[1]	YS1_SEL_2[0]	YS2_XOR_2	YS1_XOR_2	YS_FLAG_EN_2	ALL_ON_EN_2	94
		8	USER_GIP_GATE1_2[7]	USER_GIP_GATE1_2[6]	USER_GIP_GATE1_2[5]	USER_GIP_GATE1_2[4]	USER_GIP_GATE1_2[3]	USER_GIP_GATE1_2[2]	USER_GIP_GATE1_2[1]	USER_GIP_GATE1_2[0]	00
		9	CK_ALL_ON_EN_2	STV_ALL_ON_EN_2	CK_ALL_ON_WIDTH1_2[5]	CK_ALL_ON_WIDTH1_2[4]	CK_ALL_ON_WIDTH1_2[3]	CK_ALL_ON_WIDTH1_2[2]	CK_ALL_ON_WIDTH1_2[1]	CK_ALL_ON_WIDTH1_2[0]	00
		10	x	x	CK_ALL_ON_WIDTH2_2[5]	CK_ALL_ON_WIDTH2_2[4]	CK_ALL_ON_WIDTH2_2[3]	CK_ALL_ON_WIDTH2_2[2]	CK_ALL_ON_WIDTH2_2[1]	CK_ALL_ON_WIDTH2_2[0]	00
		11	x	x	CK_ALL_ON_WIDTH3_2[5]	CK_ALL_ON_WIDTH3_2[4]	CK_ALL_ON_WIDTH3_2[3]	CK_ALL_ON_WIDTH3_2[2]	CK_ALL_ON_WIDTH3_2[1]	CK_ALL_ON_WIDTH3_2[0]	00
		12	YS_FLAG_PERIOD_2[7]	YS_FLAG_PERIOD_2[6]	YS_FLAG_PERIOD_2[5]	YS_FLAG_PERIOD_2[4]	YS_FLAG_PERIOD_2[3]	YS_FLAG_PERIOD_2[2]	YS_FLAG_PERIOD_2[1]	YS_FLAG_PERIOD_2[0]	00
		13	COS1_L_GS[3]	COS1_L_GS[2]	COS1_L_GS[1]	COS1_L_GS[0]	COS2_L_GS[3]	COS2_L_GS[2]	COS2_L_GS[1]	COS2_L_GS[0]	00
		14	COS3_L_GS[3]	COS3_L_GS[2]	COS3_L_GS[1]	COS3_L_GS[0]	COS4_L_GS[3]	COS4_L_GS[2]	COS4_L_GS[1]	COS4_L_GS[0]	00
		15	COS5_L_GS[3]	COS5_L_GS[2]	COS5_L_GS[1]	COS5_L_GS[0]	COS6_L_GS[3]	COS6_L_GS[2]	COS6_L_GS[1]	COS6_L_GS[0]	00
		:	:	:	:	:	:	:	:	:	:
		21	COS17_L_GS[3]	COS17_L_GS[2]	COS17_L_GS[1]	COS17_L_GS[0]	COS18_L_GS[3]	COS18_L_GS[2]	COS18_L_GS[1]	COS18_L_GS[0]	00
		22	COS19_L_GS[3]	COS19_L_GS[2]	COS19_L_GS[1]	COS19_L_GS[0]	COS20_L_GS[3]	COS20_L_GS[2]	COS20_L_GS[1]	COS20_L_GS[0]	00
		23	COS21_L_GS[3]	COS21_L_GS[2]	COS21_L_GS[1]	COS21_L_GS[0]	COS22_L_GS[3]	COS22_L_GS[2]	COS22_L_GS[1]	COS22_L_GS[0]	00
		24	COS1_R_GS[3]	COS1_R_GS[2]	COS1_R_GS[1]	COS1_R_GS[0]	COS2_R_GS[3]	COS2_R_GS[2]	COS2_R_GS[1]	COS2_R_GS[0]	00
		25	COS3_R_GS[3]	COS3_R_GS[2]	COS3_R_GS[1]	COS3_R_GS[0]	COS4_R_GS[3]	COS4_R_GS[2]	COS4_R_GS[1]	COS4_R_GS[0]	00
		26	COS5_R_GS[3]	COS5_R_GS[2]	COS5_R_GS[1]	COS5_R_GS[0]	COS6_R_GS[3]	COS6_R_GS[2]	COS6_R_GS[1]	COS6_R_GS[0]	00
		:	:	:	:	:	:	:	:	:	:
		32	COS17_R_GS[3]	COS17_R_GS[2]	COS17_R_GS[1]	COS17_R_GS[0]	COS18_R_GS[3]	COS18_R_GS[2]	COS18_R_GS[1]	COS18_R_GS[0]	00
		33	COS19_R_GS[3]	COS19_R_GS[2]	COS19_R_GS[1]	COS19_R_GS[0]	COS20_R_GS[3]	COS20_R_GS[2]	COS20_R_GS[1]	COS20_R_GS[0]	00
		34	COS21_R_GS[3]	COS21_R_GS[2]	COS21_R_GS[1]	COS21_R_GS[0]	COS22_R_GS[3]	COS22_R_GS[2]	COS22_R_GS[1]	COS22_R_GS[0]	00
		35	x	x	EQOPT[1]	EQOPT[0]	x	x	EQ_SEL[1]	EQ_SEL[0]	30
		36	EQ_DELAY[7]	EQ_DELAY[6]	EQ_DELAY[5]	EQ_DELAY[4]	EQ_DELAY[3]	EQ_DELAY[2]	EQ_DELAY[1]	EQ_DELAY[0]	00
		37	x	x	x	x	EQ_DELAY_HSYNC[3]	EQ_DELAY_HSYNC[2]	EQ_DELAY_HSYNC[1]	EQ_DELAY_HSYNC[0]	00

		38	x	x	x	x	x	x	HSYNC_TO_CL1_CNT10[9]	HSYNC_TO_CL1_CNT10[8]	00
		39	HSYNC_TO_CL1_CNT10[7]	HSYNC_TO_CL1_CNT10[6]	HSYNC_TO_CL1_CNT10[5]	HSYNC_TO_CL1_CNT10[4]	HSYNC_TO_CL1_CNT10[3]	HSYNC_TO_CL1_CNT10[2]	HSYNC_TO_CL1_CNT10[1]	HSYNC_TO_CL1_CNT10[0]	02
EBh	SETCOLOR		1	1	1	0	1	0	1	1	-
		1	Bkx[1]	Bkx[0]	Bky[1]	Bky[0]	Wx[1]	Wx[0]	Wy[1]	Wy[0]	00
		2	BKx[9]	BKx[8]	BKx[7]	BKx[6]	BKx[5]	BKx[4]	BKx3]	BKx[2]	00
		3	BKy[9]	BKy[8]	BKy[7]	BKy[6]	BKy[5]	BKy[4]	BKy3]	BKy[2]	00
		4	Wx[9]	Wx[8]	Wx[7]	Wx[6]	Wx[5]	Wx[4]	Wx3]	Wx[2]	00
		5	Wy[9]	Wy[8]	Wy[7]	Wy[6]	Wy[5]	Wy[4]	Wy3]	Wy[2]	00
		6	Rx[1]	Rx[0]	Ry[1]	Ry[0]	Gx[1]	Gx[0]	Gy[1]	Gy[0]	00
		7	Rx[9]	Rx[8]	Rx[7]	Rx[6]	Rx[5]	Rx[4]	Rx3]	Rx[2]	00
		8	Ry[9]	Ry[8]	Ry[7]	Ry[6]	Ry[5]	Ry[4]	Ry3]	Ry[2]	00
		9	Gx[9]	Gx[8]	Gx[7]	Gx[6]	Gx[5]	Gx[4]	Gx3]	Gx[2]	00
		10	Gy[9]	Gy[8]	Gy[7]	Gy[6]	Gy[5]	Gy[4]	Gy3]	Gy[2]	00
		11	Bx[1]	Bx[0]	By[1]	By[0]	Ax[1]	Ax[0]	Ay[1]	Ay[0]	00
		12	Bx[9]	Bx[8]	Bx[7]	Bx[6]	Bx[5]	Bx[4]	Bx3]	Bx[2]	00
		13	By[9]	By[8]	By[7]	By[6]	By[5]	By[4]	By3]	By[2]	00
		14	Ax[9]	Ax[8]	Ax[7]	Ax[6]	Ax[5]	Ax[4]	Ax3]	Ax[2]	00
		15	Ay[9]	Ay[8]	Ay[7]	Ay[6]	Ay[5]	Ay[4]	Ay3]	Ay[2]	00
F1h	TEMP_SENSOR		1	1	1	1	0	0	0	1	-
		1	PASSWORD[7]	PASSWORD[6]	PASSWORD[5]	PASSWORD[4]	PASSWORD[3]	PASSWORD[2]	PASSWORD[1]	PASSWORD[0]	00
		2	TEMP_ST[3]	TEMP_ST[2]	TEMP_ST[1]	TEMP_ST[0]	TEMP_FRA[3]	TEMP_FRA[2]	TEMP_FRA[1]	TEMP_FRA[0]	3F
		3	x	x	L_TH[5]	L_TH[4]	L_TH[3]	L_TH[2]	L_TH[1]	L_TH[0]	14
		4	x	x	H_TH[5]	H_TH[4]	H_TH[3]	H_TH[2]	H_TH[1]	H_TH[0]	30
		5	x	L_PLUS[2]	L_PLUS[1]	L_PLUS[0]	x	L_MINUS[2]	L_MINUS[1]	L_MINUS[0]	55
		6	x	H_PLUS[2]	H_PLUS[1]	H_PLUS[0]	x	H_MINUS[2]	H_MINUS[1]	H_MINUS[0]	55
		7	TEMP_FILTER_EN	x	x	x	SAME_NUM[3]	SAME_NUM[2]	SAME_NUM[1]	SAME_NUM[0]	0F

(Hex)	Operation code	Para.	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
F2h	TEMP_VOLTAGE		1	1	1	1	0	0	1	0	-
		1	VBTHS1[3]	VBTHS1[2]	VBTHS1[1]	VBTHS1[0]	VBTLS1[3]	VBTLS1[2]	VBTLS1[1]	VBTLS1[0]	53
		2	ECP_DC_DIV1[3]	ECP_DC_DIV1[2]	ECP_DC_DIV1[1]	ECP_DC_DIV1[0]	VGLREG1[3]	VGLREG1[2]	VGLREG1[1]	VGLREG1[0]	43
		3	VCOMDC_F1[7]	VCOMDC_F1[6]	VCOMDC_F1[5]	VCOMDC_F1[4]	VCOMDC_F1[3]	VCOMDC_F1[2]	VCOMDC_F1[1]	VCOMDC_F1[0]	4D
		4	VCOMDC_B1[7]	VCOMDC_B1[6]	VCOMDC_B1[5]	VCOMDC_B1[4]	VCOMDC_B1[3]	VCOMDC_B1[2]	VCOMDC_B1[1]	VCOMDC_B1[0]	4D
		5	x	x	PVR01[5]	PVR01[4]	PVR01[3]	PVR01[2]	PVR01[1]	PVR01[0]	00
		6	x	x	PVR51[5]	PVR51[4]	PVR51[3]	PVR51[2]	PVR51[1]	PVR51[0]	00
		7	x	x	NVR01[5]	NVR01[4]	NVR01[3]	NVR01[2]	NVR01[1]	NVR01[0]	00
		8	x	x	NVR51[5]	NVR51[4]	NVR51[3]	NVR51[2]	NVR51[1]	NVR51[0]	00
		9	x	x	x	x	x	N_NW_HT[2]	N_NW_HT[1]	N_NW_HT[0]	00
		10	VBTHS4[3]	VBTHS4[2]	VBTHS4[1]	VBTHS4[0]	VBTLS4[3]	VBTLS4[2]	VBTLS4[1]	VBTLS4[0]	53
		11	ECP_DC_DIV4[3]	ECP_DC_DIV4[2]	ECP_DC_DIV4[1]	ECP_DC_DIV4[0]	VGLREG4[3]	VGLREG4[2]	VGLREG4[1]	VGLREG4[0]	43
		12	VCOMDC_F4[7]	VCOMDC_F4[6]	VCOMDC_F4[5]	VCOMDC_F4[4]	VCOMDC_F4[3]	VCOMDC_F4[2]	VCOMDC_F4[1]	VCOMDC_F4[0]	4D
		13	VCOMDC_B4[7]	VCOMDC_B4[6]	VCOMDC_B4[5]	VCOMDC_B4[4]	VCOMDC_B4[3]	VCOMDC_B4[2]	VCOMDC_B4[1]	VCOMDC_B4[0]	4D
		14	x	x	PVR04[5]	PVR04[4]	PVR04[3]	PVR04[2]	PVR04[1]	PVR04[0]	00
		15	x	x	PVR54[5]	PVR54[4]	PVR54[3]	PVR54[2]	PVR54[1]	PVR54[0]	00
		16	x	x	NVR04[5]	NVR04[4]	NVR04[3]	NVR04[2]	NVR04[1]	NVR04[0]	00
		17	x	x	NVR54[5]	NVR54[4]	NVR54[3]	NVR54[2]	NVR54[1]	NVR54[0]	00
		18	x	x	x	x	x	N_NW_LT[2]	N_NW_LT[1]	N_NW_LT[0]	00
		19	x	x	x	x	x	x	x	TEMP_SENSOR_ON	00

6.2 Command description

6.2.1 NOP (00h)

<table>
<tr><td>00 H</td><td colspan="10">NOP (No Operation)</td></tr>
<tr><td></td><td>R/W</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Parameter</td><td colspan="10">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="10">This command is an empty command; it does not have any effect on the display module.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10">-</td></tr>
</table>

6.2.2 Software reset (01h)

01 H	SWRESET (Software Reset)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER									
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) The display is blank immediately.									
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5m sec. If SW Reset is applied during Sleep Out mode, it will be necessary to wait 120m sec before sending Sleep Out command. SW Reset command cannot be sent during Sleep Out sequence.									

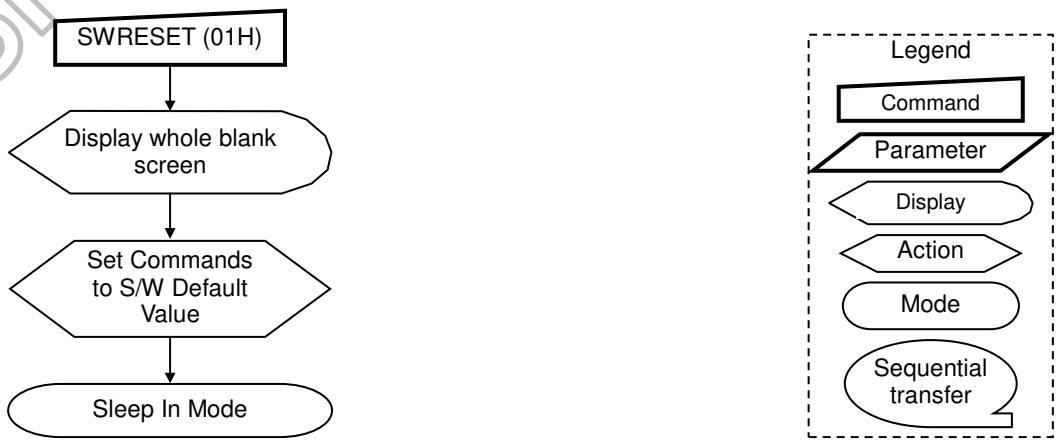
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



6.2.3 Read Display ID (04h)

04 H	RDDID (Read Display ID)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	0	1	0	0	04
1st parameter	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	38
2nd parameter	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	21
3rd parameter	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	1F
Description	This read byte returns 24-bit display identification information.									
Restriction	-									

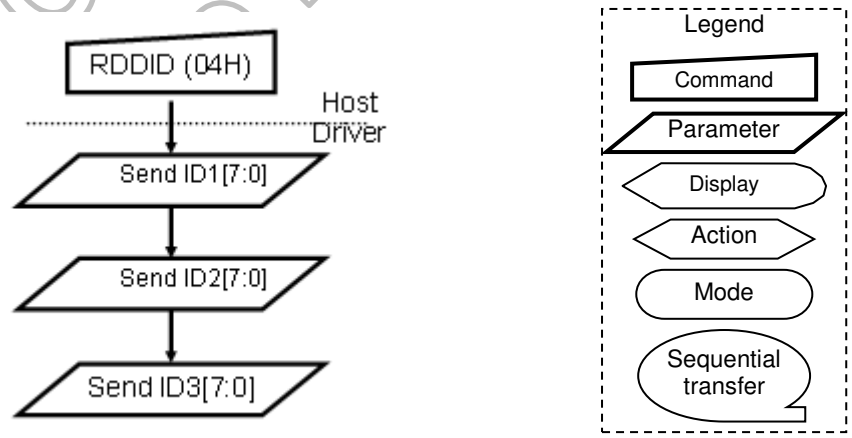
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	38
S/W Reset	21
H/W Reset	1F

Flow Chart



6.2.4 Read Display Power Mode (0Ah)

0A H	RDDPM (Read Display Power Mode)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	0	1	0	0A
1st parameter	-	D7	D6	D5	D4	D3	D2	0	0	-
Description	This command indicates the current status of the display as described in the table below:									

Bit	Description	Value
D7	Booster Voltage Status	'1'=Booster on, '0'=Booster off
D6	Idle Mode On/Off	'1'=Idle Mode on, '0'=Idle Mode off
D5	Partial Mode On/Off	'1'=Partial Mode on, '0'= Partial Mode off
D4	Sleep In/Out	'1'=Sleep out , '0'=Sleep in
D3	Display Normal Mode On/Off	'1'=Display Normal on, '0'=Display Normal off
D2	Display On/Off	'1'=Display on, '0'=Display off
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Restriction: -

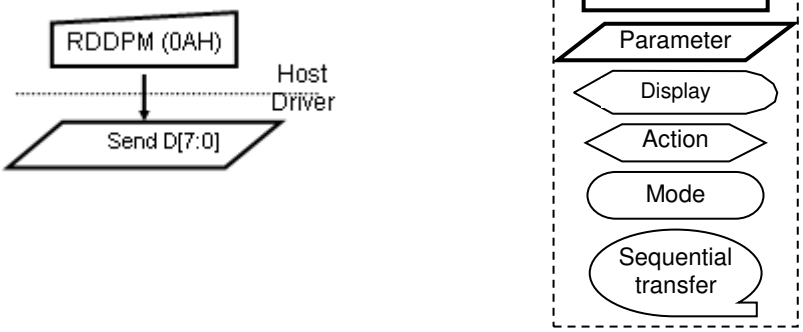
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



6.2.5 Read Display MADCTR (0Bh)

0B H	RDDMADCTR (Read Display MADCTR)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	0	1	1	0B
1st parameter	-	D7	D6	0	0	D3	D2	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Page Address Order (MY)	'0'=Increment, '1' = Decrement
D6	Column Address Order (MX)	'0'=Increment, '1' = Decrement
D5	Page/Column Exchange (MV)	Set to '0'
D4	Line Address Order (ML)	Set to '0'
D3	RGB/BGR Order	'0'=Increment, '1' = Decrement
D2	Display Data Latch Order (MH)	'0'=Increment, '1' = Decrement
D1	Flip horizontal	Set to '0'
D0	Flip vertical	Set to '0'

Restriction

-

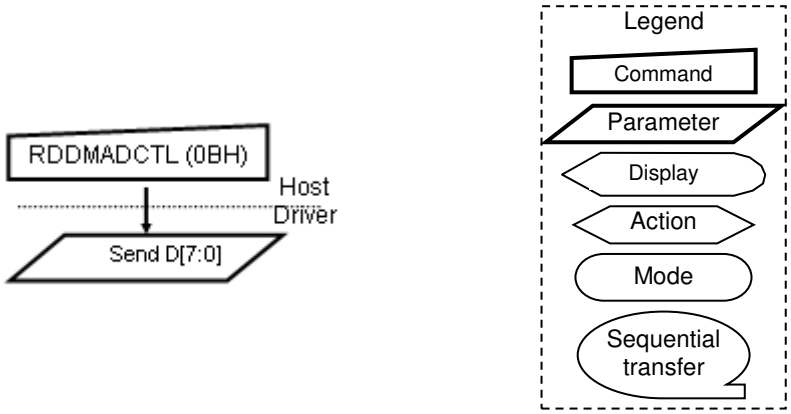
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.6 Read Display Pixel Format (0Ch)

0C H	RDDCOLMOD (Read Display COLMOD)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	1	0	0	0C
1st parameter	-	D7	D6	0	0	D3	D2	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Reserved	Set to '0'
D6	RGB Interface Pixel format	'101' =16-bit/pixel
D5		'110' =18-bit/pixel
D4		'111' =24-bit/pixel
D3	Reserved	Set to '0'
D2	DBI Interface Pixel format	Set to '0'
D1		Set to '0'
D0		Set to '0'

Restriction

-

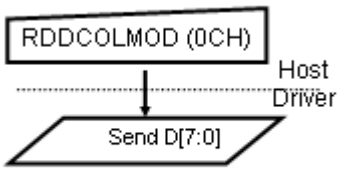
Register Availability

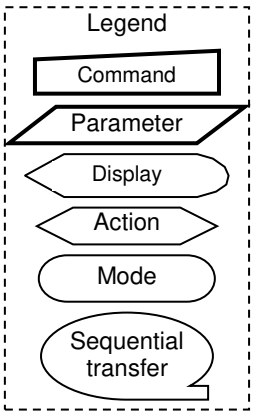
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	70h
S/W Reset	No Change
H/W Reset	70h

Flow Chart





6.2.7 Read Display Image Mode (0Dh)

0D H	RDDIM (Read Display Image Mode)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	1	0	1	0D
1st parameter	-	D7	D6	0	0	D3	D2	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Vertical Scrolling On/Off	Set to '0'
D6	Horizontal Scrolling On/off	Set to '0'
D5	Inversion On/off	'1' = Inversion On, '0' = Inversion Off
D4	All Pixel On	'1' = White display, '0' = Normal display
D3	All Pixel Off	'1' = Black display, '0' = Normal display
D2	Gamma Curve Selection	'000'=GC0, '001'=GC1 '010'=GC2, '011'=GC3 '100' to '111' = not define
D1		
D0		

Restriction

-

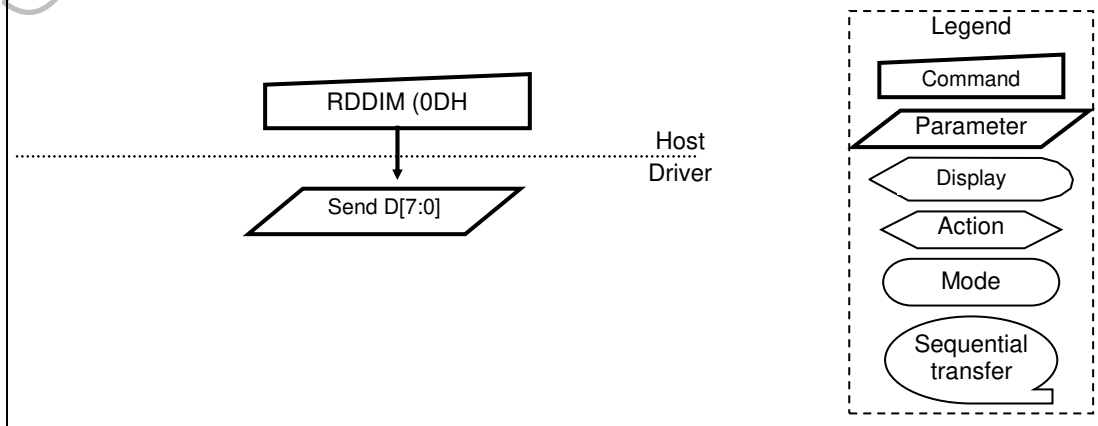
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.8 Read Display Signal Mode (0Eh)

0E H	RDDSM (Read Display Signal Mode)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	1	1	0	0E
1st parameter	-	D7	D6	0	0	D3	D2	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	Set to '0'
D6	Tearing Effect Line Mode	Set to '0'
D5	Horizontal Sync. On/Off	'1'= HS bit is '1', '0' = HS bit is '0'
D4	Vertical Sync. On/Off	'1'= VS bit is '1', '0' = VS bit is '0'
D3	Pixel Clock. On/Off	'1'= PCLK line is '1', '0' = PCLK line is '0'
D2	Data Enable On/Off	'1'= DE bit is '1', '0' = DE bit is '0'
D1	Not Define	Set to '0'
D0	Error on DSI	'1'= Error, '0' = No Error

Restriction

-

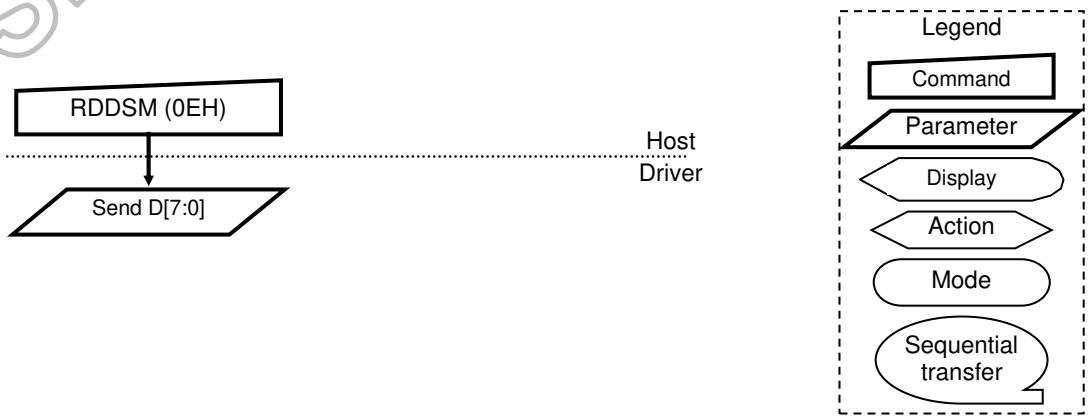
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.9 Read Display Self-Diagnostic Result (0Fh)

0F H	RDDSDR (Read Display Self-Diagnostic Result)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	1	1	1	0F
1st parameter	-	D7	D6	0	0	0	0	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	See Section 5.5.1
D6	Functionality Detection	See Section 5.5.2
D5	Chip Attachment Detection	Set to '0'
D4	Display Glass Break Detection	Set to '0'
D3	Not Define	Set to '0'
D2	Not Define	Set to '0'
D1	Not Define	Set to '0'
D0	Checksums Comparison	'1'= Checksums are not the same '0'= Checksums are the same

Restriction

-

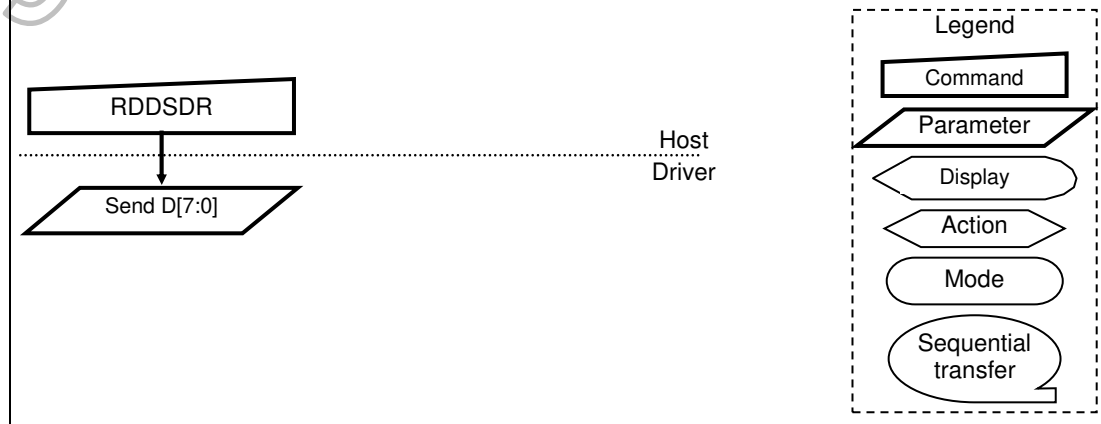
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

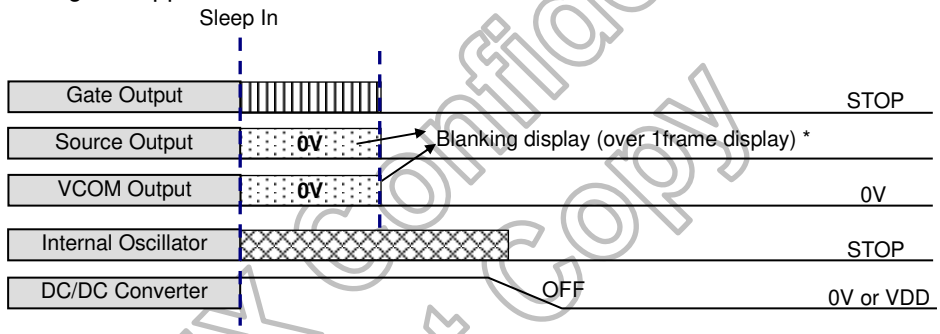
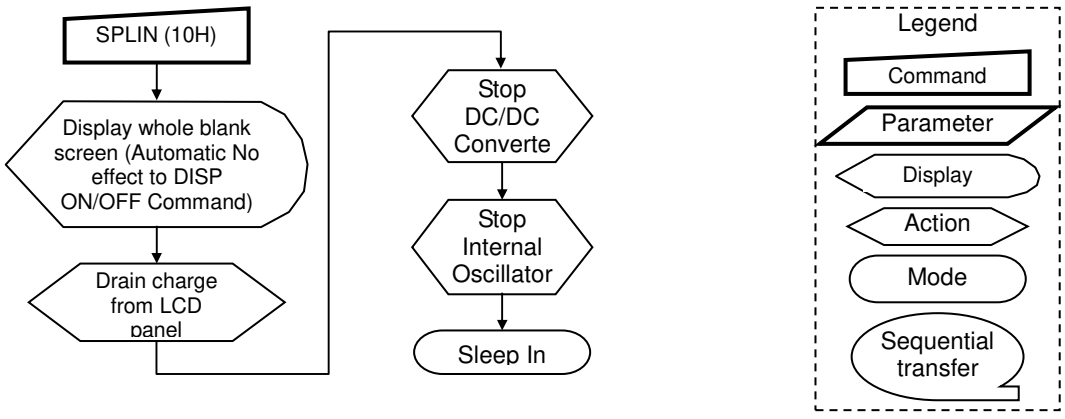
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

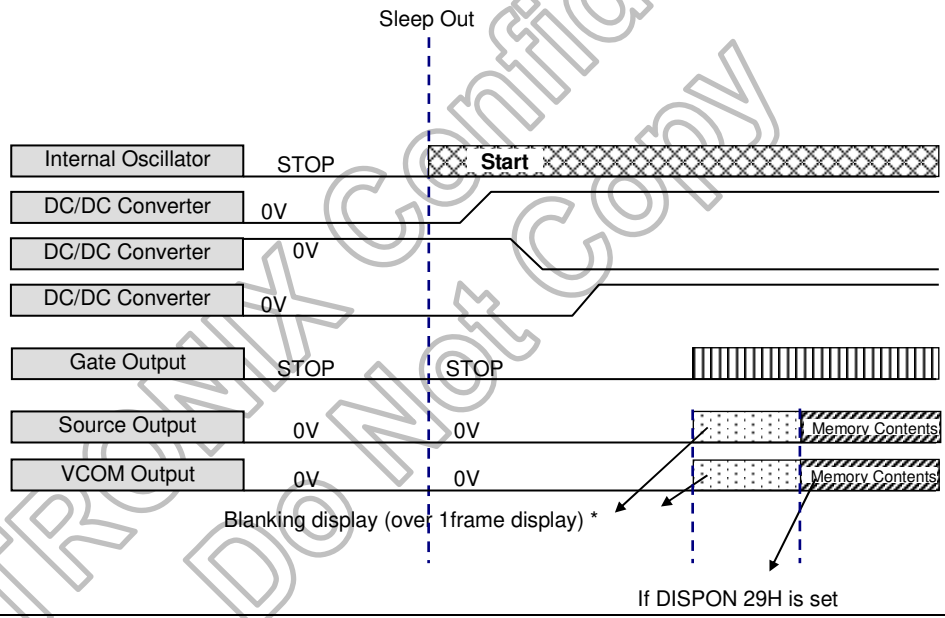
Flow Chart



6.2.10 Sleep In (10h)

10 H	SLPIN (Sleep In)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	0	0	10
Parameter	No Parameter									
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. 									
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11H). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.									
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes									
Default	Status / Default Value Power On Sequence: Sleep In mode S/W Reset: Sleep In mode H/W Reset: Sleep In mode									
Flow Chart	It takes about 120msec to get into Sleep In mode after SLPIN command issued. 									

6.2.11 Sleep Out (11h)

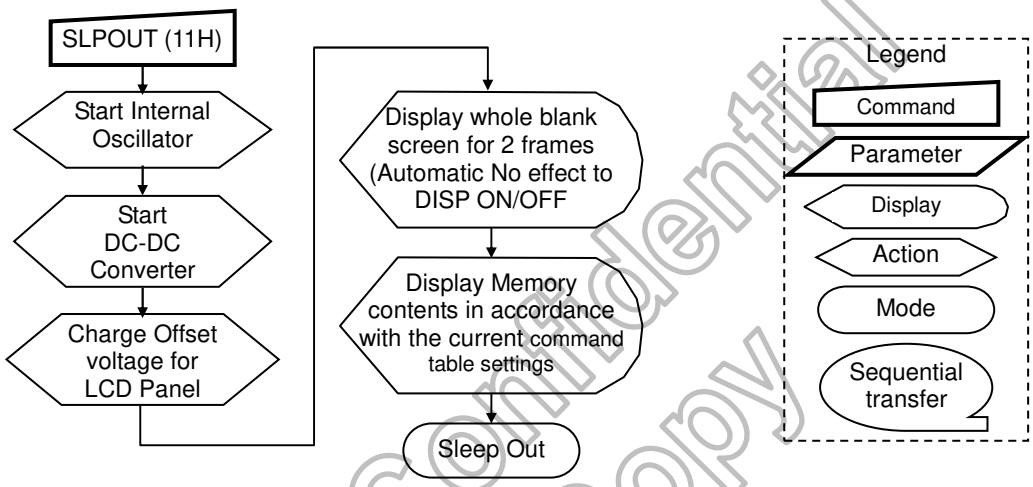
11 H	SLPOUT (Sleep Out)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	0	1	11
Parameter	No Parameter									
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.  									
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 15msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 15msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 15msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Sleep In mode
S/W Reset	Sleep In mode
H/W Reset	Sleep In mode

Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued.



6.2.12 Normal Display Mode On (13h)

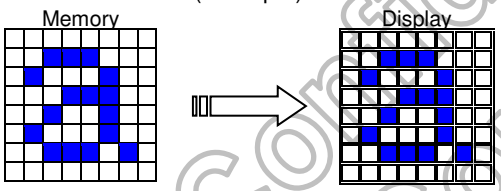
13 H	NORMON (Normal Display Mode On)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	1	1	13
Parameter	No Parameter									
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off.									
Restriction	This command has no effect when module is already in Normal Display mode.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Normal mode ON
S/W Reset	Normal mode ON
H/W Reset	Normal mode ON

6.2.13 Display Inversion Off (20h)

20 H	INVOFF (Display Inversion Off)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	0	0	20
Parameter	No Parameter									
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in inversion off mode									

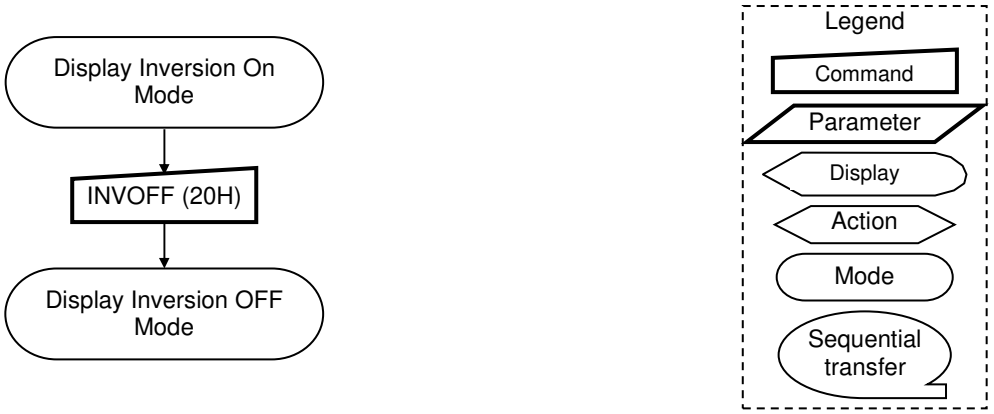
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

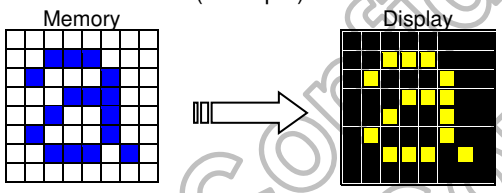
Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



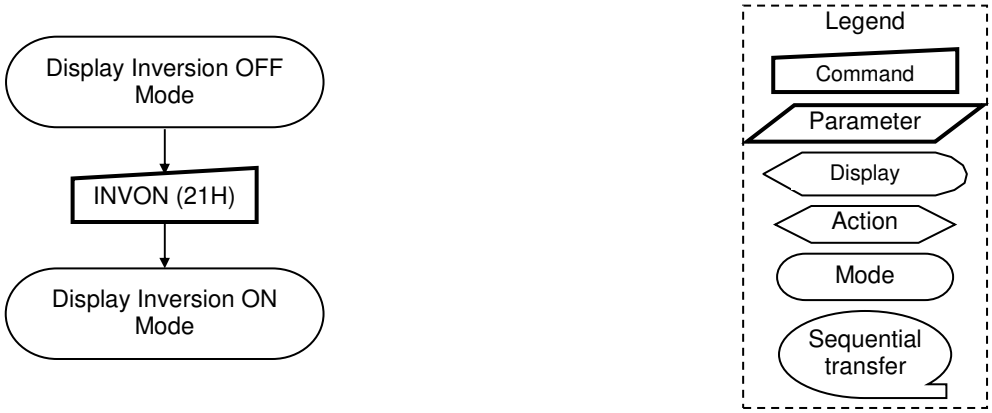
6.2.14 Display Inversion On (21h)

21 H	INVON (Display Inversion On)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	0	1	21
Parameter	No Parameter									
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in inversion on mode									

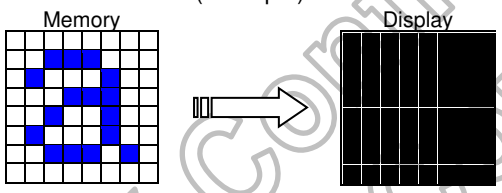
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default	Status	Default Value
	Power On Sequence	Display Inversion off
	S/W Reset	Display Inversion off
	H/W Reset	Display Inversion off

Flow Chart



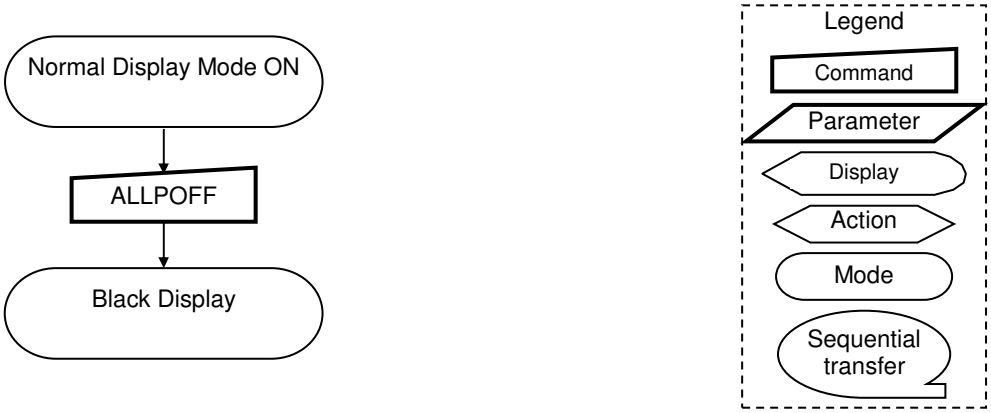
6.2.15 All Pixel Off (22h)

22 H	ALLPOFF (All Pixel Off)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	1	0	22
Parameter	No Parameter									
Description	This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory → Display 									
Restriction	This command has no effect when module is already in all pixel off mode									

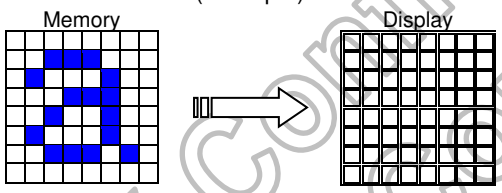
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default	Status	Default Value
	Power On Sequence	All pixel off
	S/W Reset	All pixel off
	H/W Reset	All pixel off

Flow Chart



6.2.16 All Pixel On (23h)

23 H	ALLPON (All Pixel On)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	1	1	23
Parameter	No Parameter									
Description	This command turns the display panel white in Sleep Out mode and a status of the Display On/Off –register can be on or off. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory → Display 									
Restriction	This command has no effect when module is already in all pixel on mode									

Register Availability

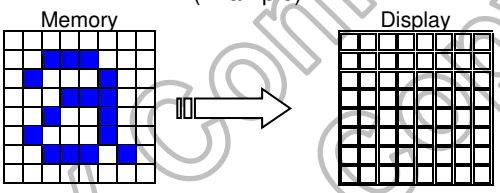
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	All pixel off
S/W Reset	All pixel off
H/W Reset	All pixel off

Flow Chart

6.2.17 Display Off (28h)

28 H	DISPOFF (Display off)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	0	0	28
Parameter	NO Parameter									
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) 									
Restriction	This command has no effect when module is already in display off mode.									

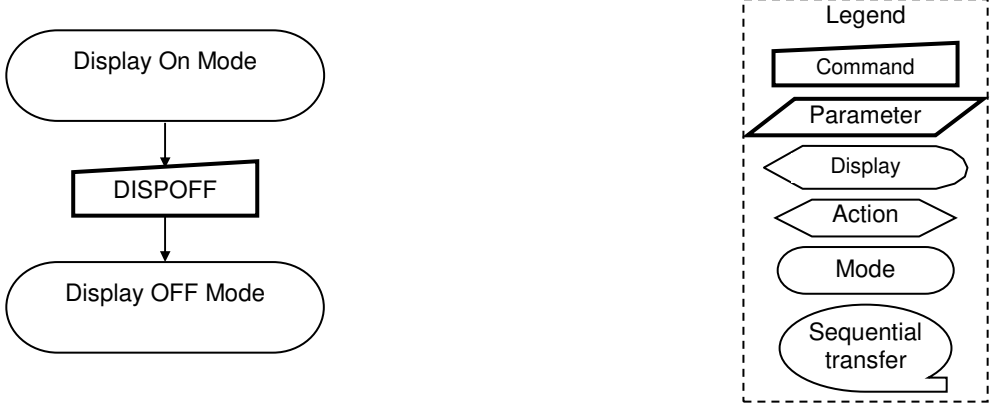
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

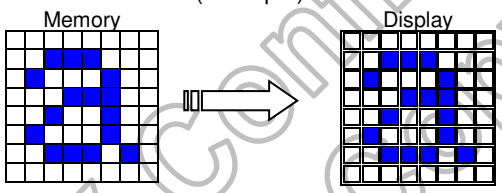
Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



6.2.18 Display On (29h)

29 H	DISPON (Display on)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	0	1	29
Parameter	NO Parameter									
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example)  									
Restriction	This command has no effect when module is already in display on mode.									

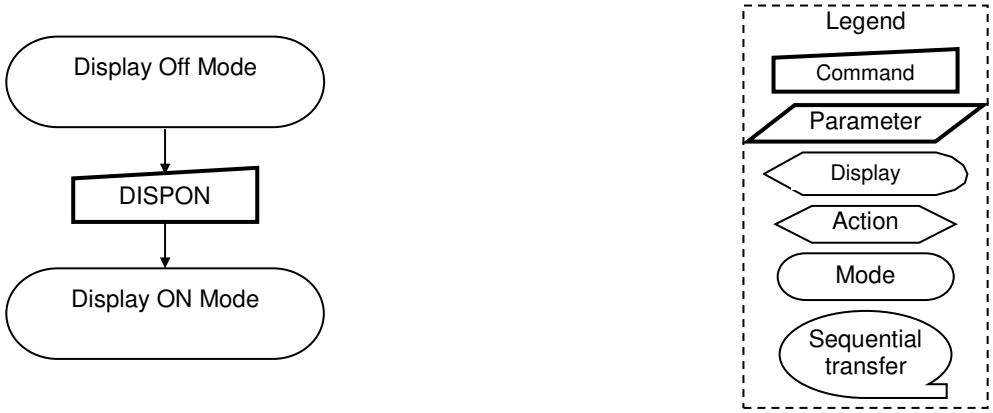
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



6.2.19 Memory Access Control (36h)

36 H	MADCTR (Memory Access Control)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	1	1	0	36
Parameter	-	MY	MX	-	-	RGB	SS	-	-	-

Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

Bit Assignment

BIT	NAME	DESCRIPTION
D7	PAGE ADDRESS ORDER (MY)	These 2 bits controls interface to display direction
D6	COLUMN ADDRESS ORDER (MX)	
D3	RGB-BGR ORDER (BGR)	Color selector switch control 0=RGB color sequence, 1=BGR color sequence
D2	Horizontal ORDER (SS)	LCD horizontal refresh direction control

Restriction

-

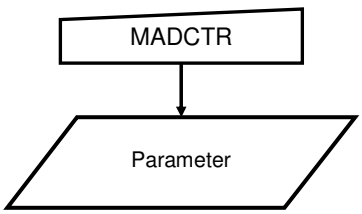
Register Availability

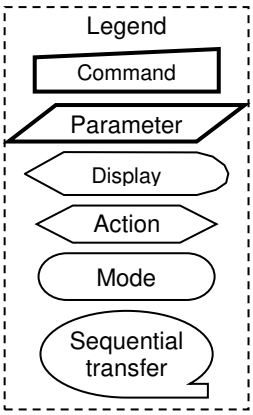
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No Change
H/W Reset	00h

Flow Chart





6.2.20 Idle Mode Off (38h)

38 H	IDMOFF (Idle Mode Off)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	0	0	38
Parameter	No Parameter									
Description	This command is used to recover from idle mode on In the idle off mode, display panel can display maximum 16.7M colors									
Restriction	This command has no effect when module is already in idle off mode.									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart

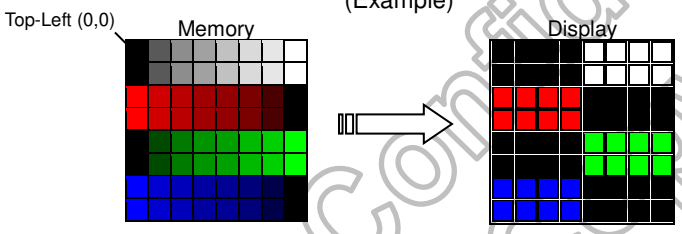
6.2.21 Idle Mode On (39h)

39 H	IDMON (Idle Mode on)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	0	1	39
Parameter	No Parameter									

Description

This command is used to enter idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

(Example)



"x" Don't care

Color	R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	G_7 G_6 G_5 G_4 G_3 G_2 G_1 G_0	B_7 B_6 B_5 B_4 B_3 B_4 B_1 B_0
Black	0xxx xxxx	0xxx xxxx	0xxx xxxx
Blue	0xxx xxxx	0xxx xxxx	1xxx xxxx
Red	1xxx xxxx	0xxx xxxx	0xxx xxxx
Magenta	1xxx xxxx	0xxx xxxx	1xxx xxxx
Green	0xxx xxxx	1xxx xxxx	0xxx xxxx
Cyan	0xxx xxxx	1xxx xxxx	1xxx xxxx
Yellow	1xxx xxxx	1xxx xxxx	0xxx xxxx
White	1xxx xxxx	1xxx xxxx	1xxx xxxx

Restriction

This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart

6.2.22 Write Display Brightness (51h)

51 H	WRDISBV (Write Display Brightness)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	0	0	1	51
Parameter	Write	DBV1[7]	DBV1[6]	DBV1[5]	DBV1[4]	DBV1[3]	DBV1[2]	DBV1[1]	DBV1[0]	00h
		DBV2[7]	DBV2[6]	DBV2[5]	DBV2[4]	DBV2[3]	DBV2[2]	DBV2[1]	DBV2[0]	00h

Description

This command is used to adjust brightness value.
In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

DBV[7:0]	Brightness Ratio	Brightness %
00h	0/256	0%
01h	1/256	0.39%
:	:	:
FEh	255/256	99.6%
FFH	256/256	100%

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

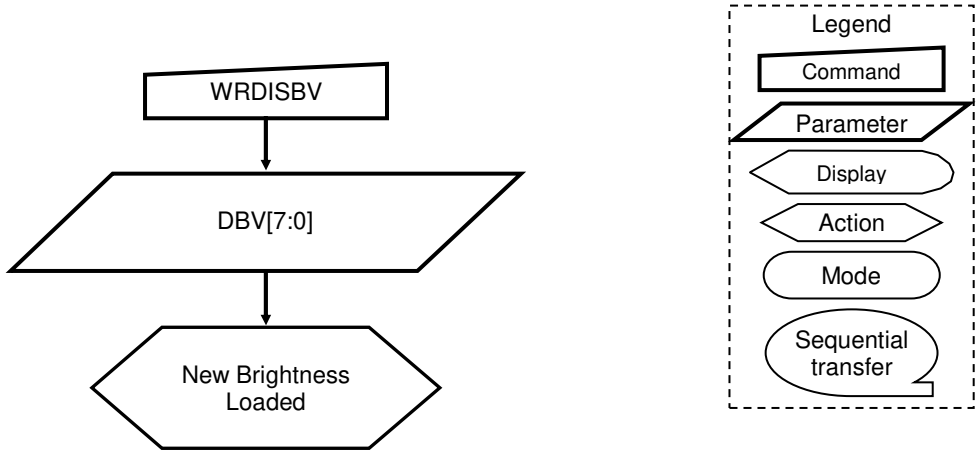
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.23 Read Display Brightness (52h)

52 H	RDDISBV (Read Display Brightness)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	0	1	0	0	1	0	52
Parameter	Read	DBV1[7]	DBV1[6]	DBV1[5]	DBV1[4]	DBV1[3]	DBV1[2]	DBV1[1]	DBV1[0]	00h
		DBV2[7]	DBV2[6]	DBV2[5]	DBV2[4]	DBV2[3]	DBV2[2]	DBV2[1]	DBV2[0]	00h
Description	This command is used to read brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	-									

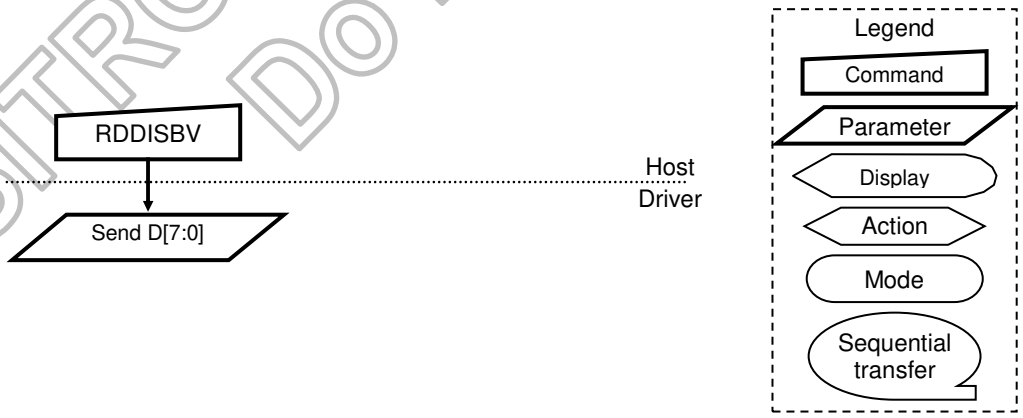
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.24 Write CTRL Display (53h)

53 H	WRCTRLD (Write CTRL Display Value)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	0	1	1	53
Parameter	Write	0	0	BCTRL	0	DD	BL	0	0	-

Description

This command is used to control display brightness.
I

Bits	Value
BCTRL	'0' off, DBV[7:0] is 00h; PWM keep low '1' On, DBV[7:0] is active; PWM output
DD	'0' Brightness dimming is off '1' Brightness dimming is on
BL	'0' Backlight Control is off '1' Backlight Control is on

Restriction

-

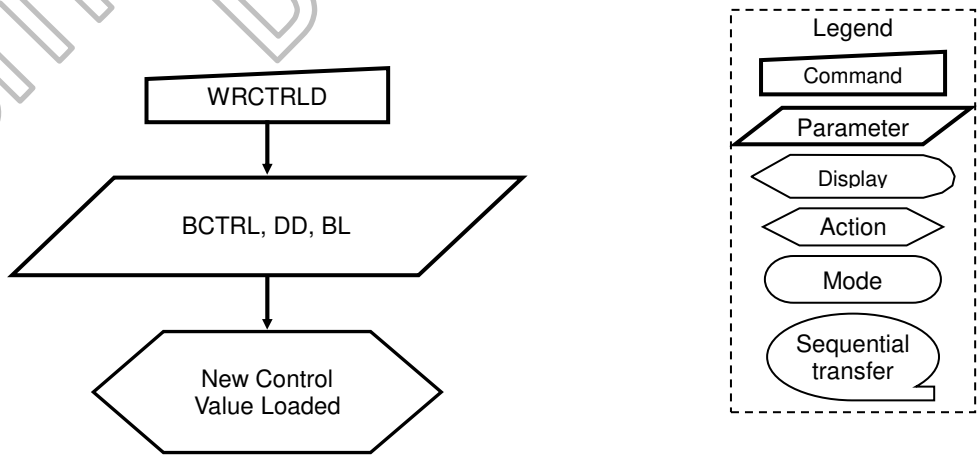
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.25 Read CTRL Display Value (54h)

54 H	RDCTRLD (Read CTRL Display Value)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	0	1	0	1	0	0	54
Parameter	Read	0	0	BCTRL	0	DD	BL	0	0	-
Description	This command is used to read brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	-									

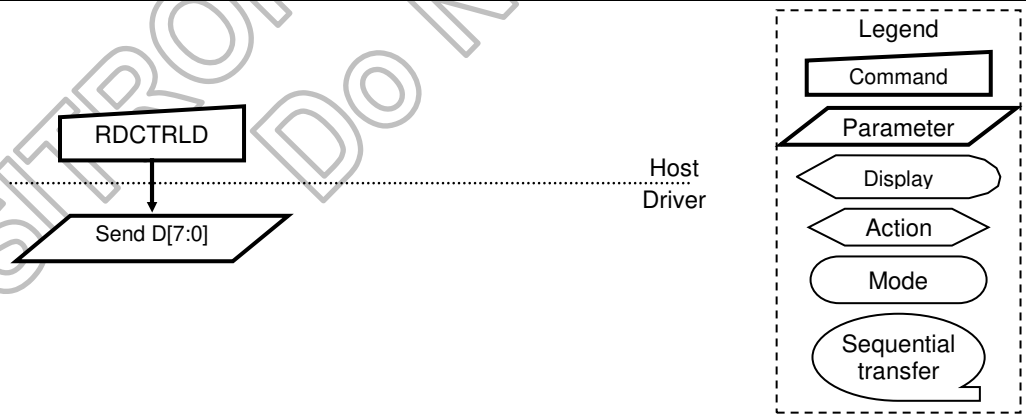
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.26 Write Content Adaptive Brightness Control (55h)

55 H	WRCABC (Write Content Adaptive Brightness Control)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	1	0	1	55
Parameter	Write	0	0	0	0	0	0	C1	C0	-

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

I

C1	C0	Function
0	0	Off
0	1	User Interface Image (UI mode)
1	0	Still Picture Image (Still mode)
1	1	Moving Picture Image (Moving mode)

Restriction

This register is synchronized with V-sync by internal circuit.

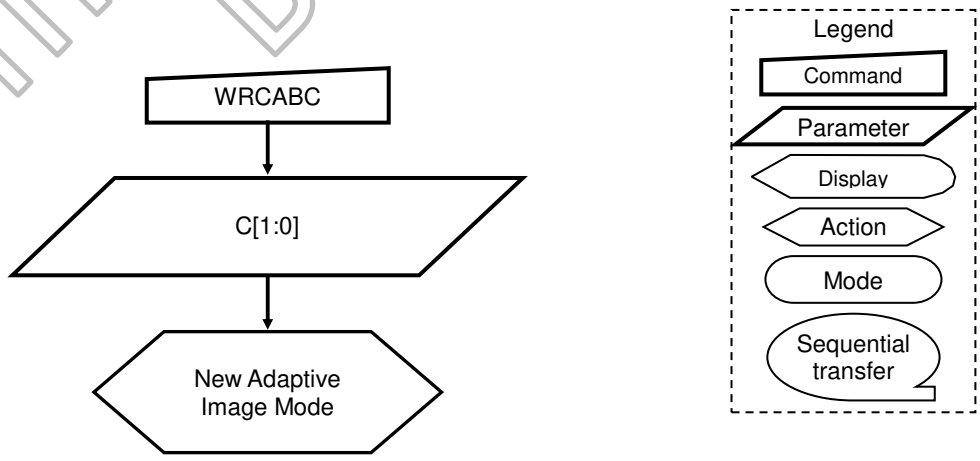
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.27 Read Content Adaptive Brightness Control (56h)

56 H	RDCABC (Read Content Adaptive Brightness Control)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	0	1	1	1	1	0	56
Parameter	Read	0	0	0	0	0	0	C1	C0	-

Description

This command is used to read parameters for image content based adaptive brightness control functionality.

I

C1	C0	Function
0	0	Off
0	1	User Interface Image (UI mode)
1	0	Still Picture Image (Still mode)
1	1	Moving Picture Image (Moving mode)

Restriction

-

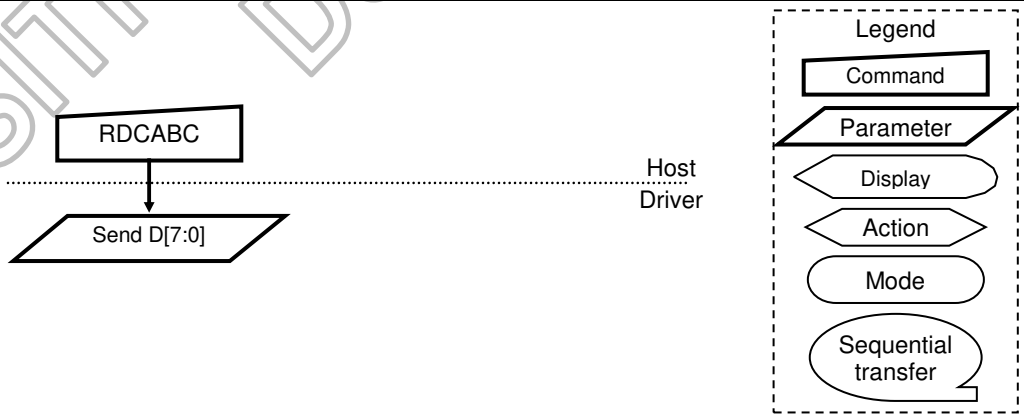
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.28 Write CABC Minimum Brightness (5Eh)

5E H	WRCABCMB (Write CABC minimum brightness)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	1	1	1	0	5E
Parameter	Write	CMB1[7]	CMB1[6]	CMB1[5]	CMB1[4]	CMB1[3]	CMB1[2]	CMB1[1]	CMB1[0]	00h
		CMB2[7]	CMB2[6]	CMB2[5]	CMB2[4]	CMB2[3]	CMB2[2]	CMB2[1]	CMB2[0]	00h
Description	This command is used to set the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.									
Restriction	-									

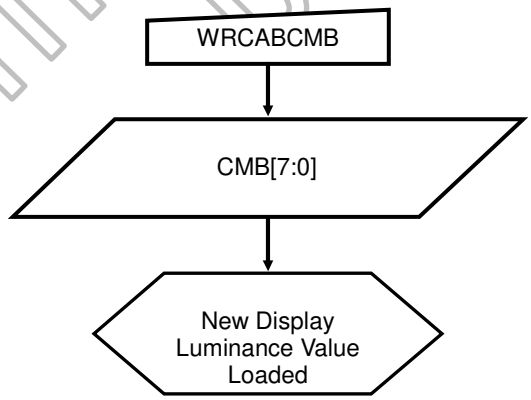
Register Availability

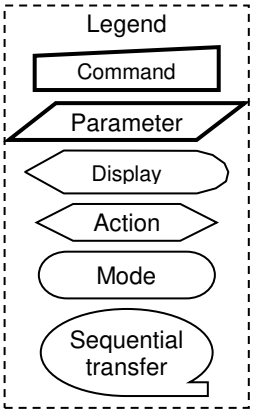
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart





6.2.29 Read CABC minimum brightness (5Fh)

5F H	RDCABCMB (Read CABC minimum brightness)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	0	1	1	1	1	1	5F
Parameter	Read	CMB1[7]	CMB1[6]	CMB1[5]	CMB1[4]	CMB1[3]	CMB1[2]	CMB1[1]	CMB1[0]	00h
		CMB2[7]	CMB2[6]	CMB2[5]	CMB2[4]	CMB2[3]	CMB2[2]	CMB2[1]	CMB2[0]	00h
Description	This command is used to read the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.									
Restriction	-									

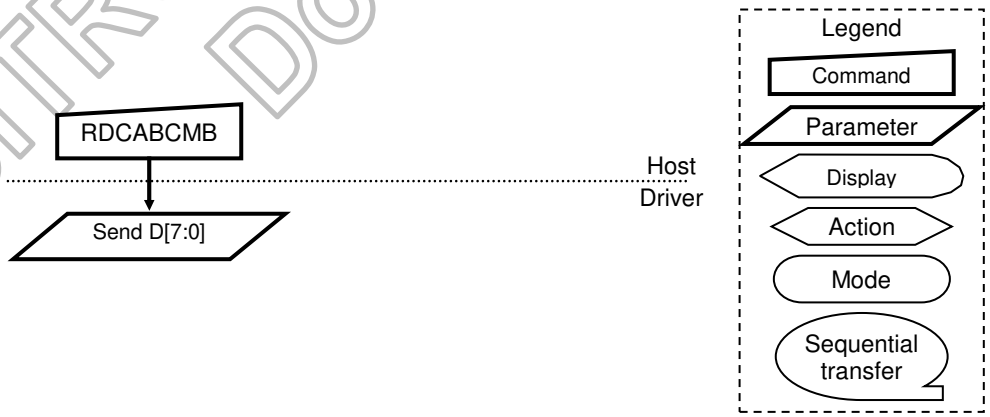
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.30 Read Black/White Low Bits (70h)

70 H	RDBWLB (Read Black White Low Bits)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	0	0	0	70
Parameter	Read	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	-
Description	This command returns the lowest bits of black and white color characteristic. Black: Bkx and Bky White: Wx and Wy									
Restriction	-									

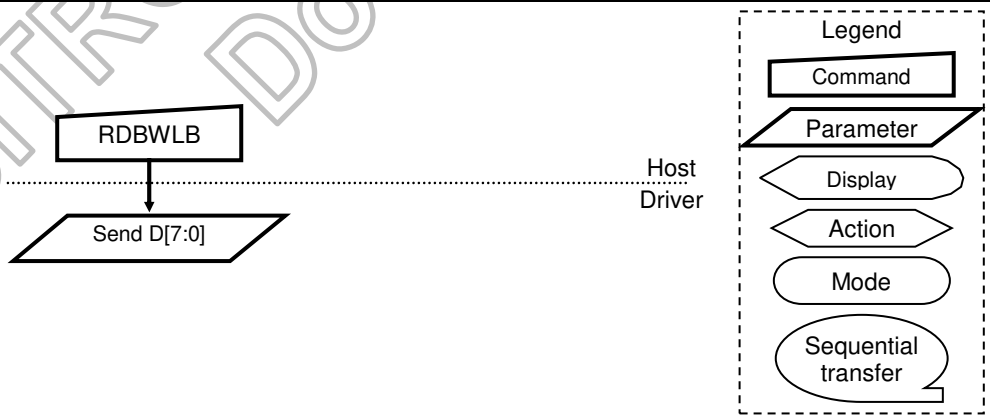
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.31 Read Bkx (71h)

71 H	RDBkx (Read Bkx)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	0	0	1	71
Parameter	Read	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	-
Description	This command returns the Bkx bits of black color characteristic.									
Restriction	-									

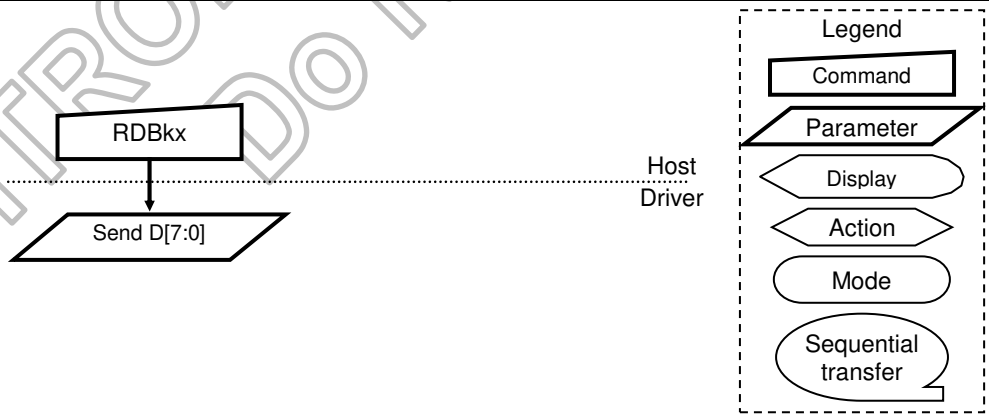
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.32 Read Bky (72h)

72 H	RDBky (Read Bky)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	0	1	0	72
Parameter	Read	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	-
Description	This command returns the Bky bits of black color characteristic.									
Restriction	-									

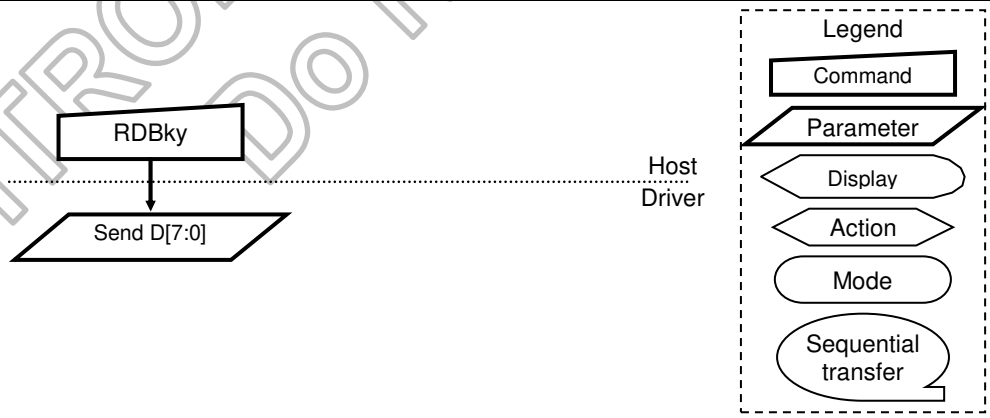
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.33 Read Wx (73h)

73 H	RDWx (Read Wx)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	0	1	1	73
Parameter	Read	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	-
Description	This command returns the Wx bits of White color characteristic.									
Restriction	-									

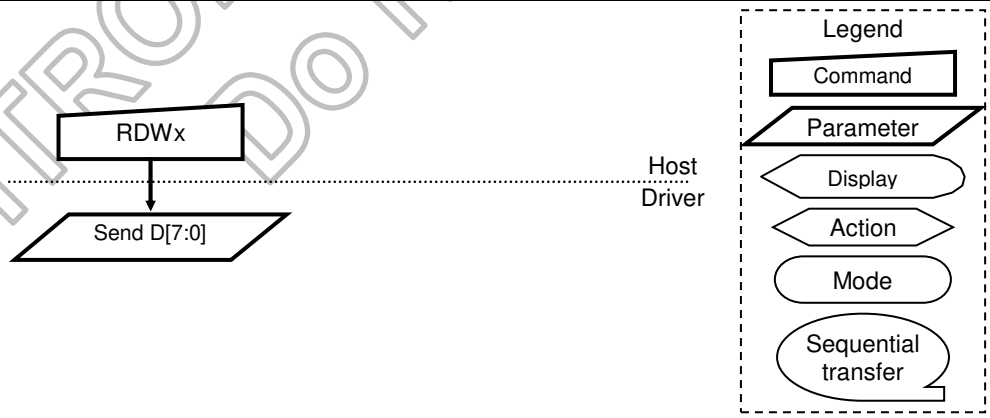
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.34 Read Wy (74h)

74 H	RDWy (Read Wy)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	1	0	0	74
Parameter	Read	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	-
Description	This command returns the Wy bits of White color characteristic.									
Restriction	-									

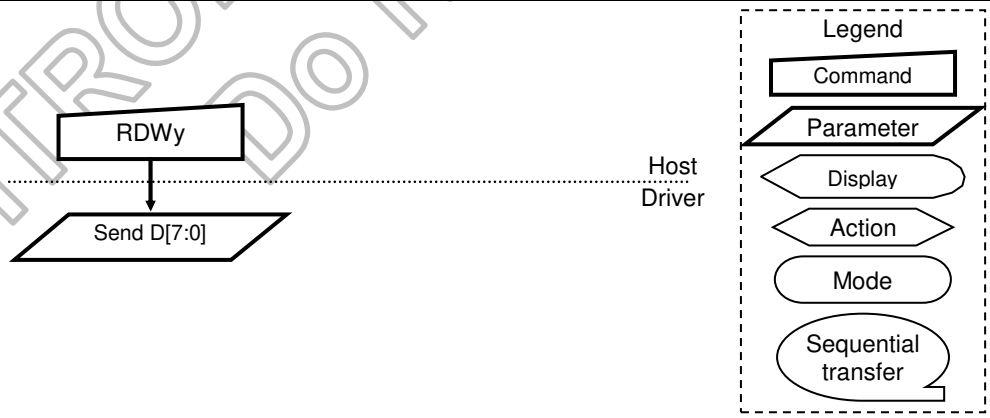
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.35 Read Red/Green Low Bits (75h)

75 H	RDRGLB (Read Red Green Low Bits)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	1	0	1	75
Parameter	Read	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	-
Description	This command returns the lowest bits of Red and Green color characteristic. Red: Rx and Ry Green: Gx and Gy									
Restriction	-									

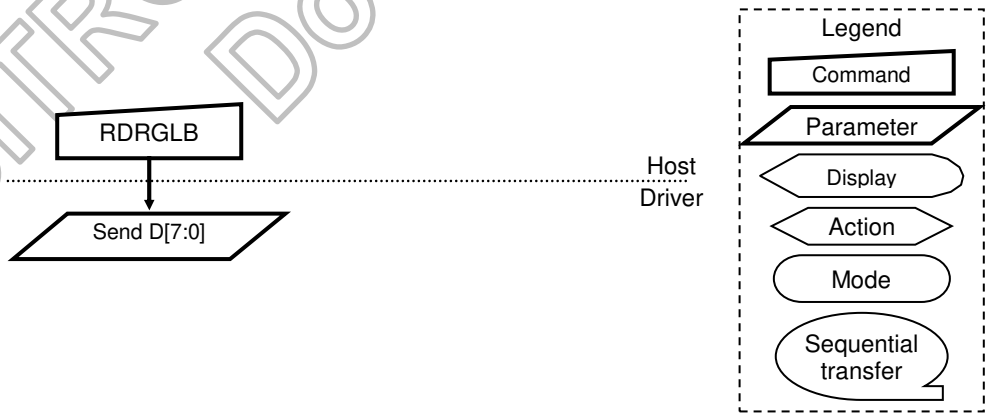
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.36 Read Rx (76h)

76 H	RDRx (Read Rx)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	1	1	0	76
Dummy Cycle										
Parameter	Read	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	-
Description	This command returns the Rx bits of Red color characteristic.									
Restriction	-									

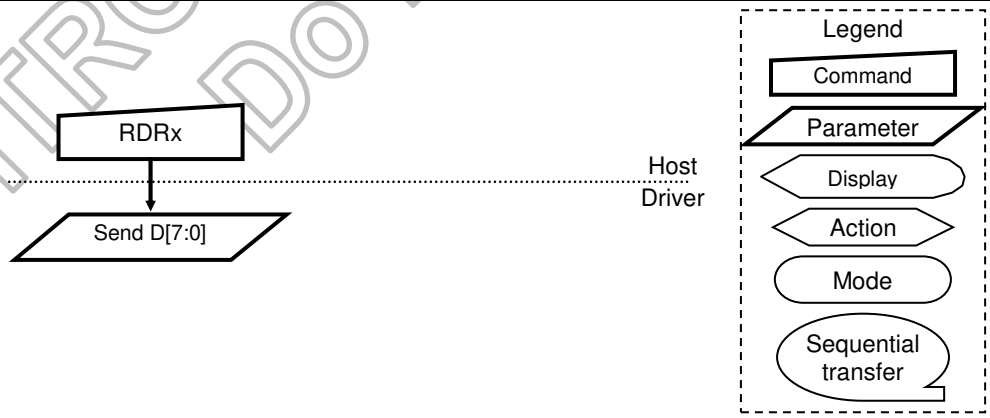
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.37 Read Ry (77h)

77 H	RDRy (Read Ry)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	1	1	1	77
Dummy Cycle										
Parameter	Read	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	-
Description	This command returns the Ry bits of Red color characteristic.									
Restriction	-									

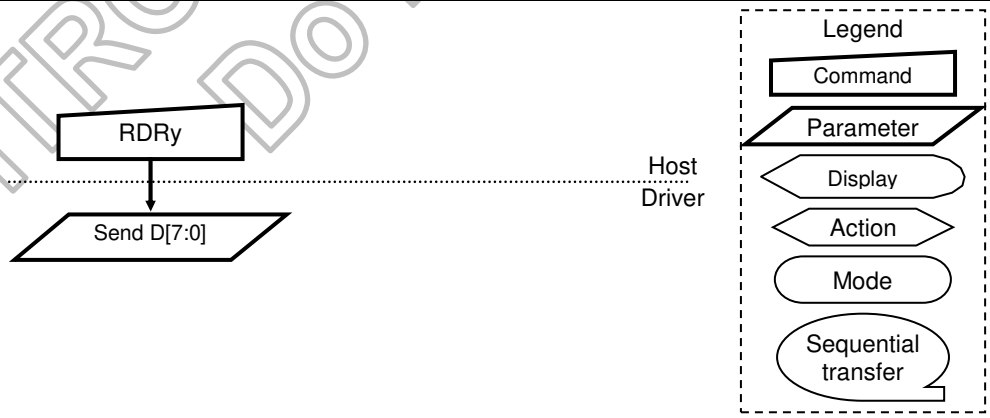
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.38 Read Gx (78h)

78 H	RDGx (Read Gx)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	0	0	0	78
Dummy Cycle										
Parameter	Read	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	-
Description	This command returns the Gx bits of Green color characteristic.									
Restriction	-									

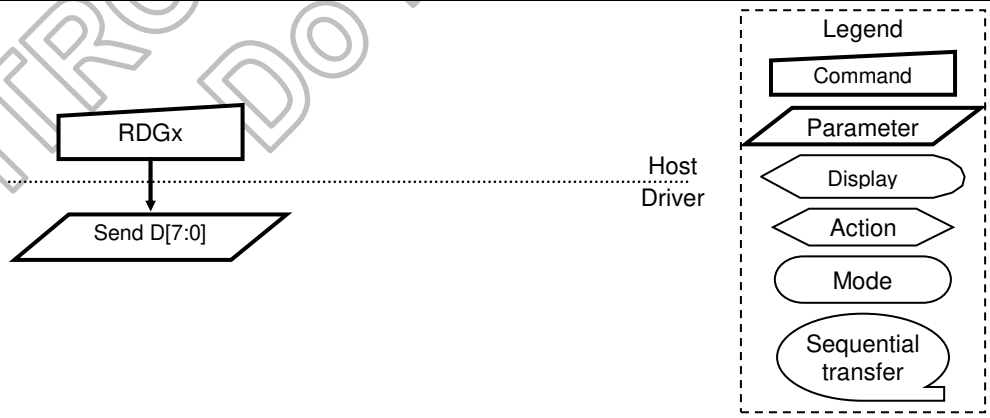
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.39 Read Gy (79h)

79 H	RDGy (Read Gy)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	0	0	1	79
Dummy Cycle										
Parameter	Read	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	-
Description	This command returns the Gy bits of Green color characteristic.									
Restriction	-									

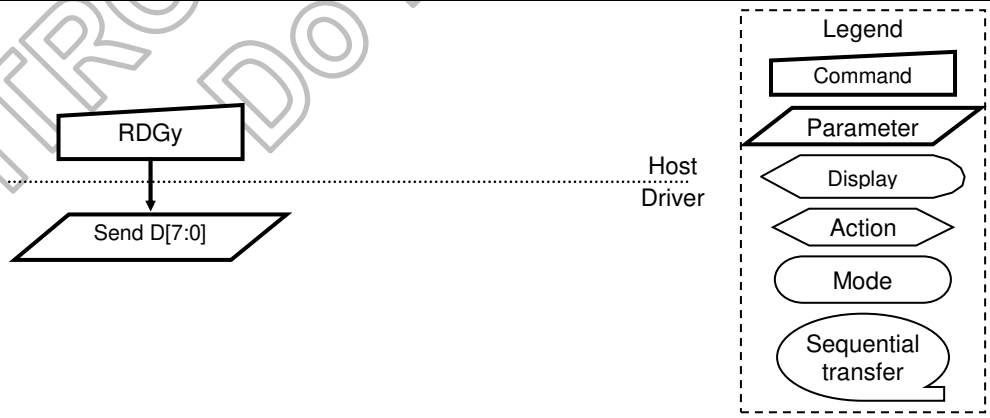
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.40 Read Blue/AColor Low Bits (7Ah)

7A H	RDBALB (Read Blue AColor Low Bits)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	0	1	0	7A
Dummy Cycle										
Parameter	Read	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	-
Description	This command returns the lowest bits of Blue and AColor color characteristic. Blue: Bx and By A: Ax and Ay									
Restriction	-									

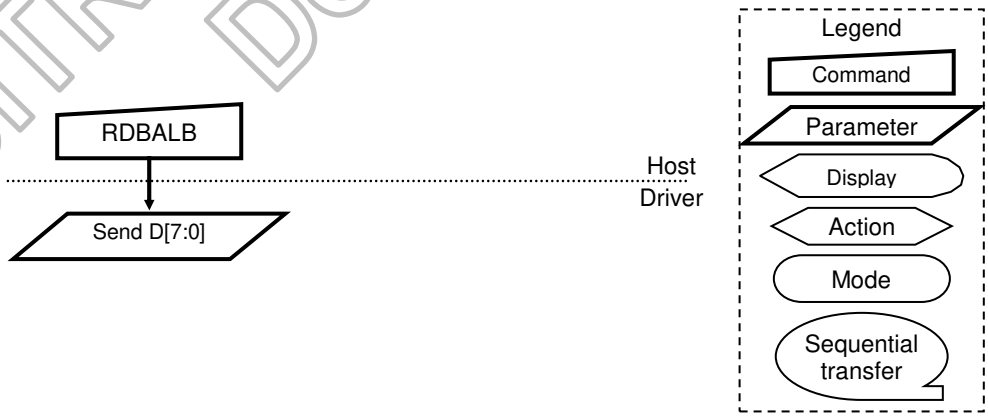
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.41 Read Bx (7Bh)

7B H	RDBx (Read Bx)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	0	1	1	7B
Dummy Cycle										
Parameter	Read	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	-
Description	This command returns the Bx bits of Blue color characteristic.									
Restriction	-									

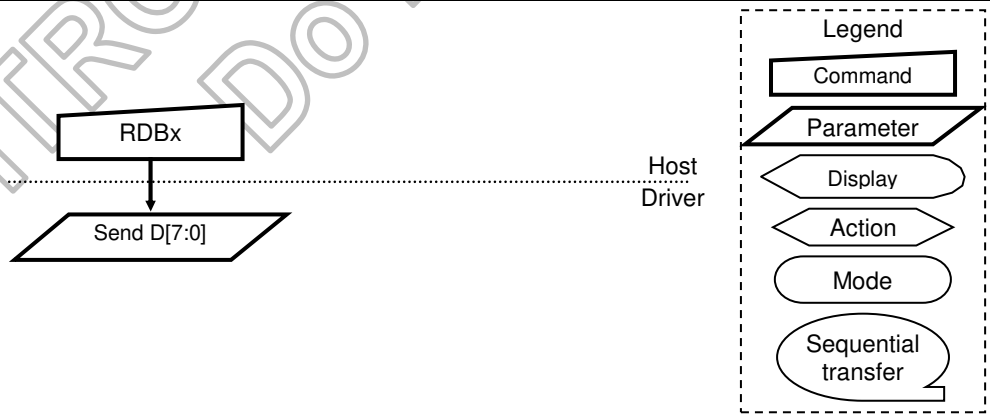
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.42 Read By (7Ch)

7C H	RDBy (Read By)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	1	0	0	7C
Dummy Cycle										
Parameter	Read	By9	By8	By7	By6	By5	By4	By3	By2	-
Description	This command returns the By bits of Blue color characteristic.									
Restriction	-									

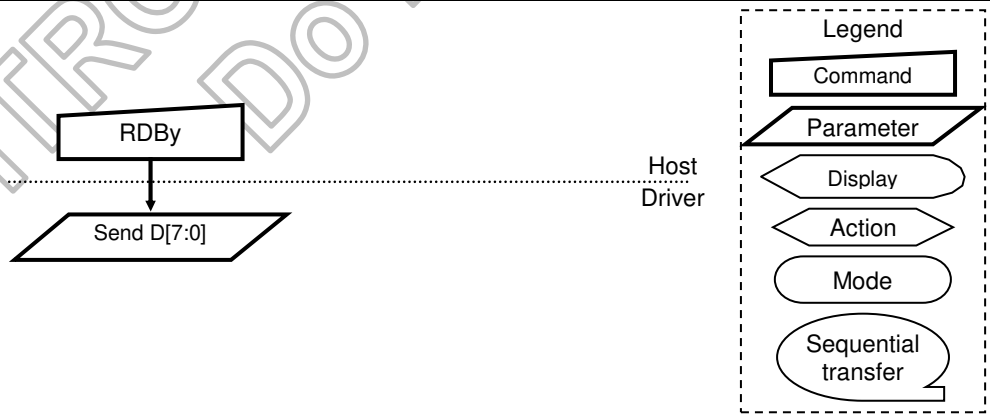
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.43 Read Ax (7Dh)

7D H	RDAx (Read Ax)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	1	0	1	7D
Dummy Cycle										
Parameter	Read	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	-
Description	This command returns the Ax bits of A color characteristic.									
Restriction	-									

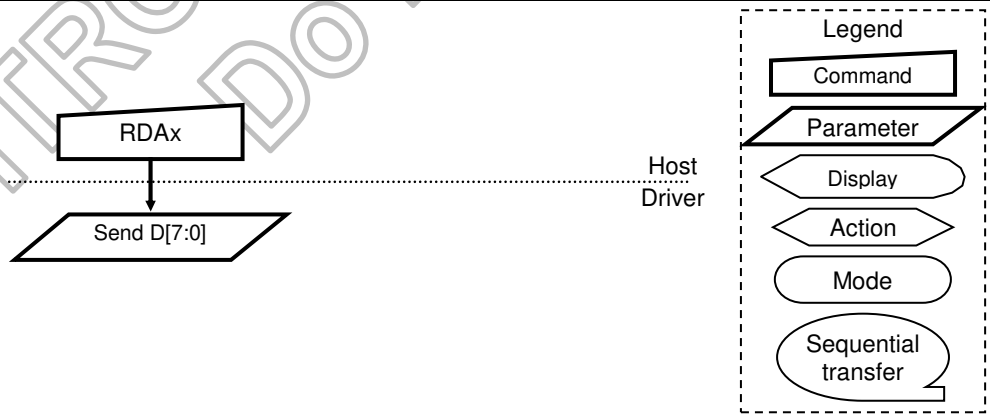
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.44 Read Ay (7Eh)

7E H	RDAy (Read Ay)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	1	1	0	7E
Dummy Cycle										
Parameter	Read	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	-
Description	This command returns the Ay bits of A color characteristic.									
Restriction	-									

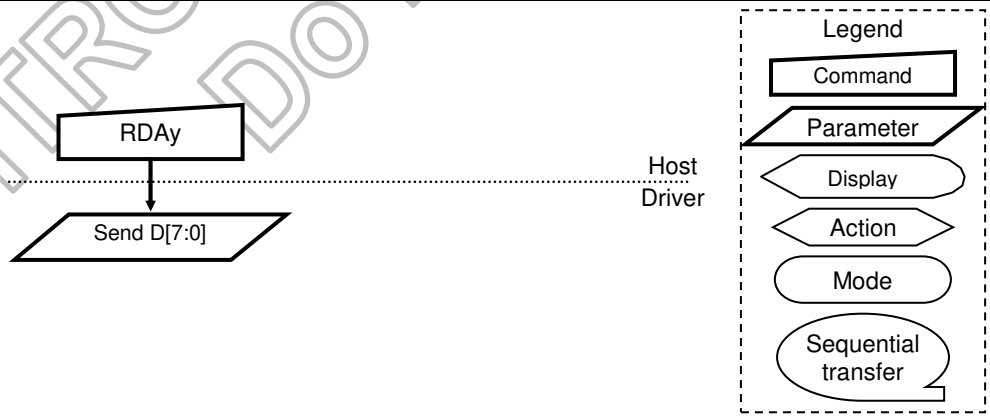
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.45 Read DDB Start (A1h)

A1 H	RDDDBS (Read DDB Start)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	0	1	0	0	0	0	1	A1
1st Parameter	Read	x	x	x	x	x	x	x	x	-
2nd Parameter		x	x	x	x	x	x	x	x	
3Rd Parameter		x	x	x	x	x	x	x	x	
4th parameter		x	x	x	x	x	x	x	x	
5th parameter		1	1	1	1	1	1	1	1	
Description	This command returns the supplier identification and display module mode/revision information. Note: This information is not the same what "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)"commands are returning. Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block. This read sequence can be interrupted by any command and it can be continued by "Read DDB Continue (A8h)" command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd parameter has been sent=> interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.									
Restriction	-									

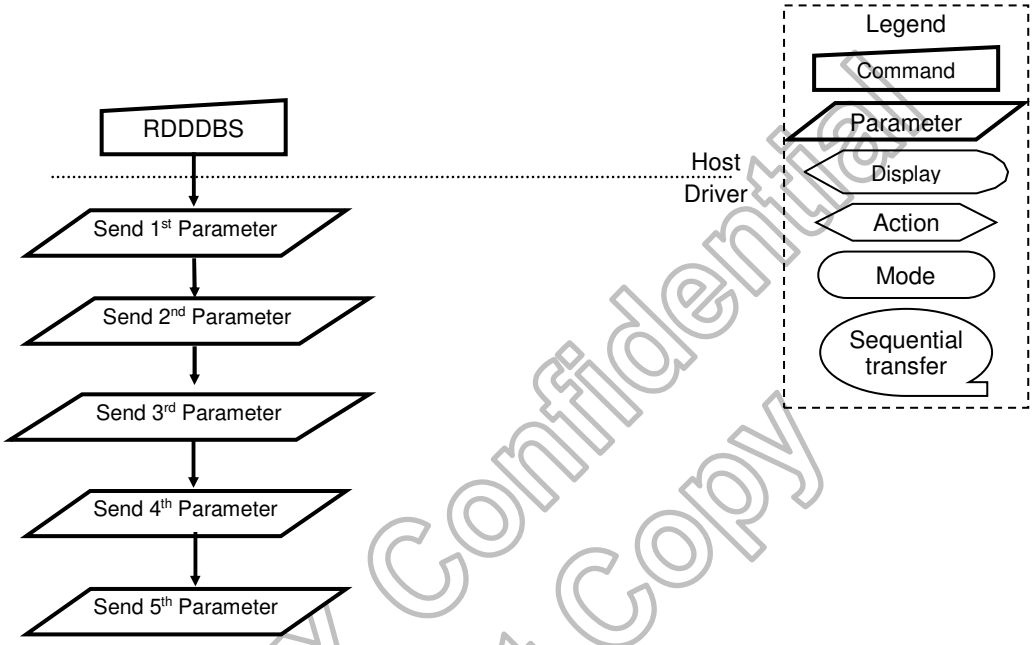
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.46 Read DDB Continue (A8h)

A8 H	RDDDBC (Read DDB Continue)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	0	1	0	1	0	0	0	A8
1st Parameter	Read	x	x	x	x	x	x	x	x	-
2nd Parameter		x	x	x	x	x	x	x	x	
3Rd Parameter		x	x	x	x	x	x	x	x	
4th parameter		x	x	x	x	x	x	x	x	
5th parameter		1	1	1	1	1	1	1	1	
Description	This command returns the supplier identification and display module mode/revision information from the point where RDDDBS command was interrupted by an other command. Note: Parameter 0xFF is an “Exit Code”, this means that there is no more data in the DDB block.									
Restriction	-									

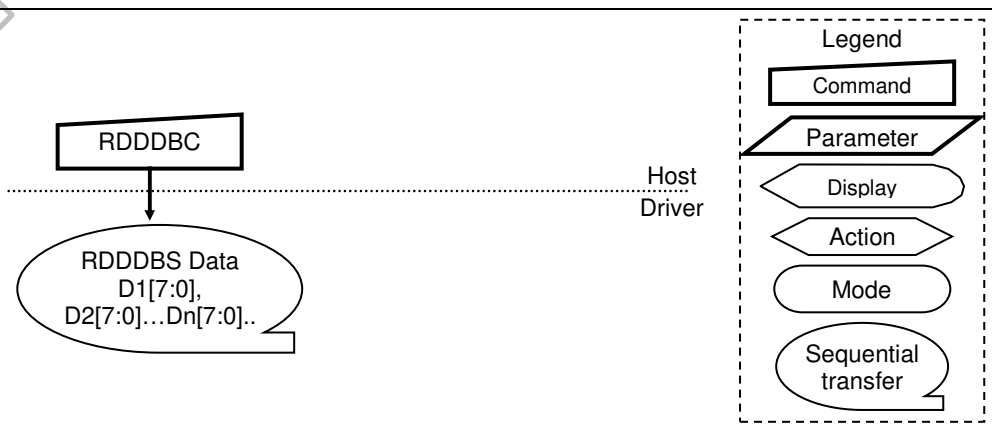
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.47 Read ID1 Value (DAh)

DA H	RDID1 (Read ID1 Value)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	1	0	1	1	0	1	0	DA
Parameter	Read	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
Description	This read byte identifies the LCD module's manufacturer.									
Restriction	-									

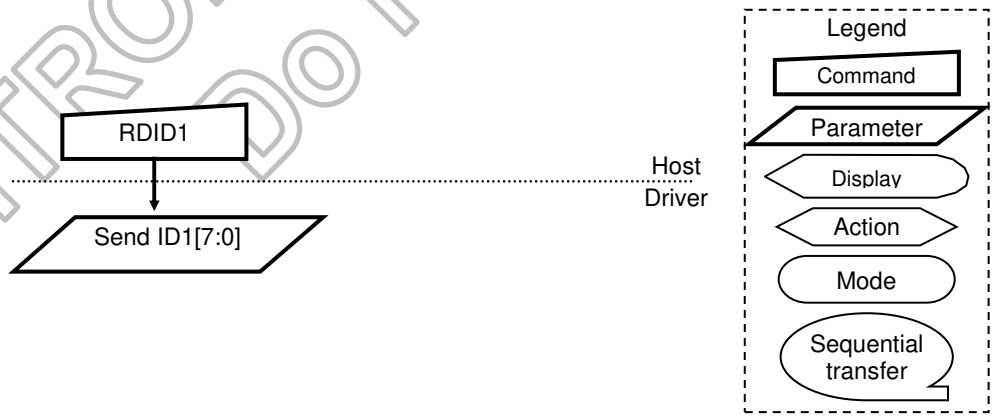
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	38h	OTP Value
S/W Reset	38h	OTP Value
H/W Reset	38h	OTP Value

Flow Chart



6.2.48 Read ID2 Value (DBh)

DB H	RDID2 (Read ID2 Value)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	1	0	1	1	0	1	1	DB
Parameter	Read	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
Description	This read byte identifies the LCD module version.									
Restriction	-									

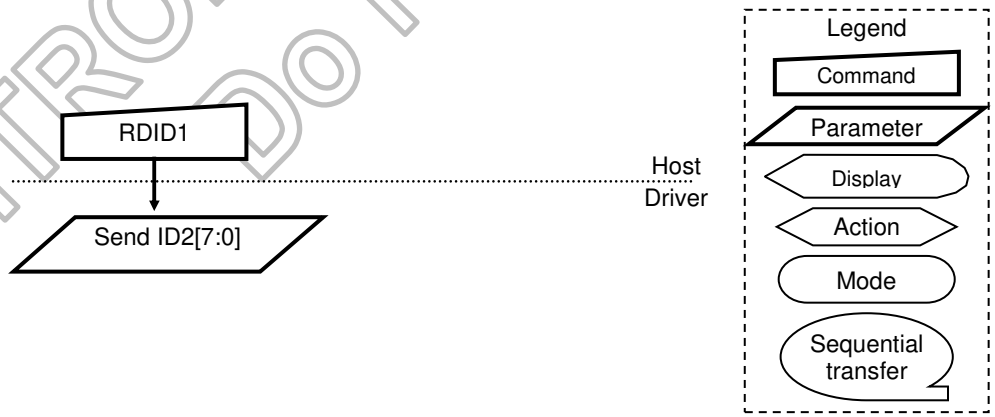
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	21h	OTP Value
S/W Reset	21h	OTP Value
H/W Reset	21h	OTP Value

Flow Chart



6.2.49 Read ID3 Value (DCh)

DC H	RDID3 (Read ID3 Value)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	1	0	1	1	1	0	0	DC
Dummy Cycle										
Parameter	Read	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-
Description	This read byte identifies the LCD module/driver.									
Restriction	-									

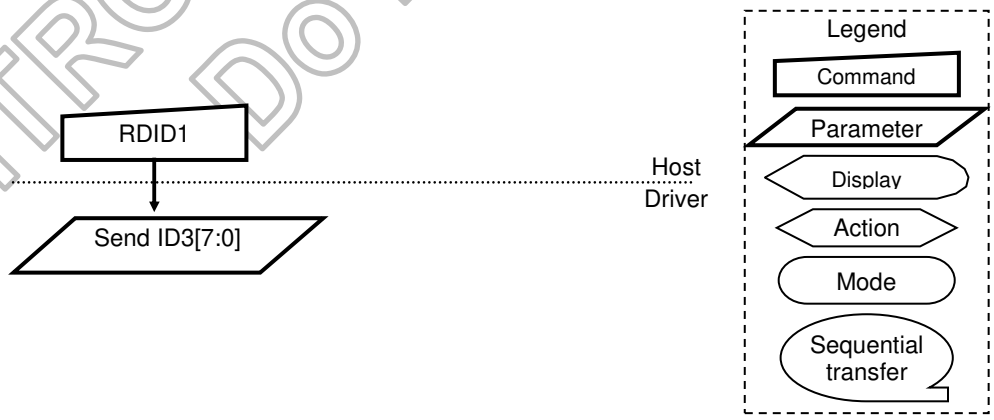
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	1Fh	OTP Value
S/W Reset	1Fh	OTP Value
H/W Reset	1Fh	OTP Value

Flow Chart



6.2.50 SETEXTC (B9h)

B9 H	SETEXTC									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	1	0	0	1	B9
Parameter 1st	W	EXTC1[7]	EXTC1[6]	EXTC1[5]	EXTC1[4]	EXTC1[3]	EXTC1[2]	EXTC1[1]	EXTC1[0]	00
Parameter 2nd	W	EXTC2[7]	EXTC2[6]	EXTC2[5]	EXTC2[4]	EXTC2[3]	EXTC2[2]	EXTC2[1]	EXTC2[0]	00
Parameter 3rd	W	EXTC3[7]	EXTC3[6]	EXTC3[5]	EXTC3[4]	EXTC3[3]	EXTC3[2]	EXTC3[1]	EXTC3[0]	00
Description	This command is used to enable USER Command. Enable User command: Set B9H=F1h, 12h, 83h Disable User command: Set B9H=00h, 00h, 00h									

6.2.51 SETAPID (B1h)

B1 H	SETAPID									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	0	0	0	1	B1
Parameter 1st	W	RES_V_SEL	x	x	x	x	RES_V_[10]	RES_V_[9]	RES_V_[8]	00
Parameter 2nd	W	x	x	x	x	PWM_DUTY_RESO[2]	PWM_DUTY_RESO[1]	PWM_DUTY_RESO[0]	DBV_TYPE	00
Description	This command is used to set APID. • **PWM_DUTY_RESO[2:0]**：Select PWM Duty Resolution. - 000：8 bit - 001：9 bit - 010：10 bit - 011：11 bit - 100：12 bit • **DBV_TYPE**：Select RDDBV MSB's Location.									

6.2.52 SETDISP (B2h)

B2 H	SETDISP									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	0	0	1	0	B2
Parameter 1st	R/W	NL[7]	NL[6]	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	C8
Parameter 2nd	R/W	RES_V_LSB[1]	RES_V_LSB[0]	BLK_CON[1]	BLK_CON[0]	x	RESO_SEL[2]	RESO_SEL[1]	RESO_SEL[0]	02
Parameter 3rd	R/W	WHITE_GND_EN	WHITE_FRAME_SEL[2]	WHITE_FRAME_SEL[1]	WHITE_FRAME_SEL[0]	x	ISC[2]	ISC[1]	ISC[0]	A0

Description

This command is used to control the display resolution.

• **NL[7:0] / RES_V_LSB[1:0]：**Specify the gate number of vertical direction.

- RES_V_SEL=0
  Gate Number = 480 + NL*4 + RES_V_LSB
- RES_V_SEL=1 (Max. Gate Number = 2047)
  Gate Number = ((480 + NL*4 + RES_V_LSB)%256) + (RES_V_[10:8]*256)

• **BLK_CON[1:0]：**Non-display area source output control.

BLK_CON		Source output
0	0	Keep last data
0	1	VSSD
1	0	Hi-Z
1	1	Setting inhibited

• **RESO_SEL[2:0]：**Specify the channel number of source direction.

RESO_SEL[2:0] (Hex)	Channel number
0	-
1	-
2	720RGB
3	640RGB
4	600RGB
5	540RGB
others	Setting inhibited

• **WHITE_GND_EN：**Determine source voltage during Blanking Time when accessing Sleep-Out / Sleep-In command.

- 1：Source Voltage = GND
- 0：Source Voltage = Lowest Voltage

• **WHITE_FRAME_SEL[2:0]**：Blank timing control when access sleep out command.

WHITE_FRAME			Blank Frame Period
0	0	0	0 frame
0	0	1	1 frame
0	1	0	2 frames
0	1	1	3 frames
1	0	0	4 frames
1	0	1	5 frames
1	1	0	6 frames
1	1	1	7 frames

• **ISC[2:0]**：Source output refresh control.

ISC			Refresh Period
0	0	0	0 frame
0	0	1	1 frame
0	1	0	2 frames
:			:
1	1	1	7 frames

6.2.53 SETRGBIF (B3h)

B3 H	SETRGBIF									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	0	0	1	1	B3
Parameter 1st	R/W	VBP_RGB_GEN[7]	VBP_RGB_GEN[6]	VBP_RGB_GEN[5]	VBP_RGB_GEN[4]	VBP_RGB_GEN[3]	VBP_RGB_GEN[2]	VBP_RGB_GEN[1]	VBP_RGB_GEN[0]	28
Parameter 2nd	R/W	VFP_RGB_GEN[7]	VFP_RGB_GEN[6]	VFP_RGB_GEN[5]	VFP_RGB_GEN[4]	VFP_RGB_GEN[3]	VFP_RGB_GEN[2]	VFP_RGB_GEN[1]	VFP_RGB_GEN[0]	28
Parameter 3rd	R/W	DE_BP_RGB_GEN[7]	DE_BP_RGB_GEN[6]	DE_BP_RGB_GEN[5]	DE_BP_RGB_GEN[4]	DE_BP_RGB_GEN[3]	DE_BP_RGB_GEN[2]	DE_BP_RGB_GEN[1]	DE_BP_RGB_GEN[0]	28
Parameter 4th	R/W	DE_FP_RGB_GEN[7]	DE_FP_RGB_GEN[6]	DE_FP_RGB_GEN[5]	DE_FP_RGB_GEN[4]	DE_FP_RGB_GEN[3]	DE_FP_RGB_GEN[2]	DE_FP_RGB_GEN[1]	DE_FP_RGB_GEN[0]	28

Description

This command is used to control RGB I/F porch timing for internal use.

- **VBP_RGB_GEN[7:0]**：Vertical back porch HS number selection in Blank Frame Period.
- **VFP_RGB_GEN[7:0]**：Vertical front porch HS number selection in Blank Frame Period.

VBP_RGB_GEN[7:0] VFP_RGB_GEN[7:0] (Hex)	Hsync number
0	Setting inhibited
1	Setting inhibited
2	2
:	:
FE	254
FF	Setting inhibited

- **DE_BP_RGB_GEN[7:0]**：HBP OSC number selection in Blank Frame Period.
- **DE_FP_RGB_GEN[7:0]**：HFP OSC number selection in Blank Frame Period.

DE_BP_RGB_GEN[7:0] DE_FP_RGB_GEN[7:0] (Hex)	OSC number
0	Setting inhibited
1	Setting inhibited
2	2
:	:
FE	254
FF	Setting inhibited

6.2.54 SETCYC (B4h)

B4 H	SETCYC									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	0	1	0	0	B4
Parameter 1st	R/W	ZINV_S2401_EN	ZINV_G_EVEN_EN	ZINV_EN	ZINV2_EN	x	N_NW[2]	N_NW[1]	N_NW[0]	80
Parameter 2nd	R/W	x	x	x	x	x	I_NW[2]	I_NW[1]	I_NW[0]	00

Description

This command is used to control display inversion type.

• **ZINV_S2401_EN**：Specify extra source for Zig-Zag Inversion.
- 1：S2401 for use
- 0：S0 for use

• **ZINV_G_EVEN_EN**：Specify in which row source data dislocates.
- 1：Odd row
- 0：Even row

• **ZINV_EN**：Enable Zig-Zag inversion.
- 1：Enable Zig-Zag Inversion
- 0：Disable Zig-Zag Inversion.

• **ZINV2_EN**：Specify Zig-Zag inversion selection.
- 1：Enable Zig-Zag2 Inversion
- 0：Enable Zig-Zag1 Inversion.

◎ For Zig-Zag2 Inversion Type Definition, please refer to the following table.

ZINV2_EN	ZINV_S2401_EN	ZINV_G_EVEN_EN	Zig-Zag Inversion Type
0	0	1	Type A
0	0	0	Type B
0	1	0	Type C
0	1	1	Type D
1	0	1	Type E
1	0	0	Type F
1	1	0	Type G
1	1	1	Type H

• **N_NW[2:0]:** Normal mode inversion type selection.
• **I_NW[2:0] :** IDLE mode inversion type selection.

N_NW[2:0] I_NW[2:0]			Inversion Type
0	0	0	Column inversion
0	0	1	1-dot inversion
0	1	0	1+2-dot inversion
0	1	1	3-dot inversion
1	0	0	4-dot inversion
1	0	1	8-dot inversion
1	1	0	2-dot inversion
1	1	1	Setting invalid

6.2.55 SETBGP (B5h)

B5 H	SETBGP									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	0	1	0	1	B5
Parameter 1st	R/W	x	x	x	VREF_SEL[4]	VREF_SEL[3]	VREF_SEL[2]	VREF_SEL[1]	VREF_SEL[0]	09
Parameter 2nd	R/W	x	x	x	NVREF_SEL[4]	NVREF_SEL[3]	NVREF_SEL[2]	NVREF_SEL[1]	NVREF_SEL[0]	09

Description

This command is used for internal reference voltage setting.

• **VREF_SEL[4:0] / NVREF_SEL[4:0]：** Specify the VREF/NVREF voltage.

VREF_SEL[4:0] NVREF_SEL[4:0] (Hex)	VREF |NVREF| (V)	VREF_SEL[4:0] NVREF_SEL[4:0] (Hex)	VREF |NVREF| (V)
0	3.5	10	5.1
1	3.6	11	5.2
2	3.7	12	5.3
3	3.8	13	5.4
4	3.9	14	5.45
5	4.0	15	5.5
6	4.1	16	5.55
7	4.2	17	5.6
8	4.3	18	5.65
9	4.4	19	5.7
A	4.5	1A	5.75
B	4.6	1B	5.8
C	4.7	1C	5.85
D	4.8	1D	5.9
E	4.9	1E	5.95
F	5.0	1F	6.0

6.2.56 SETVCOM (B6h)

B6 H	SETVCOM									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	0	1	1	0	B6
Parameter 1st	R/W	VCOMDC_F[7]	VCOMDC_F[6]	VCOMDC_F[5]	VCOMDC_F[4]	VCOMDC_F[3]	VCOMDC_F[2]	VCOMDC_F[1]	VCOMDC_F[0]	4D
Parameter 2nd	R/W	VCOMDC_B[7]	VCOMDC_B[6]	VCOMDC_B[5]	VCOMDC_B[4]	VCOMDC_B[3]	VCOMDC_B[2]	VCOMDC_B[1]	VCOMDC_B[0]	4D
Parameter 3rd	R	x	x	x	x	x	VCOM_OTP_TIME[2]	VCOM_OTP_TIME[1]	VCOM_OTP_TIME[0]	00

Description

This command is used to set VCOM Voltage.

- **VCOMDC_F[7:0]**：Specify the VCOMDC voltage at GS_PANEL="0".
- **VCOMDC_B[7:0]**：Specify the VCOMDC voltage at GS_PANEL="1".

VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)	VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)	VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)
0	0	10	-0.36	20	-0.55
1	-0.025	11	-0.375	21	-0.56
2	-0.05	12	-0.39	22	-0.57
3	-0.075	13	-0.405	23	-0.58
4	-0.1	14	-0.42	24	-0.59
5	-0.125	15	-0.435	25	-0.6
6	-0.15	16	-0.45	26	-0.61
7	-0.175	17	-0.46	27	-0.62
8	-0.2	18	-0.47	28	-0.63
9	-0.225	19	-0.48	29	-0.64
A	-0.25	1A	-0.49	2A	-0.65
B	-0.275	1B	-0.5	2B	-0.66
C	-0.3	1C	-0.51	2C	-0.67
D	-0.315	1D	-0.52	2D	-0.68
E	-0.33	1E	-0.53	2E	-0.69
F	-0.345	1F	-0.54	2F	-0.7

VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)	VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)	VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)
30	-0.71	40	-0.87	50	-1.03
31	-0.72	41	-0.88	51	-1.04
32	-0.73	42	-0.89	52	-1.05
33	-0.74	43	-0.9	53	-1.06
34	-0.75	44	-0.91	54	-1.07
35	-0.76	45	-0.92	55	-1.08
36	-0.77	46	-0.93	56	-1.09
37	-0.78	47	-0.94	57	-1.1
38	-0.79	48	-0.95	58	-1.11
39	-0.8	49	-0.96	59	-1.12
3A	-0.81	4A	-0.97	5A	-1.13
3B	-0.82	4B	-0.98	5B	-1.14
3C	-0.83	4C	-0.99	5C	-1.15
3D	-0.84	4D	-1	5D	-1.16
3E	-0.85	4E	-1.01	5E	-1.17
3F	-0.86	4F	-1.02	5F	-1.18

VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)	VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)	VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)
60	-1.19	70	-1.35	80	-1.51
61	-1.2	71	-1.36	81	-1.52
62	-1.21	72	-1.37	82	-1.53
63	-1.22	73	-1.38	83	-1.54
64	-1.23	74	-1.39	84	-1.55
65	-1.24	75	-1.4	85	-1.56
66	-1.25	76	-1.41	86	-1.57
67	-1.26	77	-1.42	87	-1.58
68	-1.27	78	-1.43	88	-1.59
69	-1.28	79	-1.44	89	-1.6
6A	-1.29	7A	-1.45	8A	-1.61
6B	-1.3	7B	-1.46	8B	-1.62
6C	-1.31	7C	-1.47	8C	-1.63
6D	-1.32	7D	-1.48	8D	-1.64
6E	-1.33	7E	-1.49	8E	-1.65
6F	-1.34	7F	-1.5	8F	-1.66

VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)	VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)	VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)
90	-1.67	A0	-1.845	B0	-2.085
91	-1.68	A1	-1.86	B1	-2.1
92	-1.69	A2	-1.875	B2	-2.115
93	-1.7	A3	-1.89	B3	-2.13
94	-1.71	A4	-1.905	B4	-2.145
95	-1.72	A5	-1.92	B5	-2.16
96	-1.73	A6	-1.935	B6	-2.175
97	-1.74	A7	-1.95	B7	-2.19
98	-1.75	A8	-1.965	B8	-2.205
99	-1.76	A9	-1.98	B9	-2.22
9A	-1.77	AA	-1.995	BA	-2.235
9B	-1.78	AB	-2.01	BB	-2.25
9C	-1.79	AC	-2.025	BC	-2.265
9D	-1.8	AD	-2.04	BD	-2.28
9E	-1.815	AE	-2.055	BE	-2.295
9F	-1.83	AF	-2.07	BF	-2.31

VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)	VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)	VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)
C0	-2.325	D0	-2.565	E0	-2.88
C1	-2.34	D1	-2.58	E1	-2.9
C2	-2.355	D2	-2.6	E2	-2.92
C3	-2.37	D3	-2.62	E3	-2.94
C4	-2.385	D4	-2.64	E4	-2.96
C5	-2.4	D5	-2.66	E5	-2.98
C6	-2.415	D6	-2.68	E6	-3
C7	-2.43	D7	-2.7	E7	-3.02
C8	-2.445	D8	-2.72	E8	-3.04
C9	-2.46	D9	-2.74	E9	-3.06
CA	-2.475	DA	-2.76	EA	-3.08
CB	-2.49	DB	-2.78	EB	-3.1
CC	-2.505	DC	-2.8	EC	-3.12
CD	-2.52	DD	-2.82	ED	-3.14
CE	-2.535	DE	-2.84	EE	-3.16
CF	-2.55	DF	-2.86	EF	-3.18

VCOMDC_F[7:0] VCOMDC_B[7:0] (Hex)	VCOMDC (V)
F0	-3.2
F1	-3.22
F2	-3.24
F3	-3.26
F4	-3.28
F5	-3.3
F6	-3.32
F7	-3.34
F8	-3.36
F9	-3.38
FA	-3.4
FB	-3.42
FC	-3.44
FD	-3.46
FE	-3.48
FF	-3.5

• **VCOM_OTP_TIME[2:0]** : Read VCOM OTP programming times.

VCOM_OTP_TIME[2:0]	OTP Programming times
0	NO OTPED
1	1
2	2
3	3
4	4

6.2.57 SETOTP (B7h)

B7 H	SETOTP									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	0	1	1	1	B7
Parameter 1st	R/W	OTP_KEY[7]	OTP_KEY[6]	OTP_KEY[5]	OTP_KEY[4]	OTP_KEY[3]	OTP_KEY[2]	OTP_KEY[1]	OTP_KEY[0]	FF
Parameter 2nd	R/W	OTP_MASK[7]	OTP_MASK[6]	OTP_MASK[5]	OTP_MASK[4]	OTP_MASK[3]	OTP_MASK[2]	OTP_MASK[1]	OTP_MASK[0]	00
Parameter 3rd	R/W	x	VPP_SEL[2]	VPP_SEL[1]	VPP_SEL[0[	x	X	x	OTP_INDEX[8]	30
Parameter 4th	R/W	OTP_INDEX[7]	OTP_INDEX[6]	OTP_INDEX[5]	OTP_INDEX[4]	OTP_INDEX[3]	OTP_INDEX[2]	OTP_INDEX[1]	OTP_INDEX[0]	00
Parameter 5th	R/W	Load_DIS	VPP_EN	OTP_SEL	OTP_PWE	OTP_PTM[1]	OTP_PTM[0]	OTP_POR	OTP_PORG	00
Parameter 6th	R	OTP_DATA[7]	OTP_DATA[6]	OTP_DATA[5]	OTP_DATA[4]	OTP_DATA[3]	OTP_DATA[2]	OTP_DATA[1]	OTP_DATA[0]	00

Description

This command is used to set OTP related setting.

• **OTP_KEY[7:0]**：Enable OTP function key.
- OTP_KEY = “5A”, enable OTP function.
- OTP_KEY = “00”, disable OTP function.

• **OTP_MASK[7:0]**：Mask function for OTP programming.
- 1：Means this bit will not be OTP in all programming process.
- 0：Means this bit will be OTP in all programming process.

• **VPPSEL[2:0]**：Specify VPP Voltage selection.

VPPSEL[2:0]	VPP Voltage (V)
0	7.2
1	7.3
2	7.4
3	7.5
4	7.6
5	7.7
6	7.8
7	External Power

• **OTP_INDEX[8:0]**：Set OTP Index of target register or byte.

• **Load_DIS**：Disable OTP load function.
- 1：Disable OTP load function.
- 0：Enable OTP load function.

• **VPP_EN**：Enable VPP Power.
- 1：Enable VPP Power.
- 0：Disable VPP Power.

• **OTP_SEL**：OTP functional block selection.
- Automatically set by IC in auto OTP.
- Manually set by user in manual OTP of DG register.

Description	• **OTP_PWE**：OTP Write Signal. - 1：OTP Write - 0：OTP don't Write • **OTP_PTM[1:0]**：For testing OTP robustness in test mode. - For CP usage. • **OTP_POR**：OTP Read Signal. - 1：OTP Read - 0：OTP don't Read • **OTP_PORG**：OTP Auto programming with related register. - 1：OTP auto programming start. - 0：OTP auto programming stop. • **OTP_DATA[7:0]**：OTP Data read back when VPP_POR="1".

6.2.58 SETPOWER_EXT (B8h)

B8 H	SETPOWER_EXT									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	1	0	0	0	B8
Parameter 1st	R/W	x	PCCS[2]	PCCS[1]	PCCS[0]	ECP_DC_DIV[3]	ECP_DC_DIV[2]	ECP_DC_DIV[1]	ECP_DC_DIV[0]	34
Parameter 2nd	R/W	x	SINGLE_PUMP	DT[1]	DT[0]	SYNC_STB	XDK_ECP[1]	XDK_ECP[0]	x	22
Parameter 3rd	R/W	x	x	x	x	x	PFM_DC_DIV[2]	PFM_DC_DIV[1]	PFM_DC_DIV[0]	00
Parameter 4th	R/W	x	x	x	x	x	x	ECP_SYNC_EN	VGX_SYNC_EN	03
Parameter 5th	R/W	A_DC[1]	A_DC[0]	A_DTP[2]	A_DTP[1]	A_DTP[0]	A_DTN[2]	A_DTN[1]	A_DTN[0]	ED
Parameter 6th	R/W	DCS[1]	DCS[0]	DTPS[2]	DTPS[1]	DTPS[0]	DTNS[2]	DTNS[1]	DTNS[0]	00

Description

This command is used to set display related register.

• **PCCS[2:0]**：External power IC or PFM selection.

PCCS[2:0]			IOVCC	VCI	VSP	VSN
0	0	0	IOVCC	VCI	PFM TYPE-A	PFM TYPE-A
0	0	1	IOVCC	VCI	PFM TYPE-C	PFM TYPE-C
0	1	0	IOVCC	VCI	FL1002	FL1002
0	1	1	IOVCC	VCI	PFM TYPE-B	PFM TYPE-B
1	0	0	IOVCC	VCI	PFM TYPE-A	PFM TYPE-A
1	1	1	IOVCC	VCI	External VSP	External VSN

• **ECP_DC_DIV[3:0]**：Specify VCSW1 / VCSW2 Frequency for Pumping VSP / VSN.

ECP_DC_DIV[3:0]	VCSW1/2 Period	ECP_DC_DIV[3:0]	VCSW1/2 Period
0	8 Hsync	8	1/12 Hsync
1	4 Hsync	9	1/16 Hsync
2	2 Hsync	A	1/20 Hsync
3	1 Hsync	B	1/25 Hsync
4	1/2 Hsync	C	1/36 Hsync
5	1/4 Hsync	D	1/56 Hsync
6	1/6 Hsync	E	1/72 Hsync
7	1/8 Hsync	F	Setting invalid

• **SINGLE_PUMP:** Specify signal pump state.
- 1：VCSW1 Toggle；VSCW2 GND.
- 0：VCSW1 / VCSW2 Toggle.

• **DT[1:0]**：Specify VCSW1/VCSW2 soft start time.

DT[1:0]	Period (ms)
0	5
1	10
2	15
3	20

• **SYNC_STB**：Enter synchronous standby mode.
- 1：All power signal synchronous turn off.
- 0：All power signal sequence turn off.

Description

• **XDK_ECP[1:0]**：Specify Pumping ratio of VSP / VSN with VCI.

XDK_ECP[1:0]	Ratio
0	X1.5
1	X2
2	X3
3	Setting Inhibited

• **PFM_DC_DIV[2:0]**：Specify PFM operation frequency FoscD.

PFM_DC_DIV[2:0]	FoscD
0	Fosc/1
1	Fosc/2
2	Fosc/3
3	Fosc/4
4	Fosc/5
5	Fosc/6
6	Fosc/7
7	Fosc/8

• **ECP_SYNC_EN**：Enable power IC pumping frequency synchronization.
- 1：Synchronize with external Hsync.
- 0：Synchronize with internal Hsync.

• **VGX_SYNC_EN**：Enable VGH/VGL pumping frequency synchronization.
- 1：Synchronize with external Hsync.
- 0：Synchronize with internal Hsync.

• **A_DC[1:0]**：Specify PFM operation half period.

A_DC[1:0]	Period
0	4/FoscD
1	6/FoscD
2	8/FoscD
3	12/FoscD

• **A_DTP[2:0]**：Specify PFM period of VSP.
• **A_DTN[2:0]**：Specify PFM period of VSN.
• **DTPS[2:0]**：Specify PFM period of VSP at soft start stage.
• **DTNS[2:0]**：Specify PFM period of VSN at soft start stage.

DTN[2:0] DTP[2:0] DTPS[2:0] DTNS[2:0]	Period
0	1/FoscD
1	2/FoscD
2	3/FoscD
3	4/FoscD
4	5/FoscD
5	6/FoscD
6	7/FoscD
7	8/FoscD

• **DCS[1:0]**：Specify PFM operation half period at soft start stage.

DCS[1:0]	Period
0	12/FoscD
1	24/FoscD
2	48/FoscD
3	60/FoscD

6.2.59 SETMIPI (BAh)

BA H	SETMIPI									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	1	0	1	0	BA
Parameter 1st	R/W	x	x	x	x	VC_Main [1]	VC_Main [0]	Lane_Number[1]	Lane_Number[0]	33
Parameter 2nd	R/W	DSI_LDO_SEL[2]	DSI_LDO_SEL[1]	DSI_LDO_SEL[0]	x	x	x	RTERM[1]	RTERM[0]	61
Parameter 3rd	R/W	x	x	x	x	IHSRX[3]	IHSRX[2]	IHSRX[1]	IHSRX[0]	06
Parameter 4th	R/W	x	x	x	x	Tx_clk_sel[1]	Tx_clk_sel[0]	x	x	F9
Parameter 5th	R/W	HFP_OSC[7]	HFP_OSC[6]	HFP_OSC[5]	HFP_OSC[4]	HFP_OSC[3]	HFP_OSC[2]	HFP_OSC[1]	HFP_OSC[0]	FF
Parameter 6th	R/W	HBP_OSC[7]	HBP_OSC[6]	HBP_OSC[5]	HBP_OSC[4]	HBP_OSC[3]	HBP_OSC[2]	HBP_OSC[1]	HBP_OSC[0]	0A

Description

This command is used to set MIPI related register.

• **VC_Main [1:0]**：Specify the virtual channel ID for multiple slave ID.

• **Lane_Number [1:0]**：Specify the lane number selection.

Lane[1:0]	MIPI Lane
0	1 lane
1	2 lanes
2	3 lanes
3	4 lanes

• **DSI_LDO_SEL[2:0]**：Specify the MIPI LDO voltage selection.

DSI_LDO_SEL[2:0]	LDO voltage (V)	DSI_LDO_SEL[2:0]	LDO voltage (V)
0	1.4	4	1.7
1	1.45	5	1.8
2	1.5	6	1.9
3	1.6	7	2.0

• **RTERM[1:0]**：Specify the terminal resistance

RTERM [1:0]	Resistance (Ω)
0	80
1	90
2	100
3	110

• **IHSRX[3:0]**：Specify the MIPI Low High Speed driving ability .

IHSRX [3:0]	Driving Ability	IHSRX [3:0]	Driving Ability
0	X1	8	X9
1	X2	9	X10
2	X3	10	X11
3	X4	11	X12
4	X5	12	X13
5	X6	13	X14
6	X7	14	X15
7	X8	15	X16

• **Tx_clk[1:0]**：Specify TXCLK speed in DSI LP mode for transmission.

Tx_clk[1:0]	TXCLK
0	fDSICLK/4
1	fDSICLK/8
2	fDSICLK/16
3	fDSICLK/32

• **HFP_OSC[7:0]**：Specify the min. HFP number in DSI mode.
• **HBP_OSC[7:0]**：Specify the min. HBP number in DSI mode.

6.2.60 SETVDC (BCh)

BC H	SETVDC									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	1	1	0	0	BC
Parameter 1st	R/W	x	NVDDD_SEL[2]	NVDDD_SEL[1]	NVDDD_SEL[0]	x	VDDD_SEL[2]	VDDD_SEL[1]	VDDD_SEL[0]	47

Description

This command is used to control NVDDD/VDDD Voltage.

• **NVDDD_SEL[2:0]**：Specify the NVDDD voltage selection.

NVDDD_SEL[2:0]	NVDDD (V)
0	-1.5
1	-1.6
2	-1.7
3	-1.75
4	-1.8
5	-1.85
6	-1.9
7	-2.0

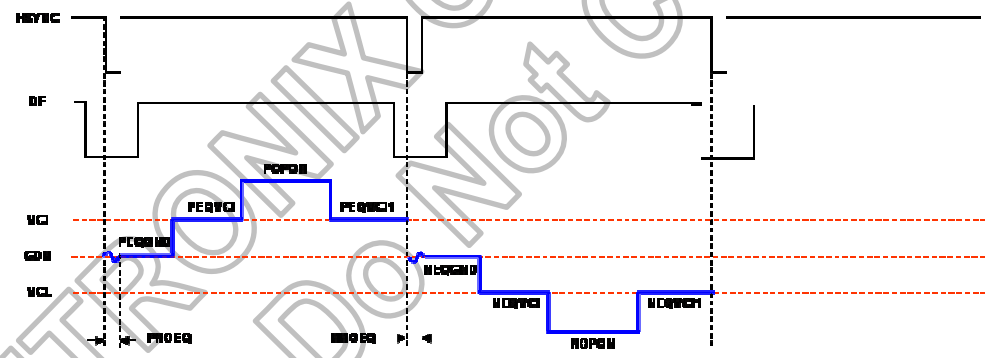
• **VDDD_SEL[2:0]**：Specify the VDDD voltage selection.

VDDD_SEL[2:0]	VDDD (V)
0	VREF*0.43
1	VREF*0.45
2	VREF*0.46
3	VREF*0.47
4	VREF*0.49
5	VREF*0.51
6	1.9
7	2.0

6.2.61 SETSCR (C0h)

C0 H	SETSCR									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	0	0	0	0	C0
Parameter 1st	R/W	N_POPO N[7]	N_POPO N[6]	N_POPO N[5]	N_POPO N[4]	N_POPO N[3]	N_POPO N[2]	N_POPO N[1]	N_POPO N[0]	73
Parameter 2nd	R/W	N_NOPO N[7]	N_NOPO N[6]	N_NOPO N[5]	N_NOPO N[4]	N_NOPO N[3]	N_NOPO N[2]	N_NOPO N[1]	N_NOPO N[0]	73
Parameter 3rd	R/W	I_POPO N[7]	I_POPO N[6]	I_POPO N[5]	I_POPO N[4]	I_POPO N[3]	I_POPO N[2]	I_POPO N[1]	I_POPO N[0]	50
Parameter 4th	R/W	I_NOPO N[7]	I_NOPO N[6]	I_NOPO N[5]	I_NOPO N[4]	I_NOPO N[3]	I_NOPO N[2]	I_NOPO N[1]	I_NOPO N[0]	50
Parameter 5th	R/W	SCR[31]	SCR[30]	SCR[29]	SCR[28]	SCR[27]	SCR[26]	SCR[25]	SCR[24]	C0
Parameter 6th	R/W	SCR[23]	SCR[22]	SCR[21]	SCR[20]	SCR[19]	SCR[18]	SCR[17]	SCR[16]	00
Parameter 7th	R/W	SCR[15]	SCR[14]	SCR[13]	SCR[12]	SCR[11]	SCR[10]	SCR[9]	SCR[8]	08
Parameter 8th	R/W	SCR[7]	SCR[6]	SCR[5]	SCR[4]	SCR[3]	SCR[2]	SCR[1]	SCR[0]	70

This command is used to set related setting of Source driving.



Description

- **N_POPON [7:0]**
  - Specify the source OP Amp driving period for positive polarity in Normal Mode.
- **N_NOPON[7:0]**
  - Specify the source OP Amp driving period for negative polarity in Normal Mode.
- **I_POPON [7:0]**
  - Specify the source OP Amp driving period for positive polarity in Idle mode.
- **I_NOPON [7:0]**
  - Specify the source OP Amp dirivng period for negative polarity in Idle Mode.

OPON[7:0]	Source OP Period
0	1*4/Fosc
1	1*4/Fosc
2	2*4/Fosc
3	3*4/Fosc
:	:
FD	253*4/Fosc
FE	254*4/Fosc
FF	255*4/Fosc

Description

• **SCR [3:0]**：Source and Gamma bias current core tune.

SCR[3:0]	Ibias	SCR[3:0]	Ibias
0	1	C	3.0
1	1.25	D	3.25
2	1.5	E	3.5
3	1.75	F	3.75
4	2.0	others	Setting Inhibited
5	2.25		
6	2.5		
7	2.75		

• **SCR [8:4]**：Source bias current fine tune.

• **SCR [13:9]**：Gamma bias current fine tune.

SCR[8:4] SCR[13:9] (Hex)	Current xIbias	SCR[8:4] SCR[13:9]	Current xIbias
0	Setting Inhibited	0	16
1	1	1	17
2	2	2	18
3	3	3	19
4	4	4	20
5	5	5	21
6	6	6	22
7	7	7	23
8	8	8	24
9	9	9	25
A	10	A	26
B	11	B	27
C	12	C	28
D	13	D	29
E	14	E	30
F	15	F	31

6.2.62 SETPOWER (C1h)

C1 H	SETPOWER									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	0	0	0	1	C1
Parameter 1st	R/W	VBTHS[3]	VBTHS[2]	VBTHS[1]	VBTHS[0]	VBTLS[3]	VBTLS[2]	VBTLS[1]	VBTLS[0]	53
Parameter 2nd	R/W	FBOFF_VGH	FBOFF_VGL	x	x	x	x	x	x	C0
Parameter 3rd	R/W	x	x	VRP[5]	VRP[4]	VRP[3]	VRP[2]	VRP[1]	VRP[0]	16
Parameter 4th	R/W	x	x	VRN[5]	VRN[4]	VRN[3]	VRN[2]	VRN[1]	VRN[0]	16
Parameter 5th	R/W	x	x	x	x	x	x	x	x	00
Parameter 6th	R/W	VGL_DET_EN	VGH_DET_EN	VGL_TURBO	VGH_TURBO	x	APS[2]	APS[1]	APS[0]	D1
Parameter 7th	R/W	VGH1_L_DIV[3]	VGH1_L_DIV[2]	VGH1_L_DIV[1]	VGH1_L_DIV[0]	VGL1_L_DIV[3]	VGL1_L_DIV[2]	VGL1_L_DIV[1]	VGL1_L_DIV[0]	CC
Parameter 8th	R/W	VGH1_R_DIV[3]	VGH1_R_DIV[2]	VGH1_R_DIV[1]	VGH1_R_DIV[0]	VGL1_R_DIV[3]	VGL1_R_DIV[2]	VGL1_R_DIV[1]	VGL1_R_DIV[0]	DD
Parameter 9th	R/W	VGH2_L_DIV[3]	VGH2_L_DIV[2]	VGH2_L_DIV[1]	VGH2_L_DIV[0]	VGL2_L_DIV[3]	VGL2_L_DIV[2]	VGL2_L_DIV[1]	VGL2_L_DIV[0]	67
Parameter 10th	R/W	VGH2_R_DIV[3]	VGH2_R_DIV[2]	VGH2_R_DIV[1]	VGH2_R_DIV[0]	VGL2_R_DIV[3]	VGL2_R_DIV[2]	VGL2_R_DIV[1]	VGL2_R_DIV[0]	77
Parameter 11h	R/W	VGH3_L_DIV[3]	VGH3_L_DIV[2]	VGH3_L_DIV[1]	VGH3_L_DIV[0]	VGL3_L_DIV[3]	VGL3_L_DIV[2]	VGL3_L_DIV[1]	VGL3_L_DIV[0]	33
Parameter 12h	R/W	VGH3_R_DIV[3]	VGH3_R_DIV[2]	VGH3_R_DIV[1]	VGH3_R_DIV[0]	VGL3_R_DIV[3]	VGL3_R_DIV[2]	VGL3_R_DIV[1]	VGL3_R_DIV[0]	33
Parameter 13h	R/W	VGH4_L_DIV[3]	VGH4_L_DIV[2]	VGH4_L_DIV[1]	VGH4_L_DIV[0]	VGL4_L_DIV[3]	VGL4_L_DIV[2]	VGL4_L_DIV[1]	VGL4_L_DIV[0]	11
Parameter 14h	R/W	VGH4_R_DIV[3]	VGH4_R_DIV[2]	VGH4_R_DIV[1]	VGH4_R_DIV[0]	VGL4_R_DIV[3]	VGL4_R_DIV[2]	VGL4_R_DIV[1]	VGL4_R_DIV[0]	11
Parameter 15h	R/W	VGH5_L_DIV[3]	VGH5_L_DIV[2]	VGH5_L_DIV[1]	VGH5_L_DIV[0]	VGL5_L_DIV[3]	VGL5_L_DIV[2]	VGL5_L_DIV[1]	VGL5_L_DIV[0]	00
Parameter 16h	R/W	VGH5_R_DIV[3]	VGH5_R_DIV[2]	VGH5_R_DIV[1]	VGH5_R_DIV[0]	VGL5_R_DIV[3]	VGL5_R_DIV[2]	VGL5_R_DIV[1]	VGL5_R_DIV[0]	00

Description

This command is used to set related setting of power.

• **VBTHS[3:0]**：The voltage adjustment of VGH.
- FBOFF_VGH must be 0

VBTHS[3:0] (Hex)	VGH Voltage (V)	VBTHS[3:0] (Hex)	VGH Voltage (V)	VBTHS[3:0] (Hex)	VGH Voltage (V)
0	10	4	14	8	18
1	11	5	15	9	18
2	12	6	16	A	18
3	13	7	17	B~F	18

• **VBTLS[3:0]**：The voltage adjustment of VGL.
- FBOFF_VGL must be 0

VBTLS[3:0] (Hex)	VGL Voltage (V)	VBTLS[3:0] (Hex)	VGL Voltage (V)	VBTLS[3:0] (Hex)	VGL Voltage (V)
0	-7	4	-11	8	-15
1	-8	5	-12	9	-15
2	-9	6	-13	A	-15
3	-10	7	-14	B~F	-15

• **FBOFF_VGH**：Enable VGH feedback detect function.
- 1：Disable VGH feedback voltage detection. Output voltage = 15V
- 0：Enable VGH feedback voltage detection. Output voltage = VBTHS

• **FBOFF_VGL**：Enable VGL feedback detect function.
- 1：Disable VGL feedback voltage detection. Output voltage = -10V.
- 0：Enable VGL feedback voltage detection. Output voltage = VBTLS.

Description

• **VRP[5:0]/VRN[5:0]**：Specify the VSPROUT/VSNROUT voltage.
- VSPROUT= {Decimal (VRH [5:0]) x0.05+3.3} x (VREF/4.8) if VREF [4] =0.
- VSNROUT= {Decimal (VRH [5:0]) x0.05+3.3} x (VREF/5.6) if VREF [4] =1.

VRP[5:0] VRN[5:0] (Hex)	VSPROUT |VSNROUT| (V)	VRP[5:0] VRN[5:0] (Hex)	VSPROUT |VSNROUT| (V)	VRP[5:0] VRN[5:0] (Hex)	VSPROUT |VSNROUT| (V)
0	3.23	E	3.92	1C	4.60
1	3.28	F	3.97	1D	4.65
2	3.33	10	4.01	1E	4.70
3	3.38	11	4.06	1F*	4.70
4	3.43	12	4.11	20*	5.2
5	3.48	13	4.16	21*	5.3
6	3.53	14	4.21	22*	5.4
7	3.57	15	4.26	23*	5.5
8	3.62	16	4.31	24*	5.55
9	3.67	17	4.36	25*	5.6
A	3.72	18	4.41	26*	5.65
B	3.77	19	4.46	27*	5.7
C	3.82	1A	4.50	28	STOP
D	3.87	1B	4.55	29~3F	STOP

Note: When VREF [4] =0, the max voltage of VSPROUT/VSNROUT will be 4.7V/-4.7V.

• **VGL_DET_EN**：Enable VGL voltage Detect Function.
- 09h_01[3] = 1: VGL voltage Abnormal.
- 09h_01[3] = 0: VGL voltage Normal.

• **VGH_DET_EN**：Enable VGH voltage Detect Function.
- 09h_01[0] = 1：VGH voltage Abnormal.
- 09h_01[0] = 0：VGH voltage Normal.

• **VGL_TURBO**：Enlarge VGL Voltage at FBOFF_VGL=1.
- 1：VGL=-15V
- 0：VGL=-10V

• **VGH_TURBO**：Enlarge VGH Voltage at FBOFF_VGH=1.
- 1：VGH=20V
- 0：VGH=15V

Description

• **APS[2:0]**：Adjust power bias current of all regulator voltage.

APS[2:0]			Bias Current
0	0	0	Stop
0	0	1	Small
0	1	0	Medium Small
0	1	1	Medium Large
1	0	0	Large
others			Setting Invalid

• **VGH1_L_DIV[3:0]**：Specify left side VGH stage 1 pumping frequency.
• **VGH1_R_DIV[3:0]**：Specify right side VGH stage 1 pumping frequency.
• **VGH2_L_DIV[3:0]**：Specify left side VGH stage 2 pumping frequency.
• **VGH2_R_DIV[3:0]**：Specify right side VGH stage 2 pumping frequency.
• **VGH3_L_DIV[3:0]**：Specify left side VGH stage 3 pumping frequency.
• **VGH3_R_DIV[3:0]**：Specify right side VGH stage 3 pumping frequency.
• **VGH4_L_DIV[3:0]**：Specify left side VGH stage 4 pumping frequency.
• **VGH4_R_DIV[3:0]**：Specify right side VGH stage 4 pumping frequency.
• **VGH5_L_DIV[3:0]**：Specify left side VGH stage 5 pumping frequency.
• **VGH5_R_DIV[3:0]**：Specify right side VGH stage 5 pumping frequency.
• **VGL1_L_DIV[3:0]**：Specify left side VGL stage 1 pumping frequency.
• **VGL1_R_DIV[3:0]**：Specify right side VGL stage 1 pumping frequency.
• **VGL2_L_DIV[3:0]**：Specify left side VGL stage 2 pumping frequency.
• **VGL2_R_DIV[3:0]**：Specify right side VGL stage 2 pumping frequency.
• **VGL3_L_DIV[3:0]**：Specify left side VGL stage 3 pumping frequency.
• **VGL3_R_DIV[3:0]**：Specify right side VGL stage 3 pumping frequency.
• **VGL4_L_DIV[3:0]**：Specify left side VGL stage 4 pumping frequency.
• **VGL4_R_DIV[3:0]**：Specify right side VGL stage 4 pumping frequency.
• **VGL5_L_DIV[3:0]**：Specify left side VGL stage 5 pumping frequency.
• **VGL5_R_DIV[3:0]**：Specify right side VGL stage 5 pumping frequency.

VGH1/2/3/4/5_DIV[3:0] VGL1/2/3/4/5_DIV[3:0]				Frequency (MHz)
0	0	0	0	36
0	0	0	1	18
0	0	1	0	12
0	0	1	1	9
0	1	0	0	7.2
0	1	0	1	6
0	1	1	0	5.1
0	1	1	1	4.5
1	0	0	0	4
1	0	0	1	3.6
1	0	1	0	3.3
1	0	1	1	3
1	1	0	0	2.6
1	1	0	1	2.1
1	1	1	0	1.8
1	1	1	1	1.5

6.2.63 SETID (C3h)

C3 H	SETID									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	0	0	1	1	C3
Parameter 1st	R/W	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	38
Parameter 2nd	R/W	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	21
Parameter 3rd	R/W	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	1F
Parameter 4th	R	x	x	x	x	x	ID_TIME[2]	ID_TIME[1]	ID_TIME[0]	00
Description	This command is used for setting ID. • **ID1[7:0]** / **ID2[7:0]** / **ID3[7:0]**：Set ID1 / ID2 / ID3 respectively - 04h / DAh / DBh / DEh change correspondingly • **ID_TIME[2:0]**：Read ID OTP programming times.									

ID_TIME[2:0]	OTP Programming times
0	NO OTPED
1	1
2	2
3	3
4	4

6.2.64 SETDDB (C4h)

C4 H	SETDBB									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	0	1	0	0	C4
Parameter 1st	R/W	DDB1[7]	DDB1[6]	DDB1[5]	DDB1[4]	DDB1[3]	DDB1[2]	DDB1[1]	DDB1[0]	00
Parameter 2nd	R/W	DDB2[7]	DDB2[6]	DDB2[5]	DDB2[4]	DDB2[3]	DDB2[2]	DDB2[1]	DDB2[0]	00
Parameter 3rd	R/W	DDB3[7]	DDB3[6]	DDB3[5]	DDB3[4]	DDB3[3]	DDB3[2]	DDB3[1]	DDB3[0]	00
Parameter 4th	R/W	DDB4[7]	DDB4[6]	DDB4[5]	DDB4[4]	DDB4[3]	DDB4[2]	DDB4[1]	DDB4[0]	00
Description	This command is used to set CMD DDB1~4 value. • **DDB1[7:0]** ~ **DDB4[7:0]**：Set DDB1 ~ DDB4.									

6.2.65 SETECO (C6h)

C6 H	SETECO									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	0	1	1	0	C6
Parameter 1st	R/W	ECO0[7]	ECO0[6]	ECO0[5]	ECO0[4]	ECO0[3]	ECO0[2]	ECO0[1]	ECO0[0]	01
Parameter 2nd	R/W	ECO1[7]	ECO1[6]	ECO1[5]	ECO1[4]	ECO1[3]	ECO1[2]	ECO1[1]	ECO1[0]	00
Parameter 3rd	R/W	ECO2[7]	ECO2[6]	ECO2[5]	ECO2[4]	ECO2[3]	ECO2[2]	ECO2[1]	ECO2[0]	CF
Parameter 4th	R/W	ECO3[7]	ECO3[6]	ECO3[5]	ECO3[4]	ECO3[3]	ECO3[2]	ECO3[1]	ECO3[0]	FF
Parameter 5th	R/W	ECO4[7]	ECO4[6]	ECO4[5]	ECO4[4]	ECO4[3]	ECO4[2]	ECO4[1]	ECO4[0]	00
Parameter 6th	R/W	ECO5[7]	ECO5[6]	ECO5[5]	ECO5[4]	ECO5[3]	ECO5[2]	ECO5[1]	ECO5[0]	FF

Description

This command is used to control ECO register.

• ECO0[2]：VGL_DET_SEL0_INV (1:Off, 0:On)
• ECO0[6:3]：VGL_DET_SEL4~VGL_DET_SEL1 (1:On, 0:Off)
- Control VGL detected voltage

VGL_DET_SEL4	VGL_DET_SEL3	VGL_DET_SEL2	VGL_DET_SEL1	VGL_DET_SEL0_INV	VGL Detected Voltage (V)	
					VREF=4.5V	VREF=4.8V
0	0	0	0	0	-7.0	-7.5
0	0	0	1	1	-7.5	-8.0
0	0	1	0	1	-8.0	-8.5
0	1	0	0	1	-8.5	-9.0
1	0	0	0	1	-9.0	-9.5

• ECO1[1]：VGHL_PUMPING_DIV4_EN
- 1：VGH and VGL pumping frequency divided by 4 @ VGHL_PUMPING_DIV_EN=1.
- 0：VGH and VGL pumping frequency divided by 2 @ VGHL_PUMPING_DIV_EN=1.

• ECO1[6]：VGHL_PUMPING_DIV_EN
- 1：Enable VGH and VGL pumping frequency divided function.

• ECO2[4]：VSP_DET_EN
- 1：Enable VSP detection function
◎C1h 5th parameter VSPS[3:0] to fine tune VSP detection voltage.

• ECO2[5]：VSN_DET_EN
- 1：Enable VSN detection function
◎C6h 6th parameter ECO5[5:0] to fine tune VSN detection voltage.

• ECO2[7]：MIPI_STOP_ALL_GH_EN_BAR
- Source/VCOM pull GND and GIP all gate high @ MIPI Stop

• ECO4[1:0]：TCON_CLK_DIV[1:0] - Control TCON clock.

ECO4[1:0]	OSC (MHz)	SD_LE (ns)
00	36	324
01	9	1332
10	6	1992
11	4.5	2664

• ECO4[7:5]：VGH_DET_SEL2、VGH_DET_SEL1、VGH_DET_SEL0
- Control VGH detected voltage

VGH_DET_SEL2	VGH_DET_SEL1	VGH_DET_SEL0	VGH Detected Voltage (V)
0	0	0	9
0	0	1	11
0	1	0	13
1	0	0	15

• ECO5[5:0]：VSN_DET_LEVEL_SEL[5:0] - Fine tune VSN detected voltage
◎ 0x20h is about -4.0v.
◎ 0x3Fh is about -2.3v.

6.2.66 SETIO (C7h)

C7 H	SETIO									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	0	1	1	1	C7
Parameter 1st	R/W	PWM_OE	x	INVPWM	VOUT_OE	HOUT_OE	x	x	x	00
Parameter 2nd	R/W	x	V_DELAY[2]	V_DELAY[1]	V_DELAY[0]	x	H_DELAY[2]	H_DELAY[1]	H_DELAY[0]	00

Description

This command is used to set I/O related register.

• **PWM_OE**：PWM output CABC PWM signal.
- 1：Enable CABC PWM signal.
- 0：Disable CABC PWM signal.

• **INVPWM**：Inverse polarity of CABC PWM signal.
- 1：CABC PWM signal is inversed.
- 0：Original CABC PWM signal.

• **VOUT_OE**：VOUT pin output frame synchronization signal.

• **HOUT_OE**：HOUT pin output horizontal synchronization signal.

• **V_DELAY[2:0]**：Specify Vertical Sync. delay time.

V_DELAY[2:0]	Delay time (ns)
0	0
1	1666
2	3332
3	4998
4	6664
5	8330
6	9996
7	11662

• **H_DELAY[2:0]**：Specify horizontal sync delay time.

H_DELAY[2:0]	Delay time (ns)
0	0
1	1666
2	3332
3	4998
4	6664
5	8330
6	9996
7	11662

6.2.67 SETCABC (C8h)

C8 H	SETCABC									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	1	0	0	0	C8
Parameter 1st	R/W	x	PWMDIV [2]	PWMDIV [1]	PWMDIV [0]	x	x	x	x	10
Parameter 2nd	R/W	PWM_PE RIOD[7]	PWM_PE RIOD[6]	PWM_PE RIOD[5]	PWM_PE RIOD[4]	PWM_PE RIOD[3]	PWM_PE RIOD[2]	PWM_PE RIOD[1]	PWM_PE RIOD[0]	40

Description

This command is used to set CABC related register.

• **PWMDIV[2:0]**：CABC PWM Frequency Fpwm control.

PWMDIV[2:0]	PWM Fpwm
0	Fosc/1
1	Fosc/2
2	Fosc/4
3	Fosc/8
4	Fosc/16

• **PWMPERIOD[7:0]**：CABC PWM output frequency control.

PWMPERIOD[7:0]	PWM frequency
0	Fpwm/1
1	Fpwm/1
2	Fpwm/2
:	:
3F	Fpwm/127

6.2.68 SETCLOCK (CBh)

CB H	SETCLOCK									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	1	0	1	1	CB
Parameter 1st	R/W	OSC_DI V2	FORCE_ ULP[2]	FORCE_ ULP[1]	FORCE_ ULP[0]	x	FRADJ[2]	FRADJ[1]	FRADJ[0]	03

Description

This command is used to set OSC related register.

• **OSC_DIV2**：Halve PWM Frequency
- 1：Halve PWM Frequency
- 0：Not Halve PWM Frequency

• **FORCE_ULP**：Enter ULP Mode
- 5：Enter ULP Mode
- Leave ULP Mode by HWRESET only

• **FRADJ[2:0]**：Adjust internal oscillator frequency (Fosc).
- 100% OSC = 36MHz

FRADJ			Internal oscillator frequency
0	0	0	50%
0	0	1	67%
0	1	0	83%
0	1	1	100%
1	0	0	116%
1	0	1	133%
1	1	0	150%
1	1	1	167%

6.2.69 SETPANEL (CCh)

CC H	SETPANEL									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	1	1	0	0	CC
Parameter 1st	R/W		x	x	x	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	00
Description	This command is used to set display related register. • **SS_PANEL**：Reverse the source scan direction. - 1：enable reverse the source scan direction. - 0：normal scan direction from S1->S1440. • **GS_PANEL**：Reverse the vertical scan direction. - 1：Enable reverse the vertical scan direction. - 0：Normal vertical scan direction. • **REV_PANEL**：Reverse the source polarity. - 1：Normally black panel - 0：Normally white panel. • **BGR_PANEL:** reverse the source mapping direction with RGB. - 1：S1:S2:S3 = “B” : ”G” : ”R” - 0：S1:S2:S3 = “R” : ”G” : ”B”									

6.2.70 DGC_R (CDh)

CD H	DGC_R									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	1	1	0	1	CD
Parameter 1st	R/W	x	x	x	x	x	x	x	DGC_EN	00
Parameter 2nd	W	DGC_LUT_R00[7]	DGC_LUT_R00[6]	DGC_LUT_R00[5]	DGC_LUT_R00[4]	DGC_LUT_R00[3]	DGC_LUT_R00[2]	DGC_LUT_R00[1]	DGC_LUT_R00[0]	80
Parameter 3rd	W	DGC_LUT_R01[7]	DGC_LUT_R01[6]	DGC_LUT_R01[5]	DGC_LUT_R01[4]	DGC_LUT_R01[3]	DGC_LUT_R01[2]	DGC_LUT_R01[1]	DGC_LUT_R01[0]	80
Parameter 4th	W	DGC_LUT_R02[7]	DGC_LUT_R02[6]	DGC_LUT_R02[5]	DGC_LUT_R02[4]	DGC_LUT_R02[3]	DGC_LUT_R02[2]	DGC_LUT_R02[1]	DGC_LUT_R02[0]	80
:	:	:	:	:	:	:	:	:	:	
Parameter 10th	W	DGC_LUT_R08[7]	DGC_LUT_R08[6]	DGC_LUT_R08[5]	DGC_LUT_R08[4]	DGC_LUT_R08[3]	DGC_LUT_R08[2]	DGC_LUT_R08[1]	DGC_LUT_R08[0]	80
Parameter 11th	W	DGC_LUT_R09[7]	DGC_LUT_R09[6]	DGC_LUT_R09[5]	DGC_LUT_R09[4]	DGC_LUT_R09[3]	DGC_LUT_R09[2]	DGC_LUT_R09[1]	DGC_LUT_R09[0]	80
Parameter 12th	W	DGC_LUT_R10[7]	DGC_LUT_R10[6]	DGC_LUT_R10[5]	DGC_LUT_R10[4]	DGC_LUT_R10[3]	DGC_LUT_R10[2]	DGC_LUT_R10[1]	DGC_LUT_R10[0]	80
Parameter 13th	W	DGC_LUT_R11[7]	DGC_LUT_R11[6]	DGC_LUT_R11[5]	DGC_LUT_R11[4]	DGC_LUT_R11[3]	DGC_LUT_R11[2]	DGC_LUT_R11[1]	DGC_LUT_R11[0]	80
:	:	:	:	:	:	:	:	:	:	
Parameter 20th	W	DGC_LUT_R18[7]	DGC_LUT_R18[6]	DGC_LUT_R18[5]	DGC_LUT_R18[4]	DGC_LUT_R18[3]	DGC_LUT_R18[2]	DGC_LUT_R18[1]	DGC_LUT_R18[0]	80
Parameter 21th	W	DGC_LUT_R19[7]	DGC_LUT_R19[6]	DGC_LUT_R19[5]	DGC_LUT_R19[4]	DGC_LUT_R19[3]	DGC_LUT_R19[2]	DGC_LUT_R19[1]	DGC_LUT_R19[0]	80
Parameter 22th	W	DGC_LUT_R20[7]	DGC_LUT_R20[6]	DGC_LUT_R20[5]	DGC_LUT_R20[4]	DGC_LUT_R20[3]	DGC_LUT_R20[2]	DGC_LUT_R20[1]	DGC_LUT_R20[0]	80
Parameter 23th	W:	DGC_LUT_R21[7]	DGC_LUT_R21[6]	DGC_LUT_R21[5]	DGC_LUT_R21[4]	DGC_LUT_R21[3]	DGC_LUT_R21[2]	DGC_LUT_R21[1]	DGC_LUT_R21[0]	80
:	:	:	:	:	:	:	:	:	:	
Parameter 30th	W	DGC_LUT_R28[7]	DGC_LUT_R28[6]	DGC_LUT_R28[5]	DGC_LUT_R28[4]	DGC_LUT_R28[3]	DGC_LUT_R28[2]	DGC_LUT_R28[1]	DGC_LUT_R28[0]	80
Parameter 31th	W	DGC_LUT_R29[7]	DGC_LUT_R29[6]	DGC_LUT_R29[5]	DGC_LUT_R29[4]	DGC_LUT_R29[3]	DGC_LUT_R29[2]	DGC_LUT_R29[1]	DGC_LUT_R29[0]	80
Parameter 32th	W	DGC_LUT_R30[7]	DGC_LUT_R30[6]	DGC_LUT_R30[5]	DGC_LUT_R30[4]	DGC_LUT_R30[3]	DGC_LUT_R30[2]	DGC_LUT_R30[1]	DGC_LUT_R30[0]	80
Parameter 33th	W	DGC_LUT_R31[7]	DGC_LUT_R31[6	DGC_LUT_R31[5]	DGC_LUT_R31[4]	DGC_LUT_R31[3]	DGC_LUT_R31[2]	DGC_LUT_R31[1]	DGC_LUT_R31[0]	80
Parameter 34th	W	DGC_LUT_R32[7]	DGC_LUT_R32[6	DGC_LUT_R32[5]	DGC_LUT_R32[4]	DGC_LUT_R32[3]	DGC_LUT_R32[2]	DGC_LUT_R32[1]	DGC_LUT_R32[0]	80
Description	This command is used to set Red color digital gamma. • **DGC_EN**：Control digital gamma function. - 1：Enable digital gamma function. - 0：Disable digital gamma function. • **DGC_LUT_R00 [7:0] ~ DGC_LUT_R32 [7:0]**：Red color digital gamma LUT table.									

6.2.71 DGC_G (CEh)

CE H	DGC_G									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	1	1	1	0	CE
Parameter 1st	W	DGC_LUT_G00[7]	DGC_LUT_G00[6]	DGC_LUT_G00[5]	DGC_LUT_G00[4]	DGC_LUT_G00[3]	DGC_LUT_G00[2]	DGC_LUT_G00[1]	DGC_LUT_G00[0]	80
Parameter 2nd	W	DGC_LUT_G01[7]	DGC_LUT_G01[6]	DGC_LUT_G01[5]	DGC_LUT_G01[4]	DGC_LUT_G01[3]	DGC_LUT_G01[2]	DGC_LUT_G01[1]	DGC_LUT_G01[0]	80
Parameter 3rd	W	DGC_LUT_G02[7]	DGC_LUT_G02[6]	DGC_LUT_G02[5]	DGC_LUT_G02[4]	DGC_LUT_G02[3]	DGC_LUT_G02[2]	DGC_LUT_G02[1]	DGC_LUT_G02[0]	80
Parameter 4th	W	DGC_LUT_G03[7]	DGC_LUT_G03[6]	DGC_LUT_G03[5]	DGC_LUT_G03[4]	DGC_LUT_G03[3]	DGC_LUT_G03[2]	DGC_LUT_G03[1]	DGC_LUT_G03[0]	80
:	:	:	:	:	:	:	:	:	:	
Parameter 10th	W	DGC_LUT_G09[7]	DGC_LUT_G09[6]	DGC_LUT_G09[5]	DGC_LUT_G09[4]	DGC_LUT_G09[3]	DGC_LUT_G09[2]	DGC_LUT_G09[1]	DGC_LUT_G09[0]	80
Parameter 11th	W	DGC_LUT_G10[7]	DGC_LUT_G10[6]	DGC_LUT_G10[5]	DGC_LUT_G10[4]	DGC_LUT_G10[3]	DGC_LUT_G10[2]	DGC_LUT_G10[1]	DGC_LUT_G10[0]	80
Parameter 12th	W	DGC_LUT_G11[7]	DGC_LUT_G11[6]	DGC_LUT_G11[5]	DGC_LUT_G11[4]	DGC_LUT_G11[3]	DGC_LUT_G11[2]	DGC_LUT_G11[1]	DGC_LUT_G11[0]	80
Parameter 13th	W	DGC_LUT_G12[7]	DGC_LUT_G12[6]	DGC_LUT_G12[5]	DGC_LUT_G12[4]	DGC_LUT_G12[3]	DGC_LUT_G12[2]	DGC_LUT_G12[1]	DGC_LUT_G12[0]	80
:	:	:	:	:	:	:	:	:	:	
Parameter 19th	W	DGC_LUT_G18[7]	DGC_LUT_G18[6]	DGC_LUT_G18[5]	DGC_LUT_G18[4]	DGC_LUT_G18[3]	DGC_LUT_G18[2]	DGC_LUT_G18[1]	DGC_LUT_G18[0]	80
Parameter 20th	W	DGC_LUT_G19[7]	DGC_LUT_G19[6]	DGC_LUT_G19[5]	DGC_LUT_G19[4]	DGC_LUT_G19[3]	DGC_LUT_G19[2]	DGC_LUT_G19[1]	DGC_LUT_G19[0]	80
Parameter 21th	W	DGC_LUT_G20[7]	DGC_LUT_G20[6]	DGC_LUT_G20[5]	DGC_LUT_G20[4]	DGC_LUT_G20[3]	DGC_LUT_G20[2]	DGC_LUT_G20[1]	DGC_LUT_G20[0]	80
Parameter 22th	W	DGC_LUT_G21[7]	DGC_LUT_G21[6]	DGC_LUT_G21[5]	DGC_LUT_G21[4]	DGC_LUT_G21[3]	DGC_LUT_G21[2]	DGC_LUT_G21[1]	DGC_LUT_G21[0]	80
:	:	:	:	:	:	:	:	:	:	
Parameter 30th	W	DGC_LUT_G29[7]	DGC_LUT_G29[6]	DGC_LUT_G29[5]	DGC_LUT_G29[4]	DGC_LUT_G29[3]	DGC_LUT_G29[2]	DGC_LUT_G29[1]	DGC_LUT_G29[0]	80
Parameter 31th	W	DGC_LUT_G30[7]	DGC_LUT_G30[6]	DGC_LUT_G30[5]	DGC_LUT_G30[4]	DGC_LUT_G30[3]	DGC_LUT_G30[2]	DGC_LUT_G30[1]	DGC_LUT_G30[0]	80
Parameter 32th	W	DGC_LUT_G31[7]	DGC_LUT_G31[6]	DGC_LUT_G31[5]	DGC_LUT_G31[4]	DGC_LUT_G31[3]	DGC_LUT_G31[2]	DGC_LUT_G31[1]	DGC_LUT_G31[0]	80
Parameter 33th	W	DGC_LUT_G32[7]	DGC_LUT_G32[6	DGC_LUT_G32[5]	DGC_LUT_G32[4]	DGC_LUT_G32[3]	DGC_LUT_G32[2]	DGC_LUT_G32[1]	DGC_LUT_G32[0]	80
Description	This command is used to set Green color digital gamma. • **DGC_LUT_G00 [7:0] ~ DGC_LUT_G32 [7:0]**：Green color digital gamma LUT table.									

6.2.72 DGC_B (CFh)

CF H	DGC_B									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	0	0	1	1	1	1	CF
Parameter 1st	W	DGC_LUT_B00[7]	DGC_LUT_B00[6]	DGC_LUT_B00[5]	DGC_LUT_B00[4]	DGC_LUT_B00[3]	DGC_LUT_B00[2]	DGC_LUT_B00[1]	DGC_LUT_B00[0]	80
Parameter 2nd	W	DGC_LUT_B01[7]	DGC_LUT_B01[6]	DGC_LUT_B01[5]	DGC_LUT_B01[4]	DGC_LUT_B01[3]	DGC_LUT_B01[2]	DGC_LUT_B01[1]	DGC_LUT_B01[0]	80
Parameter 3rd	W	DGC_LUT_B02[7]	DGC_LUT_B02[6]	DGC_LUT_B02[5]	DGC_LUT_B02[4]	DGC_LUT_B02[3]	DGC_LUT_B02[2]	DGC_LUT_B02[1]	DGC_LUT_B02[0]	80
Parameter 4th	W	DGC_LUT_B03[7]	DGC_LUT_B03[6]	DGC_LUT_B03[5]	DGC_LUT_B03[4]	DGC_LUT_B03[3]	DGC_LUT_B03[2]	DGC_LUT_B03[1]	DGC_LUT_B03[0]	80
:	:	:	:	:	:	:	:	:	:	
Parameter 10th	W	DGC_LUT_B09[7]	DGC_LUT_B09[6]	DGC_LUT_B09[5]	DGC_LUT_B09[4]	DGC_LUT_B09[3]	DGC_LUT_B09[2]	DGC_LUT_B09[1]	DGC_LUT_B09[0]	80
Parameter 11th	W	DGC_LUT_B10[7]	DGC_LUT_B10[6]	DGC_LUT_B10[5]	DGC_LUT_B10[4]	DGC_LUT_B10[3]	DGC_LUT_B10[2]	DGC_LUT_B10[1]	DGC_LUT_B10[0]	80
Parameter 12th	W	DGC_LUT_B11[7]	DGC_LUT_B11[6]	DGC_LUT_B11[5]	DGC_LUT_B11[4]	DGC_LUT_B11[3]	DGC_LUT_B11[2]	DGC_LUT_B11[1]	DGC_LUT_B11[0]	80
Parameter 13th	:W	DGC_LUT_B12[7]	DGC_LUT_B12[6]	DGC_LUT_B12[5]	DGC_LUT_B12[4]	DGC_LUT_B12[3]	DGC_LUT_B12[2]	DGC_LUT_B12[1]	DGC_LUT_B12[0]	80
:	:	:	:	:	:	:	:	:	:	
Parameter 19th	W	DGC_LUT_B18[7]	DGC_LUT_B18[6]	DGC_LUT_B18[5]	DGC_LUT_B18[4]	DGC_LUT_B18[3]	DGC_LUT_B18[2]	DGC_LUT_B18[1]	DGC_LUT_B18[0]	80
Parameter 20th	W	DGC_LUT_B19[7]	DGC_LUT_B19[6]	DGC_LUT_B19[5]	DGC_LUT_B19[4]	DGC_LUT_B19[3]	DGC_LUT_B19[2]	DGC_LUT_B19[1]	DGC_LUT_B19[0]	80
Parameter 21th	W	DGC_LUT_B20[7]	DGC_LUT_B20[6]	DGC_LUT_B20[5]	DGC_LUT_B20[4]	DGC_LUT_B20[3]	DGC_LUT_B20[2]	DGC_LUT_B20[1]	DGC_LUT_B20[0]	80
Parameter 22th	W	DGC_LUT_B21[7]	DGC_LUT_B21[6]	DGC_LUT_B21[5]	DGC_LUT_B21[4]	DGC_LUT_B21[3]	DGC_LUT_B21[2]	DGC_LUT_B21[1]	DGC_LUT_B21[0]	80
:	:	:	:	:	:	:	:	:	:	
Parameter 30th	W	DGC_LUT_B29[7]	DGC_LUT_B29[6]	DGC_LUT_B29[5]	DGC_LUT_B29[4]	DGC_LUT_B29[3]	DGC_LUT_B29[2]	DGC_LUT_B29[1]	DGC_LUT_B29[0]	80
Parameter 31th	W	DGC_LUT_B30[7]	DGC_LUT_B30[6]	DGC_LUT_B30[5]	DGC_LUT_B30[4]	DGC_LUT_B30[3]	DGC_LUT_B30[2]	DGC_LUT_B30[1]	DGC_LUT_B30[0]	80
Parameter 32th	W	DGC_LUT_B31[7]	DGC_LUT_B31[6]	DGC_LUT_B31[5]	DGC_LUT_B31[4]	DGC_LUT_B31[3]	DGC_LUT_B31[2]	DGC_LUT_B31[1]	DGC_LUT_B31[0]	80
Parameter 33th	W	DGC_LUT_B32[7]	DGC_LUT_B32[6	DGC_LUT_B32[5]	DGC_LUT_B32[4]	DGC_LUT_B32[3]	DGC_LUT_B32[2]	DGC_LUT_B32[1]	DGC_LUT_B32[0]	80
Description	This command is used to set Blue color digital gamma. • **DGC_LUT_B00 [7:0] ~ DGC_LUT_B32 [7:0]**：Blue color digital gamma LUT table.									

6.2.73 SETGAMMA (E0h)

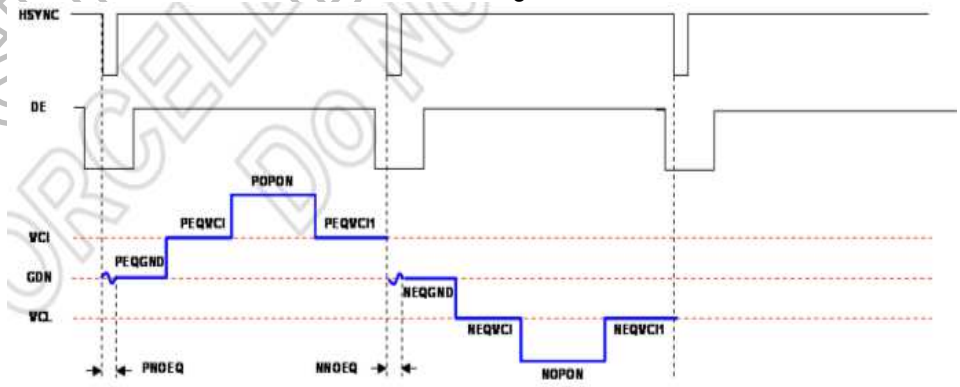
E0 H	SETGAMMA									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	1	0	0	0	0	0	E0
Parameter 1st	R/W	x	x	PVR0[5]	PVR0[4]	PVR0[3]	PVR0[2]	PVR0[1]	PVR0[0]	00
Parameter 2nd	R/W	x	x	PVR1[5]	PVR1[4]	PVR1[3]	PVR1[2]	PVR1[1]	PVR1[0]	11
Parameter 3rd	R/W	x	x	PVR2[5]	PVR2[4]	PVR2[3]	PVR2[2]	PVR2[1]	PVR2[0]	17
Parameter 4th	R/W	x	x	PVR3[5]	PVR3[4]	PVR3[3]	PVR3[2]	PVR3[1]	PVR3[0]	2C
Parameter 5th	R/W	x	x	PVR4[5]	PVR4[4]	PVR4[3]	PVR4[2]	PVR4[1]	PVR4[0]	32
Parameter 6th	R/W	x	x	PVR5[5]	PVR5[4]	PVR5[3]	PVR5[2]	PVR5[1]	PVR5[0]	3F
Parameter 7th	R/W	x	PPR0[6]	PPR0[5]	PPR0[4]	PPR0[3]	PPR0[2]	PPR0[1]	PPR0[0]	49
Parameter 8th	R/W	x	PPR1[6]	PPR1[5]	PPR1[4]	PPR1[3]	PPR1[2]	PPR1[1]	PPR1[0]	3E
Parameter 9th	R/W	x	x	x	PPK0[4]	PPK0[3]	PPK0[2]	PPK0[1]	PPK0[0]	07
Parameter 10th	R/W	x	x	x	PPK1[4]	PPK1[3]	PPK1[2]	PPK1[1]	PPK1[0]	0D
Parameter 11th	R/W	x	x	x	PPK2[4]	PPK2[3]	PPK2[2]	PPK2[1]	PPK2[0]	0E
Parameter 12th	R/W	x	x	x	PPK3[4]	PPK3[3]	PPK3[2]	PPK3[1]	PPK3[0]	12
Parameter 13th	R/W	x	x	x	PPK4[4]	PPK4[3]	PPK4[2]	PPK4[1]	PPK4[0]	13
Parameter 14th	R/W	x	x	x	PPK5[4]	PPK5[3]	PPK5[2]	PPK5[1]	PPK5[0]	11
Parameter 15th	R/W	x	x	x	PPK6[4]	PPK6[3]	PPK6[2]	PPK6[1]	PPK6[0]	13
Parameter 16th	R/W	x	x	x	PPK7[4]	PPK7[3]	PPK7[2]	PPK7[1]	PPK7[0]	10
Parameter 17th	R/W	x	x	x	PPK8[4]	PPK8[3]	PPK8[2]	PPK8[1]	PPK8[0]	17
Parameter 18th	R/W	x	x	NVR0[5]	NVR0[4]	NVR0[3]	NVR0[2]	NVR0[1]	NVR0[0]	00
Parameter 19th	R/W	x	x	NVR1[5]	NVR1[4]	NVR1[3]	NVR1[2]	NVR1[1]	NVR1[0]	11
Parameter 20th	R/W	x	x	NVR2[5]	NVR2[4]	NVR2[3]	NVR2[2]	NVR2[1]	NVR2[0]	17
Parameter 21st	R/W	x	x	NVR3[5]	NVR3[4]	NVR3[3]	NVR3[2]	NVR3[1]	NVR3[0]	2C
Parameter 22nd	R/W	x	x	NVR4[5]	NVR4[4]	NVR4[3]	NVR4[2]	NVR4[1]	NVR4[0]	32
Parameter 23rd	R/W	x	x	NVR5[5]	NVR5[4]	NVR5[3]	NVR5[2]	NVR5[1]	NVR5[0]	3F
Parameter 24th	R/W	x	NPR0[6]	NPR0[5]	NPR0[4]	NPR0[3]	NPR0[2]	NPR0[1]	NPR0[0]	49
Parameter 25th	R/W	x	NPR1[6]	NPR1[5]	NPR1[4]	NPR1[3]	NPR1[2]	NPR1[1]	NPR1[0]	3E
Parameter 26th	R/W	x	x	x	NPK0[4]	NPK0[3]	NPK0[2]	NPK0[1]	NPK0[0]	07
Parameter 27th	R/W	x	x	x	NPK1[4]	NPK1[3]	NPK1[2]	NPK1[1]	NPK1[0]	0D
Parameter 28th	R/W	x	x	x	NPK2[4]	NPK2[3]	NPK2[2]	NPK2[1]	NPK2[0]	0E
Parameter 29th	R/W	x	x	x	NPK3[4]	NPK3[3]	NPK3[2]	NPK3[1]	NPK3[0]	12
Parameter 30th	R/W	x	x	x	NPK4[4]	NPK4[3]	NPK4[2]	NPK4[1]	NPK4[0]	13
Parameter 31st	R/W	x	x	x	NPK5[4]	NPK5[3]	NPK5[2]	NPK5[1]	NPK5[0]	11
Parameter 32nd	R/W	x	x	x	NPK6[4]	NPK6[3]	NPK6[2]	NPK6[1]	NPK6[0]	13
Parameter 33rd	R/W	x	x	x	NPK7[4]	NPK7[3]	NPK7[2]	NPK7[1]	NPK7[0]	10
Parameter 34th	R/W	x	x	x	NPK8[4]	NPK8[3]	NPK8[2]	NPK8[1]	NPK8[0]	17
Description	This command is used to set the gray scale voltage to adjust the gamma characteristics of the TFT panel.									

6.2.74 SETEQ (E3h)

E3 H	SETEQ									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	1	0	0	0	1	1	E3
Parameter 1st	R/W	PNOEQ[7]	PNOEQ[6]	PNOEQ[5]	PNOEQ[4]	PNOEQ[3]	PNOEQ[2]	PNOEQ[1]	PNOEQ[0]	00
Parameter 2nd	R/W	NNOEQ[7]	NNOEQ[6]	PEOEQ[5]	NNOEQ[4]	NNOEQ[3]	NNOEQ[2]	NNOEQ[1]	NNOEQ[0]	00
Parameter 3rd	R/W	PEQGND[7]	PEQGND[6]	PEQGND[5]	PEQGND[4]	PEQGND[3]	PEQGND[2]	PEQGND[1]	PEQGND[0]	03
Parameter 4th	R/W	NEQGND[7]	NEQGND[6]	NEQGND[5]	NEQGND[4]	NEQGND[3]	NEQGND[2]	NEQGND[1]	NEQGND[0]	03
Parameter 5th	R/W	PEQVCI[7]	PEQVCI[6]	PEQVCI[5]	PEQVCI[4]	PEQVCI[3]	PEQVCI[2]	PEQVCI[1]	PEQVCI[0]	03
Parameter 6th	R/W	NEQVCI[7]	NEQVCI[6]	NEQVCI[5]	NEQVCI[4]	NEQVCI[3]	NEQVCI[2]	NEQVCI[1]	NEQVCI[0]	03
Parameter 7th	R/W	PEQVCI1[7]	PEQVCI1[6]	PEQVCI1[5]	PEQVCI1[4]	PEQVCI1[3]	PEQVCI1[2]	PEQVCI1[1]	PEQVCI1[0]	03
Parameter 8th	R/W	NEQVCI1[7]	NEQVCI1[6]	NEQVCI1[5]	NEQVCI1[4]	NEQVCI1[3]	NEQVCI1[2]	NEQVCI1[1]	NEQVCI1[0]	03
Parameter 9th	R/W	x	x	x	x	x	x	x	x	00
Parameter 10th	R/W	x	x	x	x	x	x	x	x	00
Parameter 11th	R/W	x	x	x	x	x	x	x	x	00
Parameter 12th	R/W	x	x	x	x	x	x	x	x	00
Parameter 13th	R/W	ESD_DET_DATA WHITE	ESD_WHITE_EN	x	x	x	x	x	x	C0
Parameter 14th	R/W	x	x	x	SLPIN_OPTION	VEDIO_NO_CHECK_EN	ESD_WHITE_GND_EN	ESD_DET_TIME_SEL[1]	ESD_DET_TIME_SEL[0]	14

Description

This command is used to set EQ related register.



- **PNOEQ[7:0]**：Specify the temporal spacing between HSYNC and PEQGND.
- **NNOEQ[7:0]**：Specify the temporal spacing between HSYNC and NEQGND.
- **PEQGND[7:0]**：Specify the source EQ GND period when Source up to positive voltage.
- **NEQGND[7:0]**：Specify the source EQ GND period when Source down to negative voltage.
- **PEQVCI[7:0]**：Specify the source EQ VCI period when Source up to positive voltage.
- **NEQVCI[7:0]**：Specify the source EQ VCI period when Source down to negative voltage.
- **PEQVCI1[7:0]**：Specify the temporal period of PEQVCI1.
- **NEQVCI1[7:0]**：Specify the temporal period of NEQVCI1.

Description

PNOEQ[7:0] NNOEQ[7:0] PEQGND[7:0] NEQGND[7:0] PEQVCI[7:0] NEQVCI[7:0] PEQVCI1[7:0] NEQVCI1[7:0]	EQ Period
0	0*4/Fosc
1	1*4/Fosc
2	2*4/Fosc
3	3*4/Fosc
:	:
FD	253*4/Fosc
FE	254*4/Fosc
FF	255*4/Fosc

• **ESD_DET_DATA_WHITE**：Select white or black pattern to protect GOA glass.

• **ESD_WHITE_EN**：Enble ESD detection function to protect GOA glass.
- At Sleep-Out State, IC automatically displaying white or black pattern when MIPI-DSI is interrupted or not sent.

• **SLPIN_OPTION**
- 0：Need VSYNC (additional frame) after Sleep-In command to display sleep-in blanking frame then into Sleep-In State.
- 1：No Need VSYNC (additional frame) after Sleep-In command to display sleep-in blanking frame then into Sleep-In State.

• **VEDIO_NO_CHECK_EN**：Enable vedio function detection.
- 0：Enable vedio function detection.
- 1：Disable vedio function detection, continually displaying white or black pattern after sleep-out blanking frame without detecting if MIPI video comes or not

• **ESD_WHITE_GND_EN**：Enable ESD white pattern scanning voltage pull ground.
“0”, Disable scanning voltage pull ground.
“1”, Enable scanning voltage pull ground.

• **ESD_DET_TIME_SEL[1:0]**：ESD detection function period.

ESD_TIME_SEL[1:0]	Period
0	0 frames
1	1 frames
2	2 frames
3	3 frames

6.2.75 SETCOLOREN (E4h)

E4 H	SETCOLOREN									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	1	0	0	1	0	0	E4
Parameter 1st	R/W	x	x	x	x	x	x	x	CE_MASK	01
Description	This command is to set color enhanment mode. • **CE_MASK**：Enable / Disable the color enhanced mask function. - 0：Disable - 1：Enable									

6.2.76 SETCOLOREN (E5h)

E5 H	SETCOLOREN									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	1	0	0	1	0	1	E5
Parameter 1st	R/W	SP_LEVEL[1]	SP_LEVEL[0]	CE_EN	x	x	x	x	x	00
Parameter 2nd	R/W	x	x	x	x	x	x	x	x	No use
Parameter 3rd	R/W	x	x	x	Blue_3[12]	Blue_3[11]	Blue_3[10]	Blue_3[9]	Blue_3[8]	08
Parameter 4th	R/W	Blue_3[7]	Blue_3[6]	Blue_3[5]	Blue_3[4]	Blue_3[3]	Blue_3[2]	Blue_3[1]	Blue_3[0]	32
Parameter 5th	R/W	x	x	x	Blue_2[12]	Blue_2[11]	Blue_2[10]	Blue_2[9]	Blue_2[8]	1C
Parameter 6th	R/W	Blue_2[7]	Blue_2[6]	Blue_2[5]	Blue_2[4]	Blue_2[3]	Blue_2[2]	Blue_2[1]	Blue_2[0]	71
Parameter 7th	R/W	x	x	x	Blue_1[12]	Blue_1[11]	Blue_1[10]	Blue_1[9]	Blue_1[8]	1F
Parameter 8th	R/W	Blue_1[7]	Blue_1[6]	Blue_1[5]	Blue_1[4]	Blue_1[3]	Blue_1[2]	Blue_1[1]	Blue_1[0]	90
Parameter 9th	R/W	x	x	x	Green_3[12]	Green_3[11]	Green_3[10]	Green_3[9]	Green_3[8]	1E
Parameter 10th	R/W	Green_3[7]	Green_3[6]	Green_3[5]	Green_3[4]	Green_3[3]	Green_3[2]	Green_3[1]	Green_3[0]	CD
Parameter 11th	R/W	x	x	x	Green_2[12]	Green_2[11]	Green_2[10]	Green_2[9]	Green_2[8]	07
Parameter 12th	R/W	Green_2[7]	Green_2[6]	Green_2[5]	Green_2[4]	Green_2[3]	Green_2[2]	Green_2[1]	Green_2[0]	4C
Parameter 13th	R/W	x	x	x	Green_1[12]	Green_1[11]	Green_1[10]	Green_1[9]	Green_1[8]	1E
Parameter 14th	R/W	Green_1[7]	Green_1[6]	Green_1[5]	Green_1[4]	Green_1[3]	Green_1[2]	Green_1[1]	Green_1[0]	06
Parameter 15th	R/W	x	x	x	Red_3[12]	Red _3[11]	Red _3[10]	Red _3[9]	Red _3[8]	1F
Parameter 16th	R/W	Red _3[7]	Red _3[6]	Red _3[5]	Red _3[4]	Red _3[3]	Red _3[2]	Red _3[1]	Red _3[0]	66
Parameter 17th	R/W	x	x	x	Red _2[12]	Red _2[11]	Red _2[10]	Red _2[9]	Red _2[8]	1E
Parameter 18th	R/W	Red _2[7]	Red _2[6]	Red _2[5]	Red _2[4]	Red _2[3]	Red _2[2]	Red _2[1]	Red _2[0]	2A
Parameter 19th	R/W	x	x	x	Red _1[12]	Red _1[11]	Red _1[10]	Red _1[9]	Red _1[8]	06
Parameter 20th	R/W	Red _1[7]	Red _1[6]	Red _1[5]	Red _1[4]	Red _1[3]	Red _1[2]	Red _1[1]	Red _1[0]	70

Description

This command is to set color enhanment mode.

• **SP_LEVEL[1:0]**：Specify sharpness level.

SP_LEVEL[1:0]	Sharpness Level
0	No sharpness
1	Small
2	Medium
3	Large

• **CE_EN**：Enable the color enhanced function.

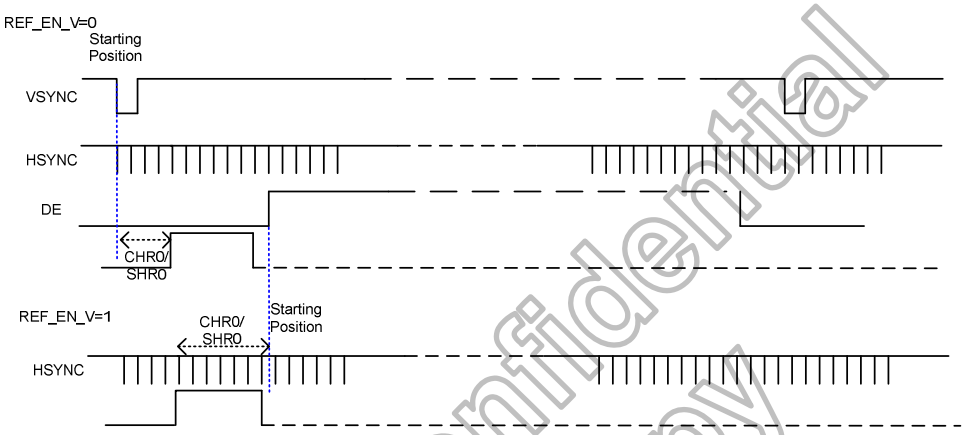
6.2.77 SETGIP1 (E9h)

E9 H	SETGIP1									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	1	0	1	0	0	1	E9
Parameter 1st	R/W	REF_EN	x	x	x	PANEL_SEL[3]	PANEL_SEL[2]	PANEL_SEL[1]	PANEL_SEL[0]	24
Parameter 2nd	R/W	x	x	x	SHR0[12]	SHR0[11]	SHR0[10]	SHR0[9]	SHR0[8]	00
Parameter 3rd	R/W	SHR0[7]	SHR0[6]	SHR0[5]	SHR0[4]	SHR0[3]	SHR0[2]	SHR0[1]	SHR0[0]	00
Parameter 4th	R/W	x	x	x	SHR1[12]	SHR1[11]	SHR1[10]	SHR1[9]	SHR1[8]	00
Parameter 5th	R/W	SHR1[7]	SHR1[6]	SHR1[5]	SHR1[4]	SHR1[3]	SHR1[2]	SHR1[1]	SHR1[0]	00
Parameter 6th	R/W	SPON[7]	SPON[6]	SPON[5]	SPON[4]	SPON[3]	SPON[2]	SPON[1]	SPON[0]	00
Parameter 7th	R/W	SPOFF[7]	SPOFF[6]	SPOFF[5]	SPOFF[4]	SPOFF[3]	SPOFF[2]	SPOFF[1]	SPOFF[0]	00
Parameter 8th	R/W	SHR0_1[3]	SHR0_1[2]	SHR0_1[1]	SHR0_1[0]	SHR0_2[3]	SHR0_2[2]	SHR0_2[1]	SHR0_2[0]	00
Parameter 9th	R/W	SHR0_3[3]	SHR0_3[2]	SHR0_3[1]	SHR0_3[0]	SHR1_1[3]	SHR1_1[2]	SHR1_1[1]	SHR1_1[0]	00
Parameter 10th	R/W	SHR1_2[3]	SHR1_2[2]	SHR1_2[1]	SHR1_2[0]	SHR1_3[3]	SHR1_3[2]	SHR1_3[1]	SHR1_3[0]	00
Parameter 11th	R/W	SHP[3]	SHP[2]	SHP[1]	SHP[0]	SCP[3]	SCP[2]	SCP[1]	SCP[0]	00
Parameter 12th	R/W	CHR [7]	CHR [6]	CHR [5]	CHR [4]	CHR [3]	CHR [2]	CHR [1]	CHR [0]	00
Parameter 13th	R/W	CON [7]	CON [6]	CON [5]	CON [4]	CON [3]	CON [2]	CON [1]	CON [0]	02
Parameter 14th	R/W	COF [7]	COF [6]	COF [5]	COF [4]	COF [3]	COF [2]	COF [1]	COF [0]	02
Parameter 15th	R/W	CHP[3]	CHP[2]	CHP[1]	CHP[0]	CCP[3]	CCP[2]	CCP[1]	CCP[0]	00
Parameter 16th	R/W	USER_GIP_GATE[7]	USER_GIP_GATE[6]	USER_GIP_GATE[5]	USER_GIP_GATE[4]	USER_GIP_GATE[3]	USER_GIP_GATE[2]	USER_GIP_GATE[1]	USER_GIP_GATE[0]	00
Parameter 17th	R/W	x	x	CGTS_L[21]	CGTS_L[20]	CGTS_L[19]	CGTS_L[18]	CGTS_L[17]	CGTS_L[16]	00
Parameter 18th	R/W	CGTS_L[15]	CGTS_L[14]	CGTS_L[13]	CGTS_L[12]	CGTS_L[11]	CGTS_L[10]	CGTS_L[9]	CGTS_L[8]	00
Parameter 19th	R/W	CGTS_L[7]	CGTS_L[6]	CGTS_L[5]	CGTS_L[4]	CGTS_L[3]	CGTS_L[2]	CGTS_L[1]	CGTS_L[0]	00
Parameter 20th	R/W	x	x	CGTS_INV_L[21]	CGTS_INV_L[20]	CGTS_INV_L[19]	CGTS_INV_L[18]	CGTS_INV_L[17]	CGTS_INV_L[16]	00
Parameter 21st	R/W	CGTS_INV_L[15]	CGTS_INV_L[14]	CGTS_INV_L[13]	CGTS_INV_L[12]	CGTS_INV_L[11]	CGTS_INV_L10]	CGTS_INV_L[9]	CGTS_INV_L[8]	00
Parameter 22nd	R/W	CGTS_INV_L[7]	CGTS_INV_L[6]	CGTS_INV_L[5]	CGTS_INV_L[4]	CGTS_INV_L[3]	CGTS_INV_L[2]	CGTS_INV_L[1]	CGTS_INV_L[0]	00
Parameter 23rd	R/W	x	x	CGTS_R[21]	CGTS_R[20]	CGTS_R[19]	CGTS_R[18]	CGTS_R[17]	CGTS_R[16]	00
Parameter 24th	R/W	CGTS_R[15]	CGTS_R[14]	CGTS_R[13]	CGTS_R[12]	CGTS_R[11]	CGTS_R[10]	CGTS_R[9]	CGTS_R[8]	00
Parameter 25th	R/W	CGTS_R[7]	CGTS_R[6]	CGTS_R[5]	CGTS_R[4]	CGTS_R[3]	CGTS_R[2]	CGTS_R[1]	CGTS_R[0]	00
Parameter 26th	R/W	x	x	CGTS_INV_R[21]	CGTS_INV_R[20]	CGTS_INV_R[19]	CGTS_INV_R[18]	CGTS_INV_R[17]	CGTS_INV_R[16]	00
Parameter 27th	R/W	CGTS_INV_R[15]	CGTS_INV_R[14]	CGTS_INV_R[13]	CGTS_INV_R[12]	CGTS_INV_R[11]	CGTS_INV_R10]	CGTS_INV_R[9]	CGTS_INV_R[8]	00
Parameter 28th	R/W	CGTS_INV_R[7]	CGTS_INV_R[6]	CGTS_INV_R[5]	CGTS_INV_R[4]	CGTS_INV_R[3]	CGTS_INV_R[2]	CGTS_INV_R[1]	CGTS_INV_R[0]	00
Parameter 29th	R/W	COS1_L[3]	COS1_L[2]	COS1_L[1]	COS1_L[0]	COS2_L[3]	COS2_L[2]	COS2_L[1]	COS2_L[0]	00
Parameter 30th	R/W	COS3_L[3]	COS3_L[2]	COS3_L[1]	COS3_L[0]	COS4_L[3]	COS4_L[2]	COS4_L[1]	COS4_L[0]	00

Parameter 31st	R/W	COS5_L[3]	COS5_L[2]	COS5_L[1]	COS5_L[0]	COS6_L[3]	COS6_L[2]	COS6_L[1]	COS6_L[0]	00
:	:	:	:	:	:	:	:	:	:	
Parameter 37th	R/W	COS17_L[3]	COS17_L[2]	COS17_L[1]	COS17_L[0]	COS18_L[3]	COS18_L[2]	COS18_L[1]	COS18_L[0]	00
Parameter 38th	R/W	COS19_L[3]	COS19_L[2]	COS19_L[1]	COS19_L[0]	COS20_L[3]	COS20_L[2]	COS20_L[1]	COS20_L[0]	00
Parameter 39th	R/W	COS21_L[3]	COS21_L[2]	COS21_L[1]	COS21_L[0]	COS22_L[3]	COS22_L[2]	COS22_L[1]	COS22_L[0]	00
Parameter 40th	R/W	COS1_R[3]	COS1_R[2]	COS1_R[1]	COS1_R[0]	COS2_R[3]	COS2_R[2]	COS2_R[1]	COS2_R[0]	00
Parameter 41st	R/W	COS3_R[3]	COS3_R[2]	COS3_R[1]	COS3_R[0]	COS4_R[3]	COS4_R[2]	COS4_R[1]	COS4_R[0]	00
Parameter 42nd	R/W	COS5_R[3]	COS5_R[2]	COS5_R[1]	COS5_R[0]	COS6_R[3]	COS6_R[2]	COS6_R[1]	COS6_R[0]	00
:	:	:	:	:	:	:	:	:	:	
Parameter 48th	R/W	COS17_R[3]	COS17_R[2]	COS17_R[1]	COS17_R[0]	COS18_R[3]	COS18_R[2]	COS18_R[1]	COS18_R[0]	00
Parameter 49th	R/W	COS19_R[3]	COS19_R[2]	COS19_R[1]	COS19_R[0]	COS20_R[3]	COS20_R[2]	COS20_R[1]	COS20_R[0]	00
Parameter 50th	R/W	COS21_R[3]	COS21_R[2]	COS21_R[1]	COS21_R[0]	COS22_R[3]	COS22_R[2]	COS22_R[1]	COS22_R[0]	00
Parameter 51st	R/W	TCON_OPT[7]	TCON_OPT[6]	TCON_OPT[5]	TCON_OPT[4]	TCON_OPT[3]	TCON_OPT[2]	TCON_OPT[1]	TCON_OPT[0]	00
Parameter 52nd	R/W	x	GIP_OPT[22]	GIP_OPT[21]	GIP_OPT[20]	GIP_OPT[19]	GIP_OPT[18]	GIP_OPT[17]	GIP_OPT[16]	00
Parameter 53rd	R/W	GIP_OPT[15]	GIP_OPT[14]	GIP_OPT[13]	GIP_OPT[12]	GIP_OPT[11]	GIP_OPT[10]	GIP_OPT[9]	GIP_OPT[8]	00
Parameter 54th	R/W	GIP_OPT[7]	GIP_OPT[6]	GIP_OPT[5]	GIP_OPT[4]	GIP_OPT[3]	GIP_OPT[2]	GIP_OPT[1]	GIP_OPT[0]	00
Parameter 55th	R/W	CHR2[7]	CHR2[6]	CHR2[5]	CHR2[4]	CHR2[3]	CHR2[2]	CHR2[1]	CHR2[0]	00
Parameter 56th	R/W	CON2[7]	CON2[6]	CON2[5]	CON2[4]	CON2[3]	CON2[2]	CON2[1]	CON2[0]	02
Parameter 57th	R/W	COFF2[7]	COFF2[6]	COFF2[5]	COFF2[4]	COFF2[3]	COFF2[2]	COFF2[1]	COFF2[0]	02
Parameter 58th	R/W	CHP2[3]	CHP2[2]	CHP2[1]	CHP2[0]	CCP2[3]	CCP2[2]	CCP2[1]	CCP2[0]	00
Parameter 59th	R/W	x	x	CKS[21]	CKS[20]	CKS[19]	CKS[18]	CKS[17]	CKS[16]	00
Parameter 60th	R/W	CKS[15]	CKS[14]	CKS[13]	CKS[12]	CKS[11]	CKS[10]	CKS[9]	CKS[8]	00
Parameter 61st	R/W	CKS[7]	CKS[6]	CKS[5]	CKS[4]	CKS[3]	CKS[2]	CKS[1]	CKS[0]	00
Parameter 62nd	R/W	COFF[9]	COFF[8]	CON[9]	CON[8]	SPOFF[9]	SPOFF[8]	SPON[9]	SPON[8]	00
Parameter 63rd	R/W	COFF2[9]	COFF[8]	CON2[9]	CON2[8]	x	x	x	x	00

Description

This command is to set forward GIP timing.



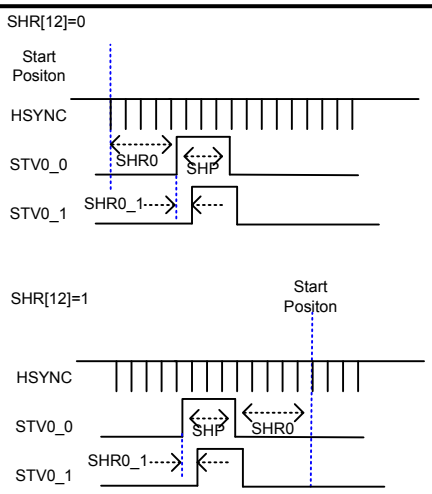
• **REF_EN：**
- 0：SHR0, SHR1, CHR, CHR2 refer to Internal VSYNC
- 1：SHR0, SHR1, CHR, CHR2 refer to Internal DE

◎ REF_EN=1：SHR0, SHR1, CHR, CHR2 = MSB Sign Bit.

• **PANELI_SEL[3:0]**：Specify GIP signal at abnormal power off state.

Panel_sel[3:0]	GIP signal State
1	GND
2	VGH2
4	VGL
8	VGH

Description



• **SHR0[12:0]**：Specify the starting position of GIP STV group 0 (STV0_0).
• **SHR1[12:0]**：Specify the starting position of GIP STV group 1 (STV1_0).

SHR0[12:0] SHR1[12:0] (Hex)	Starting Position
0	0 HSYNC
1	1 HSYNC
2	2 HSYNC
:	:
FFF	4095 HSYNC

• **SPON[9:0]**：Specify the distance of STV rising edge and HYSNC.
• **SPOFF[9:0]**：Specify the distance of STV falling edge and HYSNC.

SPON[9:0] SPOFF[9:0] (Hex)	Distance
0	0*(2/Fosc)
1	1*(2/Fosc)
2	2*(2/Fosc)
:	:
3FF	1023*(2/Fosc)

• **SHR0_1[3:0]** / **SHR0_2[3:0]** / **SHR0_3[3:0]:** Specify the STV0_x distance with STV0_0.
• **SHR1_1[3:0]** / **SHR1_2[3:0]** / **SHR1_3[3:0]:** Specify the STV1_x distance with STV1_0. (X=1~3)

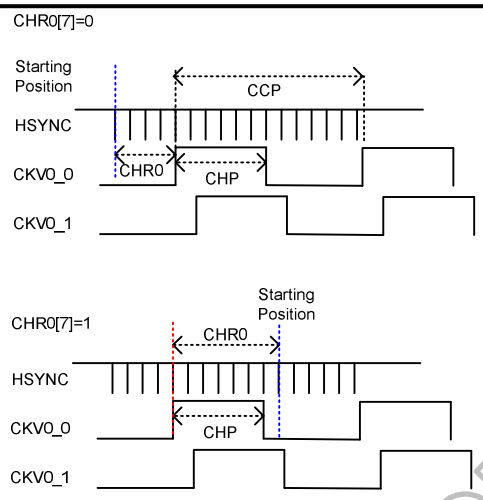
• **SHP[3:0]**：Specify the STV signal high pulse width.

SHP[3:0] (Hex)	Width
0	0 HSYNC
1	1 HSYNC
2	2 HSYNC
:	:
F	16 HSYNC

• **SCP[3:0]**：Specify the total number of STV signal.

SCP[3:0] (Hex)	STV NO.
0	1
1	2
2	3
:	:
F	16

Description



- **CHR[7:0]**：Specify the starting position of GIP CKV group 0 (CKV0_0).
- **CHR2[7:0]**：Specify the starting position of GIP CKV group 1 (CKV1_0).

CHR[7:0] CHR2[7:0] (Hex)	Starting Position
0	0 HSYNC
1	1 HSYNC
2	2 HSYNC
:	:
FF	255 HSYNC

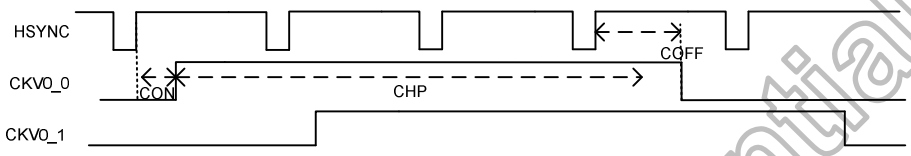
- **CHP[3:0]**：Specify the CKV signal high pulse width.
- **CHP2[3:0]**：Specify the CKV1 signal high pulse width

CHP[3:0] CHP2[3:0] (Hex)	Width
0	1 HSYNC
1	2 HSYNC
2	3 HSYNC
:	:
F	16 HSYNC

- **CCP[3:0]**：Specify the total period cycle of CKV signal.
- **CCP2[3:0]**：Specify the total period cycle of CKV1 signal.

CCP[3:0] CCP2[3:0] (Hex)	CKV Period.
0	1 HSYNC
1	2 HSYNC
2	3 HSYNC
:	:
F	16 HSYNC

Description



• **CON[9:0]**：Specify the distance of CKV rising edge and HYSNC.
• **COFF[9:0]**：Specify the distance of CKV falling edge and HYSNC.
• **CON2[9:0]**：Specify the distance of CKV1 rising edge and HYSNC.
• **COFF2[9:0]**：Specify the distance of CKV1 falling edge and HYSNC.

CON[9:0] COFF[9:0] CON2[9:0] COFF2[9:0] (Hex)	Distance
0	0*(2/Fosc)
1	1*(2/Fosc)
2	2*(2/Fosc)
:	:
FF	255*(2/Fosc)

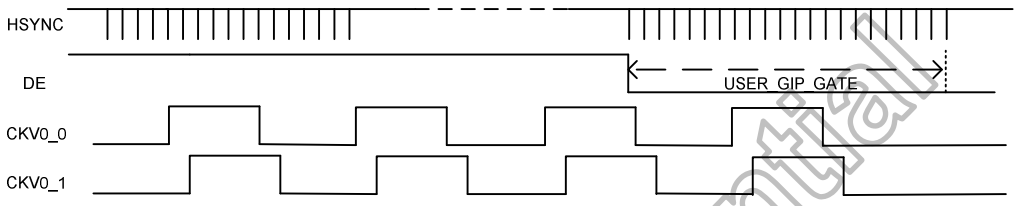
• **CGTS_L[21:0]**：Select Left side GIP output pad signal.
- 1：Output pad assign as STV.
- 0：Output pad assign as CKV.

• **CGTS_R[21:0]**：Select Right side GIP output pad signal.
- 1：Output pad assign as STV.
- 0：Output pad assign as CKV.

• **CGTS_INV_L[21:0]**：Reverse the polarity of Left side GIP output pad signal.
- 1：Reverse the polarity.
- 0：Normal polarity.

.
• **CGTS_INV_R[21:0]**：Reverse the polarity of Right side GIP output pad signal.
- 1：Reverse the polarity.
0：Normal polarity.

Description



• **USER_GIP_GATE[7:0]**：Specify the extra gate counter at blanking area.

USER_GIP_GATE[7:0] (Hex)	Gate number
0	0
1	1
2	2
:	:
FF	255

• **COSx_L[3:0]**：Specify Left side GIP output pad signal.
• **COSx_R[3:0]**：Specify Right side GIP output pad signal.
(x=1~22)

COS (Hex)	GIP OUTPUT		
	CGTS="1"	CGTS="0"	
		CKS="0"	CKS="1"
0	STV0_0	CKV0_0	CKV1_0
1	STV0_1	CKV0_1	CKV1_1
2	STV0_2	CKV0_2	CKV1_2
3	STV0_3	CKV0_3	CKV1_3
4	STV1_0	CKV0_4	CKV1_4
5	STV1_1	CKV0_5	CKV1_5
6	STV1_2	CKV0_6	CKV1_6
7	STV1_3	CKV0_7	CKV1_7
8	Always Low	Always Low	
9	STV2_0	CKV All On	
A	STV2_1	YS1_Signal	
B	STV2_2	YS2_Signal	
C	STV2_3	CKV All On_2	
D	-	YS1_Signal_2	
E	-	YS2_Signal_2	
F	Always High	Always High	

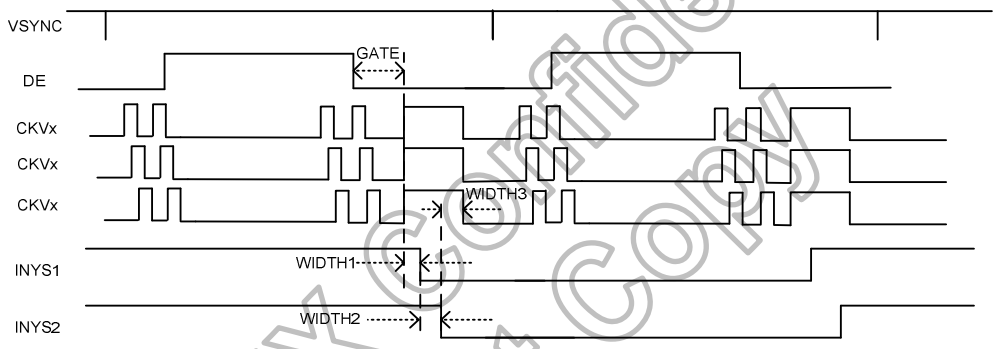
• **GIP_OPT[22:0]**：Specify GIP optional setting for GIP signal.

6.2.78 SETGIP2 (EAh)

EA H	SETGIP2									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	1	0	1	0	1	0	EA
Parameter 1st	R/W	YS2_SEL[1]	YS2_SEL[0]	YS1_SEL[1]	YS1_SEL[0]	YS2_XOR	YS1_XOR	YS_FLAG_EN	ALL_ON_EN	94
Parameter 2nd	R/W	GATE[7]	GATE[6]	GATE[5]	GATE[4]	GATE[3]	GATE[2]	GATE[1]	GATE[0]	00
Parameter 3rd	R/W	CK_ALL_ON_EN	STV_ALL_ON_EN	CK_ALL_ON_WIDTH1[5]	CK_ALL_ON_WIDTH1[4]	CK_ALL_ON_WIDTH1[3]	CK_ALL_ON_WIDTH1[2]	CK_ALL_ON_WIDTH1[1]	CK_ALL_ON_WIDTH1[0]	00
Parameter 4th	R/W	x	x	CK_ALL_ON_WIDTH2[5]	CK_ALL_ON_WIDTH2[4]	CK_ALL_ON_WIDTH2[3]	CK_ALL_ON_WIDTH2[2]	CK_ALL_ON_WIDTH2[1]	CK_ALL_ON_WIDTH2[0]	00
Parameter 5th	R/W	x	x	CK_ALL_ON_WIDTH3[5]	CK_ALL_ON_WIDTH3[4]	CK_ALL_ON_WIDTH3[3]	CK_ALL_ON_WIDTH3[2]	CK_ALL_ON_WIDTH3[1]	CK_ALL_ON_WIDTH3[0]	00
Parameter 6th	R/W	YS_FLAG_PERIOD[7]	YS_FLAG_PERIOD[6]	YS_FLAG_PERIOD[5]	YS_FLAG_PERIOD[4]	YS_FLAG_PERIOD[3]	YS_FLAG_PERIOD[2]	YS_FLAG_PERIOD[1]	YS_FLAG_PERIOD[0]	00
Parameter 7th	R/W	YS2_SEL_2[1]	YS2_SEL_2[0]	YS1_SEL_2[1]	YS1_SEL_2[0]	YS2_XOR_2	YS1_XOR_2	YS_FLAG_EN_2	ALL_ON_EN_2	94
Parameter 8th	R/W	USER_GIP_GATE1_2[7]	USER_GIP_GATE1_2[6]	USER_GIP_GATE1_2[5]	USER_GIP_GATE1_2[4]	USER_GIP_GATE1_2[3]	USER_GIP_GATE1_2[2]	USER_GIP_GATE1_2[1]	USER_GIP_GATE1_2[0]	00
Parameter 9th	R/W	CK_ALL_ON_EN_2	STV_ALL_ON_EN_2	CK_ALL_ON_WIDTH1_2[5]	CK_ALL_ON_WIDTH1_2[4]	CK_ALL_ON_WIDTH1_2[3]	CK_ALL_ON_WIDTH1_2[2]	CK_ALL_ON_WIDTH1_2[1]	CK_ALL_ON_WIDTH1_2[0]	00
Parameter 10th	R/W	x	x	CK_ALL_ON_WIDTH2_2[5]	CK_ALL_ON_WIDTH2_2[4]	CK_ALL_ON_WIDTH2_2[3]	CK_ALL_ON_WIDTH2_2[2]	CK_ALL_ON_WIDTH2_2[1]	CK_ALL_ON_WIDTH2_2[0]	00
Parameter 11th	R/W	x	x	CK_ALL_ON_WIDTH3_2[5]	CK_ALL_ON_WIDTH3_2[4]	CK_ALL_ON_WIDTH3_2[3]	CK_ALL_ON_WIDTH3_2[2]	CK_ALL_ON_WIDTH3_2[1]	CK_ALL_ON_WIDTH3_2[0]	00
Parameter 12th	R/W	YS_FLAG_PERIOD_2[7]	YS_FLAG_PERIOD_2[6]	YS_FLAG_PERIOD_2[5]	YS_FLAG_PERIOD_2[4]	YS_FLAG_PERIOD_2[3]	YS_FLAG_PERIOD_2[2]	YS_FLAG_PERIOD_2[1]	YS_FLAG_PERIOD_2[0]	00
Parameter 13th	R/W	COS1_L_GS[3]	COS1_L_GS[2]	COS1_L_GS[1]	COS1_L_GS[0]	COS2_L_GS[3]	COS2_L_GS[2]	COS2_L_GS[1]	COS2_L_GS[0]	00
Parameter 14th	R/W	COS3_L_GS[3]	COS3_L_GS[2]	COS3_L_GS[1]	COS3_L_GS[0]	COS4_L_GS[3]	COS4_L_GS[2]	COS4_L_GS[1]	COS4_L_GS[0]	00
Parameter 15th	R/W	COS5_L_GS[3]	COS5_L_GS[2]	COS5_L_GS[1]	COS5_L_GS[0]	COS6_L_GS[3]	COS6_L_GS[2]	COS6_L_GS[1]	COS6_L_GS[0]	00
:	:	:	:	:	:	:	:	:	:	:
Parameter 21th	R/W	COS17_L_GS[3]	COS17_L_GS[2]	COS17_L_GS[1]	COS17_L_GS[0]	COS18_L_GS[3]	COS18_L_GS[2]	COS18_L_GS[1]	COS18_L_GS[0]	00
Parameter 22th	R/W	COS19_L_GS[3]	COS19_L_GS[2]	COS19_L_GS[1]	COS19_L_GS[0]	COS20_L_GS[3]	COS20_L_GS[2]	COS20_L_GS[1]	COS20_L_GS[0]	00
Parameter 23th	R/W	COS21_L_GS[3]	COS21_L_GS[2]	COS21_L_GS[1]	COS21_L_GS[0]	COS22_L_GS[3]	COS22_L_GS[2]	COS22_L_GS[1]	COS22_L_GS[0]	00
Parameter 24th	R/W	COS1_R_GS[3]	COS1_R_GS[2]	COS1_R_GS[1]	COS1_R_GS[0]	COS2_R_GS[3]	COS2_R_GS[2]	COS2_R_GS[1]	COS2_R_GS[0]	00
Parameter 25th	R/W	COS3_R_GS[3]	COS3_R_GS[2]	COS3_R_GS[1]	COS3_R_GS[0]	COS4_R_GS[3]	COS4_R_GS[2]	COS4_R_GS[1]	COS4_R_GS[0]	00
Parameter 26th	R/W	COS5_R_GS[3]	COS5_R_GS[2]	COS5_R_GS[1]	COS5_R_GS[0]	COS6_R_GS[3]	COS6_R_GS[2]	COS6_R_GS[1]	COS6_R_GS[0]	00
		:	:	:	:	:	:	:	:	:
Parameter 32th	R/W	COS17_R_GS[3]	COS17_R_GS[2]	COS17_R_GS[1]	COS17_R_GS[0]	COS18_R_GS[3]	COS18_R_GS[2]	COS18_R_GS[1]	COS18_R_GS[0]	00
Parameter 33th	R/W	COS19_R_GS[3]	COS19_R_GS[2]	COS19_R_GS[1]	COS19_R_GS[0]	COS20_R_GS[3]	COS20_R_GS[2]	COS20_R_GS[1]	COS20_R_GS[0]	00
Parameter 34th	R/W	COS21_R_GS[3]	COS21_R_GS[2]	COS21_R_GS[1]	COS21_R_GS[0]	COS22_R_GS[3]	COS22_R_GS[2]	COS22_R_GS[1]	COS22_R_GS[0]	00
Parameter 35th	R/W	x	x	EQOPT[1]	EQOPT[0]	x	x	EQ_SEL[1]	EQ_SEL[0]	30
Parameter 36th	R/W	EQ_DELAY[7]	EQ_DELAY[6]	EQ_DELAY[5]	EQ_DELAY[4]	EQ_DELAY[3]	EQ_DELAY[2]	EQ_DELAY[1]	EQ_DELAY[0]	00

Parameter 37th	R/W	x	x	x	x	EQ_DELAY_HSYNC[3]	EQ_DELAY_HSYNC[2]	EQ_DELAY_HSYNC[1]	EQ_DELAY_HSYNC[0]	00
Parameter 38th	R/W	x	x	x	x	x	x	HSYNC_TO_CL1_CNT10[9]	HSYNC_TO_CL1_CNT10[8]	00
Parameter 39th	R/W	HSYNC_TO_CL1_CNT10[7]	HSYNC_TO_CL1_CNT10[6]	HSYNC_TO_CL1_CNT10[5]	HSYNC_TO_CL1_CNT10[4]	HSYNC_TO_CL1_CNT10[3]	HSYNC_TO_CL1_CNT10[2]	HSYNC_TO_CL1_CNT10[1]	HSYNC_TO_CL1_CNT10[0]	02

This command is to set backward GIP timing.



- **YS1_SEL[1:0]**：Specify YS1 Signal Mode.
- **YS2_SEL[1:0]**：Specify YS2 Signal Mode.

YS1[1:0] YS2[1:0] (Hex)	YS1/YS2 Signal Mode
0	INYS1/INYS2
1	INYS1 or INVS2
2	INYS1 and INYS2

- **YS_FLAG_EN**：Enable YS signal function.
- **YS1_XOR**：Reverse YS1 signal.
- **YS2_XOR**：Reverse YS2 signal.

- **ALL_ON_EN**：Enable ALL ON function.

- **USER_GIP_GATE[7:0]**：Specify the distance of GIP ALL On rising edge and DE.

- **CK_ALL_ON_WIDTH1[5:0]** / **CK_ALL_ON_WIDTH2[5:0]** / **CK_ALL_ON_WIDTH3[5:0]**：Specify the timing of YS1 and YS2 signal.

Description

• **EQOPT[1:0]**：Specify GIP output EQ signal.

EQOTP (Hex)	P_EQ	N_EQ
0	Yes	Yes
1	No	Yes
2	Yes	No
3	No	No

• **EQ_SEL[1:0]**：Specify GIP output EQ signal level.

EQ_SEL (Hex)	P_EQ	N_EQ
~~0~~	-	-
~~1~~	-	-
~~2~~	-	-
3	VSP	VSP

• **EQ_DELAY[7:0]**：Specify the distance of EQ rising edge and HYSNC.

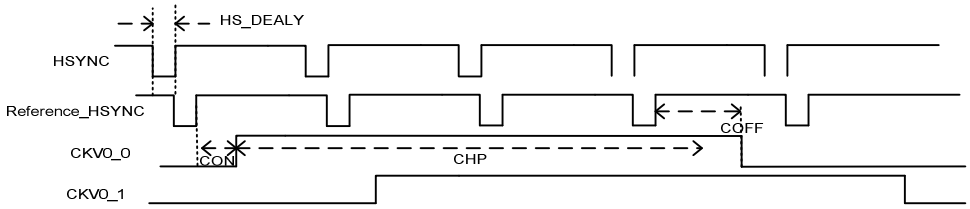
EQ_DEALY (Hex)	Distance
0	0*(2/Fosc)
1	1*(2/Fosc)
2	2*(2/Fosc)
:	:
FF	255*(2/Fosc)

• **EQ_DELAY_HSYNC[3:0]**：Specify the distance of EQ rising edge and HYSNC.

EQ_DEALY_HS (Hex)	Distance
0	0 Hsync
1	1 Hsync
2	2 Hsync
:	:
16	16 Hsync

• **HSYNC_TO_CL1_CNT10[9:0]**：Specify the GIP reference HSYNC between external HSYNC

HSYNC_TO_CL1_CNT10[9:0] (Hex)	Distance
0	0/Fosc
1	1/Fosc
2	2/Fosc
:	:
1FF	511/Fosc



6.2.79 SETCOLOR (EBh)

EB H	SETCOLOR									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	1	1	0	1	0	1	1	EB
Parameter 1st	W	Bkx[1]	Bkx[0]	Bky[1]	Bky[0]	Wx[1]	Wx[0]	Wy[1]	Wy[0]	00
Parameter 2nd	W	BKx[9]	BKx[8]	BKx[7]	BKx[6]	BKx[5]	BKx[4]	BKx3]	BKx[2]	00
Parameter 3rd	W	BKy[9]	BKy[8]	BKy[7]	BKy[6]	BKy[5]	BKy[4]	BKy3]	BKy[2]	00
Parameter 4th	W	Wx[9]	Wx[8]	Wx[7]	Wx[6]	Wx[5]	Wx[4]	Wx3]	Wx[2]	00
Parameter 5th	W	Wy[9]	Wy[8]	Wy[7]	Wy[6]	Wy[5]	Wy[4]	Wy3]	Wy[2]	00
Parameter 6th	W	Rx[1]	Rx[0]	Ry[1]	Ry[0]	Gx[1]	Gx[0]	Gy[1]	Gy[0]	00
Parameter 7th	W	Rx[9]	Rx[8]	Rx[7]	Rx[6]	Rx[5]	Rx[4]	Rx3]	Rx[2]	00
Parameter 8th	W	Ry[9]	Ry[8]	Ry[7]	Ry[6]	Ry[5]	Ry[4]	Ry3]	Ry[2]	00
Parameter 9th	W	Gx[9]	Gx[8]	Gx[7]	Gx[6]	Gx[5]	Gx[4]	Gx3]	Gx[2]	00
Parameter 10th	W	Gy[9]	Gy[8]	Gy[7]	Gy[6]	Gy[5]	Gy[4]	Gy3]	Gy[2]	00
Parameter 11th	W	Bx[1]	Bx[0]	By[1]	By[0]	Ax[1]	Ax[0]	Ay[1]	Ay[0]	00
Parameter 12th	W	Bx[9]	Bx[8]	Bx[7]	Bx[6]	Bx[5]	Bx[4]	Bx3]	Bx[2]	00
Parameter 13th	W	By[9]	By[8]	By[7]	By[6]	By[5]	By[4]	By3]	By[2]	00
Parameter 14th	W	Ax[9]	Ax[8]	Ax[7]	Ax[6]	Ax[5]	Ax[4]	Ax3]	Ax[2]	00
Parameter 15th	W	Ay[9]	Ay[8]	Ay[7]	Ay[6]	Ay[5]	Ay[4]	Ay3]	Ay[2]	00
Description	This command is used to record the Panel Optical Performance.									

7. Electrical Characteristics

7.1 Absolute maximum ratings

Item	Symbol	Unit	Spec.		
			Min.	Typ.	Max.
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3	-	+5.5
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3	-	+6.6
Power Supply Voltage 3	VSP ~ VSSA	V	-0.3	-	+6.6
Power Supply Voltage 4	VSSA ~ VSN	V	-0.3	-	+6.6
Power Supply Voltage 5	VGH ~ VGL	V	-0.3	-	+35
Logic Input Voltage	V_{IN}	V	-0.3	-	IOVCC+0.3
Logic Output Voltage	Vo	V	-0.3	-	IOVCC+0.3
Differential Input Voltage	DSI_CP/DSI_CN DSI_D0P/DSI_D0P, DSI_D1P/DSI_D1N	V	-0.3	-	2.0
Operating Temperature	Topr	℃	-40	-	+85
Storage Temperature	Tstg	℃	-55	-	+110

Table 7.1: Absolute Maximum Ratings

7.2 DC characteristics

7.2.1 Basic Characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	2.0	V
Analog Operating voltage	VCI	Operation voltage	2.5	-	6.2	
Input / Output						
Logic High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Logic Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	µA
DC/DC Converter Operation						
VSP booster voltage	VSP	IVSP=1mA	4.5		6.2	V
VSN booster voltage	VSN	IVSN=-1mA	-6.2		-4.5	
VGH booster voltage	VGH	Ivgh=1mA	10		20	
VGL booster voltage	VGL	Ivgl=-1mA	-15		-7.5	
VGH and VGL difference	|VGH-VGL|	-	-	-	32	
Oscillator tolerance	OSC	25℃	-3		3	%
Source Driver						
Gamma reference voltage	VSPR	-	3.3		5.6	V
	VSNR	-	-5.6		-3.3	
Output voltage deviation	DVOS	VSSD+1.0 ~ VSPROUT-1.0	-	-	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VSPR-1.0 ~ VSPR-0.1V	-	-	+/- 50	mV
Output offset voltage	Voff	-		-	+/-50	mV
Standby Mode Current Consumption - 3 Power Mode						
Sleep In Mode	VSP	Ta=25℃ VSP=5.4V VSN=-5.4V IOVCC=1.8V	-	50	-	µA
	VSN		-	50	-	
	IOVCC		-	35	-	

7.2.2 DSI DC Characteristics

LP Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps

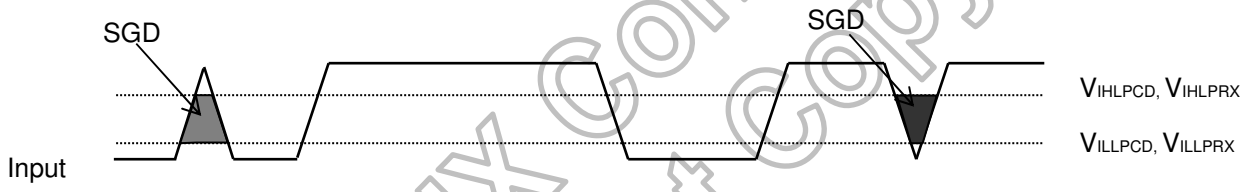


Figure 7.1: Input glitch rejections of low-power receivers

High Speed Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF

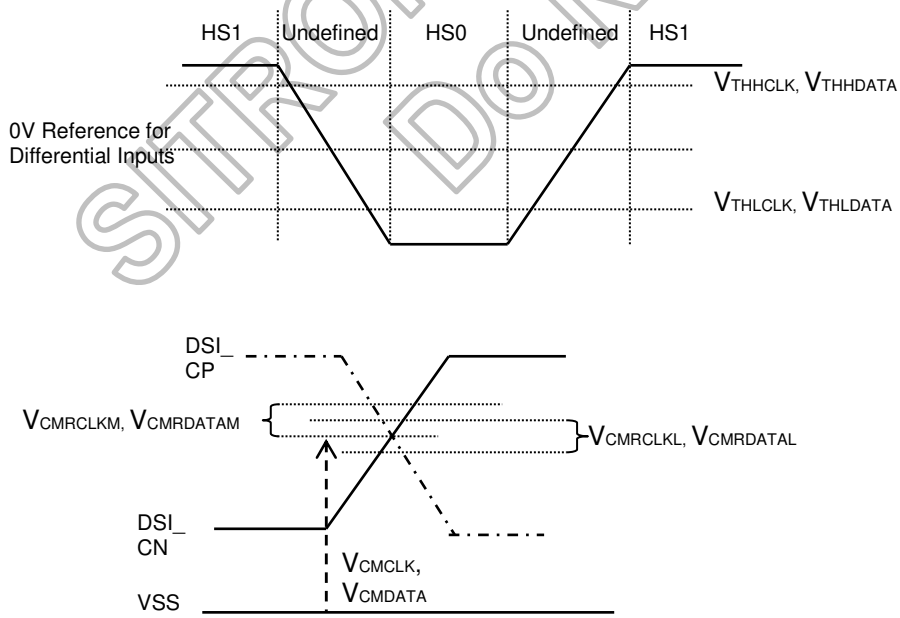


Figure 7.2: Differential voltage range and Command mode voltage

7.3 AC characteristics

7.3.1 Serial Interface Characteristics

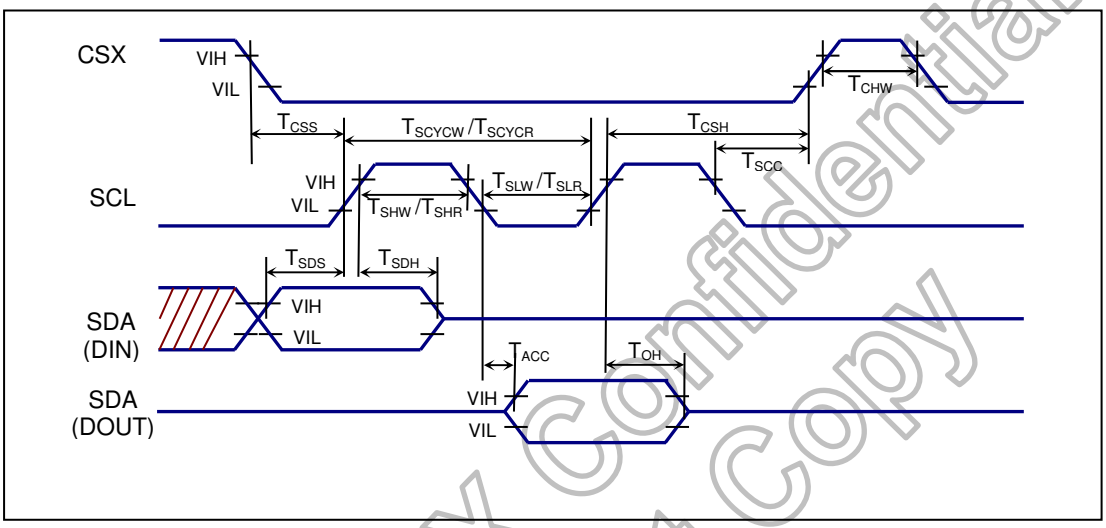


Figure 7.3: Serial Interface Characteristics

(VSSA=0V, IOVCC=1.8V, VCI=2.8V, T_A = 25°C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS}	Chip select setup time (Write)	15	-	ns	-
	t_{CSS}	Chip select setup time (Read)	60	-		
	t_{CSH}	Chip select hold time (Write)	15	-		
	t_{CSH}	Chip select hold time (Read)	65	-		
DCX	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
SCL (Write)	t_{WC}	Write cycle	66	-	ns	-
	t_{WRH}	Control pulse “H” duration	15	-		
	t_{WRL}	Control pulse “L” duration	15	-		
SCL (Read)	t_{RC}	Read cycle	150	-	ns	-
	t_{RDH}	Control pulse “H” duration	60	-		
	t_{RDL}	Control pulse “L” duration	60	-		
SDA (Input)	t_{DS}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DH}	Data hold time	10	-		
SDA (Output)	t_{ACC}	Read access time	-	100	ns	
	t_{OH}	Output disable time	10	-		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 7.2: Serial Interface Characteristics

7.3.2 DSI Interface Timing Characteristics

High Speed Mode

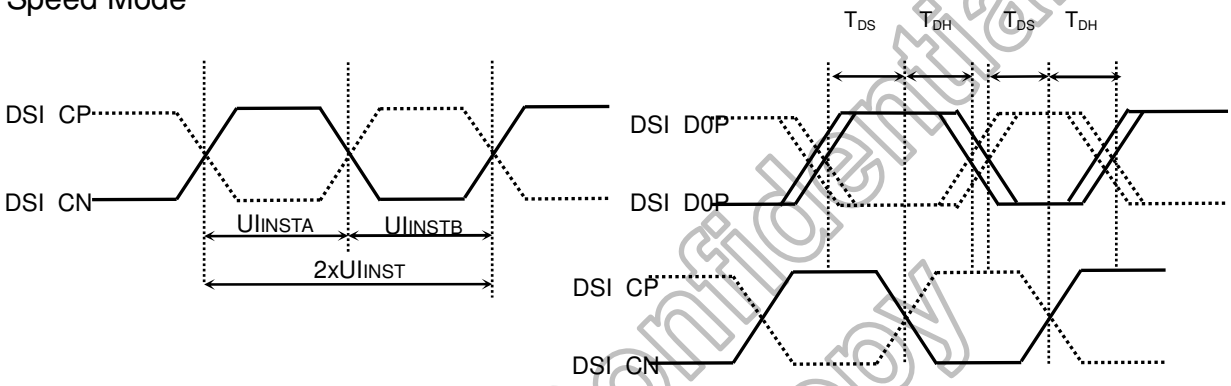


Figure 7.4: DSI clock timing Characteristics

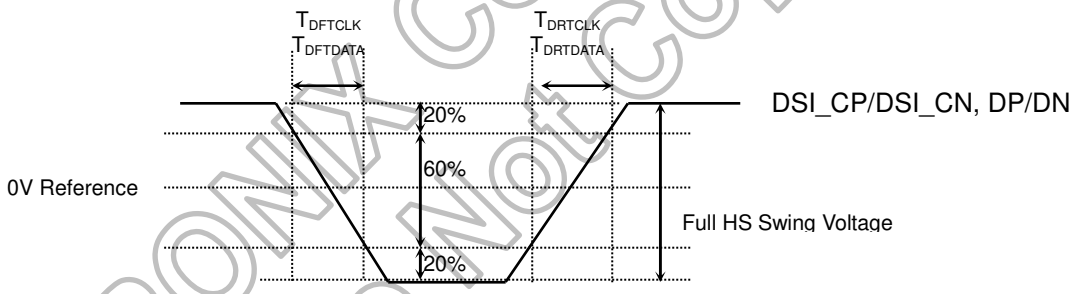


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V,T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	$2xUI_{INST}$	TBD	-	25	ns
	UI instantaneous	UI_{INSTA} UI_{INSTB}	TBD	-	12.5	ns
DP/DN	Data to clock setup time	T_{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T_{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T_{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T_{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	$T_{DRTDATA}$	150	-	0.3UI	ps
	Differential fall time for data	$T_{DFTDATA}$	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode Characteristics

Low Power Mode

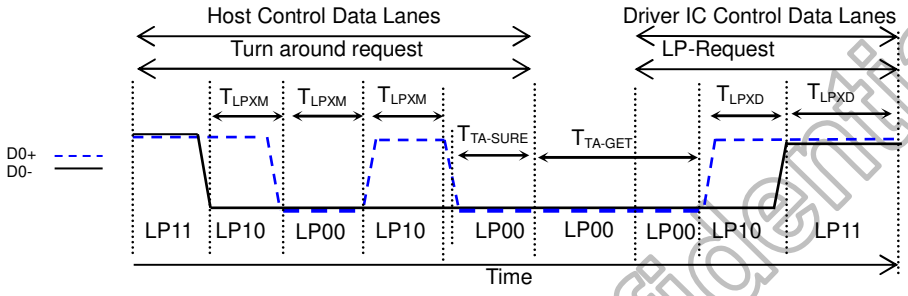


Figure 7.6: BTA from HOST to Display Module Timing

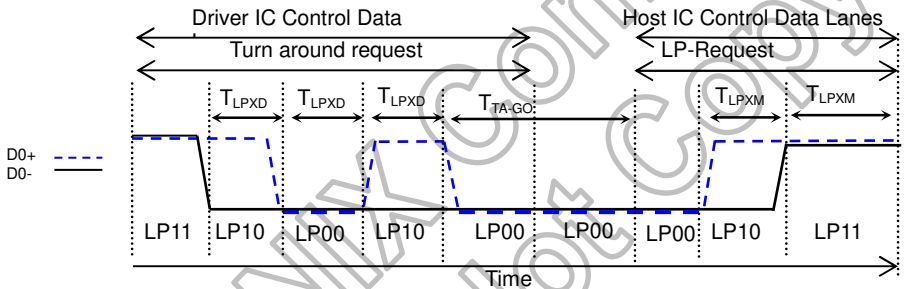


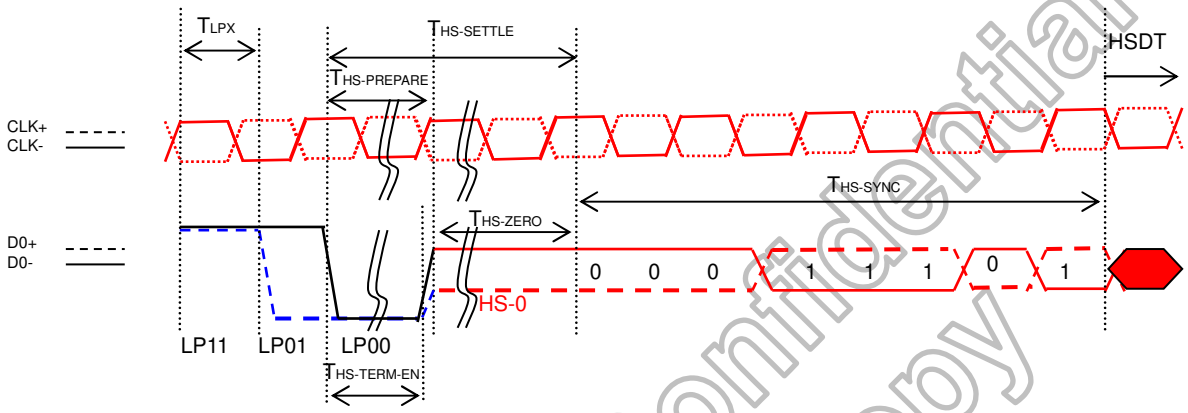
Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

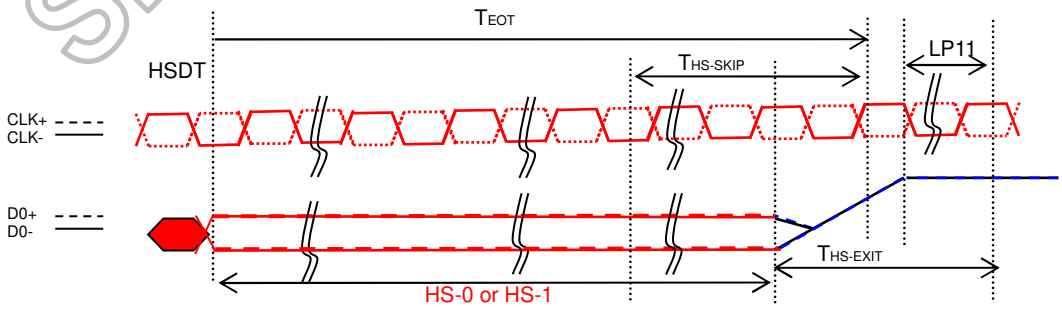
Table 7.4: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

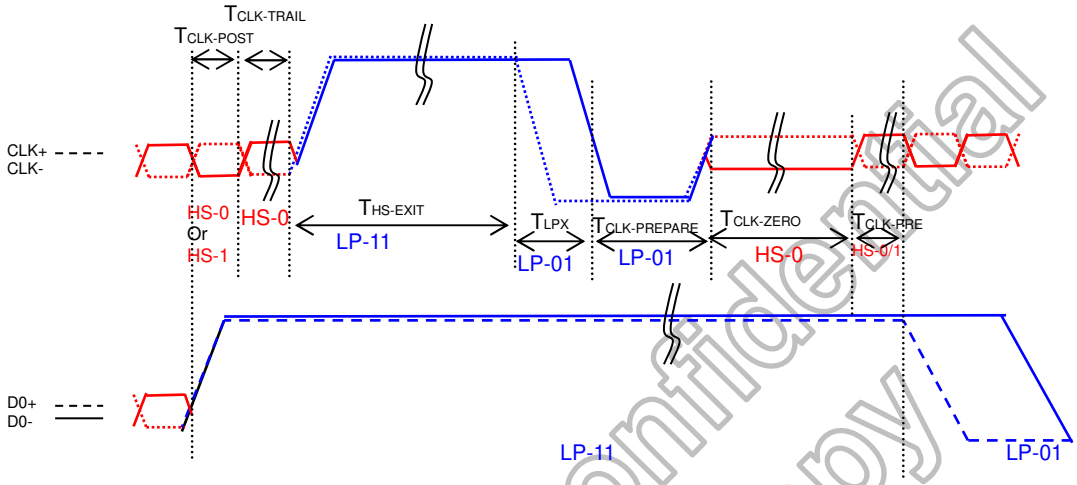
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

7.3.3 Reset input timing

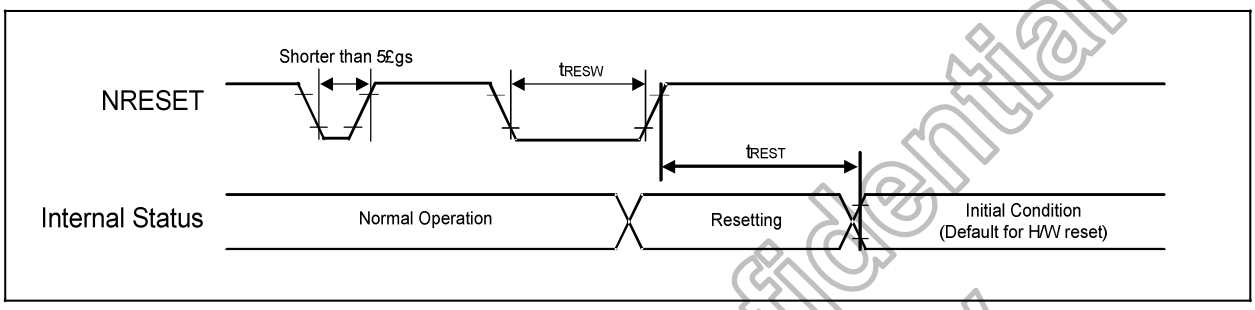


Figure 7.8: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

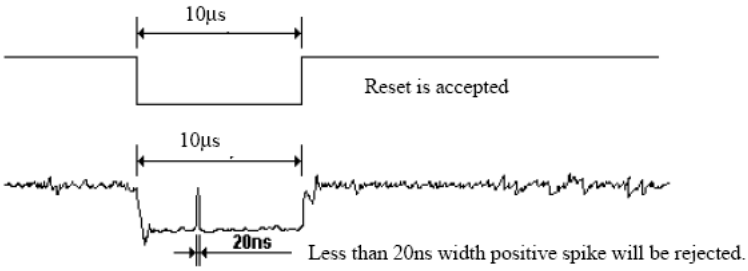
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Reference Application

8.1 Interface

The display, which is using DSI interface, is connected to the MPU as it is illustrated below.

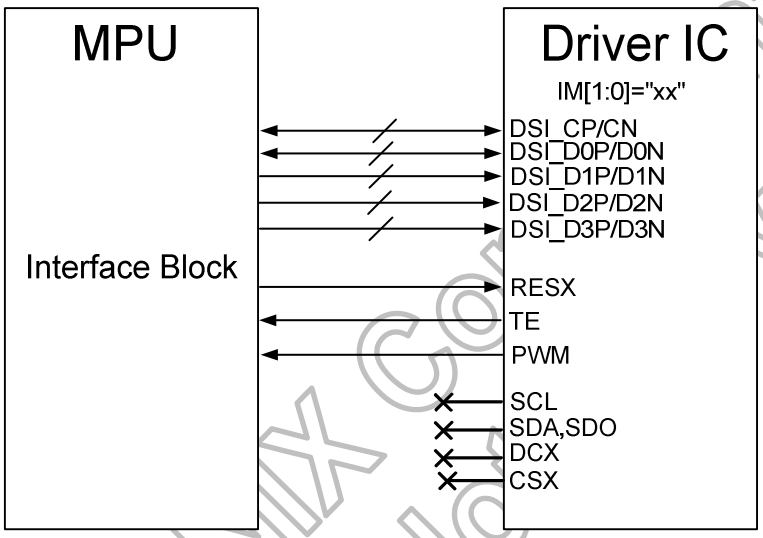


Figure 8.1: Interfacing for MIPI by Setting Lane [1:0]="11"

Notes：
1. When TE is not in use, please let it open.
2. When PWM is not in use, please let it open.
3. Connect DSI_D3_P/N to DSI_VSS in 3 data lanes application (LANE[1:0]="10").
4. Connect DSI_D3P/N and DSI_D2P/N to DSI_VSS in 2 data lanes application (LANE[1:0]="01").

8.2 Connections with Panel

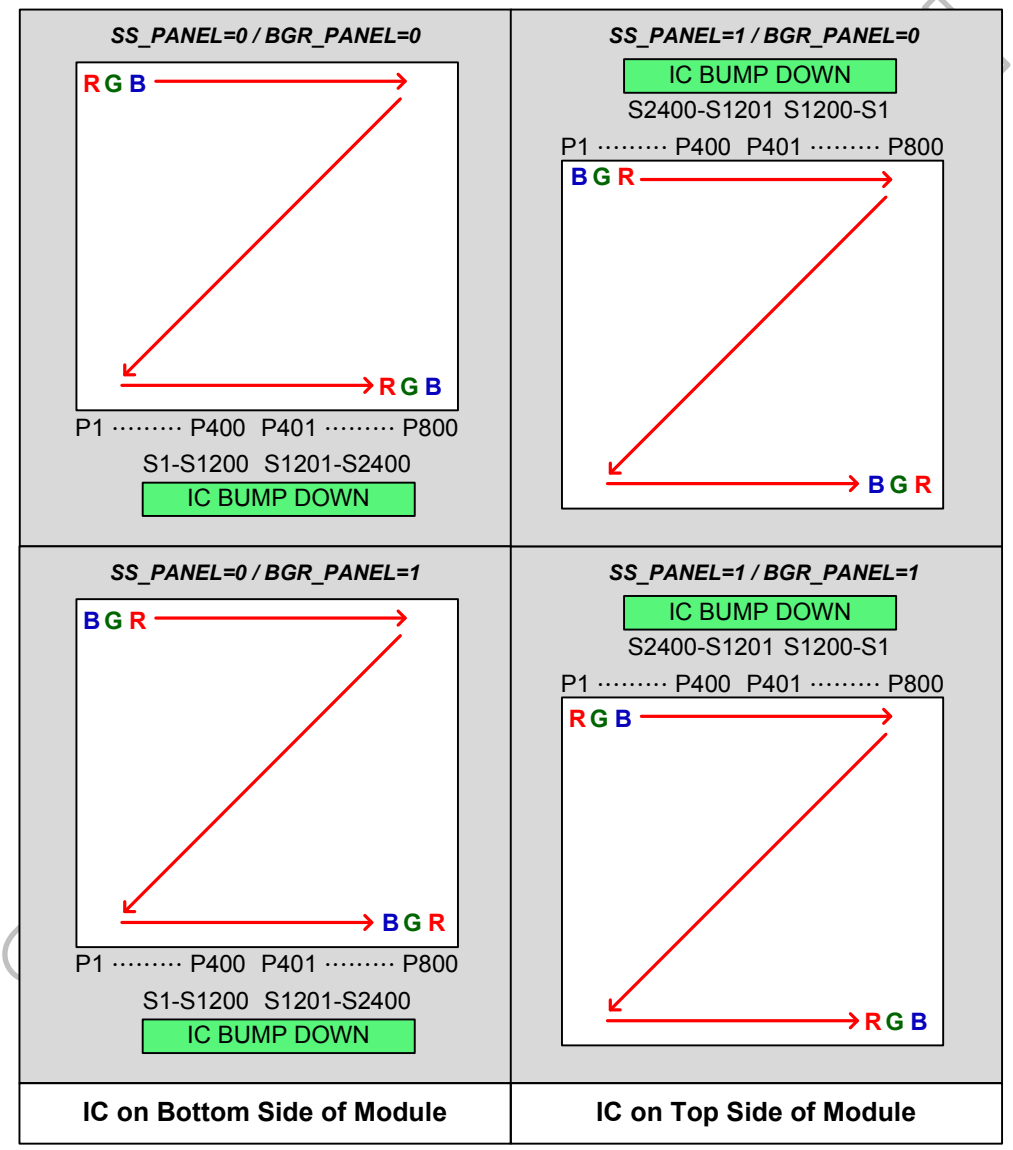


Figure 8.2: Source Pin Connection for Panel

The relationship between Sn output sequence and SS_PANEL / BGR_PANEL.

RESO SEL[2:0]	Resolution	SS PANEL	BGR PANEL	Sn Output Sequence	Used Sn Pin
2	720RGB	0	0	$S1_{(R)} \rightarrow S2_{(G)} \rightarrow S3_{(B)} \rightarrow \ldots \rightarrow S1080_{(B)} \rightarrow S1321_{(R)} \rightarrow \ldots \rightarrow S2398_{(R)} \rightarrow S2399_{(G)} \rightarrow S2400_{(B)}$	S1~S1080 and S1321~S2400
		0	1	$S1_{(B)} \rightarrow S2_{(G)} \rightarrow S3_{(R)} \rightarrow \ldots \rightarrow S1080_{(R)} \rightarrow S1321_{(B)} \rightarrow \ldots \rightarrow S2398_{(B)} \rightarrow S2399_{(G)} \rightarrow S2400_{(R)}$	
		1	0	$S2400_{(B)} \rightarrow S2399_{(G)} \rightarrow S2398_{(R)} \rightarrow \ldots \rightarrow S1321_{(R)} \rightarrow S1080_{(B)} \rightarrow \ldots \rightarrow S3_{(B)} \rightarrow S2_{(G)} \rightarrow S1_{(R)}$	
		1	1	$S2400_{(R)} \rightarrow S2399_{(G)} \rightarrow S2398_{(B)} \rightarrow \ldots \rightarrow S1321_{(B)} \rightarrow S1080_{(R)} \rightarrow \ldots \rightarrow S3_{(R)} \rightarrow S2_{(G)} \rightarrow S1_{(B)}$	
3	640RGB	0	0	$S1_{(R)} \rightarrow S2_{(G)} \rightarrow S3_{(B)} \rightarrow \ldots \rightarrow S960_{(B)} \rightarrow S1441_{(R)} \rightarrow \ldots \rightarrow S2398_{(R)} \rightarrow S2399_{(G)} \rightarrow S2400_{(B)}$	S1~S960 and S1441~S2400
		0	1	$S1_{(B)} \rightarrow S2_{(G)} \rightarrow S3_{(R)} \rightarrow \ldots \rightarrow S960_{(R)} \rightarrow S1441_{(B)} \rightarrow \ldots \rightarrow S2398_{(B)} \rightarrow S2399_{(G)} \rightarrow S2400_{(R)}$	
		1	0	$S2400_{(B)} \rightarrow S2399_{(G)} \rightarrow S2398_{(R)} \rightarrow \ldots \rightarrow S1441_{(R)} \rightarrow S960_{(B)} \rightarrow \ldots \rightarrow S3_{(B)} \rightarrow S2_{(G)} \rightarrow S1_{(R)}$	
		1	1	$S2400_{(R)} \rightarrow S2399_{(G)} \rightarrow S2398_{(B)} \rightarrow \ldots \rightarrow S1441_{(B)} \rightarrow S960_{(R)} \rightarrow \ldots \rightarrow S3_{(R)} \rightarrow S2_{(G)} \rightarrow S1_{(B)}$	
4	600RGB	0	0	$S1_{(R)} \rightarrow S2_{(G)} \rightarrow S3_{(B)} \rightarrow \ldots \rightarrow S900_{(B)} \rightarrow S1501_{(R)} \rightarrow \ldots \rightarrow S2398_{(R)} \rightarrow S2399_{(G)} \rightarrow S2400_{(B)}$	S1~S900 and S1501~S2400
		0	1	$S1_{(B)} \rightarrow S2_{(G)} \rightarrow S3_{(R)} \rightarrow \ldots \rightarrow S900_{(R)} \rightarrow S1501_{(B)} \rightarrow \ldots \rightarrow S2398_{(B)} \rightarrow S2399_{(G)} \rightarrow S2400_{(R)}$	
		1	0	$S2400_{(B)} \rightarrow S2399_{(G)} \rightarrow S2398_{(R)} \rightarrow \ldots \rightarrow S1501_{(R)} \rightarrow S900_{(B)} \rightarrow \ldots \rightarrow S3_{(B)} \rightarrow S2_{(G)} \rightarrow S1_{(R)}$	
		1	1	$S2400_{(R)} \rightarrow S2399_{(G)} \rightarrow S2398_{(B)} \rightarrow \ldots \rightarrow S1501_{(B)} \rightarrow S900_{(R)} \rightarrow \ldots \rightarrow S3_{(R)} \rightarrow S2_{(G)} \rightarrow S1_{(B)}$	
5	540RGB	0	0	$S1_{(R)} \rightarrow S2_{(G)} \rightarrow S3_{(B)} \rightarrow \ldots \rightarrow S810_{(B)} \rightarrow S1591_{(R)} \rightarrow \ldots \rightarrow S2398_{(R)} \rightarrow S2399_{(G)} \rightarrow S2400_{(B)}$	S1~S810 and S1591~S2400
		0	1	$S1_{(B)} \rightarrow S2_{(G)} \rightarrow S3_{(R)} \rightarrow \ldots \rightarrow S810_{(R)} \rightarrow S1591_{(B)} \rightarrow \ldots \rightarrow S2398_{(B)} \rightarrow S2399_{(G)} \rightarrow S2400_{(R)}$	
		1	0	$S2400_{(B)} \rightarrow S2399_{(G)} \rightarrow S2398_{(R)} \rightarrow \ldots \rightarrow S1591_{(R)} \rightarrow S810_{(B)} \rightarrow \ldots \rightarrow S3_{(B)} \rightarrow S2_{(G)} \rightarrow S1_{(R)}$	
		1	1	$S2400_{(R)} \rightarrow S2399_{(G)} \rightarrow S2398_{(B)} \rightarrow \ldots \rightarrow S1591_{(B)} \rightarrow S810_{(R)} \rightarrow \ldots \rightarrow S3_{(R)} \rightarrow S2_{(G)} \rightarrow S1_{(B)}$	

8.3 DC/DC Converter

8.3.1 External Power IC Mode - FL1002

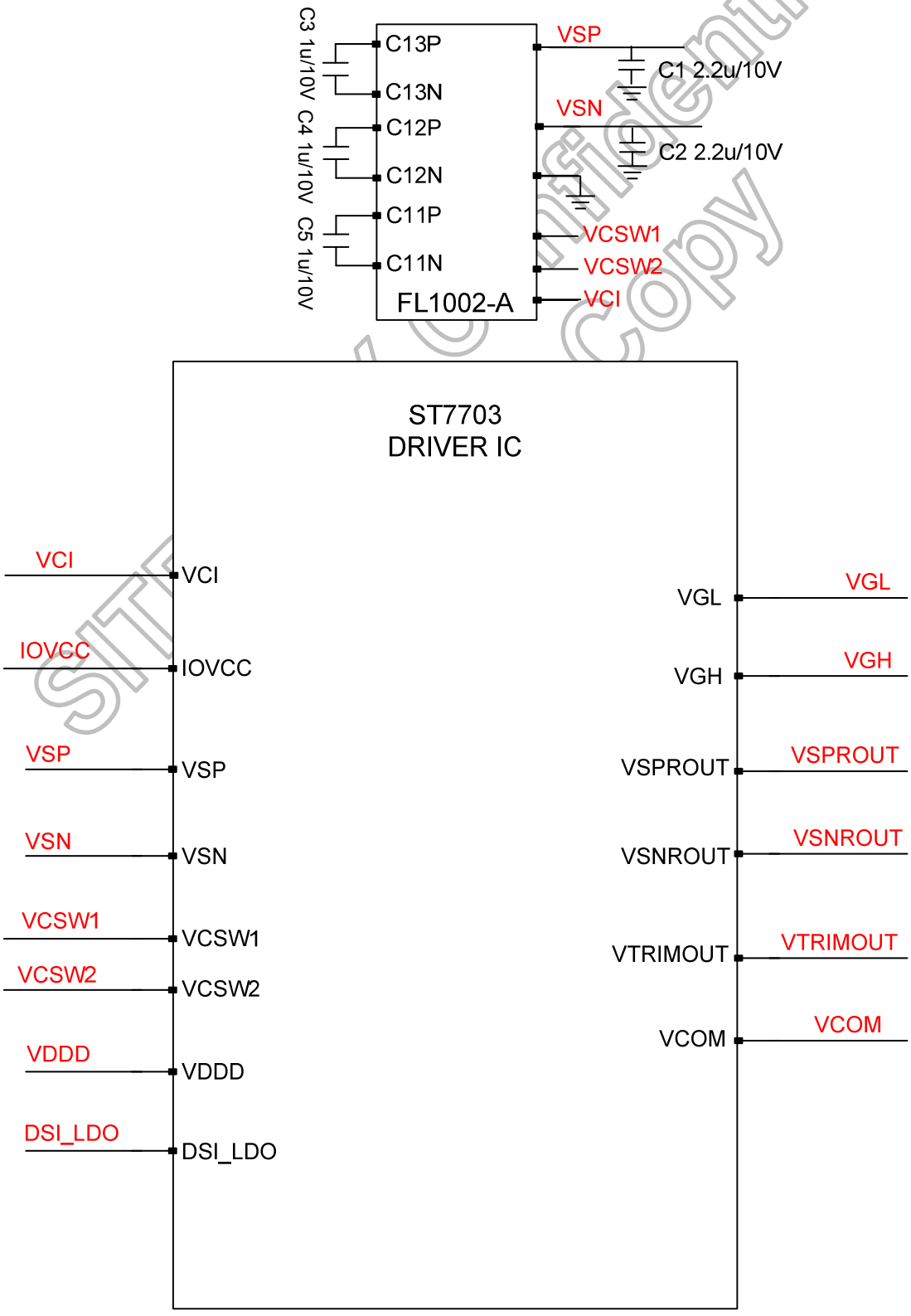


Figure 8.3: Using External Power IC Application

8.3.2 PFM Mode - Type C

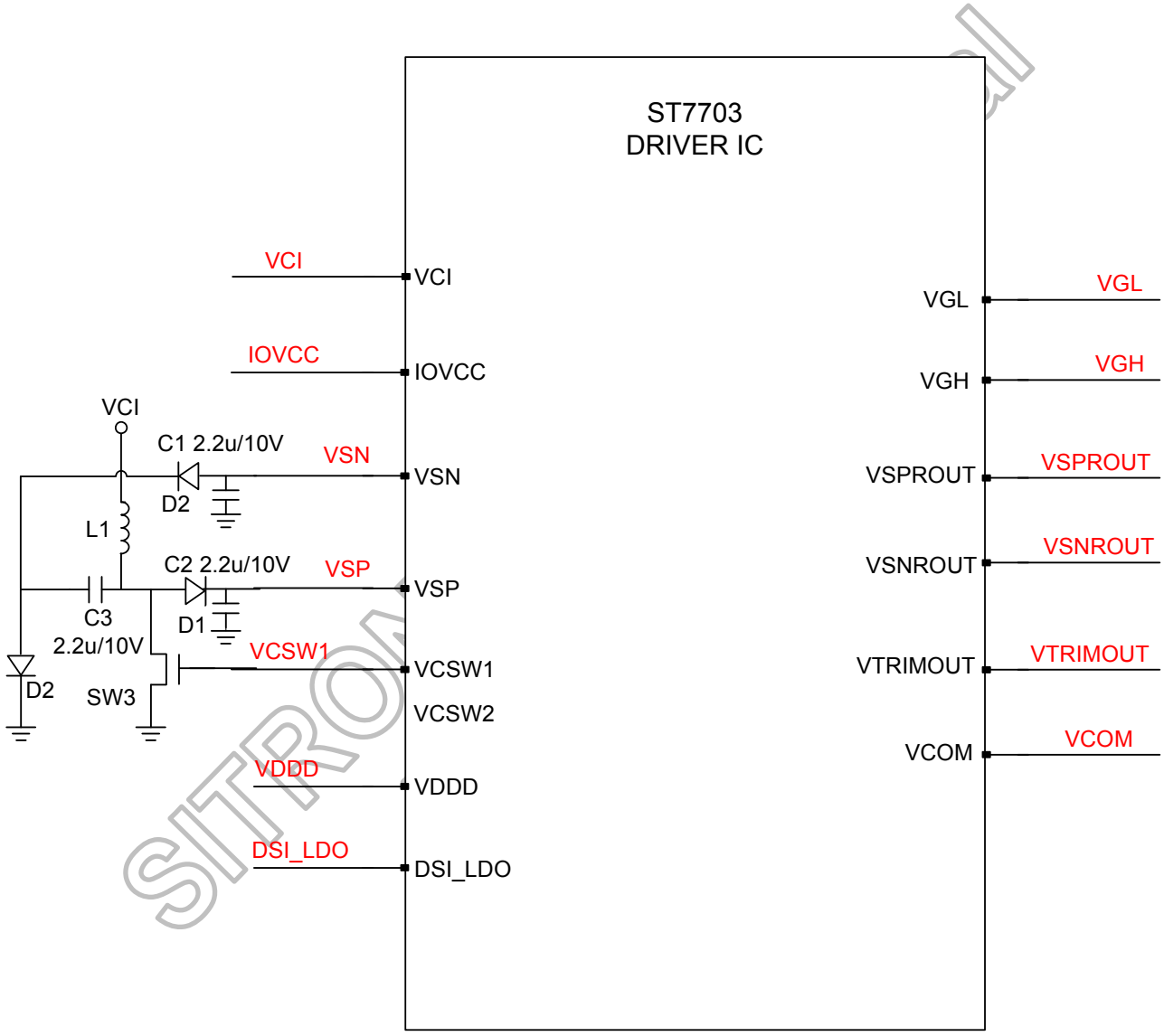


Figure 8.4: Using PFM - Type C Application

8.3.3 Three-Power Mode

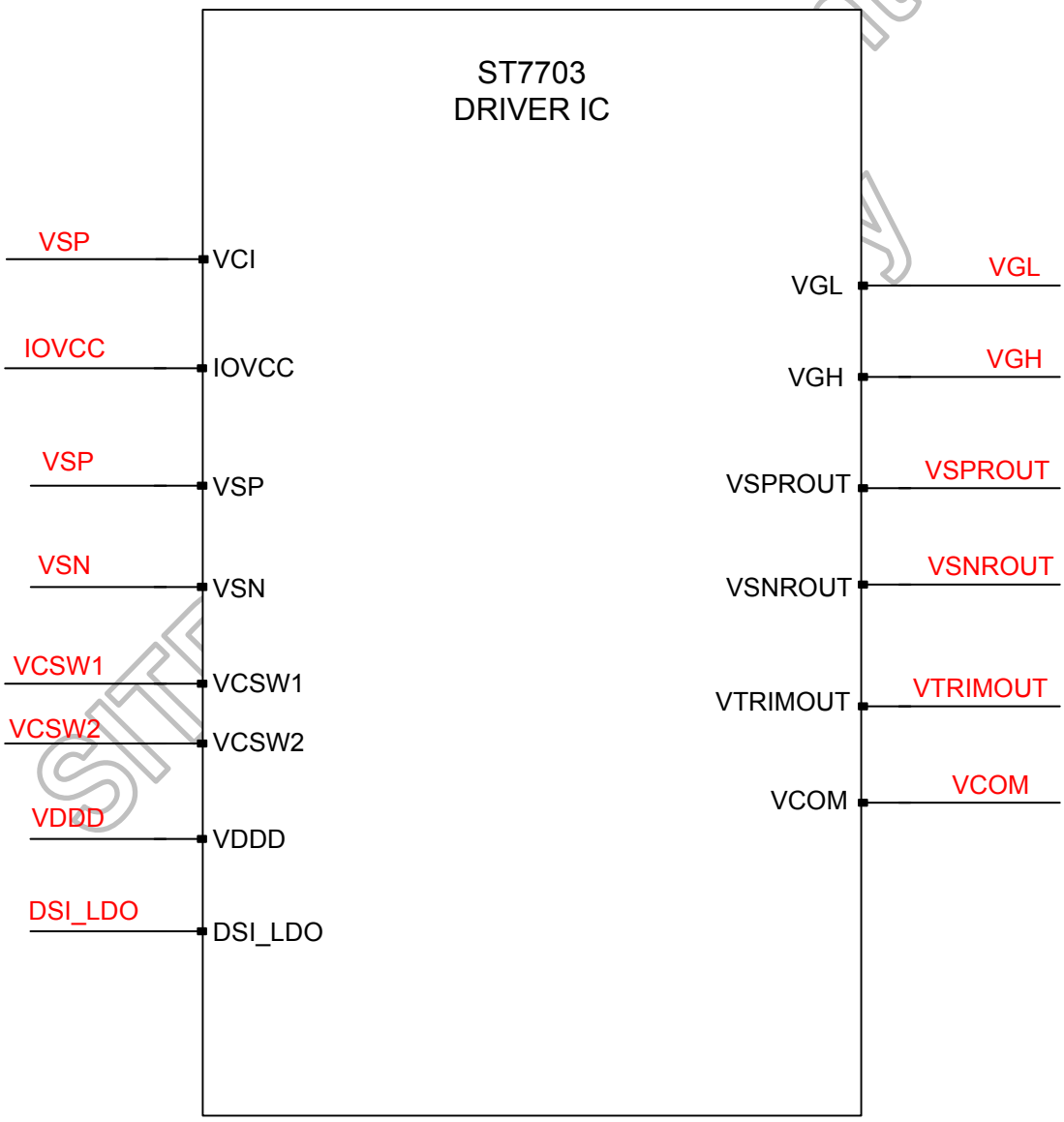


Figure 8.5: Using Three Power Mode Application

8.4 DSI Power On/Off Timing

8.4.1 Power On Timing of External Power IC

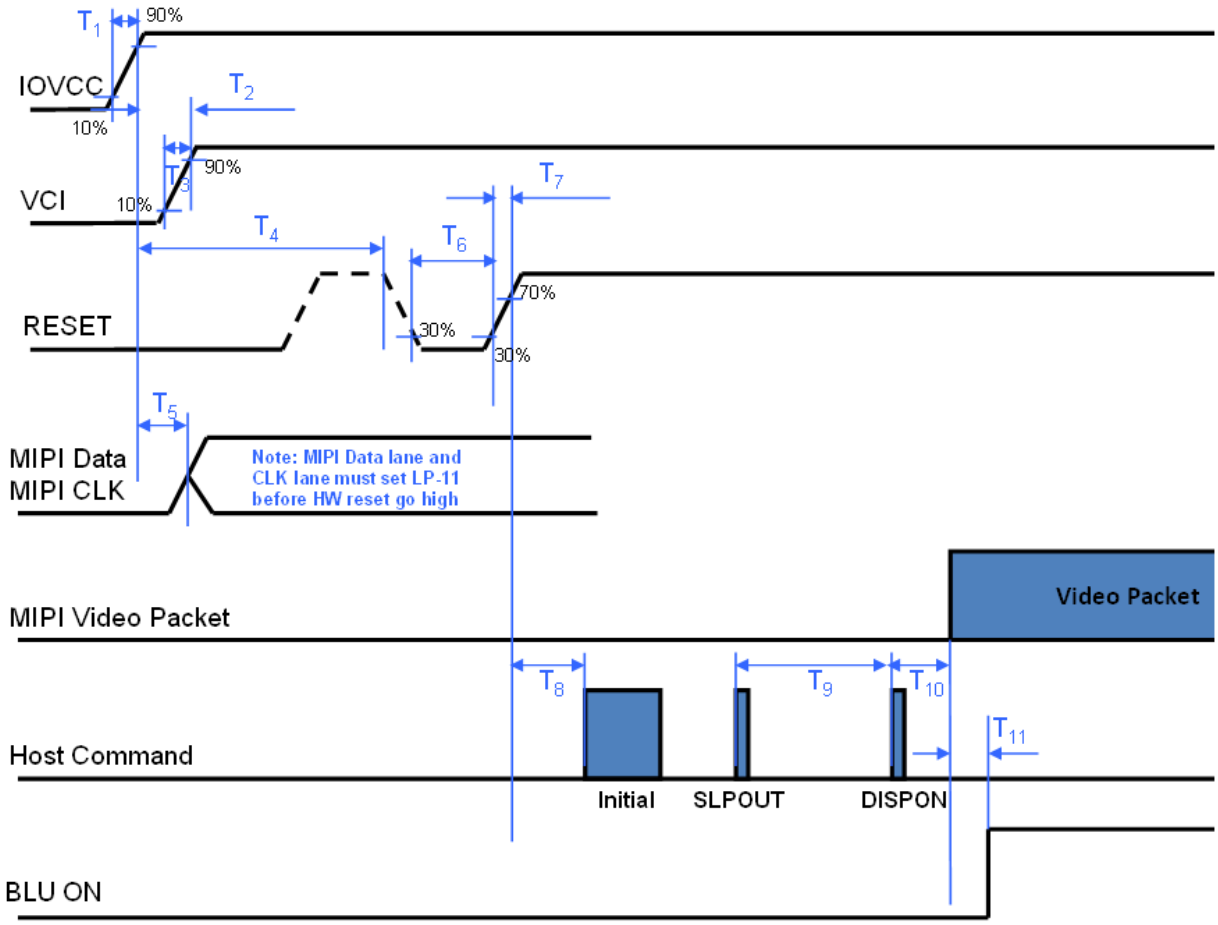


Figure 8-6: DSI Power On Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T1	0.01	-	10	ms
T2		No Limit		ms
T3	0.01	-	10	ms
T4	1	-	-	ms
T5	1	-	-	ms
T6	10	-	-	us
T7		No Limit		ns
T8	15	-	-	ms
T9	120	-	-	ms
T10		No Limit		ms
T11	100	150	-	ms

Table 8-1: DSI Power On Timing of Power IC Mode

8.4.2 Power Off Timing of External Power IC

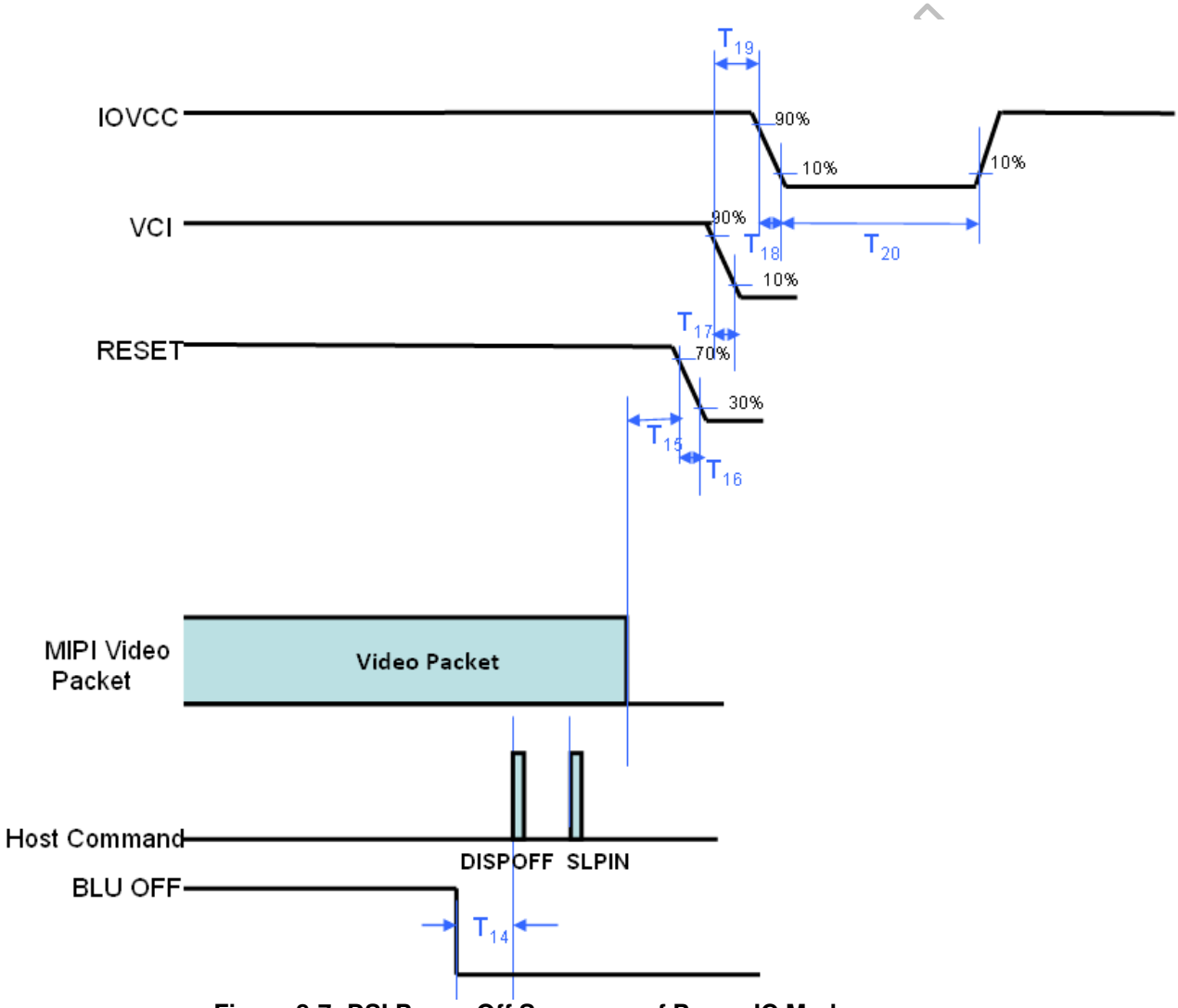


Figure 8-7: DSI Power Off Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T14	40	100	-	ms
T15	10	-	-	ms
T16	No Limit			ms
T17	No Limit			ms
T18	No Limit			ms
T19	No Limit			ms
T20	100			ms

Table 8-2: DSI Power Off Timing of Power IC Mode

8.4.3 Power On Timing of 3-Power Mode

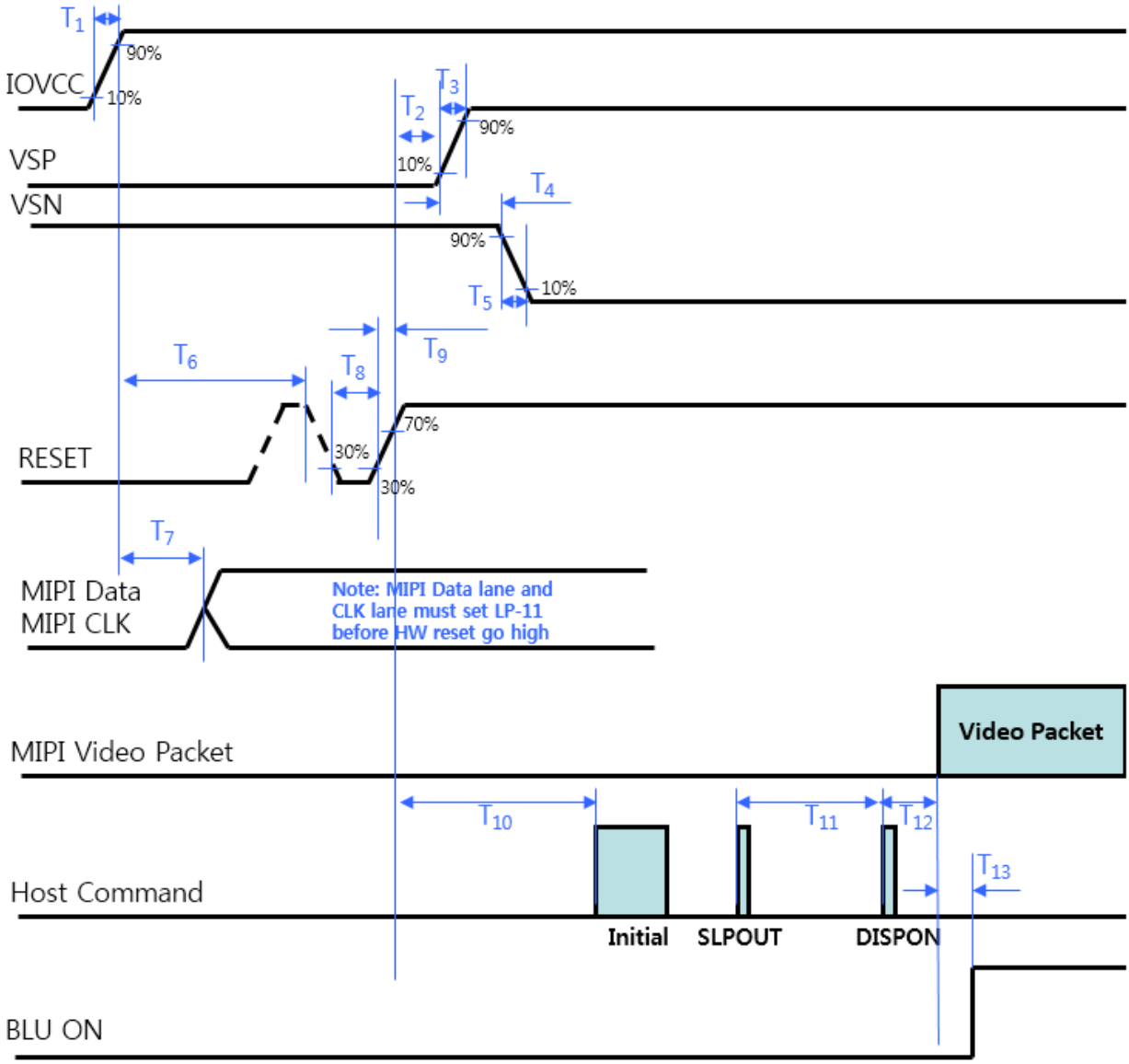


Figure 8-8: DSI Power On Sequence of 3 Power Mode

	Min.	Typ.	Max.	Unit
T1	0.01	-	10	ms
T2	10	-	-	ms
T3	0.01	-	10	ms
T4	No Limit			ms
T5	0.01	-	10	ms
T6	1	-	-	ms
T7	1	-	-	ms
T8	10	-	-	us
T9	No Limit			ns
T10	15	-	-	ms
T11	120	-	-	ms
T12	No Limit			ms
T13	100	150	-	ms

Table 8-3: DSI Power On Timing of 3 Power Mode

8.4.4 Power Off Timing of 3-Power Mode

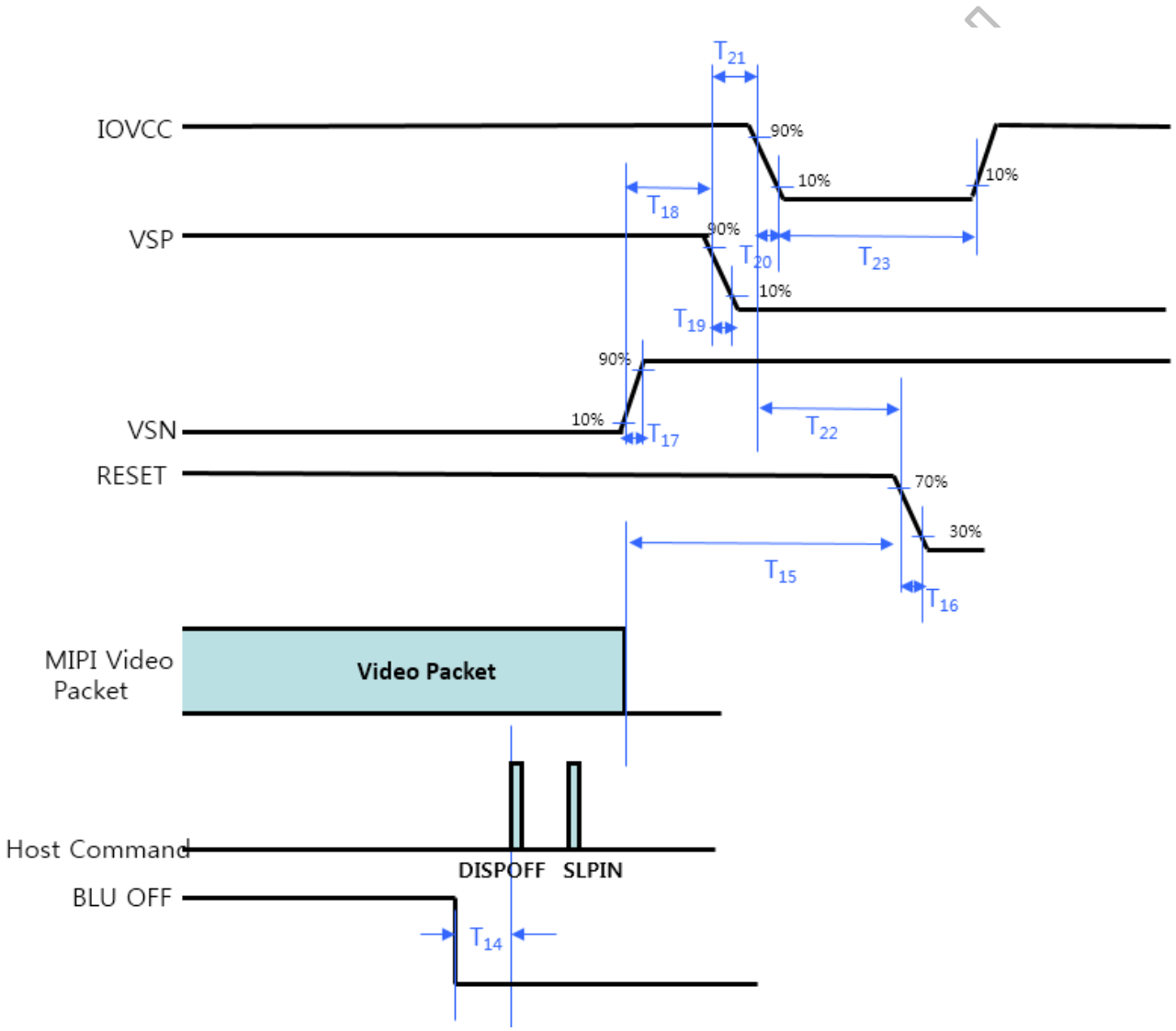


Figure 8-9: DSI Power Off Sequence of 3 Power Mode

	Min.	Typ.	Max.	Unit
T14	40	100	-	ms
T15	10	-	-	ms
T16	No Limit			ms
T17	No Limit			ms
T18	1	-	-	ms
T19	No Limit			ms
T20	No Limit			ms
T21	1	-	-	ms
T22	1	-	-	ms
T23	100	-	-	ms

Table 8-4: DSI Power Off Timing of 3 Power Mode

8.5 Maximum Layout Resistance

Name	Type	Maximum layout resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VSSD	Power supply	10	Ω
VSSA	Power supply	10	Ω
DSI_VSS	Power supply	10	Ω
IM0,IM1,LANSEL	Input	100	Ω
VCSW1, VCSW2	Output	30	Ω
DCX,SCL,CSX,RESX	Input	100	Ω
SDA	Input/Output	100	Ω
SDO	Output	100	Ω
VOUT,HOUT	Output	100	Ω
PWM	Output	100	Ω
VCOM	Output	10	Ω
DSI_D0P	Input/Output	8	Ω
DSI_D0N	Input/Output	8	Ω
DSI_CP	Input	8	Ω
DSI_CN	Input	8	Ω
DSI_D1P	Input	8	Ω
DSI_D1N	Input	8	Ω
DSI_D2P	Input	8	Ω
DSI_D2N	Input	8	Ω
DSI_D3P	Input	8	Ω
DSI_D3N	Input	8	Ω
VDDD	Output	10	Ω
VSP,VSN	Input/Output	10	Ω
VSPROUT, VSNROUT	Output	10	Ω
VTRIMOUT	Output	10	Ω
VGL	Output	10	Ω
VGH	Output	10	Ω
DSI_LDO	Output	10	Ω
OSC	Input	100	Ω
VTESTOUTP, VTESTOUTN	Output	100	Ω
CGOUTL_1~22	Output	30	Ω
CGOUTR_1~22	Output	30	Ω

Table 8-5: Maximum Layout Resistance