

Goal of the Project

- Simulate and perform layout of an operational transconductance amplifier.
- Note: Read the classic neural amplifier paper to understand the process of designing an amplifier.
- Schematic of the OTA is shown below.

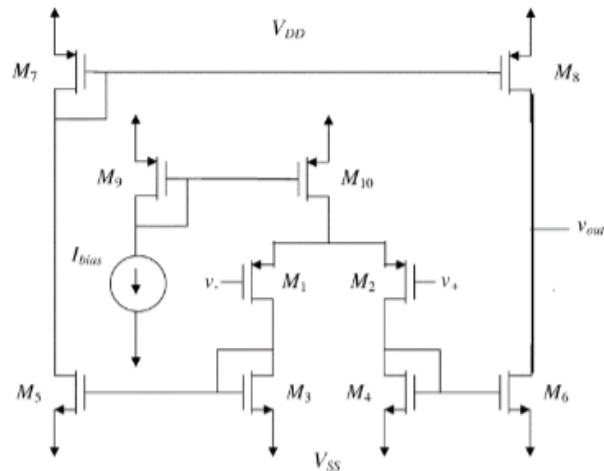


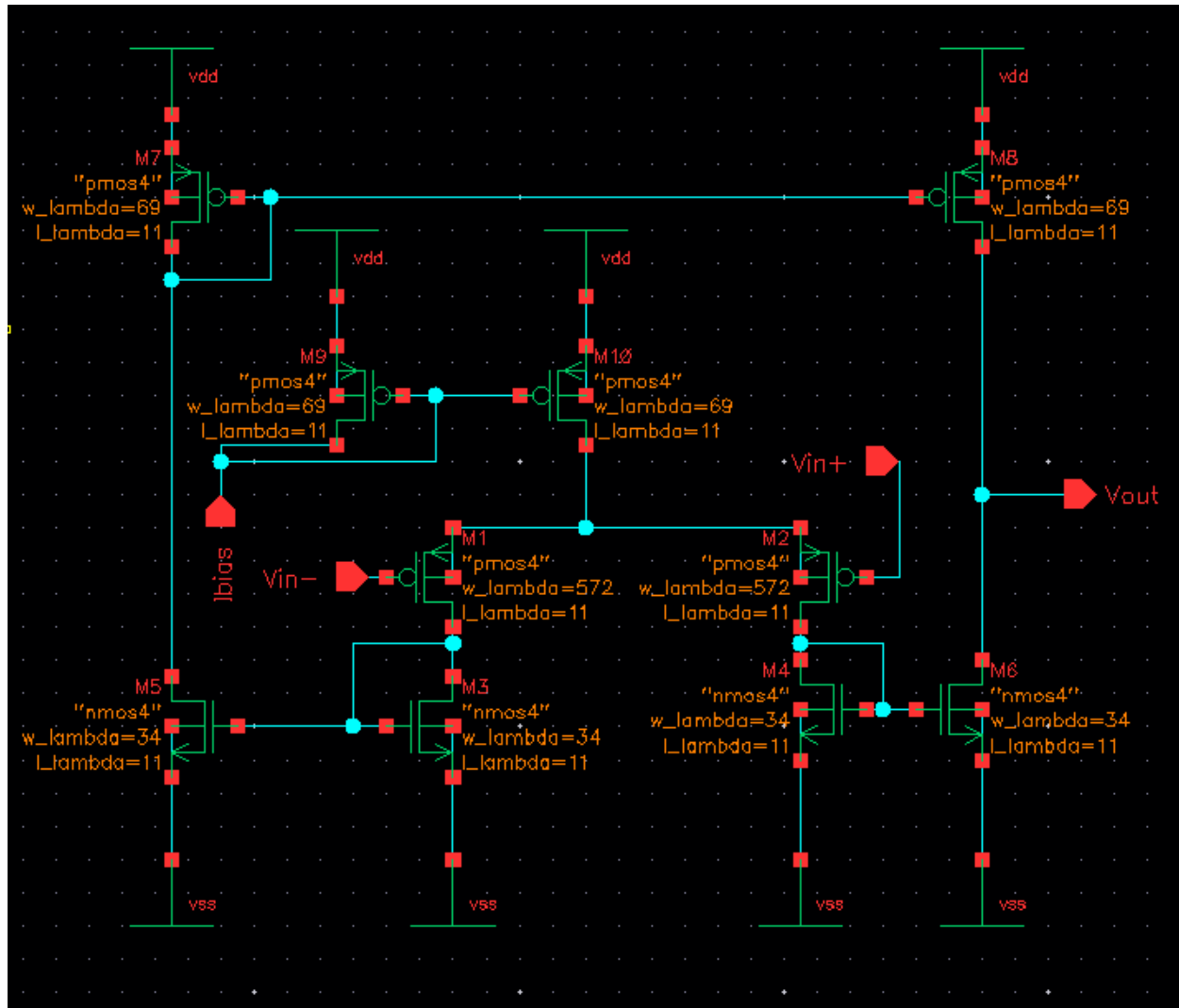
Figure 1. Schematic of an OTA.

- Using the widths and lengths given in the table below, you will find the... (*using AC analysis*) for both schematic and layout. For frequency = 1k Hz...
 - Open loop gain (dB) = -337.6 dB
 - F-3db frequency (Hz) = 14.19 Hz
 - Unity gain frequency (Hz) = 0 Hz

| Transistors | W/L (um) 2.8575 | W/L (lamda) |
|-----------------|-----------------|-------------|
| M1, M2 | 200/4 | 572/11 |
| M3, M4, M5, M6 | 12/4 | 34/11 |
| M7, M8, M9, M10 | 24/4 | 69/11 |
| Ibias | 8 uA | |

- Overall area = $((228*277.5)+(30*234))/(2.8575)^2 = 8608.4 \text{ um}^2$
- Overall power consumption = $6.15 * 10^{-5} \text{ W}$

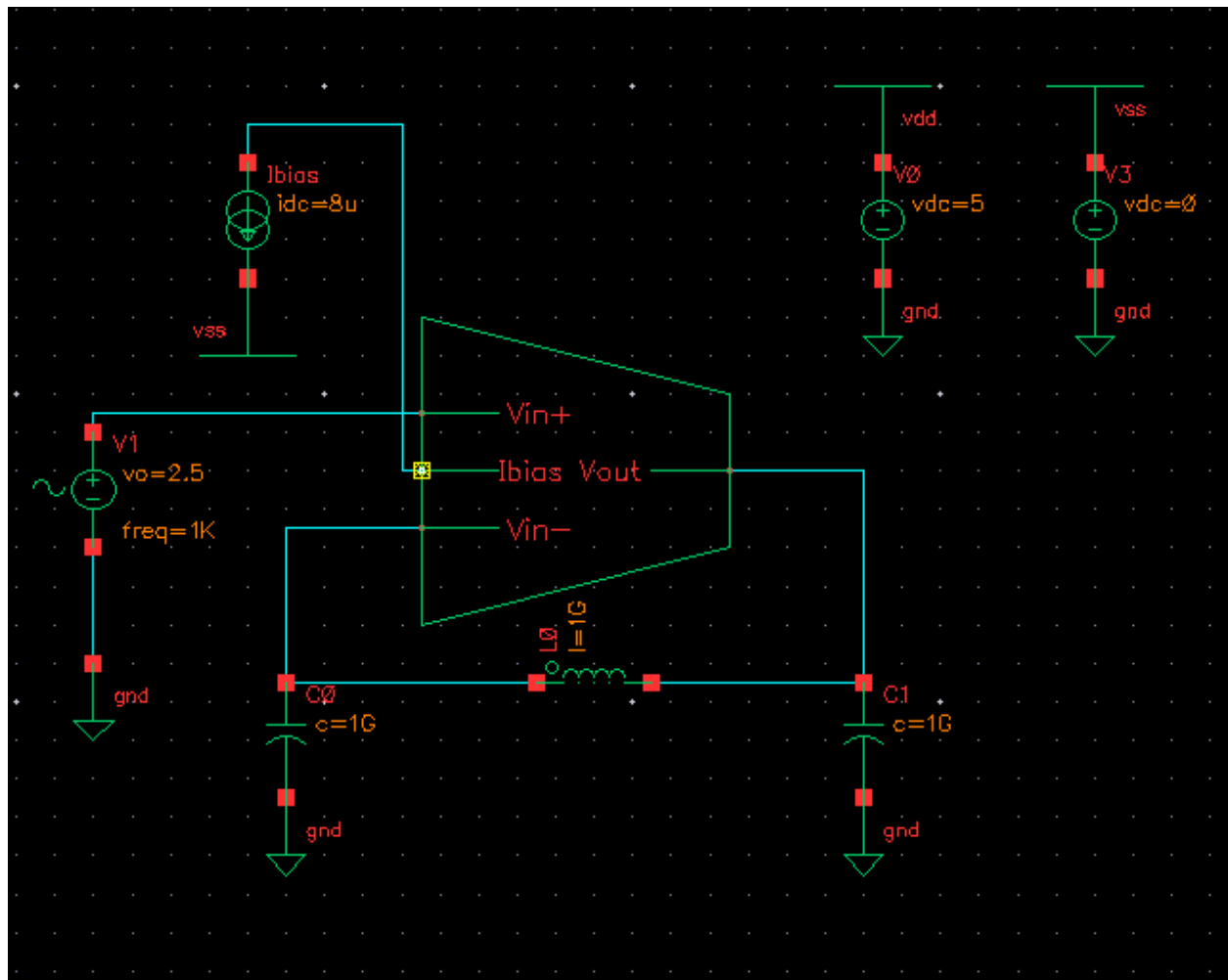
Schematic



Elick D'Rozario

ENEE 408D

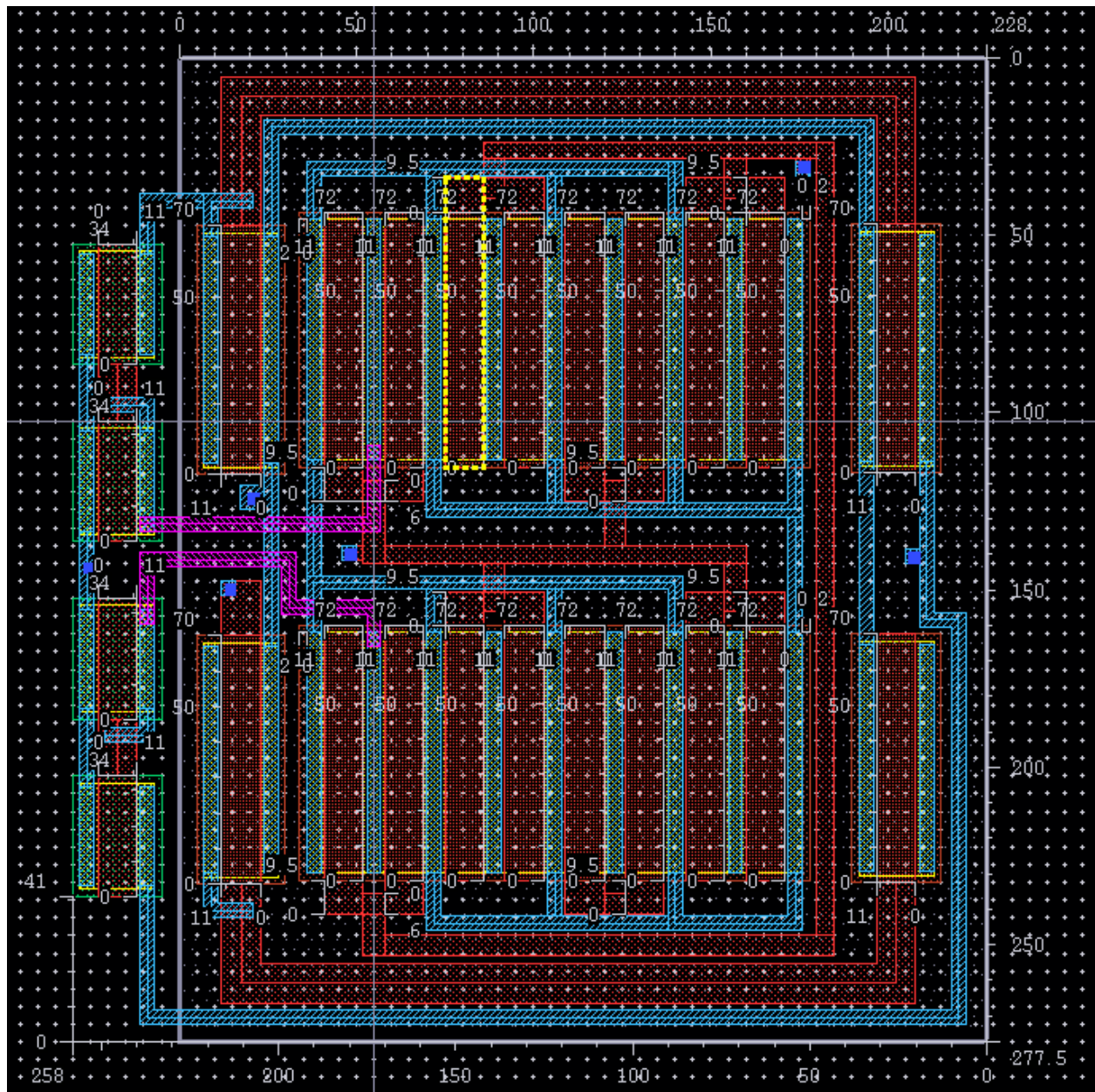
Testbench



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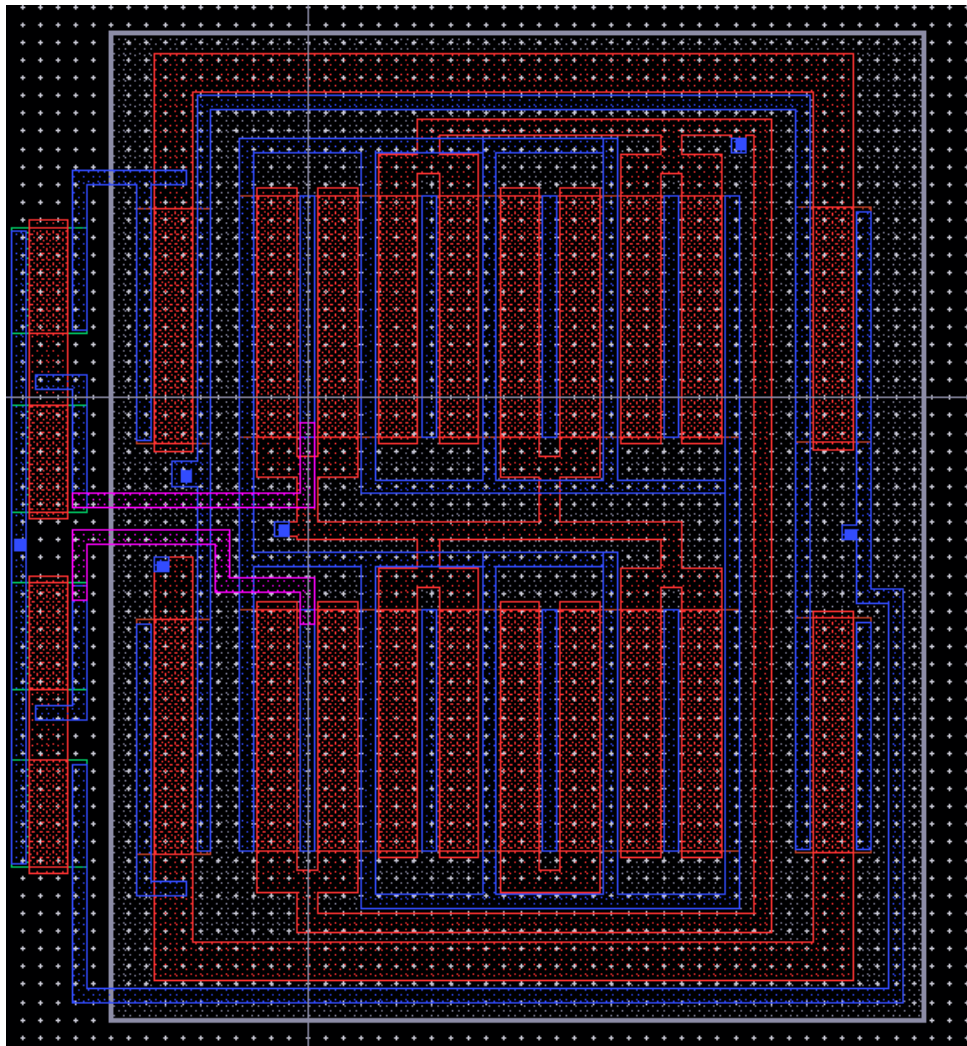
Layout



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Extracted



Run Directory: LVS Browse

Create Netlist: ☒ schematic ☒ extracted

Library: 408D 408D

Cell: INV INV

View: schematic extracted

Browse Sel by Cursor Browse Sel by Cursor

Rules File: techfiles/divaLVS.rul Browse

Run LVS

LV

Co

Sw

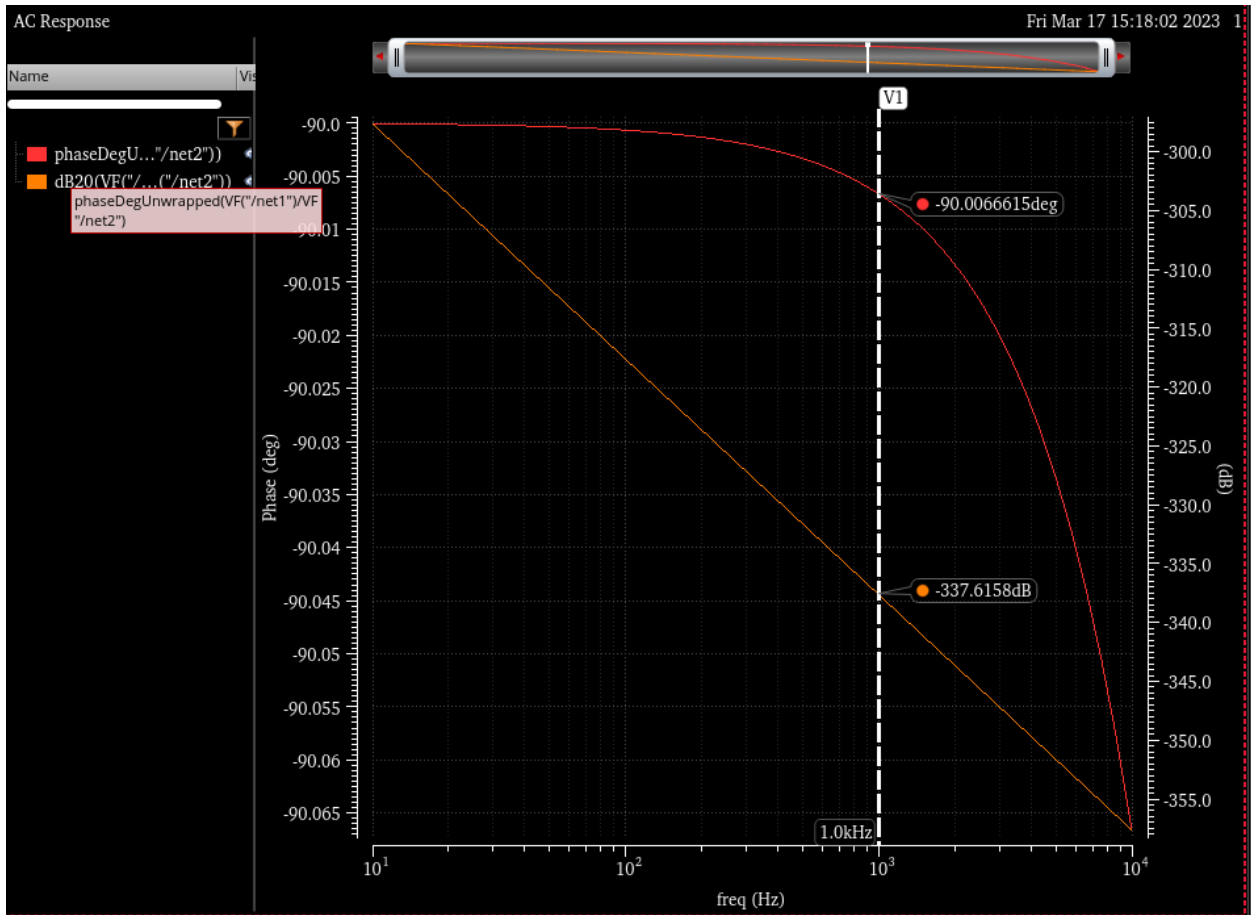
Create

! The LVS job has completed. The net-lists match.

Run Directory: /home/enee408d_student/Cadence2021/LVS

Close

AC Analysis



| Outputs | | | | |
|---------|-------------------|-------|-------------------------------------|--------------------------|
| | Name/Signal/Expr | Value | Plot | Save |
| 1 | Unity Gain Freq | | <input checked="" type="checkbox"/> | <input type="checkbox"/> |
| 2 | Open Loop Gain | wave | <input checked="" type="checkbox"/> | <input type="checkbox"/> |
| 3 | F-3db Freq | 14.19 | <input checked="" type="checkbox"/> | <input type="checkbox"/> |
| 4 | Phase | wave | <input checked="" type="checkbox"/> | <input type="checkbox"/> |
| 5 | Power Consumption | 61.5u | <input checked="" type="checkbox"/> | <input type="checkbox"/> |
| 6 | Phase Margin | | <input checked="" type="checkbox"/> | <input type="checkbox"/> |