

EEE313: ELECTRICAL CIRCUIT DESIGN

Term Project Report



Discrete OPAMP

**Elif Beray Sarışık, 22003267, EEE313 Section 01
Müge Sarıbekiroğlu, 22003046, EEE313 Section 01**

Department of Electrical and Electronics Engineering, Bilkent University

1. Introduction

The purpose of this project is to implement a simple Operational Amplifier (OPAMP) with differential input and single ended output and an output stage using BJTs. The requirements given in the project manual as follows:

- $+\text{-} \text{VDD}$ no more than $+\text{-}10\text{V}$.
- Power consumption should be less than 200mW , which total current per supply should be less than 10mA .
- $A_v = V_{\text{OUT}}/(V_+ - V_-) > 500$
- R_L should be less than $1\text{k}\Omega$, which does not affect the gain of the circuit.

Besides, the test circuit with $R_1=R_2=5\text{k}\Omega$ for this project is given as Figure 1.

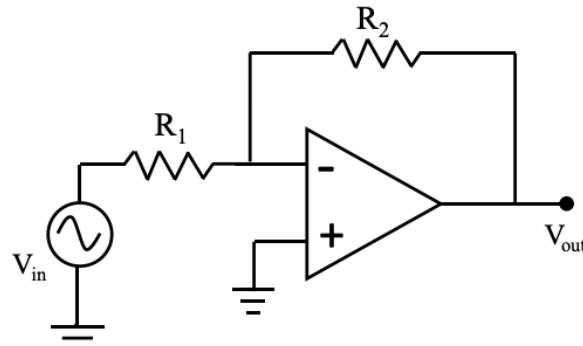


Figure 1: The Test Circuit for the OPAMP

It is observed that the test circuit behaves as a differential amplifier with gain -1. Firstly, the LTSpice simulation circuit is generated by analyzing the behavior of the test circuit.

In order to obtain the behavior of the test circuit, a differential amplifier consists of BJTs are used (see Figure 2). Since differential amplifier requires current source, a current mirror circuit is utilized in order to obtain the behavior of current source (see Figure 3).

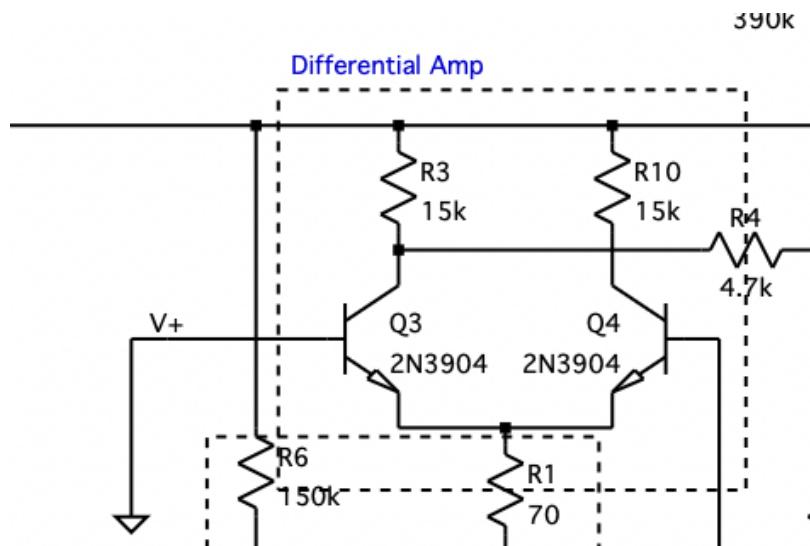


Figure 2: The Differential Amplifier Part of LTSpice Circuit Diagram

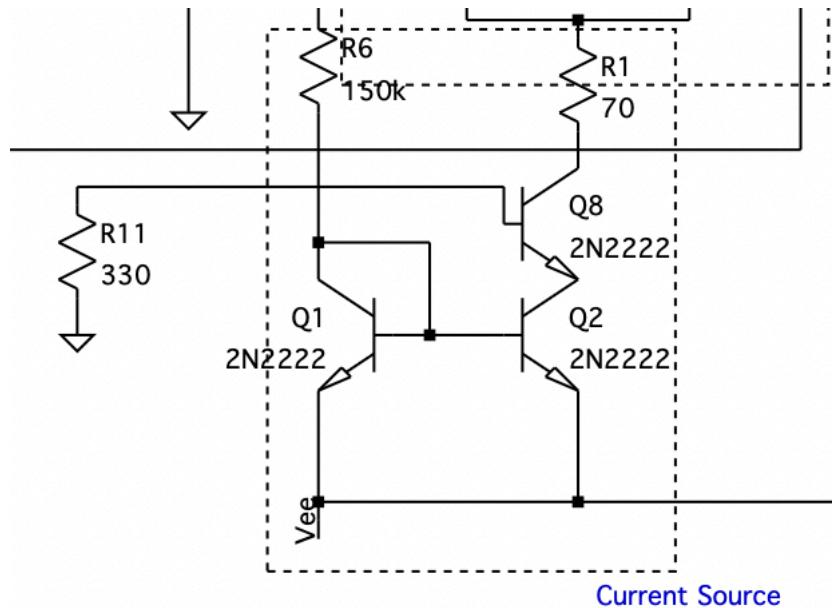
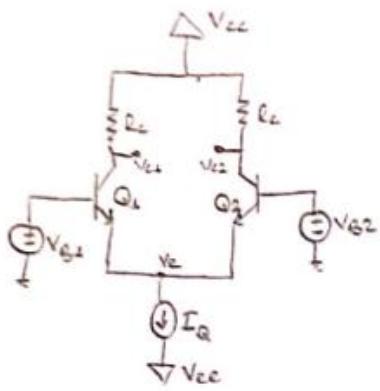


Figure 3: The Current Source Part of LTSpice Circuit Diagram

The DC and AC analysis of the differential amplifier with the provided current source circuit is computed as below:

BJT Differential Amplifier



In this circuit, Q_1 and Q_2 should match in F.A. region to make differential amplifier. Also, sum of their emitter currents should be equal to the I_Q .

In our circuit, we select $15k\Omega$ resistor as R_L and $130mA$ as I_Q .

To keep Q_1 , Q_2 and BJTs in the current source we should V_{B1} and V_{B2} carefully. Moreover, V_{B1} should be equal to V_{B2} in order to obtain common mode gain. V_{BL} and V_{B2} are common mode voltage. Our current source shown in the left.

According to this figure,

$$V_e = R_L \cdot I + V_{CE, sat, Q_2} + V_{CE, sat, Q_1} + V_{CC}$$

$$V_e = 0.07 \cdot 0.13 + 0.2 + 0.2 - 10 = -9.59V$$

This value is least value of V_e .

Therefore, least value of V_{B1} is equal to

$$-9.59 + 0.7 = -8.89V$$

To find maximum value of V_{BL} , we look at Q_1 and Q_2

$$V_{CE} \geq 0.2V$$

$$V_{CL} - (V_{BL} - 0.7) \geq 0.2V$$

$$V_{CL} + V_{CC} - I \cdot R_L = 10 - 0.065 \cdot 15 = 9.02V$$

$$9.02 - V_{BL} + 0.7 \geq 0.2$$

$$9.52 \geq V_{BL}$$

$$-9.59 \leq V_{BL} \leq 9.52$$

We select V_{BL} as $0V$. In other words, our sinusoidal signal's offset is zero.

When $V_{BL} = V_{B2} = 0V$, V_e is $-0.7V$.

$$V_{CL} = V_{C2} = V_{CC} - I \cdot R_L = 10 - 0.065 \cdot 15 = 9.03V$$

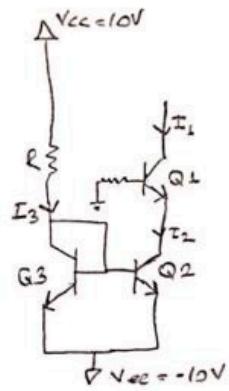
Q points of Q_1 and Q_2 is same and there are equal to;

$$V_{CE} = V_{CL} - V_{C2} = 9.03 - (-0.7) = 10.3V$$

$$I_L = 0.065mA$$

$$\text{Q}(10.3V, 0.065mA)$$

Current Source



We want to make I_1 be $130\mu A$.

Since B of the transistors is high enough.

$$I_L = I_2$$

Furthermore, I_3 is equal to I_2 because their V_{BES} are same.

$$V_{E3} = -10V$$

$$V_{B3} = V_{C3} = -10 + 0.7 = -9.3V$$

$$V_{CC} - V_{C3} = I_3 \cdot R$$

$$10 - (-9.3) = 0.13 \cdot R$$

$$R = 150k\Omega$$

R should be $150k\Omega$ to make I_3 be $130\mu A$.

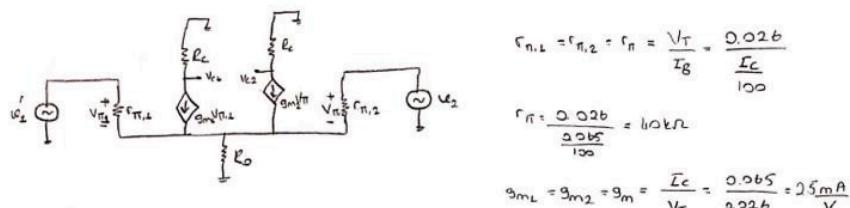
Q point of third BJT is:

$$V_{CE} = V_{C3} - V_{E3} = -9.3 - (-10) = 0.7V$$

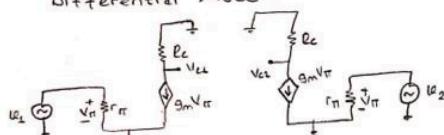
$$I_3 = 0.13mA$$

$$(Q_3: (0.7V, 0.13mA))$$

AC Analysis



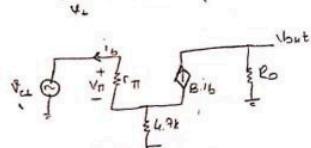
Differential Mode:



$$V_{C12} = -g_m V_{\pi} R_C$$

$$V_{\pi} = v_{in1} - v_{in2} = -2.5 \cdot 15 = -37.5 \frac{V}{V} = Adm_1 = -Adm_2$$

$$\frac{V_{C12}}{V_{in}} = -g_m R_C = -2.5 \cdot 15 = -37.5 \frac{V}{V}$$



We amplify V_{C12} in the Class AB amplifier.

$$V_{out} = B \cdot i_b \cdot R_o$$

$$V_{out} = -[r_{\pi} \cdot i_b + (\beta + 1) i_b \cdot 4.7]$$

$$\frac{V_{out}}{V_{in}} = \frac{B \cdot R_o}{r_{\pi} + (\beta + 1) \cdot 4.7}$$

By using this part in our circuit our differential mode gain which is -37.5 goes to -2065 in open loop.

R_o in the circuit came from diodes and NPN transistor in the Class AB amplifier.

After finalizing the differential amplifier circuit, a Class AB Amplifier circuit which comprises push and pull output stage is utilized. A Class AB Amplifier is used in order to prevent the crossover distortion occurred due to incorrect biasing in amplification within cycles [1]. The implementation of the Class AB Amplifier is done according to the instruction given in the fourth lab manual (see Figure 4).

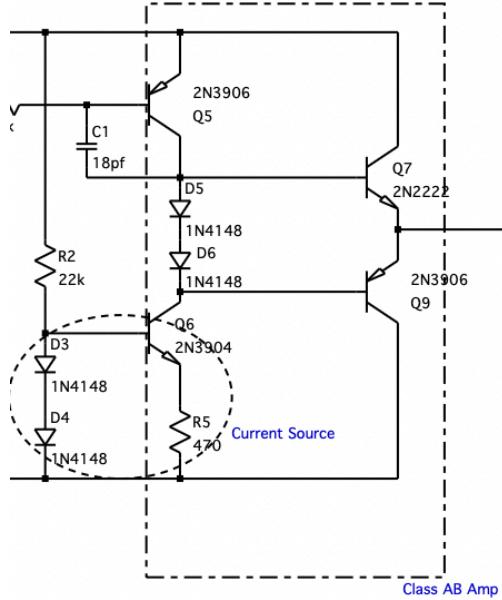


Figure 4: The Class AB Amplifier Part of LTSpice Circuit Diagram

Furthermore, a capacitor-compensation technique is used in order to enhance the linearity of the Class AB Amplifier circuit [2]. The overall circuit is implemented on LTSpice as Figure 5.

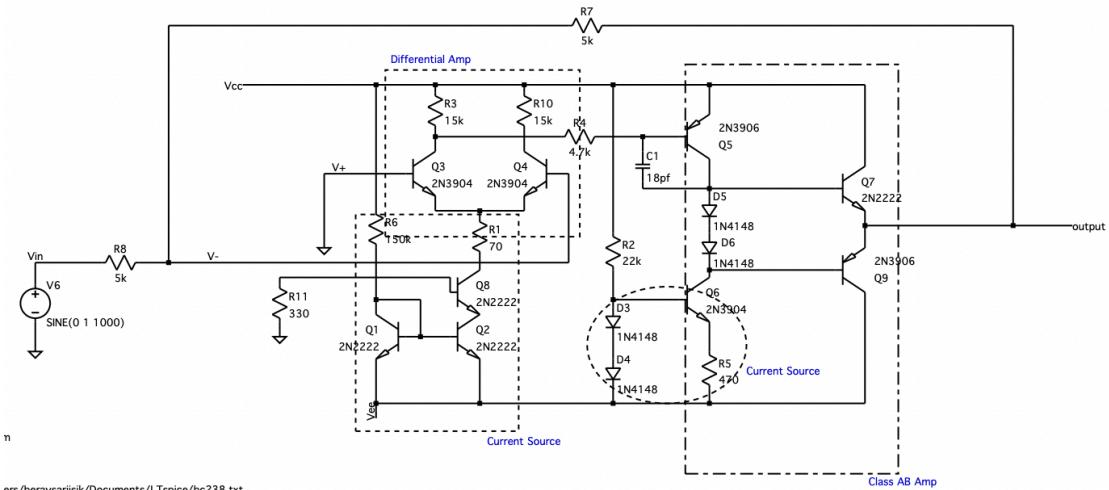


Figure 5: The Overall Circuit Diagram on LTSpice Simulation

The input voltage is given as sinusoid with 2V peak-to-peak and frequency of 1kHz. By using the implementation of the test circuit which is $R_8=R_7=5\text{k}\Omega$, the waveform of the output and input voltage is obtained (see Figure 6).

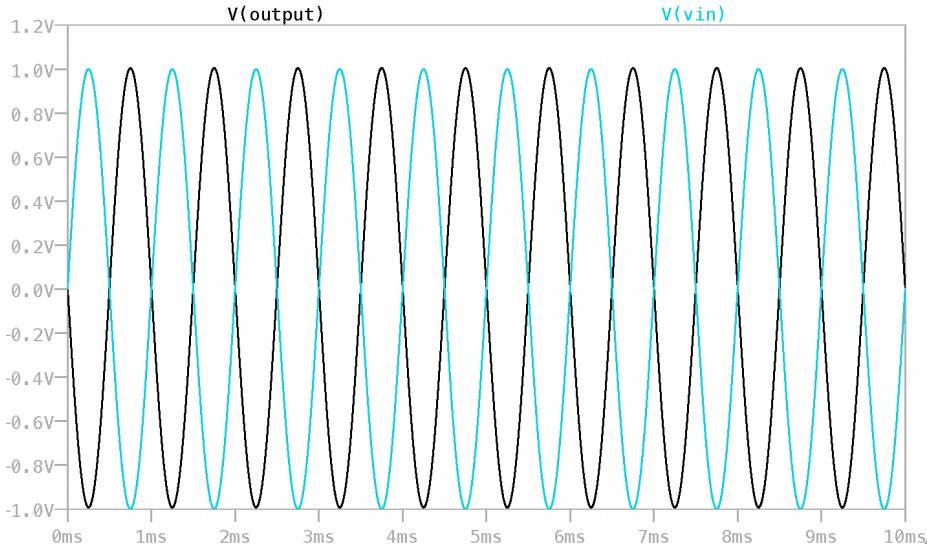


Figure 6: The Waveform of The Output and Input Voltage on LTSpice Simulation

The desired output voltage given the input voltage as sinusoid with 2V peak-to-peak and frequency of 1kHz is obtained with respect to the test circuit. As a further step, the gain of the circuit is tested by utilizing it with the resistor values which are available in lab environment. For this purpose, R7 is set as $1.2\text{M}\Omega$ and R8 is set as $1\text{k}\Omega$. The input voltage is given as sinusoid with 6mV peak-to-peak with frequency of 1kHz. The input voltage is set as very small so as to prevent the saturation after the amplification. The overall circuit for amplification is implemented on LTSpice (see Figure 7).

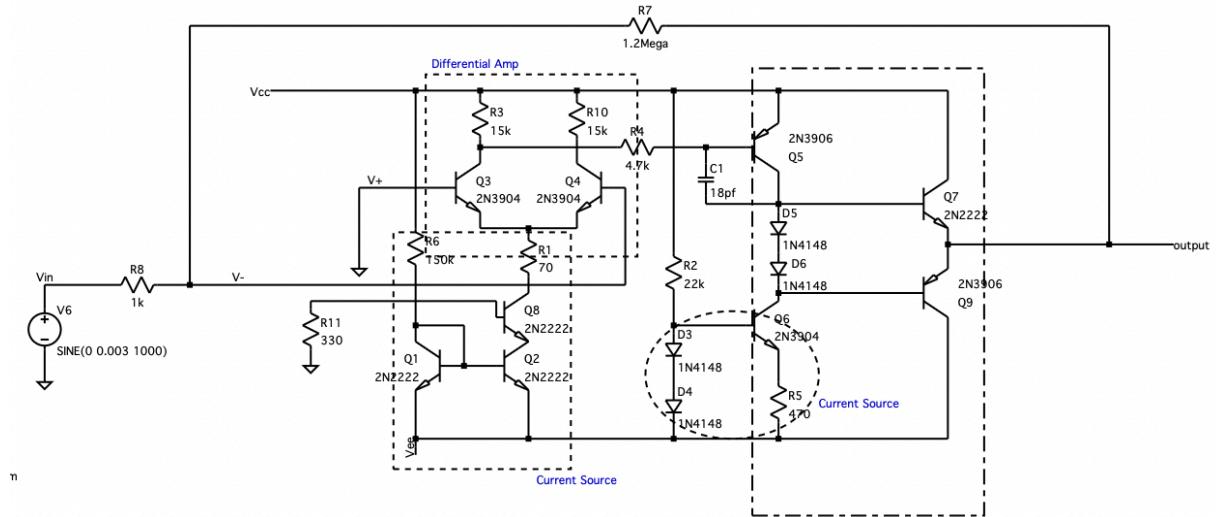


Figure 7: The Overall Circuit Diagram for Amplification on LTSpice Simulation

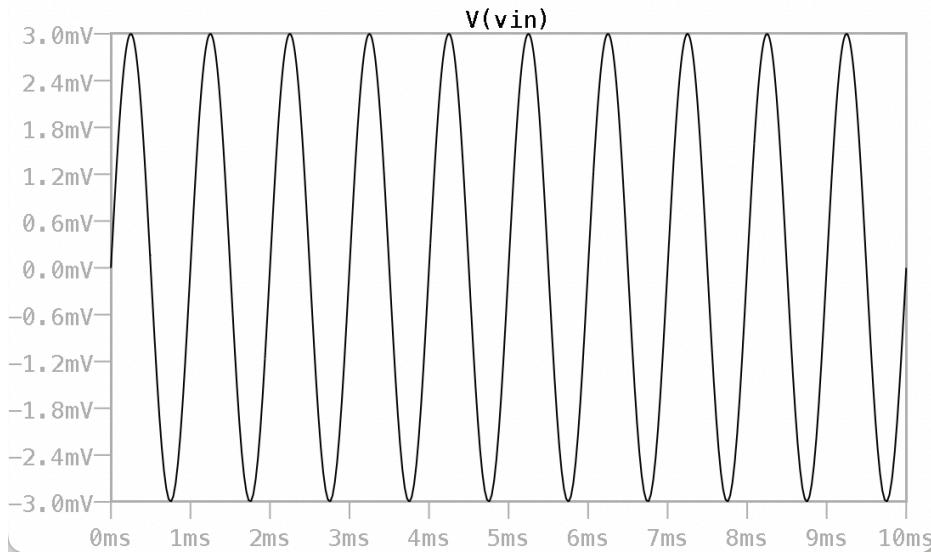


Figure 8: The Waveform of Input Voltage for Amplification on LTSpice Simulation

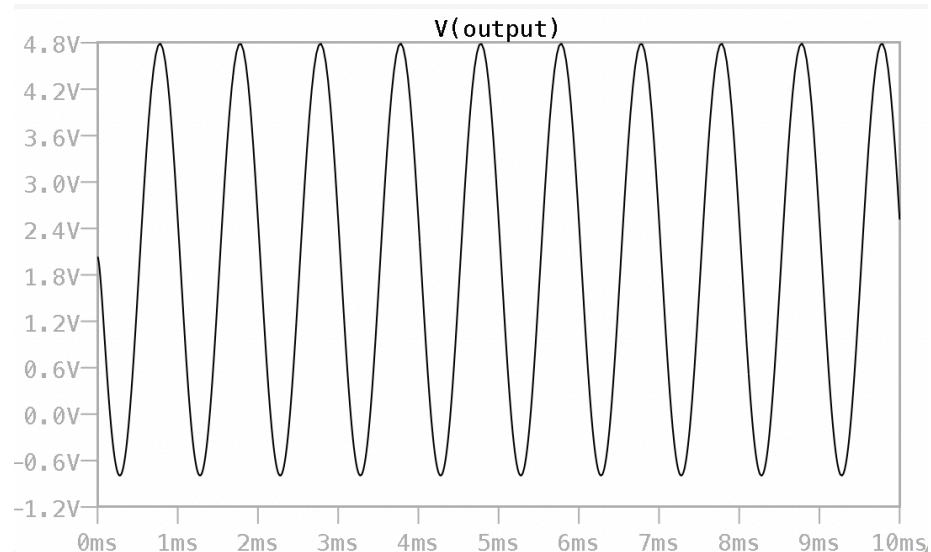


Figure 9: The Waveform of Output Voltage after Amplification on LTSpice Simulation

It is noted that the peak-to-peak voltage of the output voltage is 5.4V given the peak-to-peak voltage of input voltage as 6mV (see Figure 8 and Figure 9). The gain of the circuit is computed as 900 (see Eq. 1 and Eq. 2).

$$|Av| = \frac{V_{out}}{V_+ - V_-} \quad (Eq. 1)$$

$$\frac{V_{out}}{V_-} = \frac{5.4V}{6mV} = 900 \quad (Eq. 2)$$

The gain of the circuit which is computed as 900 satisfies the requirement of the project given in the manual that the gain of the circuit should be larger than 500.

In the last step of the simulation part, the total current per supply is investigated in order to satisfy the power requirement of the project which is provided as power consumption should

be less than 200mW can be expressed as the total current per supply should be less than 10mA.

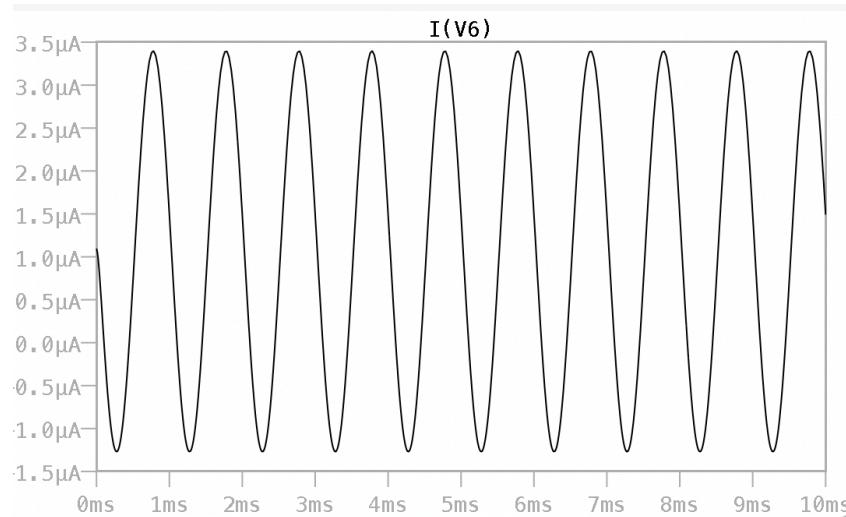


Figure 10: The Total Current Passing Through the Input Voltage

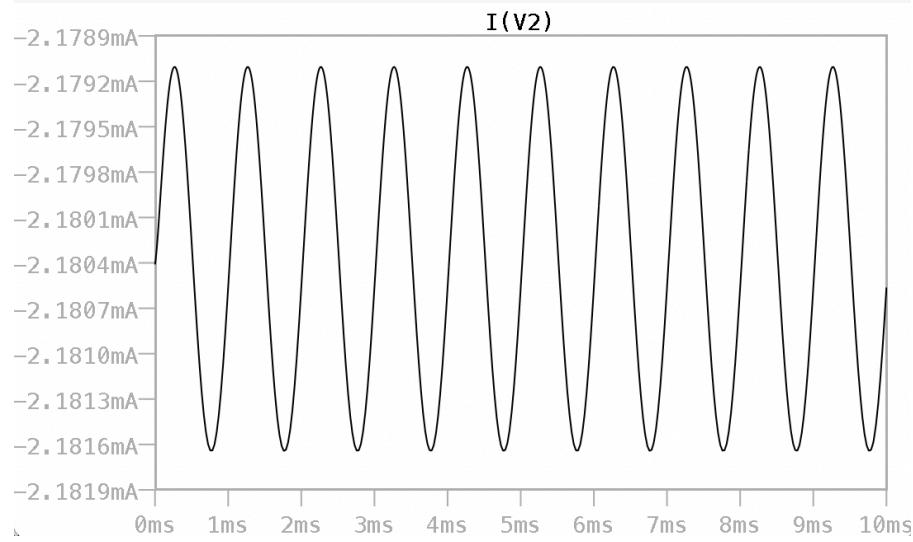


Figure 11: The Total Current Passing Through the Voltage Supplier $-V_{DD}$

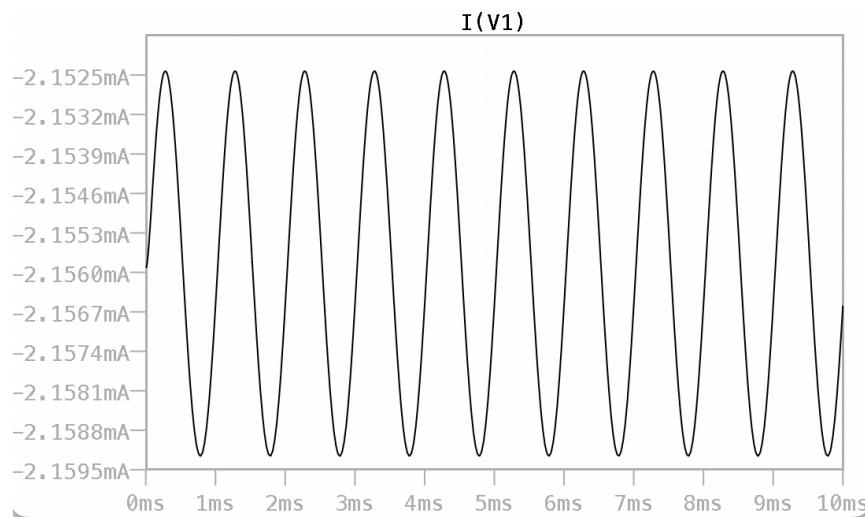


Figure 12: The Total Current Passing Through the Voltage Supplier $+V_{DD}$

It is observed that the total current per suppliers are less than 10mA which satisfies the requirement of the project (see Figure 10, Figure 11, and Figure 12).

2. Hardware Implementation and Analysis

The circuit designed in LTSpice simulation is implemented on breadboard by using the transistors NPN 2N3904, NPN 2N2222, and PNP 2N3906 which are bought from online since they are not available in lab (see Figure 13 and Figure 14).

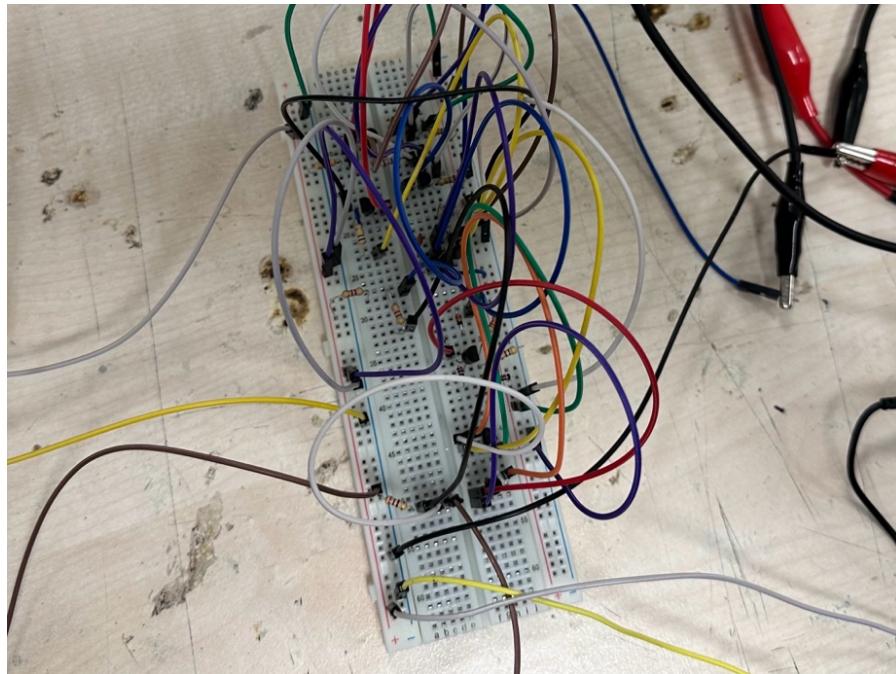


Figure 13: The Hardware Implementation of the Circuit Designed on LTSpice

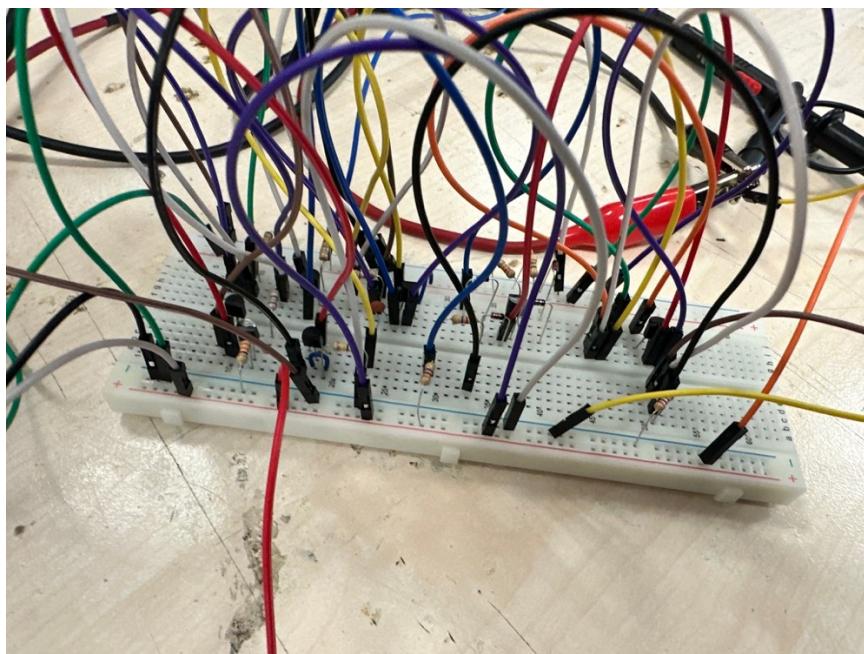


Figure 14: The Zoomed Version of the Hardware Implementation of the Circuit

The input voltage is set as sinusoid with peak-to-peak voltage 2V and frequency of 1kHz from signal generator. The output and input voltages are observed from oscilloscope as Figure 15.

The resistors R8 and R7 are set as $5\text{k}\Omega$ in order to investigate the test circuit configuration on hardware implementation.

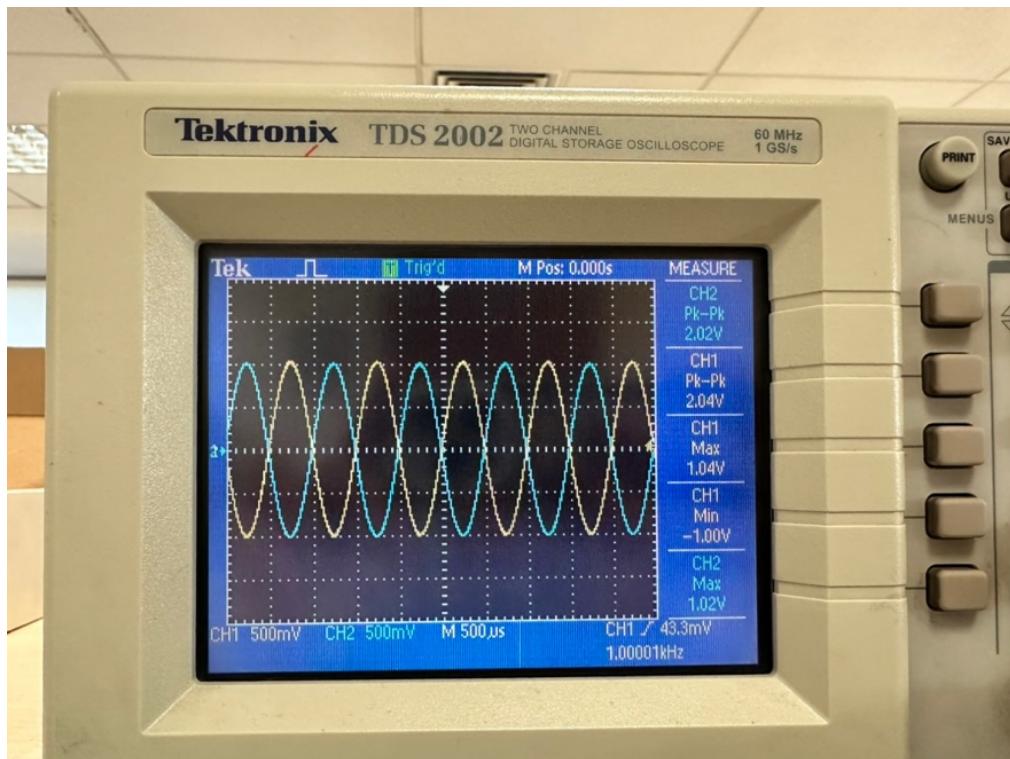


Figure 15: The Waveform of Output and Input Voltage of the Hardware Implementation

It is observed that the test circuit configuration given in Introduction part works successfully on hardware implementation. It provides a successful differential amplifier with a gain of 1 (see Figure 15).

The hardware implementation is continued with the amplification circuit designed on LTSpice simulation. However, a voltage divider circuit is utilized since the smallest input voltage from the signal generator is 10mV. The voltage divider circuit is designed with resistors $1\text{k}\Omega$ and $100\text{k}\Omega$ so as to obtain a division rate of 100 (see Figure 16). Consequently, the voltage divider circuit is properly adjusted with the overall circuit (see Figure 17).

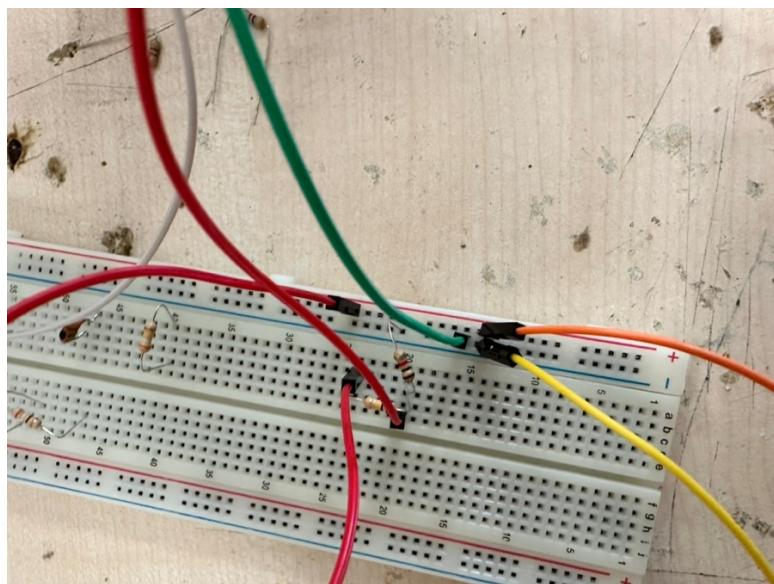


Figure 16: The Voltage Divider Circuit for Amplification on the Hardware Implementation

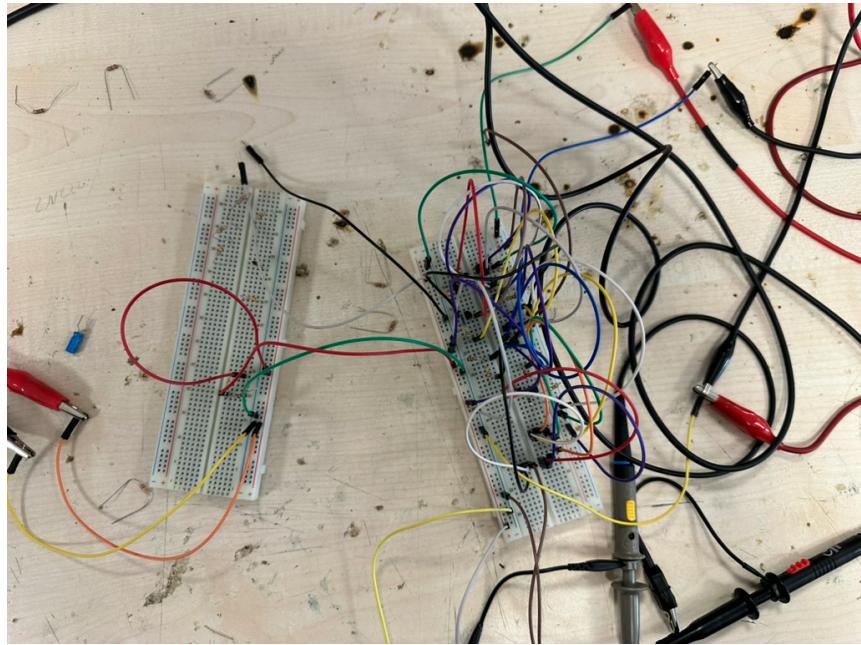


Figure 17: The Overall Circuit with Voltage Divider Circuit for Amplification on the Hardware Implementation

The signal generator is set as 0.3Vpp and 1kHz which gives a sinusoid with peak-to-peak voltage 600mV and frequency of 1kHz (see Figure 18). The DC Power Supply is set as 10V. The configuration of the suppliers can be seen from Figure 18.

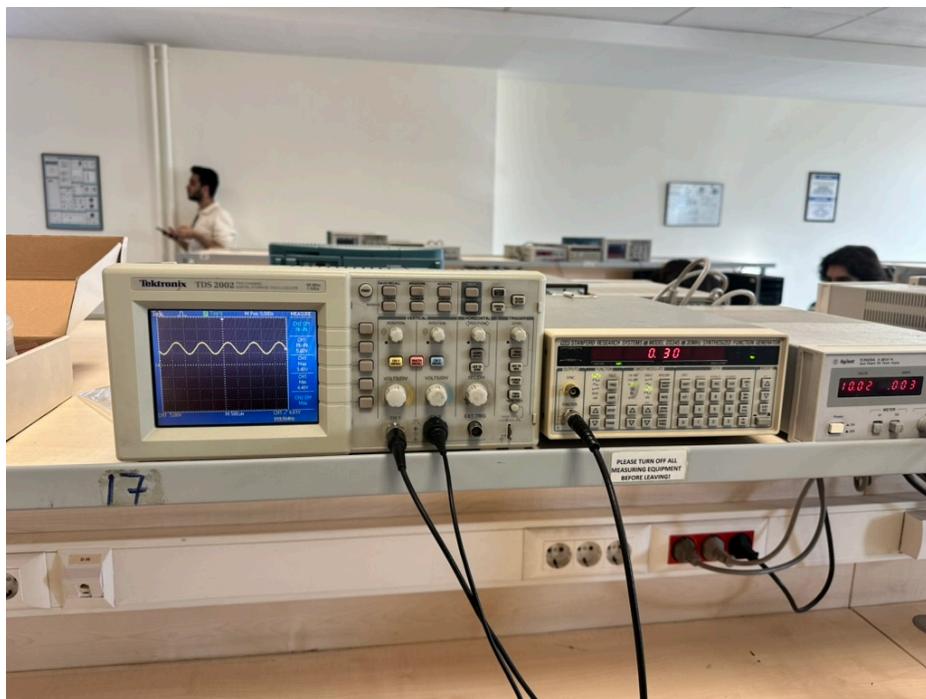


Figure 18: The Overall Supplier Configuration of the Hardware Implementation

The voltage divider circuit makes the input voltage which is supplied to the circuit as 6mV peak-to-peak voltage since it has a division rate of 100. The peak-to-peak voltage of the output voltage of the circuit is obtained 5V (see Figure 19).

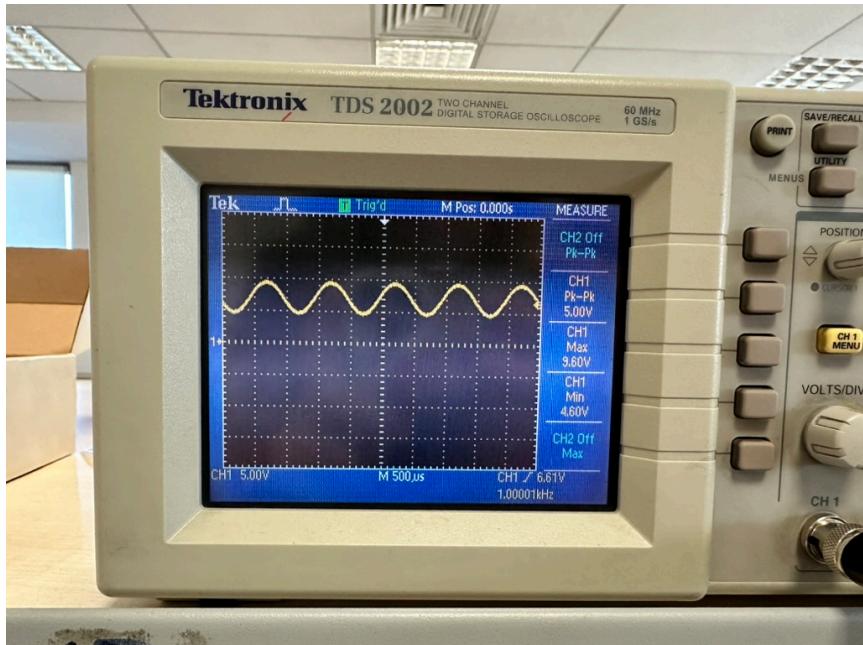


Figure 19: The Output Voltage after the Amplification on Hardware Implementation

Consequently, the gain of the circuit is obtained as 833.33, which satisfies the requirement of the project that the gain of the circuit should be greater than 500 (see Eq. 4).

$$\frac{V_{out}}{V_{in}} = \frac{5V}{6mV} = 833.33 \text{ (Eq. 4)}$$

The error percentage of the gain of the circuit is computed as 7.41% (see Eq. 5).

$$Error(\%) = \frac{|A_{v,hw} - A_{v,sim}|}{A_{v,sim}} = 7.41\% \text{ (Eq. 5)}$$

After checking the gain of the circuit, another requirement of the project that power consumption should be less than 200mW can be checked by the total current per supply should be less than 10mA is checked. It is observed by using the monitoring current on the screen of DC Power supplier that the current passing through it is 3mA which is coincides with the simulation result and less than 10mA satisfies the requirement of the project.



Figure 20: The Total Current Passing through the Power Supply

3. Conclusion

The purpose of this project is to design a simple OPAMP circuit by using differential input and single ended output and an output stage using BJTs. The requirements provided by the lab manual given in the Introduction part. Besides, it is acknowledged from the test circuit that the circuit should behave as an inverter with a gain greater than 500. Furthermore, the power consumption of the circuit should be adjusted such that it has a power consumption less than 200mW. In order to acquire the behavior of the test circuit, a differential amplifier is utilized with a current source consists of a current mirror circuit. Consequently, a Class AB Amplifier is used to prevent crossover distortion in different cycles. The final lab of the semester was beneficial for implementing a Class AB Amplifier into the circuit. By searching resources, a capacitor-compensation technique is used to improve the linearity of the circuit. These implementations are firstly done on LTSpice and the requirements are checked, which increases the efficiency of the hardware implementation.

The requirement firstly checked from the LTSpice analysis. It gives a perfect inverted signal with a gain of 900, which satisfies the requirement given by the project manual. Besides, the power consumption is considerably small than 200mW. Consequently, the circuit is implemented on breadboard using transistors NPN 2N3904, NPN 2N2222, and PNP 2N3906 are bought online due to lack of material in the lab. Firstly, the inversion operation is checked by inputting a sinusoid with peak-to-peak voltage 2V and frequency of 1kHz from signal generator. The result was successful (see Figure 15).

Secondly, the gain of the circuit is computed. Since the signal generator can supply voltages larger than 10mV, a voltage divider circuit is implemented in order to acquire an input voltage which is relatively small so that amplification does not lead any saturation in the output signal (see Figure 16 and Figure 17). After that, the gain of circuit is computed as 833.33 (see Figure 19). Therefore, the error percentage with respect to the LTSpice analysis is 7.41%. The experimental errors might have occurred due the connection problems of the jumper wires, malfunctioning of the breadboard, improper implementation of the voltage divider circuit, and transistor that are bought online. Lastly, the current per supply is checked, which gives at most 3mA. satisfying the requirement that it should be less than 10mA. Consequently, the project meets the requirements of the project manual and successfully performs an OPAMP operation.

The project may be improved by using transistors rather than resistors, whose resistance can be changed according to the current passing through it. Besides, the implementation can be done by using smaller amount of transistors which decrease the possibility of the potential experimental errors. Overall, the project was successfully done by satisfying all the requirements provided by the project manual.

References

- [1] W. Storr, "Class AB amplifier design and class AB biasing," Basic Electronics Tutorials,
<https://www.electronics-tutorials.ws/amplifier/class-ab-amplifier.html> (Accessed Jan. 2, 2024).
- [2] Chengzhou Wang, M. Vaidyanathan and L. E. Larson, "A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers," in *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 1927-1937, Nov. 2004, doi: 10.1109/JSSC.2004.835834.