Homework #2

Q1)

Do the following conversions.

Decimal	Binary	Hexadecimal
546		
128		
27.375		

Decimal	Signed 8-bit binary in 2’s complement form
-6.375	

Signed 8-bit binary in 2’s complement form	Decimal
00000011.1101	
11111111.1111	
10100110.0111	

Q2)

Calculate the binary equivalent of 127/64. If we use only 4 bits in the fraction, what is the error in the binary representation? How many bits are needed to fully represent 127/64 in signed 2’s complement binary number system? Show your work clearly.

Q3)

Perform the following binary arithmetic operations on two 8-bit signed binary numbers in 2's-complement format and indicate whether there is an overflow or not. Show the intermediate steps.

$$\begin{array}{rr} & 00111001 \\ + & 00111001 \\ \hline \end{array} \qquad \begin{array}{rr} & 11111111 \\ + & 00000001 \\ \hline \end{array}$$

$$\begin{array}{rr} & 00111001 \\ - & 00111001 \\ \hline \end{array} \qquad \begin{array}{rr} & 00000000 \\ - & 11111111 \\ \hline \end{array}$$

Q4)

Implement **F = xy + x′y′ + y′ z** using only NAND gates.

Q5)

$$\mathbf{F(x,y,z,t) = (x \oplus y)(z+t)}$$

a) Express the following function as a sum of minterms.
b) Express the following function as a product of maxterms.
c) Optimize F using Karnaugh map.

d) Assume we guarantee that xyzt will never be larger than 12. Add necessary don't care conditions and optimize F further using K-map.

Q6)

Design a combinational circuit that divides a 2-bit unsigned binary number A = (a1 a0) by another 2-bit unsigned binary number B = (b1 b0) and generates a 2-bit unsigned binary number D = (d1 d0) that gives the remainder of the division (i.e. D = A%B). Note that division-by-0 is not defined. Therefore, you can assume that the input combinations causing division-by-0 are not applied.

a_1	a_0	b_1	b_0	d_1	d_0
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

a)Derive the truth table.
b)Derive simplified boolean expressions for the outputs in sum-of-products form using K-maps.
c)Implement d0 output using NOR gates only and draw the circuit.

Q7)

Design a magnitude comparator that takes two 3-bit signed numbers in 2’s complement format, A = (a2 a1 a0) and B = (b2 b1 b0), and outputs g = 1 if A > B, otherwise g = 0. Show the boolean expression for the output g