HAFTA – 7

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1. KANONİK İFADE

F = B'D' + A'BD + AD' + A'BC'

2. GRUPLANDIRMALAR

Gruplar: (m0, m4, m12, m8), (m0, m8, m2, m10), (m5, m7), (m12, m8, m14, m10), (m4, m5).

3. MAXTERMLER

F = PRODUCT(M1, M3, M6, M9, M11, M13, M15)

4. POS GÖSTERİMİ

F = (A+B+C+D')(A+B+C'+D')(A+B'+C'+D)(A'+B'+C+D')(A'+B'+C'+D')(A'+B+C+D')(A'+B+C'+D')

5. MINTERMLER

f= SUM (m0, m2, m4, m5, m7, m8, m10, m12, m14)

6. SOP GÖSTERİMİ

F = A'B'C'D' + A'BC'D' + ABC'D'+ AB'C'D'+ A'BC'D + A'BCD + A'B'CD' + ABCD' + AB'CD'

7. MODÜL KODLARI

a. Expression Modülü

```
module exp (x_e,a,b,c,d);
input a,b,c,d;
output x_e;
wire not_a,not_b,not_c,not_d;
wire w_1,w_2,w_3,w_4;
not(not_a,a);
not(not_b,b);
not(not_c,c);
not(not_d,d);
and(w_1,not_b,not_d);
and(w_2,not_a,b,d);
and(w_3,a,not_d);
and(w_4,not_a,b,not_c);
or(x_e,w_1,w_2,w_3,w_4);
endmodule
```

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b. SOP Modülü

```
module sop(x_out,a,b,c,d);
input a,b,c,d;
output x_out;
wire w_1,w_2,w_3,w_4,w_5,w_6,w_7,w_8,w_9;
wire not_a,not_b,not_c,not_d;
not (not_a, a);
not (not_b, b);
not (not_c, c);
not (not_d, d);
and(w_1, not_a,not_b,not_c,not_d);
and(w_2, not_a,b,not_c,not_d);
and(w_3, a,b,not_c,not_d);
and(w_4, a,not_b,not_c,not_d);
and(w_5, not_a,b,not_c,d);
and(w_6, not_a,b,c,d);
and(w_7, not_a,not_b,c,not_d);
and(w_8, a,b,c,not_d);
and(w_9, a,not_b,c,not_d);
or (x_out,w_1,w_2,w_3,w_4,w_5,w_6,w_7,w_8,w_9);
endmodule
```

c. POS Modülü

```
module pos(x_out,a,b,c,d);
input a,b,c,d;
output x_out;
wire w_1,w_2,w_3,w_4,w_5,w_6,w_7;
wire not_a,not_b,not_c,not_d;
not (not_a, a);
not (not_b, b);
not (not_c, c);
not (not_d, d);
or(w_1,a,b,c,not_d);
or(w_2,a,b,not_c,not_d);
or(w_3,a,not_b,not_c,d);
or(w_4,not_a,not_b,c,not_d);
or(w_5,not_a,not_b,not_c,not_d);
or(w_6,not_a,b,c,not_d);
or(w_7,not_a,b,not_c,not_d);
and(x_out,w_1,w_2,w_3,w_4,w_5,w_6,w_7);
endmodule
```

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d. Testbench

```
module tb();
reg a,b,c,d;
wire x_e, x_s,x_p;
exp exp1(x_e, a, b, c, d);
sop sop1(x_s, a, b, c, d);
pos pos1(x_p, a, b, c, d);
initial
begin
#100

a=1'b0;
b=1'b0;
c=1'b0;
d=1'b0;

#100

a=1'b0;
b=1'b0;
c=1'b0;
d=1'b1;

#100

a=1'b0;
b=1'b0;
c=1'b1;
d=1'b0;

#100

a=1'b0;
b=1'b0;
c=1'b1;
d=1'b1;

#100

a=1'b0;
b=1'b1;
c=1'b0;
d=1'b0;

#100

a=1'b0;
b=1'b1;
c=1'b0;
d=1'b1;

#100

a=1'b0;
b=1'b1;
c=1'b1;
d=1'b0;

#100

a=1'b0;
b=1'b1;
c=1'b1;
d=1'b1;

#100

a=1'b1;
b=1'b0;
c=1'b0;
d=1'b0;

#100

a=1'b1;
b=1'b0;
c=1'b0;
d=1'b1;

#100

a=1'b1;
b=1'b0;
c=1'b1;
d=1'b0;

#100

a=1'b1;
b=1'b0;
c=1'b1;
d=1'b1;

#100

a=1'b1;
b=1'b1;
c=1'b0;
d=1'b0;

#100

a=1'b1;
b=1'b1;
c=1'b0;
d=1'b1;

#100

a=1'b1;
b=1'b1;
c=1'b1;
d=1'b0;

#100

a=1'b1;
b=1'b1;
c=1'b1;
d=1'b1;
        end
endmodule
```

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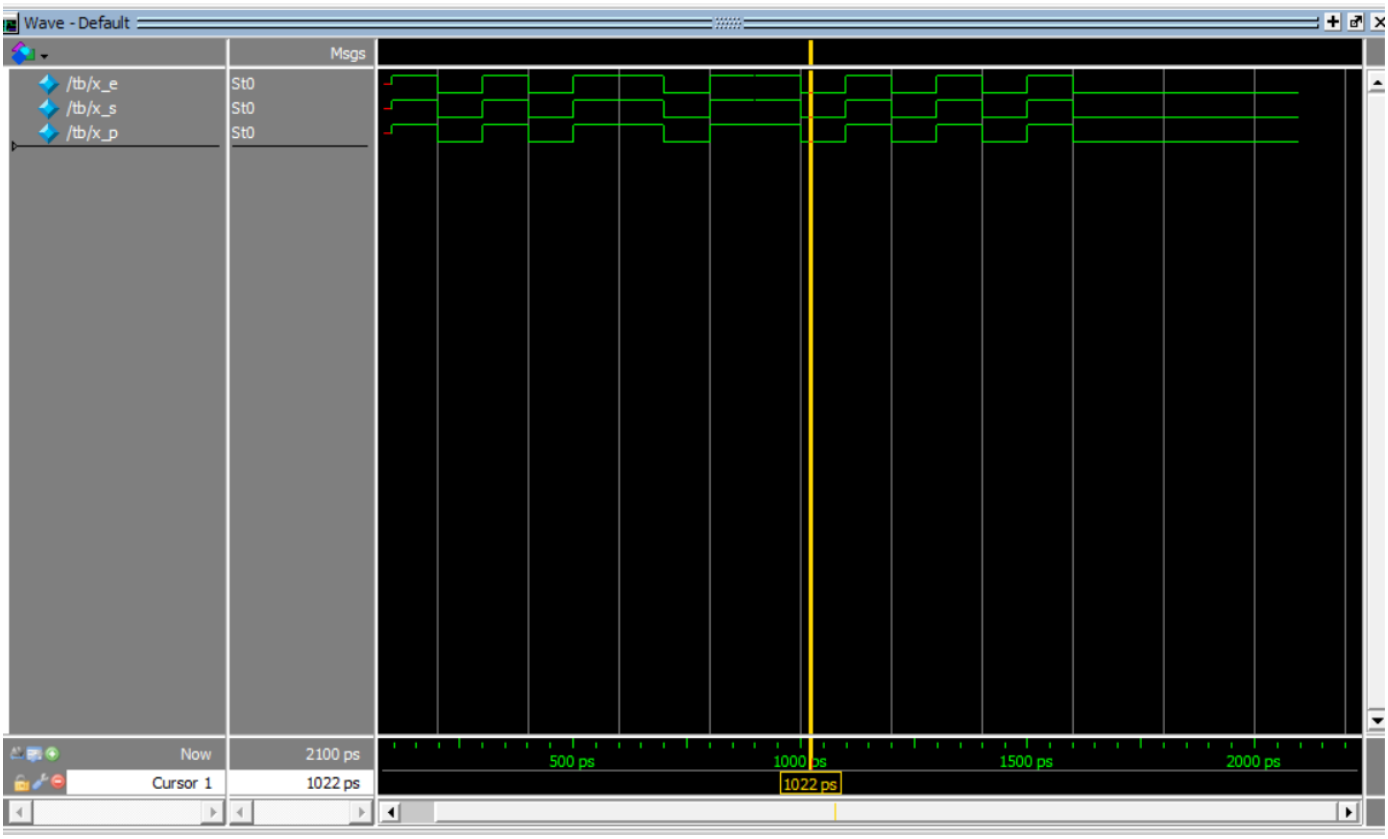
8. MODELSİM SİMÜLASYONU



Farklı giriş kombinasyonları için çıkışlar aynı sinyalleri vermektedir.