1. SUM OF PRODUCTS

X = A’B + ABC + CD’

A'B = A'B(C+C')(D+D') = A'BCD + A'BCD^+ A'BC'D + A'BC'D'

ABC = ABC(D+D') = ABCD + ABCD'

CD' = CD'(A+A')(B+B') = ABCD' + AB'CD' + A'BCD' + A'B'CD'

***X = A'BCD + A'BCD' + A'BC'D + A'BC'D' + ABCD + ABCD' + AB'CD' + A'B'CD'***

1. İFADENİN GENİŞLETİLMEMİŞ HALİNİN VERİLOG HDL KODU

module lab5 (x\_e, a, b, c, d);

input a,b,c,d;

output x\_e;

wire not\_a, not\_d;

wire w\_1, w\_2, w\_3;

not (not\_a, a);

not (not\_d, d);

and (w\_1, not\_a, b);

and (w\_2, a, b, c);

and (w\_3, c, not\_d);

or (x\_e, w\_1, w\_2, w\_3);

endmodule

1. İFADENİN GENİŞLETİLMİŞ HALİNİN VERİLOG HDL KODU

module lab5gen (x\_s, a, b, c, d);

input a,b,c,d;

output x\_s;

wire not\_a, not\_b, not\_c, not\_d;

wire w\_1, w\_2, w\_3, w\_4, w\_5, w\_6, w\_7, w\_8;

not (not\_a, a);

not (not\_b, b);

not (not\_c, c);

not (not\_d, d);

and(w\_1, not\_a,b,c,d);

and(w\_2, not\_a,b,c,not\_d);

and(w\_3, not\_a,b,not\_c,d);

and(w\_4, not\_a,b,not\_c,not\_d);

and(w\_5, a,b,c,d);

and(w\_6, a,b,c,not\_d);

and(w\_7, a,not\_b,c,not\_d);

and(w\_8, not\_a,not\_b,c,not\_d);

or(x\_s, w\_1, w\_2, w\_3, w\_4,w\_5,w\_6,w\_7,w\_8);

endmodule