Middle East Technical University
Department of Electrical and Electronics Engineering

EE464: Static Power Conversion II
Term Project Simulation Report

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Submission Date: 21.04.2024

Introduction

The aim of this project, like the previous semester, is to design a battery charger; however, the difference is that the project should utilize an isolated DC-DC type converter. The design should decrease the DC input voltage to 12V to charge the battery connected to the output by strictly using a closed loop control system. Project specifications are available at the project GitHub repository.

In this report, the candidate isolated DC-DC converter topologies for battery charging are discussed, and the corresponding calculations and simulation results regarding the selected topology are displayed. Then, using these results, the components that will be used in the hardware design are chosen. Finally, some measurements related to the initial transformer design gathered after the tests done during the laboratory is presented.

This project is still ongoing and evolving.

Topology Selection

To control the output current and voltage while achieving high efficiency in this project, a proper isolated DC-DC converter topology should be selected. In this section, several isolated converter topologies are considered and compared to select the most suitable one.

- ***Flyback Converter:*** This topology is one of the simplest designs that can be used in order to design an isolated DC-DC converter. It is advantageous due to uncomplicated design procedure since it only utilizes a single active switch. Moreover, a lower number of components are needed compared to the other types of topologies for this converter. A lower number of components makes sure that the design is cost effective compared to the other types of topologies which is an important advantage of this topology. Also, flyback converter is generally a good choice for low power applications [1] which is smaller than 200W as it is the case for this project.

  Apart from several handy advantages, there are multiple disadvantages of this topology as it single-ended type converter which means that it operates at a single quadrant of the BH curve. Also, it charges and discharges the inductors at different switching cycles, a gapped core is essential to increase the energy storage capacity. Thus, the main disadvantage can be poor transformer utilization. Moreover, due to high ripple currents at the input and output sides stemming from low inductance of the gapped core, larger capacitors should be utilized which is also a disadvantage for this topology.

- ***Forward Converter:*** This converter is mainly used for medium power applications in practice. One of the best advantages compared to the flyback is that the energy does not need to be stored as it is transferred in at the same cycle that is created. Thus, the magnetic core can be gapless, and the transformer utilization is better [2]. Using a gapless converter reduces the current ripple; thus, efficiency can be increased, and smaller rating components can be used which will probably lead to more compact design compared to the flyback converter.

The drawbacks compared to the flyback converter can be the increased cost as it uses an extra diode and an inductor, which is an important issue for low-budget projects. Moreover, as the energy is transferred for the same cycle, magnetizing current should be reset before the nest switching cycle which limits the maximum duty to 50%. If the transformer is not properly designed and controlled, higher duty cycle than 50% will lead to saturation of the core which makes a sensitive control system a must for this topology. Also, in the practical design, a third winding is added to protect the circuit from the leakage inductance effects. However, due to this winding, voltage across the primary switch is increased which results in higher voltage stress across the switch which is an important disadvantage which needs to be handled.

- ***Push-pull Converter:*** The main application area consists of higher power applications since the power is distributed and handled by two active switches. Also, this topology differs from the previous two as it is double-sided which implies that the transformer is operating at two quadrants of the magnetic core which results in better utilization of the transformer. Therefore, this is a good choice for high power applications due to high efficiency.

  However, due to the increased number of active switches, the total cost of this topology is fairly high compared to the other two. Also, control of these two active switches is more complex since the dead time should be arranged properly in order not to short circuit the source at the input. Moreover, a center-tapped transformer is used in this topology; thus, overall, the design procedure, when two active switches and transformer design is considered, is more complex. Finally, when two switches are off, voltage stress across the two switches is still quite high, which may cause problems when the switch is not properly selected and cause heating problems as well as increased losses due to possible high on resistances.

- ***Half-bridge and Full-bridge Converters:*** These two topologies are also used for high power applications, generally higher than push-pull converters. The advantage of these two compared to the push-pull converter is that the voltage stress across the switches is decreased. Moreover, these are also double sided; however, they have single primary winding which makes sure that the transformer is utilized better compared to the push-pull converter [2].

  The disadvantage of these topologies is that half-bridge cost is slightly more than the push-pull converter. For the full-bridge converter, the cost is considerably higher as it includes 4 active switches which also complexes the design and the controllers. These topologies become an overdesign for low power applications.

  When all the topologies are considered, for low power application which is the case for this project, push-pull, half-bridge and low-bridge converters are found to be overcomplicated for this specific application. Also, as the cost and complexity are important points for this project, flyback converter topology is found to be applicable and sufficient. In the nest section, a flyback converter will be designed and presented.

Validation of Design

1. General design

For this project, as explained in the previous section, a flyback converter has been selected. The general topology schematic is given below. In order to avoid sudden current changes due to the leakage inductance, an RCD snubber design is added to ensure the safety of the design and the switch.

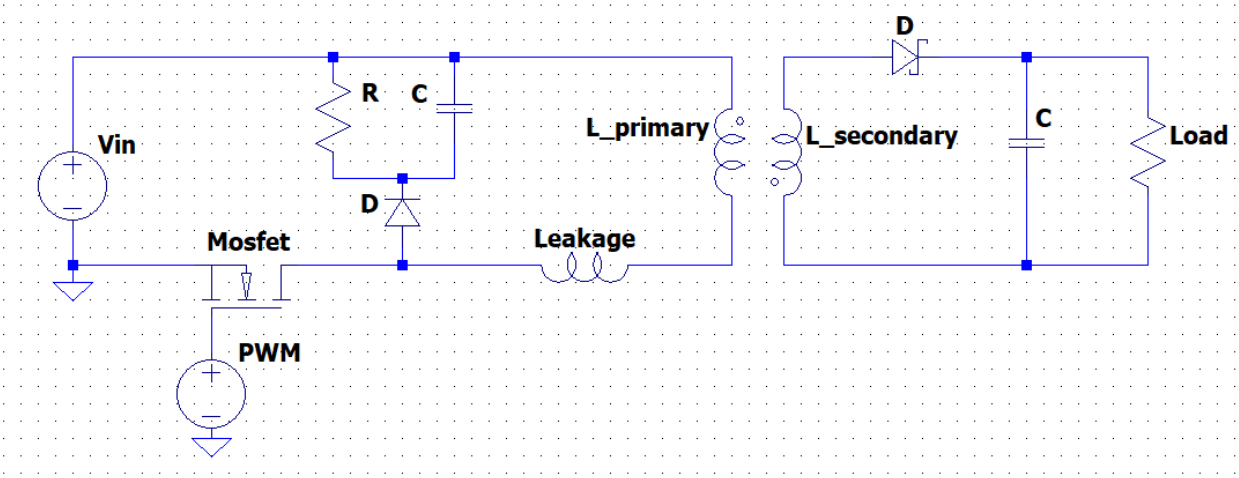

Figure 1. Flyback Topology Schematic

As the closed loop control is mandatory for the project, a controller needs to be used to ensure the voltage is 12V continuously. For this reason, an analog controller will be utilized. Due to the low side MOSFET, driver circuitry will be simpler and there will be no need for a bootstrap circuit, only a MOSFET driver will be utilized as it is the case for the previous semester's design. To ensure the isolation boundary is preserved, an optocoupler is used for the closed loop control. In the following section, analytical calculations for the transformer design and RCD snubber design will be presented.

2. Analytical calculations

- ***Magnetic Design Calculations***

To start with the magnetic design of the topology, duty cycle should be decided to calculate the corresponding turns ratio. In flyback converters, duty cycle can obtain values between zero and one. However large duty cycle values do not assure a good performance. If the input voltage is low, which implies a high duty cycle, conduction losses will increase due to increased conduction time. Moreover, for a poorly designed transformer, large duty values may result in core saturation due to decreased allocation time for the flux reduction inside the core. Both situations decrease the efficiency of the converter which is unwanted. Thus, maximum duty cycle is selected as 0.5 for this design. When the maximum duty cycle is selected, maximum turns ratio can be calculated using the following formula below. The important point in this calculation is that output voltage is taken as 13V to consider the voltage drop across the output diode and to stay within the predefined duty cycle limits. For ease of manufacturing and

simplicity, turns ratio is selected as 1. For the selected turns ratio, duty cycle for both input voltages are calculated below.

$$\frac{N_1}{N_2} \leq \frac{Vin * D}{(Vout + 1) * (1 - D)}$$

$$\frac{N_1}{N_2} \leq \frac{20 * 0.5}{13 * (1 - 0.5)} \cong 1.54\ turns$$

$$D = \frac{1}{\left(\frac{V_{in}}{V_{out} + 1} + 1\right)}$$

$$D_{max} = \frac{1}{(\frac{20}{13} + 1)} = 0.393 \cong 0.4\ \ \&\ \ D_{min} = \frac{1}{\left(\frac{40}{13} + 1\right)} = 0.245$$

Table 1. Selected turns ratio and calculated duty cycles.

Turns Ratio (N1/N2)	1
Duty Cycle Range	0 to 0.5
Maximum Duty Cycle	0.393
Minimum Duty Cycle	0.245

At this point, a target efficiency should be selected in order to move on to further parameter calculation. Target efficiency is selected as:

$$\eta_{target} = 0.8$$

After determining the efficiency target, input power can be calculated:

$$P_{in} = \frac{P_{out}}{\eta_{target}} = \frac{60W}{0.8} = 75W$$

Knowing the limits of the duty cycles, the average current flowing on the magnetizing inductance during on period when the input voltage is in its low limit can be calculated as [3]:

$$I_{EDC} = \frac{P_{in}}{V_{in,min} \cdot D_{max}} = \frac{75W}{20V \cdot 0.4} = 9.375A$$

At this point, another design decision should be given which is the value for K_{RF}, which denotes "current ripple factor".

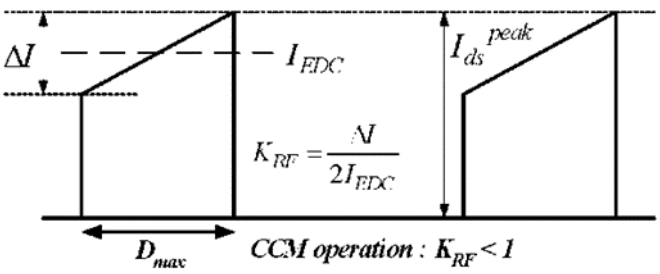

Figure 2. Current ripple factor

Here, the current ripple factor is selected as $K_{RF} = 0.33$ which is within the reasonable limit as stated in the design document. Thus, the current ripple is calculated as below.

$$\Delta I = 2 \cdot K_{RF} \cdot I_{EDC} = 2 \cdot 0.33 \cdot 9.375 = 6.1875A$$

Then:

$$I_{EDC,max} = 9.375 + \frac{6.1875}{2} = 12.47A \cong 12.5A$$
$$I_{EDC,min} = 9.375 - \frac{6.1875}{2} = 6.28A \cong 6.3A$$

This shows that the peak current on the inductor and hence the MOSFET is approximately $12.5A$.

As the minimum primary inductor voltage, the switching frequency, the duty cycle at the minimum voltage and current ripple are known, the inductance of the primary inductor can be easily calculated using the inductor equation:

$$V_L = L \cdot \frac{di}{dt}$$

Considering the on period, the same equation can be converted to the equation below. Assuming a higher current ripple factor for the higher value of the input voltage, the same equation can be written as:

$$V_L = L \cdot \frac{\Delta i}{D \cdot T_s} \rightarrow L_{min} = \frac{V_L \cdot D \cdot T_s}{\Delta i} = \frac{V_{in,max} \cdot D_{min}}{f_{sw} \cdot \Delta i} = \frac{40V \cdot 0.245}{100kHz \cdot 6.1875A} = 19.79\mu H$$

Leaving a safety margin which will in fact lower the voltage ripples on the magnetizing inductance, the primary inductance of the transformer is selected as:

$$L_m = 20\mu H$$

At this point, the core material is decided. In order to increase the energy storage capacity for the flyback converter, the core should have an airgap. After some research, the core found is "B66363G0500X187" which is an N87 type ETD39 ferrite core from TDK Electronics. It has a built-in 0.5mm airgap so that when two of them are used, a total of 1mm airgap will be obtained. Datasheet of the core provides some valuable information considering the airgaps:

$$A_L = \frac{196nH}{T^2} \;\&\; \mu_r = 115 \;\&\; I_e = 92.2mm$$

To find the number of turns in the primary side:

$$20\mu H = \frac{196nH}{T^2} \cdot N^2 \rightarrow N = 10.1\ Turns$$

The turn number is required as an integer and considering the safety left at the inductance value, the turn number selection is made as:

$$N = 11\ Turns \rightarrow L_m = 23.71\mu H$$

As the turns ratio is selected as 1, the secondary side will have the same number of turns.

Then, to find the magnetic flux density (B) inside the core, the magnetic field intensity is found using Ampere's Circuital Law:

$$N \cdot I_{max} = H_{max} \cdot \int dL \rightarrow 11 \cdot 12.5A = H_{max} \cdot 92 \cdot 10^{-3}m$$

$$H_{max} = 1490.50 \frac{A}{m}$$

Then:

$$B_{max} = \mu_0 \cdot \mu_r \cdot H_{max} = 4\pi \cdot 10^{-7} \cdot 115 \cdot 1355.75 \frac{A}{m} = 0.215T$$

Considering the information given in the datasheet of N87 materials by TDK Electronics, the found value is far away from the saturation of the core, which is given approximately as $0.4T$.

Considering the operating frequency of $80kHz$, the cable is selected as "AWG26" since it offers an operating frequency of $107kHz$ for maximum skin depth. To be able to calculate the number of parallelled conductors, the RMS value of the current flowing through the transformer should be found. RMS value for a triangular wave with an offset can be calculated using the formula given below [4].

$$I_{RMS} = I_{EDC} * \sqrt{1 + \frac{1}{12} * \left(\frac{\Delta I}{I_{EDC}}\right)^2}$$

$$I_{RMS} = 9.375 * \sqrt{1 + \frac{1}{12} * \left(\frac{6.1875}{9.375}\right)^2} \cong 9.54A$$

The AWG26 cable can carry $0.361 \frac{A}{conductor}$ so that the number of conductors that should be wound together is as follows.

$$\frac{9.54}{0.361} \cong 26.44 \rightarrow 27 \; will \; be \; used$$

One AWG26 cable has a conductor cross section of $0.128\ mm^2$ but considering the isolation on them, this value will be taken as $0.14\ mm^2$ for more realistic calculations. Assuming same number of conductors will be used for both the primary and secondary sides, the total area that will be occupied by the conductors can be calculated as:

$$2 \cdot 0.14mm^2 \cdot 27 \cdot 10 = 75.6\ mm^2$$

TDK Electronics recommends coil formers B66364B1016T001 or B66364W1016T001 to be used with the selected core which offer $178mm^2$ of window area.

This results in a fill factor of:

$$Fill\ Factor = \frac{75.6\ mm^2}{178\ mm^2} \cong 0.42$$

which is a reasonable value.

In the table of AWG cables, the resistance of the AWG26 cable is given as $\frac{133.8568\Omega}{1000m}$. The mean path length of the coil formers is given as $69mm$. For the primary or the secondary side, the total DC resistance can be calculated as:

$$R_{DC} = 10 \cdot 69 \cdot 10^{-3}m \cdot \frac{133.8568\Omega}{1000m} \cdot \frac{1}{20} = 4.618 \cdot 10^{-3}\Omega$$

The AC resistance can be calculated as follows:

$$R_{AC} = \frac{\rho \cdot l}{A_{eff}} \;\&\; A_{eff} = \delta \cdot \pi \cdot d \;\&\; \delta = \sqrt{\frac{\rho}{\pi \cdot f \cdot \mu}}$$

$$\delta = \sqrt{\frac{1.678 \cdot 10^{-8}}{\pi \cdot 80 \cdot 10^{3} \cdot 4\pi \cdot 10^{-7} \cdot 0.999991}} = 230.5 \cdot 10^{-6}m$$

Since the skin depth is larger than the actual cross section of the cable, effective area is taken as the cable's cross section area assuming that the current will flow uniformly.

$$A_{eff} = 230.5 \cdot 10^{-6}m \cdot \pi \cdot 0.40386 \cdot 10^{-3}m = 292.45 \cdot 10^{-9}m^2$$

$$R_{AC} = \frac{1.678 \cdot 10^{-8} \cdot 10 \cdot 69 \cdot 10^{-3}}{0.128 * 10^{-6}} \cdot \frac{1}{20} = 4.52 * 10^{-3}\Omega$$

It can be seen that the AC and DC resistances of AWG26 cable at the specified frequency is almost same. It is expected that AC resistance should be higher than the DC resistance, which is not the case, and this will probably stem from the given resistance multiplier in the datasheet for the DC resistance.

The total copper loss can be calculated as:

$$P_{cu} = 2 \cdot I_{DS,RMS}^2 \cdot R_{DC} = 2 \cdot 9.54^2 \cdot 4.687 \cdot 10^{-3} = 0.85W$$

As stated before, the core material is N87. Reading the datasheet of the "N87 SIFERRIT Material", the core loss values for some frequency and Tesla values can be found. In the datasheet, the core loss for $80kHz$ and $200mT$ at $100°C$ is given approximately as $280\ \frac{kW}{m^3}$. The datasheet of the B66363G0500X187 core states that the volume of a core is $11500mm^3$. Then:

$$P_{core} = 280\frac{kW}{m^3} \cdot 11500 \cdot 10^{-9}mm^3 = 3.22W$$

The total loss of the transformer can be estimated as:

$$P_{loss} = P_{core} + P_{cu} = 3.22W + 0.85W = 4.07W$$

The design does not require new iterations as the values are in acceptable limits, and most importantly the cores are found in a distributor in Turkey, who can bring them with all the additional materials in 10 days maximum.

- ***RCD Snubber Design Calculations***

For the RCD snubber design, a handbook is found from Fairchild [5]. A proper RCD snubber should be utilized in order to avoid the devastating effect of leakage inductance. Snubber values are calculated below using the formulas presented in the handbook.

$$R_{sb} = \frac{V_{sb}^2 * (V_{sb} - nV_o)}{0.5 * L_{leakage} * I_{peak}^2 * V_{sb} * f_s}$$

$$C_{sb} = \frac{V_{sb}}{R_{sn} * \Delta V_{sb} * f_s}$$

These values should be obtained using simulation software. Simulation results will be presented in the following part; however, using the values obtained from the simulation, snubber values can be calculated using the given formulas above. The calculations are presented below.

$$R_{sb} = \frac{30^2 * (30 - 12)}{0.5 * 0.25 * 10^{-6} * 11.5^2 * 30 * 80 * 10^3} = 408\ \Omega$$

$$C_{sb} = \frac{30}{408 * 2.9 * 80 * 10^3} = 317\ nF$$

In the following section, using the analytical calculations, simulations results will be presented in order to validate the design.

3. Simulation Results and Validation

Open-Loop Simulation

To be able to validate the various design decisions taken, an open-loop simulation is created as the first step. The simulation is run for input voltages of 20V and 40V separately, and the results will be presented separately also. The circuit schematic can be seen in Figure 3.

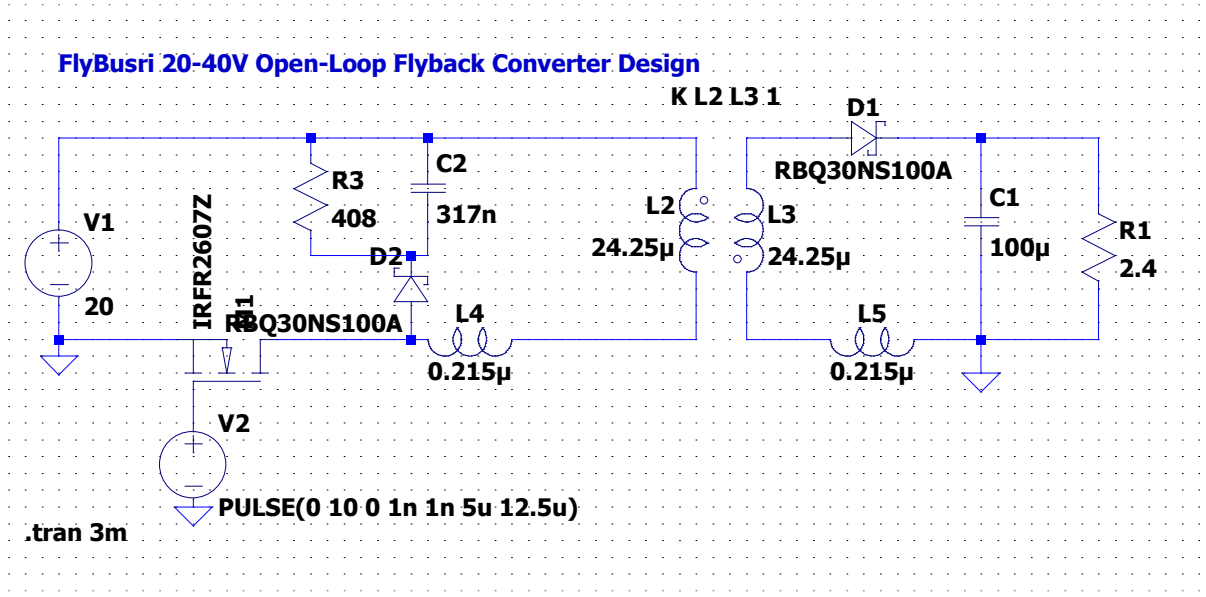

Figure 3. Circuit Schematic of the Open-Loop Flyback Converter

First of all, the input voltage is set as 20V and the duty cycle is set as 0.4. It should be noted that all of the measurements are taken in the steady state, and with the tools of LTSpice.

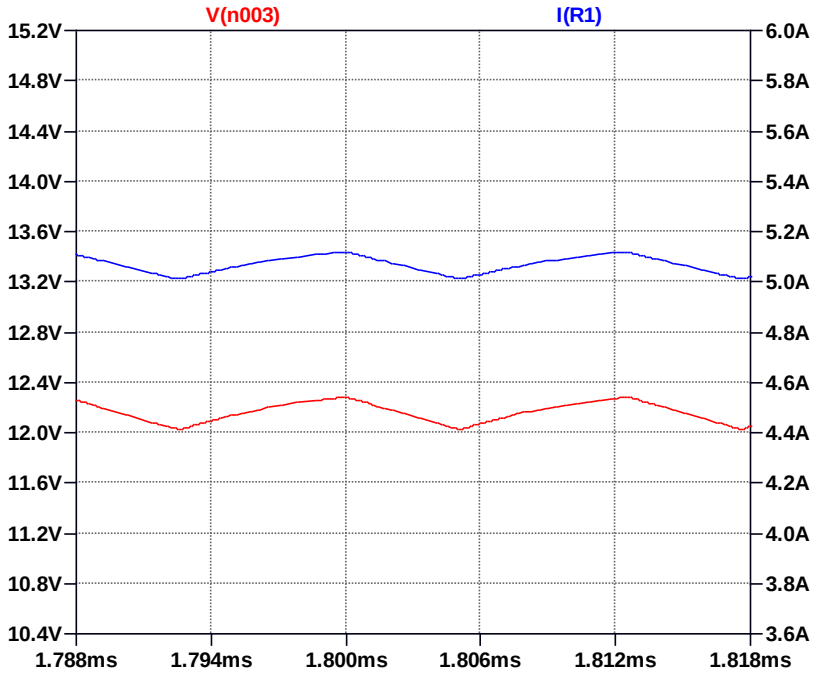

Figure 4. Output Voltage and Current Measurements for Vin = 20V

The average output voltage is measured as 12.141V, and the average output current is measured as 5.059A which results in an average output power of 61.398W. The average input power is measured as 75.738W which results in an efficiency of 0.811.

The ripple on the output voltage is equal to 249.85mV at steady state which results in an output voltage regulation of 2.06%.

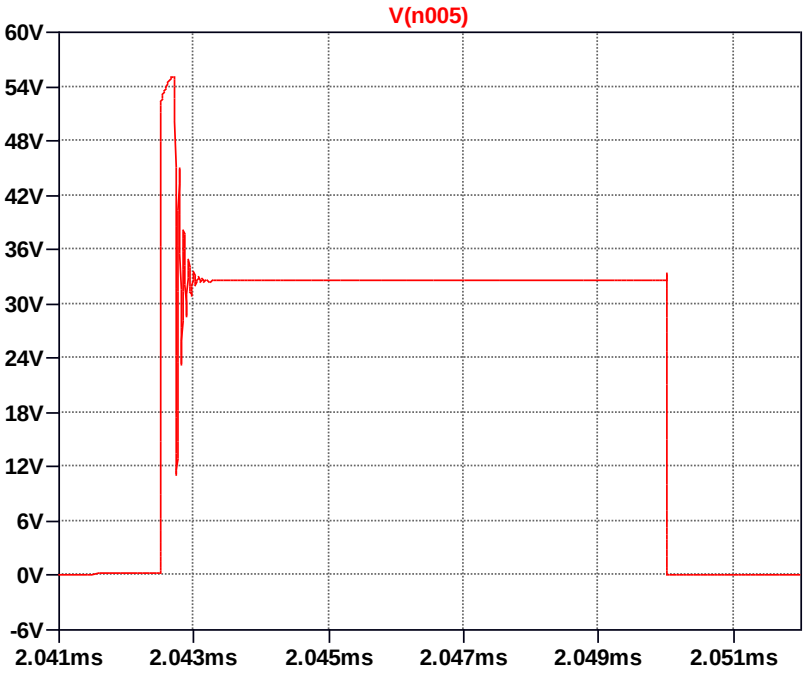

Figure 5. Vds Measurements on the MOSFET for Vin = 20V

The maximum voltage measured on the MOSFET is 55.2V at the steady state. During startup, the voltage on the MOSFET increases to 90V for an instance.

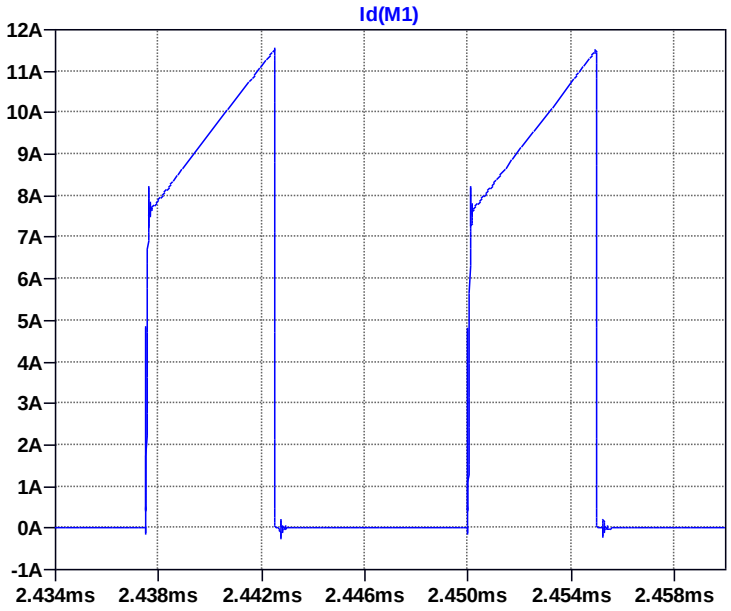

Figure 7. Ids Measurements on the MOSFET for Vin = 20V

The current on the MOSFET increases to 11.51A from 7.63A during the ON period. During startup, the current on the MOSFET increases to 27A for an instance. These maximum values of current and voltage on the MOSFET are considered when the components are chosen.

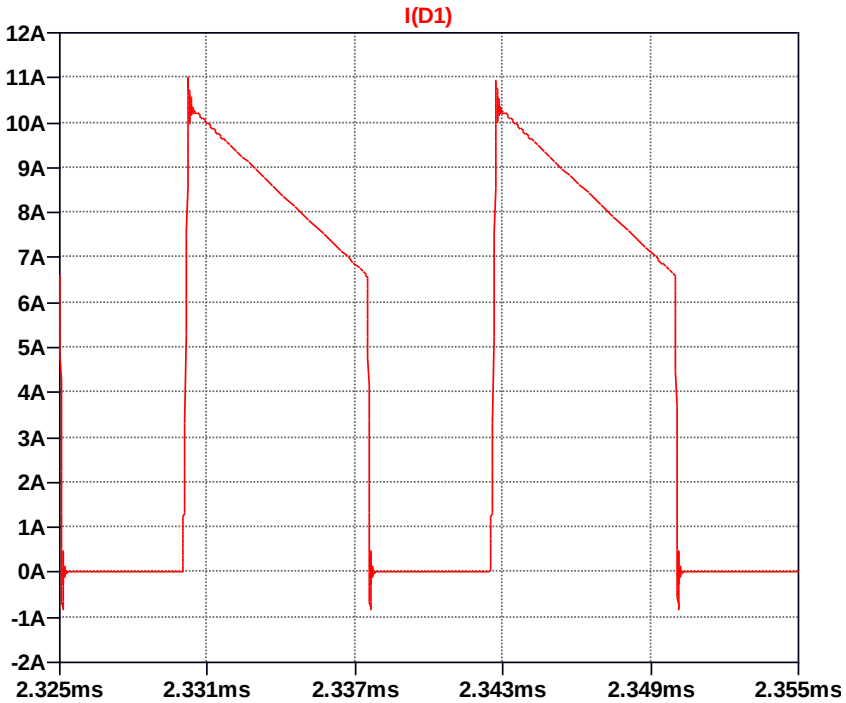

Figure 6. Forward Current on the Output Diode for Vin = 20V

The current on the output diode decreases to 6.64A from 10.95A during a cycle. During startup, the current on the output diode reaches 27A for an instance.

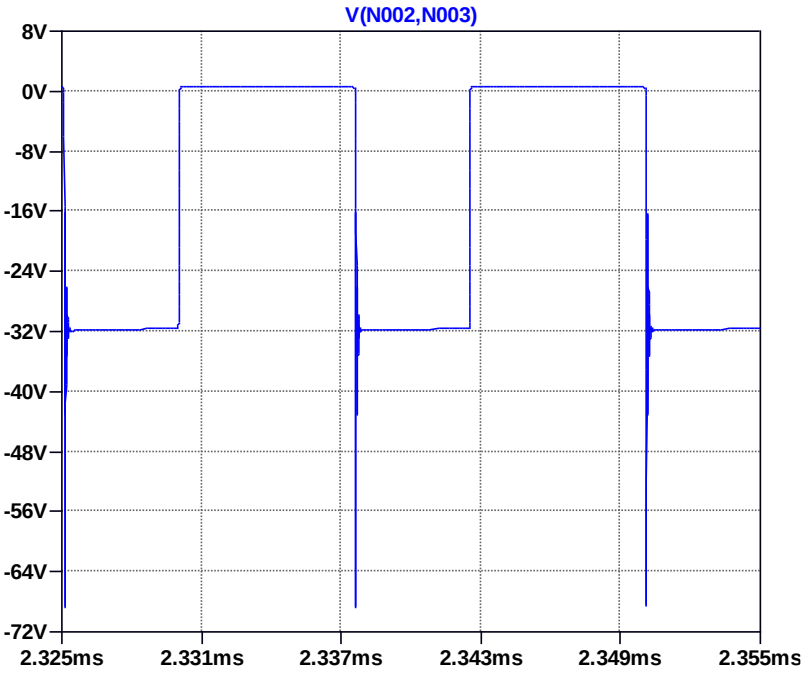

Figure 8. Voltage on the Output Diode for Vin = 20V

The output diode should be able to stand a reverse voltage of 68.54V. During startup, this value reaches up to 79V. These maximum values of current and voltage on the output diode are considered when the components are chosen.

Then, the input voltage is set to 40V and the duty cycle is set as 0.245.

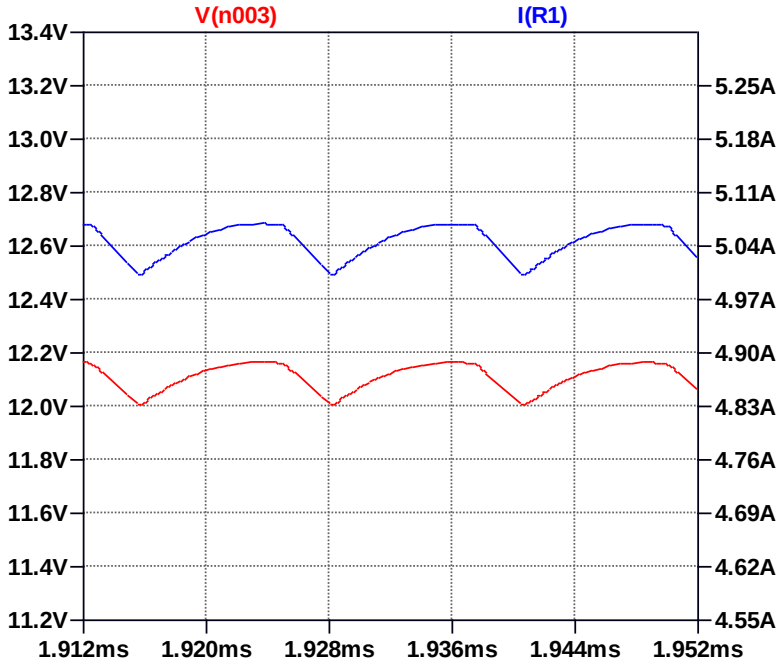

Figure 9. Output Voltage and Current Measurements for Vin = 40V

The average output voltage is measured as 12.101V, and the average output current is measured as 5.042A which results in an average output power of 60.994W. The average input power is measured as 81.95W which results in an efficiency of 0.744.

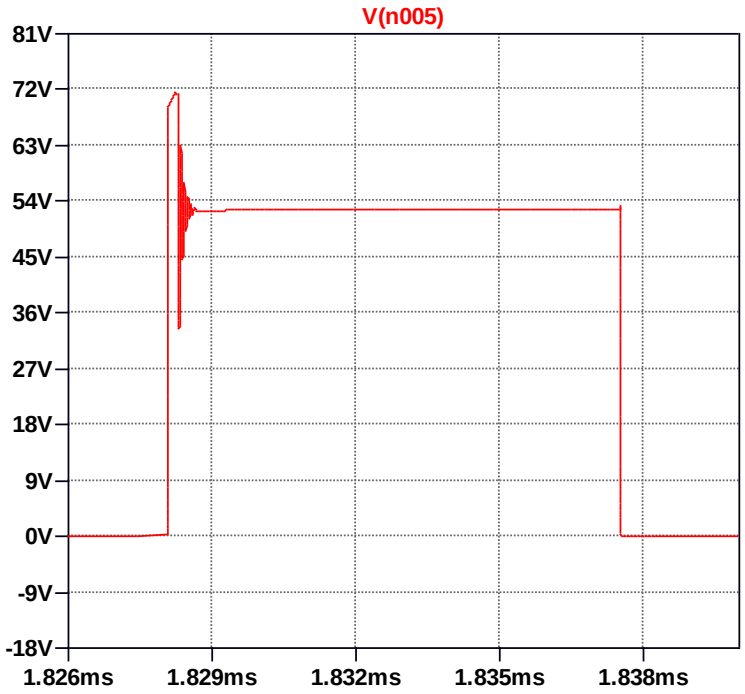

Figure 10. Vds Measurements on the MOSFET for Vin = 40V

The ripple on the output voltage is equal to 161.26mV at steady state which results in an output voltage regulation of 1.33%.

The maximum voltage measured on the MOSFET is 71.3V at the steady state. During startup, the voltage on the MOSFET increases to 107V for an instance.

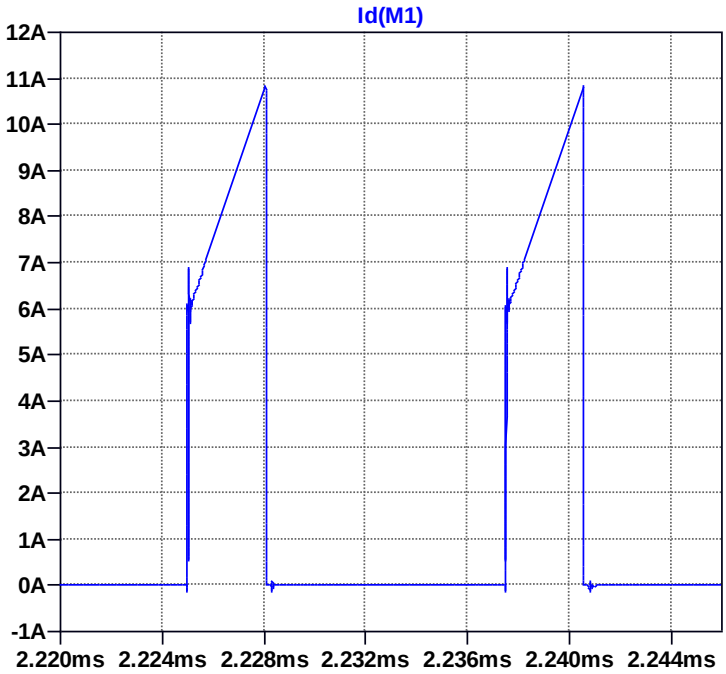

Figure 11. Ids Measurements on the MOSFET for Vin = 40V

The current on the MOSFET increases to 10.86A from 6.16A during the ON period. During startup, the current on the MOSFET increases to 27A for an instance. These maximum values of current and voltage on the MOSFET are considered when the components are chosen.

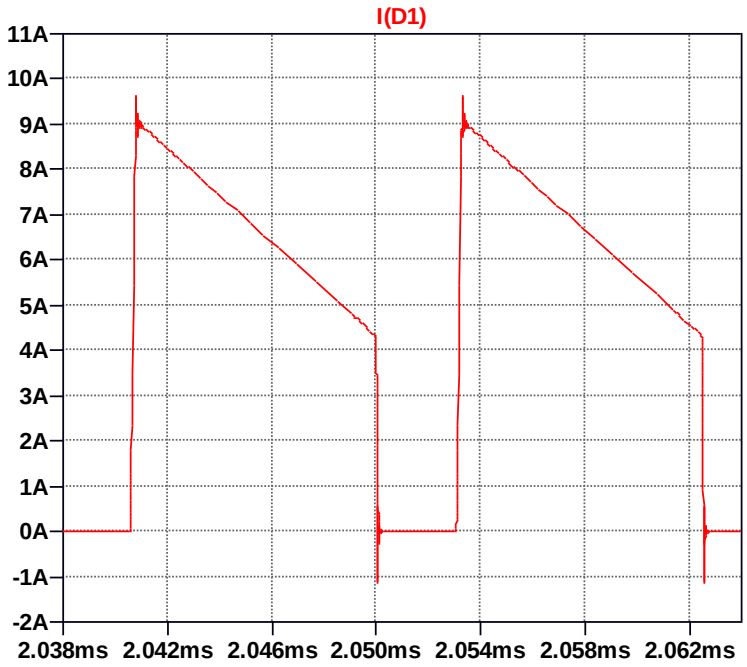

Figure 12. Forward Current on the Output Diode for Vin = 40V

The current on the output diode decreases to 4.36A from 9.32A during a cycle. During startup, the current on the output diode reaches 27A for an instance.

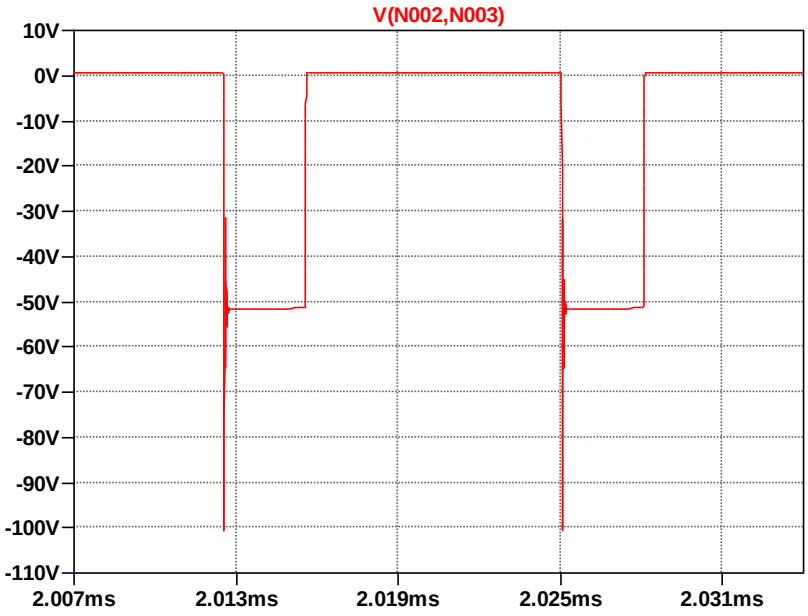

Figure 13. Voltage on the Output Diode for Vin = 40V

The output diode should be able to stand a reverse voltage of 100.59V. During startup, this value reaches up to 101V. These maximum values of current and voltage on the output diode are considered when the components are chosen.

The open-loop simulation is a good first step towards the design process, but a closed-loop simulation should be implemented for a better visualization of the real-world design.

Closed-Loop Simulation

For a real-world application, a closed-loop system should be designed so that the system can respond to changes in the input and regulate a better output even if the output load changes also.

It was stated that the bonus for using an analog IC is aimed so that a closed-loop design using an analog IC is generated. For the design, the "WEBENCH Power Designer" tool from the Texas Instruments. From many options generated, the one that uses UC3845 Analog IC is selected as the mentioned IC can be found easily in Turkey, and it fits the design considerations. Another advantage of the circuit is that by changing some of the feedback resistances, the output voltage can be regulated easily, if there is a need for that.

The reference design obtained from the tool can be seen in Figure 14.

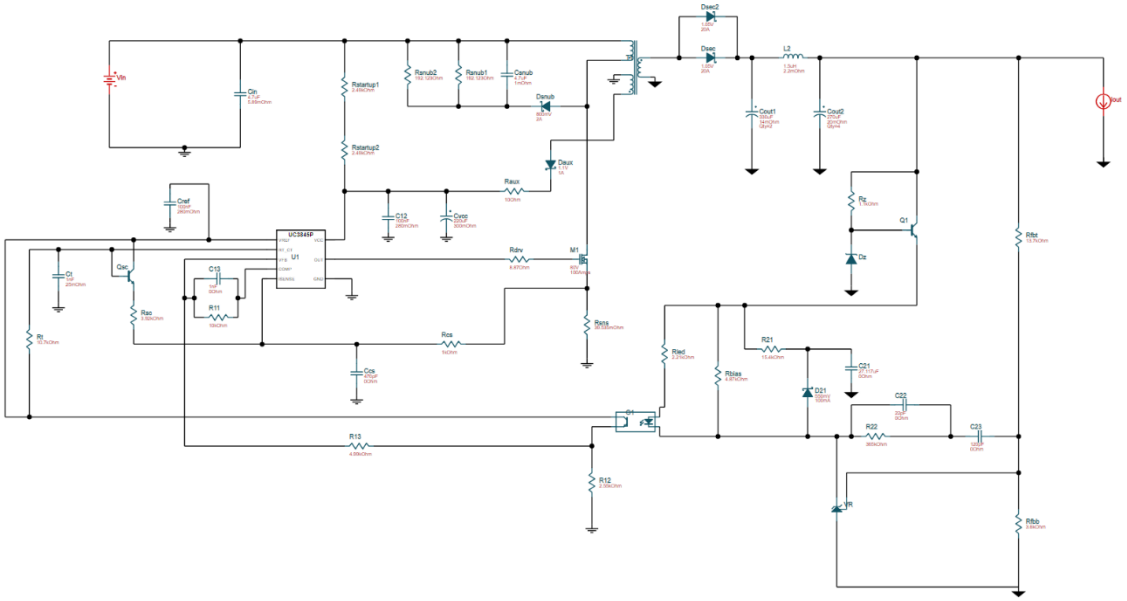

Figure 14. Reference Design of the Flyback Converter with a UC3845 IC

Then, the design is generated in LTSpice for simulations. During the generation of the circuit, the startup resistors and the auxiliary winding are not included, as we will be powering up the

UC3845 with an LM2596 directly from the input. It is tested that the LM2506 can work in the input voltage range of 20-40V, and it can supply the required voltage and current to UC3845.

The schematic of the circuit can be seen in Figure 15.

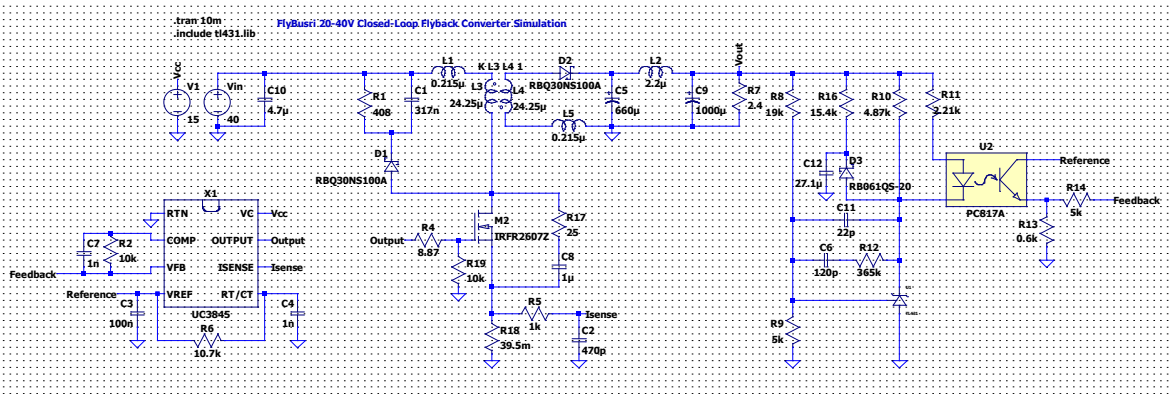

Figure 15. Closed-Loop Circuit Schematic using an UC3845 IC

The simulation consists of the isolated output voltage feedback loop, the RCD clamp, the RC snubber for the switch, output LC filter, and leakage inductances to be able to generate a circuit as close as possible to a real-life application.

The isolated feedback is obtained using an optocoupler. The feedback is generated with reference to a TL431. The feedback signal generated is sent back to the UC3845 IC.

The RCD clamp is used to decrease the voltage stress on the switching MOSFET. Also, an RC snubber is placed in parallel with the MOSFET to decrease the ringing effect.

The output LC filter helps the circuit to obtain an output which has less ripple on it.

The circuit will be operated both in inputs of 20V and 40V, and the results will be presented.

First, the input voltage is set to 20V.

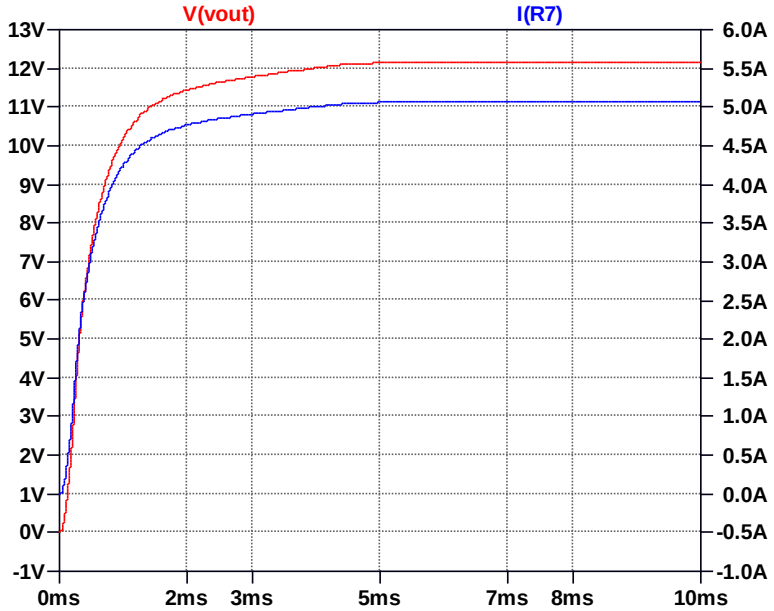

Figure 16. Output Current and Voltage Measurements of the Closed-Loop Circuit for Vin = 20V

Figure 16 represents the output current and voltage of the flyback converter. The response reaches a steady state approximately at 6 milliseconds. It can be seen that the responses include very low ripple at the steady state. The average output current at the steady state is measured as 5.065A and the average output voltage at the steady state is measured as 12.157V. The maximum and minimum values that the output voltage oscillate between are 12.164V and 12.150V respectively. This results in an output voltage regulation of 0.11%. It can be said that the result is in a safe margin as in a real-life application, many non-idealities will be disturbing the circuit, and the results may differ from an ideal scenario. The average input power is 80.695W while the average output power is 61.579W which results in an efficiency of 0.763.

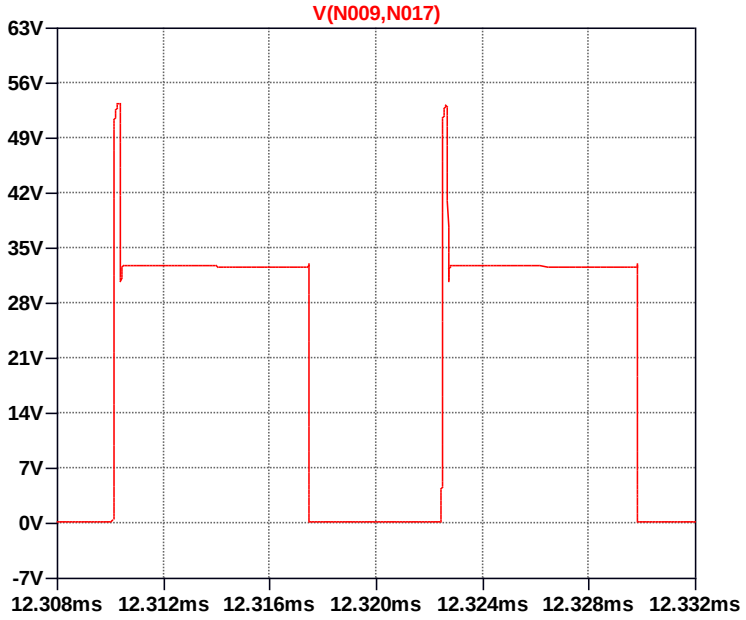

Figure 17. Vds Measurements on the MOSFET for Vin = 20V

The maximum voltage measured on the MOSFET is 53.2V at the steady state. During startup, the voltage on the MOSFET increases to 117V for an instance.

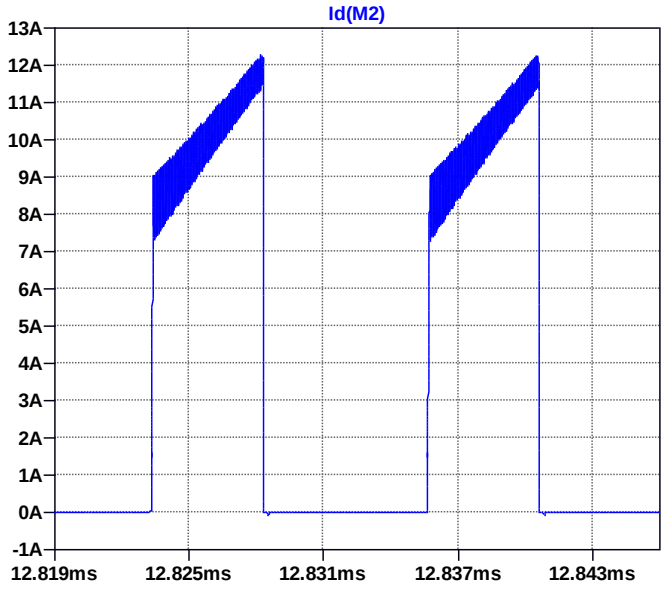

Figure 18. Ids Measurements on the MOSFET for Vin = 20V

The current on the MOSFET increases to 12.28A from 9.012A during the ON period. During startup, the current on the MOSFET increases to 52.8A for an instance. These maximum values of current and voltage on the MOSFET are considered when the components are chosen.

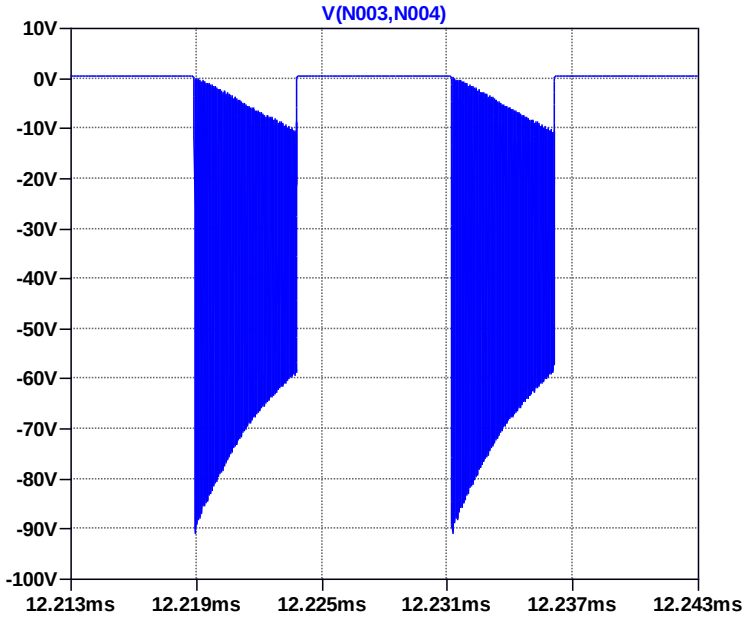

Figure 19. Voltage on the Output Diode for Vin = 20V

The output diode should be able to stand a reverse voltage of 90V. The ringing on it does not induce a power loss as no current passes through it.

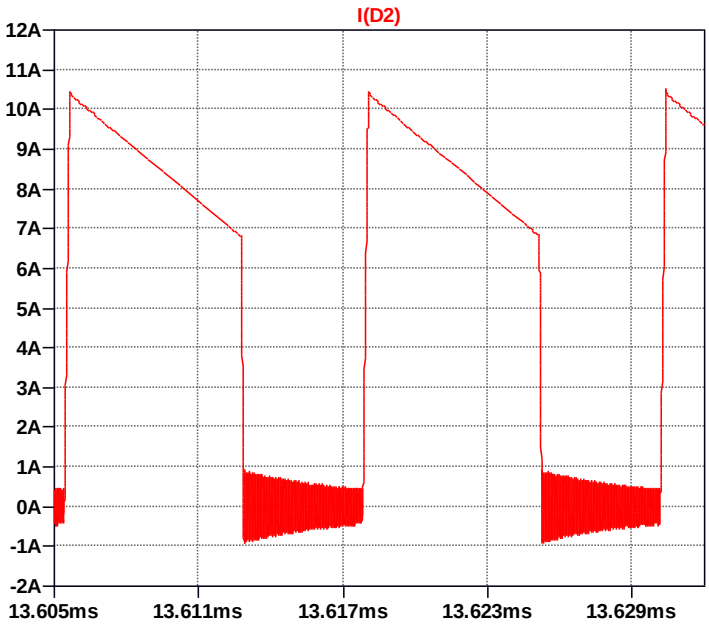

Figure 20. Forward Current on the Output Diode for Vin = 20V

The current on the output diode decreases to 6.81A from 10.39A during a cycle. These maximum values of current and voltage on the output diode are considered when the components are chosen.

Then, the input voltage is set to 40V.

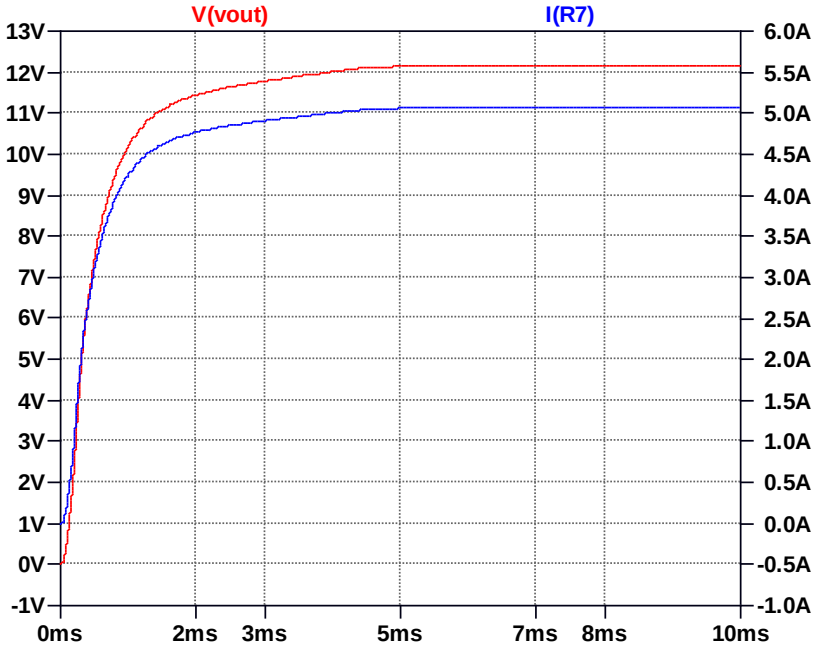

Figure 21. Output Current and Voltage Measurements of the Closed-Loop Circuit for Vin = 40V

Figure 21 represents the output current and voltage of the flyback converter. The response reaches a steady state approximately at 6 milliseconds. It can be seen that the responses include very low ripple at the steady state. The average output current at the steady state is measured as 5.185A and the average output voltage at the steady state is measured as 12.444V. The maximum and minimum values that the output voltage oscillate between are 12.45V and 12.438V respectively. This results in an output voltage regulation of 0.10%. It can be said that the result is in a safe margin as in a real-life application, many non-idealities will be disturbing the circuit, and the results may differ from an ideal scenario. The average input power is 90.603W while the average output power is 64.511W which results in an efficiency of 0.712.

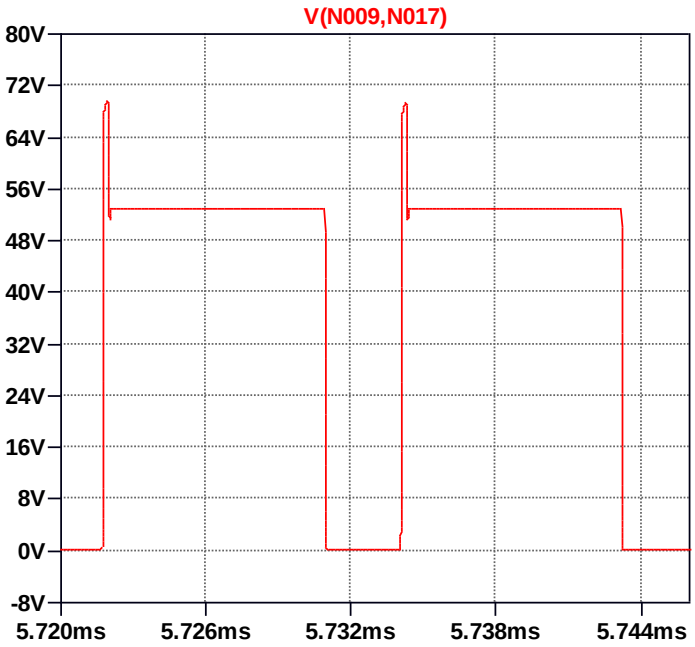

Figure 22. Vds Measurements on the MOSFET for Vin = 40V

The maximum voltage measured on the MOSFET is 69.5V at the steady state. During startup, the voltage on the MOSFET increases to 124V for an instance.

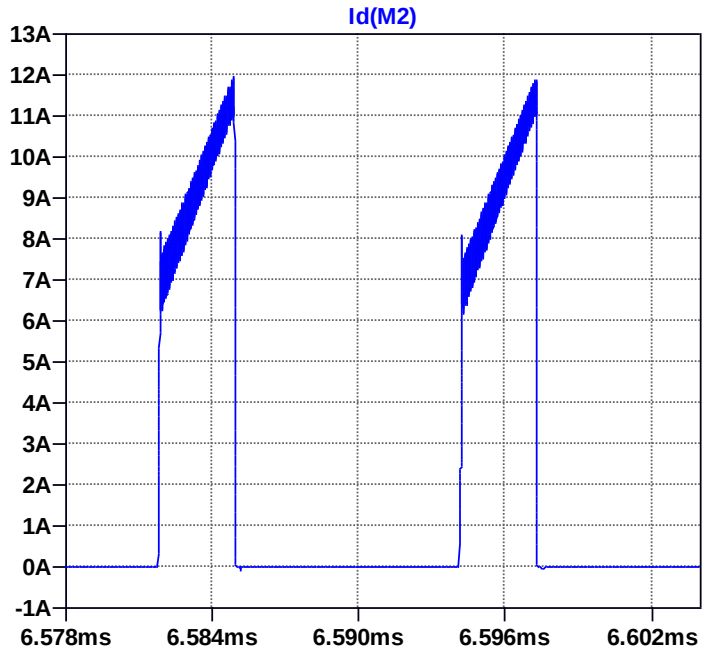

Figure 23. Ids Measurements on the MOSFET for Vin = 40V

The current on the MOSFET increases to 11.95A from 7.637A during the ON period. During startup, the current on the MOSFET increases to 87.5A for an instance. These maximum values of current and voltage on the MOSFET are considered when the components are chosen. Also, the peak one-cycle ratings are considered.

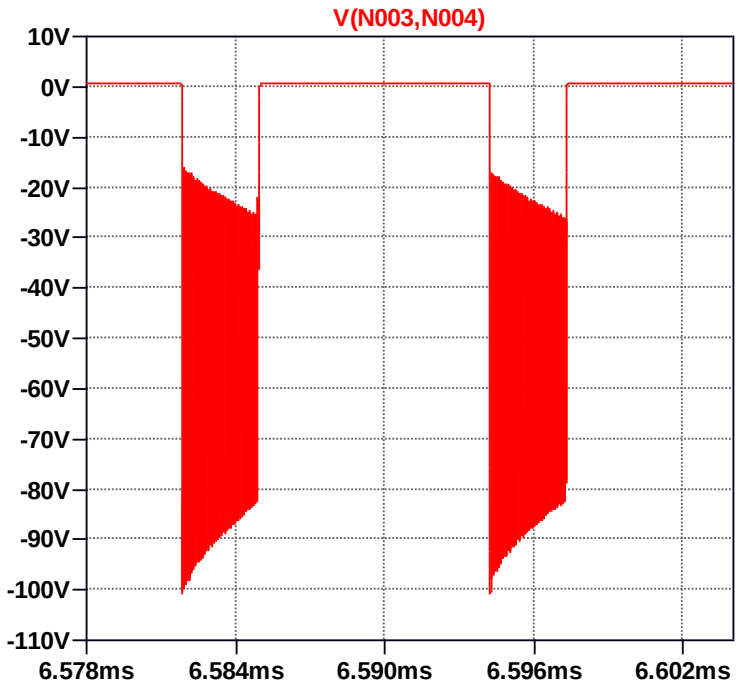

Figure 24. Voltage on the Output Diode for Vin = 40V

The output diode should be able to stand a reverse voltage of 100V. The ringing on it does not induce a power loss as no current passes through it.

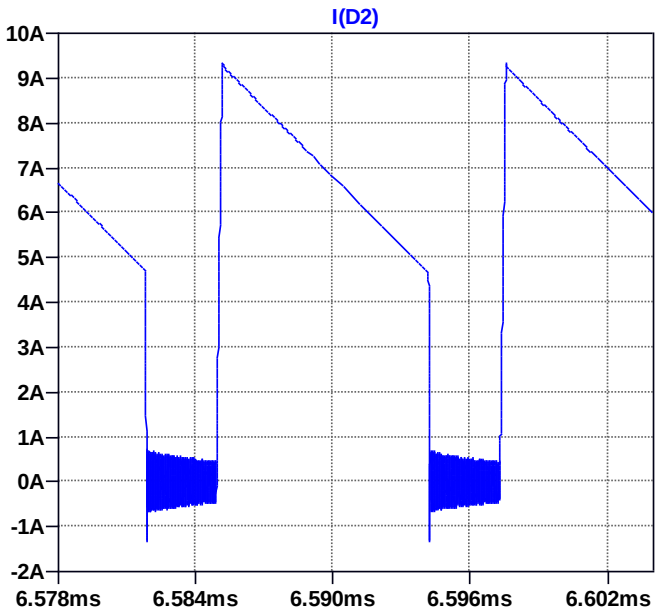

Figure 25. Forward Current on the Output Diode for Vin = 40V

The current on the output diode decreases to 4.76A from 9.41A during a cycle. These maximum values of current and voltage on the output diode are considered when the components are chosen.

Overall, it can be seen that the design can be implemented with a proper choice of the components of the circuit.

Component Selection

The components are mainly picked from the local suppliers such as "ozdisan.com" and "direnc.net". The most important components for the operation of the converter are the semiconductors such as the switching MOSFET, output diode and clamp diode. The other passive parts and ICs are also found from the mentioned suppliers.

The MOSFET selected is "SUM85N15-19-E3" produced by Vishay. It is a 85A 150V N-Channel MOSFET in D2PAK package with a 19mΩ drain-to-source resistance.

The diode selected for the output and the RCD clamp are same. BD10200CS_S2_00001 is a Schottky diode produced by Panjit in DPAK packaging which can pass through 10A and hold a reverse voltage of 200V. The forward voltage of the diode is equal to 0.9V, which is in the 1V limit that we have considered in the transformer design section. In the output, 3 or 4 of the diodes will be paralelled for enhanced safety.

TL431 will be used in the voltage feedback loop as a voltage reference IC.

UC3845 will be used as the controller of the circuit. When the datasheet of the controller is inspected, it can be seen that as well as UC3845; UC3843, and UC3844 can be also used as the properties are exactly same except the operating temperature which does not imply a problem for the project.

The optocoupler used is a PC817 which can be easily found in Turkey.

Initial Transformer Tests

For starters, to verify that the magnetic design is accurate and achievable, transformer windings are manufactured and wound to the core itself. The first design of the transformer is presented below.

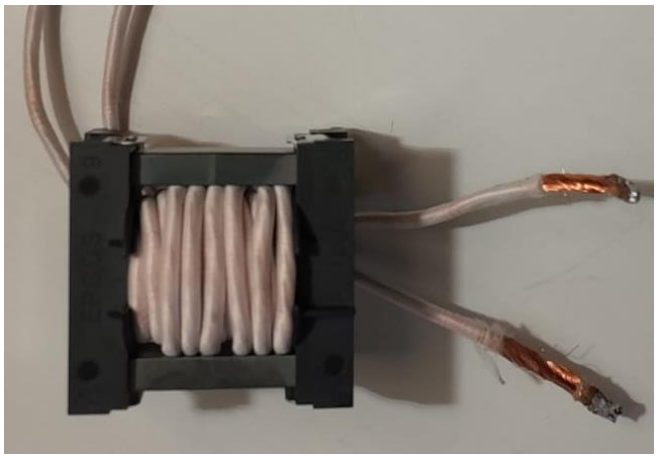

Figure 26. Manufactured Transformer Design

As it is calculated before, the inductance of the primary winding should be approximately 20µH. To achieve this, primary and secondary windings should be 10 turns. After the transformer is manufactured, some tests are conducted to evaluate the parameters of the transformer.

Initially, the primary side of the transformer is connected to the LCR meter, and the inductance and resistance are measured while the secondary is open circuited. Corresponding measurements are given in the figure below.

Figure 27. LCR meter measurements: a) secondary side is open circuited, b) secondary side is short circuit.

For the test setup, the equivalent circuit of the transformer is assumed to be as below.

As the turns ratio of the transformer is 1 in this case, leakage for the primary (L1) and the referred secondary leakage inductance (L2) are equal with small possible deviations. For the first test, the LCR meter is connected to the primary side of the transformer while the secondary size is open circuited. Therefore, measured inductance is equal to sum of the leakage inductance and the magnetizing inductance.

$$L_1 + L_m = 24.504\ \mu H$$

For the second test, the secondary side is short circuit. Thus, the measured inductance includes both the primary leakage summed with parallelly connected secondary referred leakage with the magnetizing inductance.

$$L_1 + L_2 // L_m = L_1 + L_1 // L_m = 0.5 \mu H$$

Using the two equations, leakage inductance and the magnetizing inductance can be calculated.

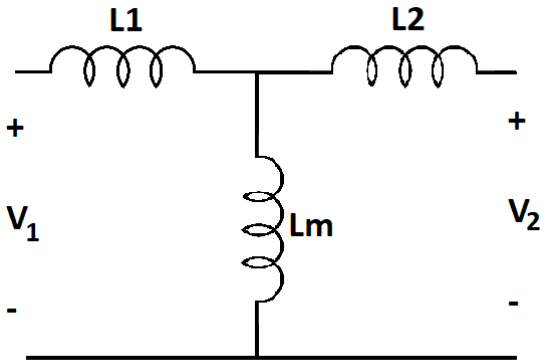

Figure 28. Equivalent Circuit of a Transformer

The results show that the magnetizing inductance is significantly higher compared to the leakage inductance. Thus, the second measurement where the secondary side is short circuit, one can assume that the parallel branch does not demand significant current which implies that the measured inductance is approximately equal to twice of the leakage inductance. Lastly, the ratio of the leakage to the magnetizing inductance is calculated as approximately 1% which is reasonable.

$$L_1 \cong 0.2513\ \mu H$$
$$L_m \cong\ 24.2527\ \mu H$$
$$\frac{L_1}{L_m}(\%) = \frac{0.2513}{24.2527} * 100 \cong 1.04\%$$

Aimed Bonuses

In terms of the bonuses, efficiency, analog controller IC, PCB, and compactness bonuses are aimed. The efficiency is aimed to be as high as possible while achieving at least 80% efficiency to avoid negative points. The controller will primarily be implemented as an analog controller. In case the analog controller does not work, digital controller will be utilized by giving up for the bonus. Also, this semester, the project will try to be implemented on a printed circuit board to gain bonus points both considering the PCB and compactness bonuses. If the project is

implemented successfully, a box can be designed to have a better-looking project and gain some bonus points.

Future Work

As mentioned before, this project is under construction. After the feedback presentations, we will finalize our tests and transformer implementation as well as the overall project. Until the demo day. The hardware project will be implemented as soon as possible so that the tests will be conducted on the implemented design to eliminate the errors faster to finalize the project for the demo day. The closed loop control will try to be implemented using an analog controller , and the simulation for the controller will be implemented before the actual design; however, if it does not work during the tests, the same system will be implemented using a digital controller. Overall design and the design particulars will be explained broadly in the final report.

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