Elijah Sprung

CSC 2410 – 01

Dr. Yong Wei

Homework 5

1) **Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode, and the remainder the immediate operand or an operand address.**
    a. **What is the maximum directly addressable memory capacity, in Mbytes?**

        The maximum directly addressable memory capacity would be 16MB. This is because every byte has 8 bits, meaning that there are only 24 bits left after subtracting the 8 bits for the opcode. 2^{24} = 16,777,216 B = 16MB.
    b. **Discuss the number of bus cycles needed to transmit memory addresses and data if the microprocessor bus has**
        i. **A 32-bit local address bus and a 16-bit local data bus, or**

            The 32-bit address bus need 1 cycle and the 16-bit local data bus needs 2 cycles for a total of 3 cycles.
        ii. **A 16-bit local address bus and a 16-bit local data bus.**

            Both the local address bus and the local data bus need 2 cycles each for a total of 4 cycles.

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2) **For a synchronous read operation, the memory module must place the data on the bus sufficiently ahead of the falling edge of the Read signal to allow for signal settling. Assume a microprocessor bus frequency is 10 MHz and the Read signal begins to fall in the middle of the second half of T3. (Show your steps. Answers without steps will have zero credit.)**

   a. **Determine the length of memory read instruction cycle. Hint: How many clock cycles does a read instruction need?**

      10 MHz = 10^7 because of 10 * 10^6 = 10,000,000 Hz. T = 1/F = 1/10,000,000 = 0.0000001 s = 100 ns. The cycle at T_3 starts at 200 ns and ends at 300 ns.

   b. **When, at least, should the memory data be placed on the bus? Allow 20 ns (1 ns = 10-9 s) for the settling of data signal.**

      A whole cycle can be split up into 5 parts: beginning, middle of first half, middle, middle of second half, and end. Each part has a length of 25 ns. The middle of the second half happens 75 ns after the beginning of the cycle which is 100 ns in length. Accounting for the settling of the data signal, 75 ns – 20 ns = 55 ns, means that the memory data should be placed on the bus before 55 ns have passed since the beginning of the cycle at T_3 which translates to 255 ns since the beginning.