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CSC 2410 – 01

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Homework 6

1. Consider a dynamic RAM that must be given a refresh cycle 128 times per ms ($1\text{ms} = 10^{-3}$ second).

Assume each refresh cycle requires 300 ns ($1\text{ns} = 10^{-9}$ second). What percentage of the memory's total operating time must be given to the refreshes?

$$128 * 300 = 38,400 \text{ ns}$$

$$0.0000384 \text{ s} / 0.001 \text{ s} = 3.84 \% \text{ of the memory's total operating time given to the refreshes.}$$

2. The memory of a particular computer is built from 64K×1 DRAMs. The cell array of the DRAM is organized into 256 rows. Each row must be refreshed at least once every 4 ms. Suppose we refresh the memory on a strictly periodic basis.

(a). What is the maximum time allowed for refreshing a row?

$$4 \text{ ms} / 256 \text{ rows} = 0.015625 \text{ ms per row.}$$

(b). How many bits does the refresh address counter need?

It needs 8 bits because $2^8 = 256$ and an individual address is needed for each row.