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CSC 2410 – 01

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Homework 3

Assume the main memory size is 32 bytes. One word has one byte. Main memory block size is 4 words. The cache memory has 4 lines. The cache line size is 32 bits. Direct mapping is used. The tags of cache lines are shown as follows:

Cache Line Id	Tag	
0	1	
1	0	
2	1	
3	0	

1. **How many bits at least are needed for memory addresses? Why?**

   At least 5 bits are needed for memory addresses because each bit must correspond with a memory address and there are 32. $2^5 = 32$.

2. **How many bits in the memory address are needed to identify words? Why?**

   There are 4 words per block, so individual words can be identified by 2 bits because $2^2 = 4$.

3. **How many bits in the memory address are needed to identify cache lines? Why?**

   3 bits are needed in the memory address to identify cache lines, 2 for each of the 4 possible Cache Line Id's because $2^2 = 4$ and the final one is used to determine the tag for each cache line.

4. **If The CPU needs to access the information contained in memory address 29_{10}. Will it be a miss or hit? Explain your answer.**

   The physical address of 29_{10} is 11101. The tag is 1, the cache line is 11, and the word offset is 01. Using the formula i = j % m where j = 7, m = 4, 7 % 4 = 1 which does not match the tag of cache line 3 which is 0. This means that it would be a miss.