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CS241

HW21

Isub3 = 111111111000001111100010000101000000

iand3 = 111111111000000011000010000101000000

iload2 = 00000001000001111000000000010100011 Assuming that the next instruction is at position 1

21. The shift register of Fig. 4-27 has a maximum capacity of 6 bytes. Could a cheaper version of the IFU be built with a 5-byte shift register? How about a 4-byte one?

- Yes, both of these are possible since the shift register only fetches 4 bytes from the memory at a given time, and they are read before being discarded.

22. No, this would not be very effective, as the bottleneck comes from the speed at which the values can be read from the shift register into the MBR1, not the speed at which they arrive in the shift register. If the register had more space it would have to read from memory less often, thereby reducing traffic on the bus, but these improvements would be marginal gains next to the space that such a change would require.

26. 14nsec