# ECE/CSE 371 HW5

Elijah Melton, 2164822
Ankith Tunuguntla, 2334509

## Problem 1

Given variables:

$T_{co} = 2\,ns$

$T_{data,min} = 3\,ns$

$T_{data,max} = 5\,ns$

$T_{su} = 2\,ns$

$T_H = 1.5\,ns$

Setup slack $= T_{clk} - (T_{co} + T_{data,max} + T_{su})$

$= T_{clk} - (2 + 5 + 2)$

$= T_{clk} - 9\,ns$

$= 1/150 \times 10^6 - 9\,ns$

$= 6.67 \times 10^{-9}\,s - 9\,ns$

$= -2.33\,ns$ ✗

Hold slack $= T_{co} + T_{data,min} - T_H$

$= 2 + 3 - 1.5$

$= 3.5\,ns$ ✓

System does not meet timing because set up time is violated at 150 MHz.

Problem 2

$$\text{Setup slack} = t_{period} - (t_{co,MAX} + t_{clk1,max} + t_{AND,max} + t_{In,max} + t_{clk2,max} + t_{NOR,max} + t_{su})$$

$$= 100 - (10 + 5 + 40 + 17 + 3 + 30 + 10)$$

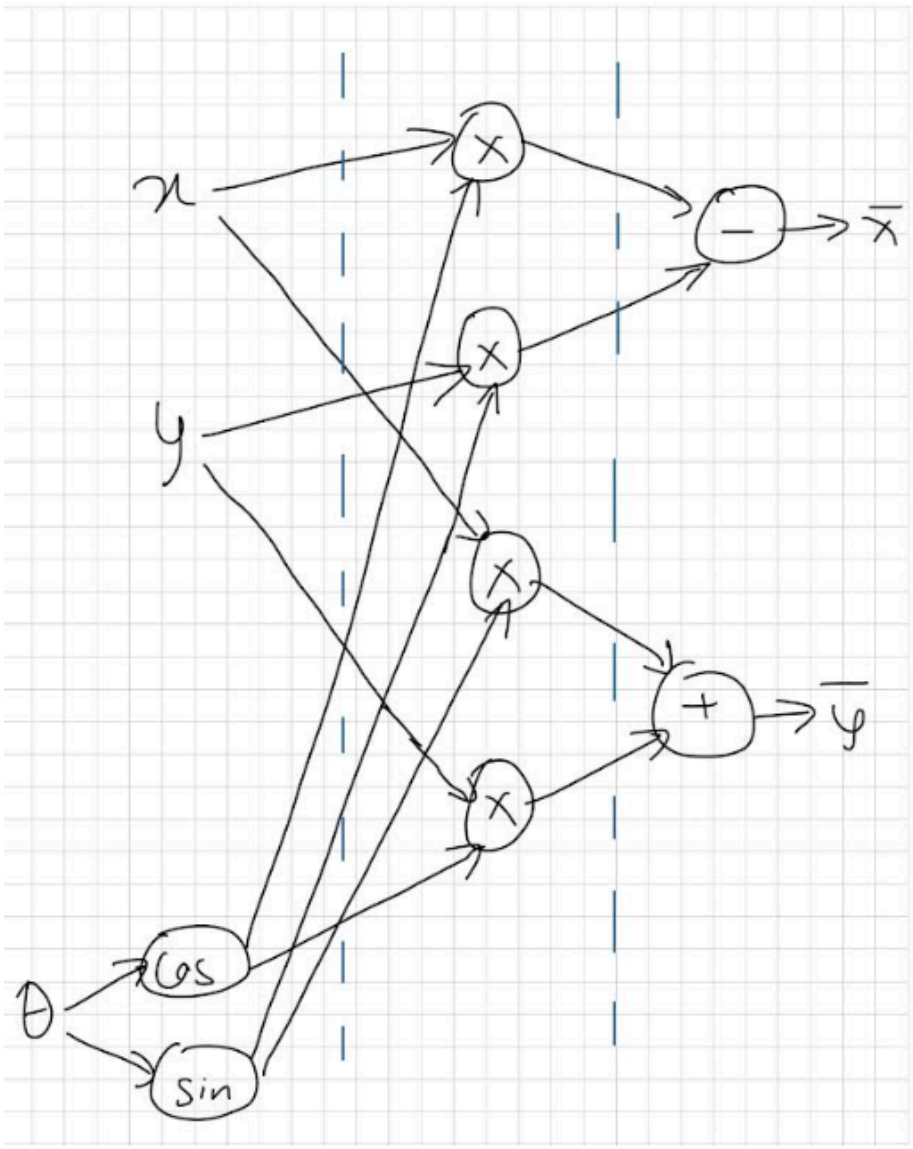
$$= 100 - 115 = \underline{-15 \text{ ns}}$$

$$\text{Hold Slack} = (t_{co,min} + t_{clk1,min} + t_{AND,min} + t_{In,min} + t_{clk2,min} + t_{NOR,min}) - t_h$$

$$= (8 + 4 + 35 + 13 + 2 + 25) - 5 = \underline{82 \text{ ns}}$$

Problem 3

**a) And b)**



c)

| | Op | Delay |
|---|---|---|
| Stage 1 | cos / sin | 100 ns (max) |
| Stage 2 | X | 60 ns |
| Stage 3 | −/+ | 30 ns |

So latency (3-stage) = 3 × 100 ns

= 300 ns

latency (2-stage) = (100 + 60) × 2

= 320 ns

# Part 4

18. What element adds the most delay? How can we change the clock parameters such that setup slack does meet timing requirements?

Mult0~921|resulfa[2], incr time = 3.392

setup slack = data required time - data arrival time
calculated: -15.589 = 4.659 - 20.248
reported: -15.759

To meet the timing constraint, we need to increase the clock period to somewhere around the deficit in slack, e.g. ~16 ns

19. Repeat the "**Report Timing…**" steps to investigate the *hold slack* results. Does the same element add the most delay for hold slack? Why does this make sense?

Mult0~2921|by[4], incr time = 5.439

No, the same element doesn't add the most delay. This makes sense because we're evaluating two different constraints, i.e. a maximum delay for setup time and minimum delay time for hold time.

22. What is the fastest frequency you can set the clock to for this to pass setup timing?

Fasted clock I could pass with:
period: 16.760
fall: 8.380
freq: 59.67 MHz

Now that it passes, the main difference is that the total setup time is much higher, totaling 20.419

33. Now use the "Summary (Setup)" reports to answer the following questions:

| | |
|---|---|
| Slow 1100mV 85C Model | 1.560 |
| Slow 1100mV 0C Model | 1.220 |
| Fast 1100mV 85C Model | 3.487 |
| Fast 1100mV 0C Model | 4.688 |

a. Which of the options has the most setup slack?

Fast 1100mV 0C Model

b. How does increasing voltage speed change the speed of a circuit?

Increasing voltage speed should, in theory, increase the speed of the circuit/decrease the delays. This makes sense on a physical level because an increased voltage makes capacitors charge/discharge faster, and transistor switching happen quicker. This is reflected in our data, as both of the fast models have higher setup slack, meaning there is more room for delay

c. How does increasing temperature change the speed of a circuit?

Increasing temperature should in theory decrease the speed of the circuit/increase delays. With increased temperature, effective resistance increases within the semiconductors, meaning it will take a higher voltage for a transistor to switch. This wasn't consistently reflected in the data, but that's likely due to other factors, perhaps some relationship between voltage speed and effectiveness at high temperatures

34. repeat with hold slacks

| | |
|---|---|
| Slow 1100mV 85C Model | .672 |
| Slow 1100mV 0C Model | .245 |
| Fast 1100mV 85C Model | .673 |
| Fast 1100mV 0C Model | .348 |

a. Which of the options has the most hold slack?

Fast 1100mV 85C Model

d. How does increasing voltage speed change the speed of a circuit?

It seems that at high temperatures, the voltage speed has very little effect on the hold time of the circuit (only a .001 increase from slow -> fast). However, at low temperatures we see a marginally higher hold time slack

e. How does increasing temperature change the speed of a circuit?

Increasing temperature significantly increased the hold time slack (roughly doubled), which makes sense because increasing temperature should in theory slow down the circuit, giving us more delay and therefore more slack for hold time.

## Difficulty rating for each assignment:

Problem 1 - Easy

Problem 2 - Moderate

Problem 3 - Moderate

Problem 4 - Easy/Moderate

## Time Spent

5 hours