Power Electronics Final Examination 2025

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Github Repository: https://github.com/elisabethvirgie/PEFinal-Virgie

Task 1: Buck Converter Design

You are assigned to design a buck converter for step-down voltage conversion. Follow the detailed instructions below:

1. **Determine the key specifications**

   To design a buck converter for step-down voltage conversion, we define the following specifications:

Parameter	Value	Description
Input Voltage	36 V	Common DC source (e.g., battery or adapter)
Output Voltage	12 V	Typical voltage for low-power DC load
Switching Frequency	100 kHz	High enough to reduce passive component size
Output Power	24 W	Moderate power requirement
Load Resistance	6 Ω	Derived from
Allowed Inductor Ripple	20% of Iout	To ensure continuous conduction mode (CCM)
Allowed Voltage Ripple	1% of Vout	To ensure voltage stability

   Using the data mentioned above, we can obtain following variable values:

   Output Current

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{24}{12} = 2$$

   Inductor Current Ripple (Peak to Peak)

$$\Delta I_L = 0.2 \times 2 = 0.4$$

   Output Voltage Ripple

$$\Delta V_{out} = 0.01 \times 12 = 0.12$$

2. **Calculate and determine suitable values**
    a. Duty Cycle

    The duty cycle (D) is the ratio of the output voltage to the input voltage:

$$D = \frac{V_{out}}{V_{in}} = \frac{12}{24} = 0.5 = 50\%$$

    This means the switch is ON for 50% of the switching period.

    b. Inductor Current

    Since the inductor is in series with the load, the inductor current is equal to the output current:

$$I_o = \frac{V_{out}}{R_{load}} = \frac{12}{6} = 2$$

    The peak-to-peak ripple is 20% of the output current:

$$\Delta I_L = 0.2 \cdot I_o = 0.2 \cdot 2 = 0.4$$

    c. Switching Period

    The switching period is the inverse of the switching frequency:

$$T_s = \frac{1}{f_{sw}} = \frac{1}{100{,}000} = 10^{-5}$$

    d. <u>Inductor Value</u>

    Using the ripple current formula:

$$L = \frac{V_{out} \cdot (1 - D)}{\Delta I_L \cdot f_{sw}} = \frac{12 \cdot (1 - 0.5)}{0.4 \cdot 100{,}000} = \frac{6}{40{,}000} = 150$$

    e. <u>Capacitor Value</u>

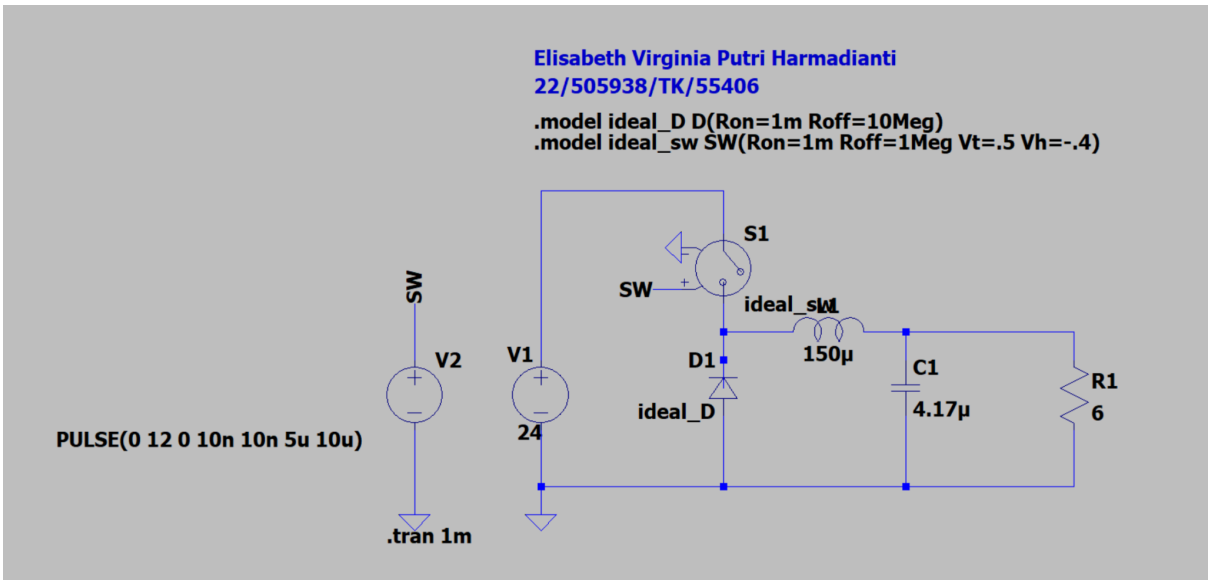
    Allowed output voltage ripple:

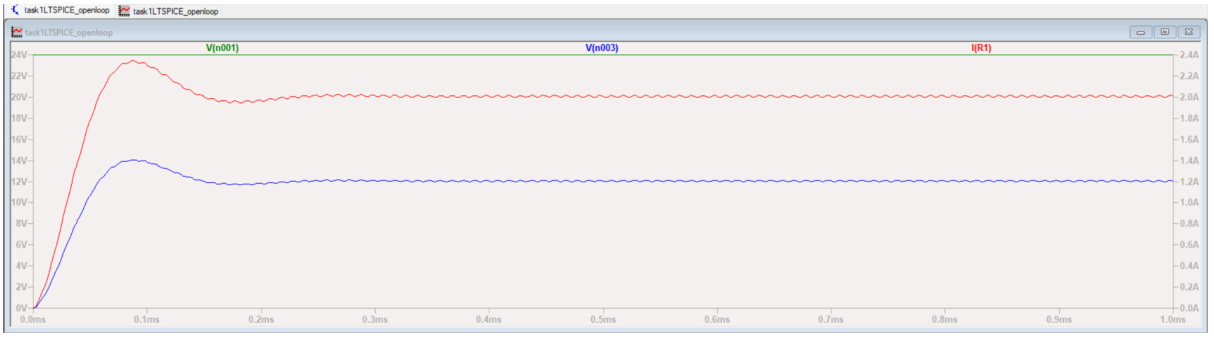
$$\Delta V_o = 0.01 \cdot V_{out} = 0.01 \cdot 12 = 0.12$$

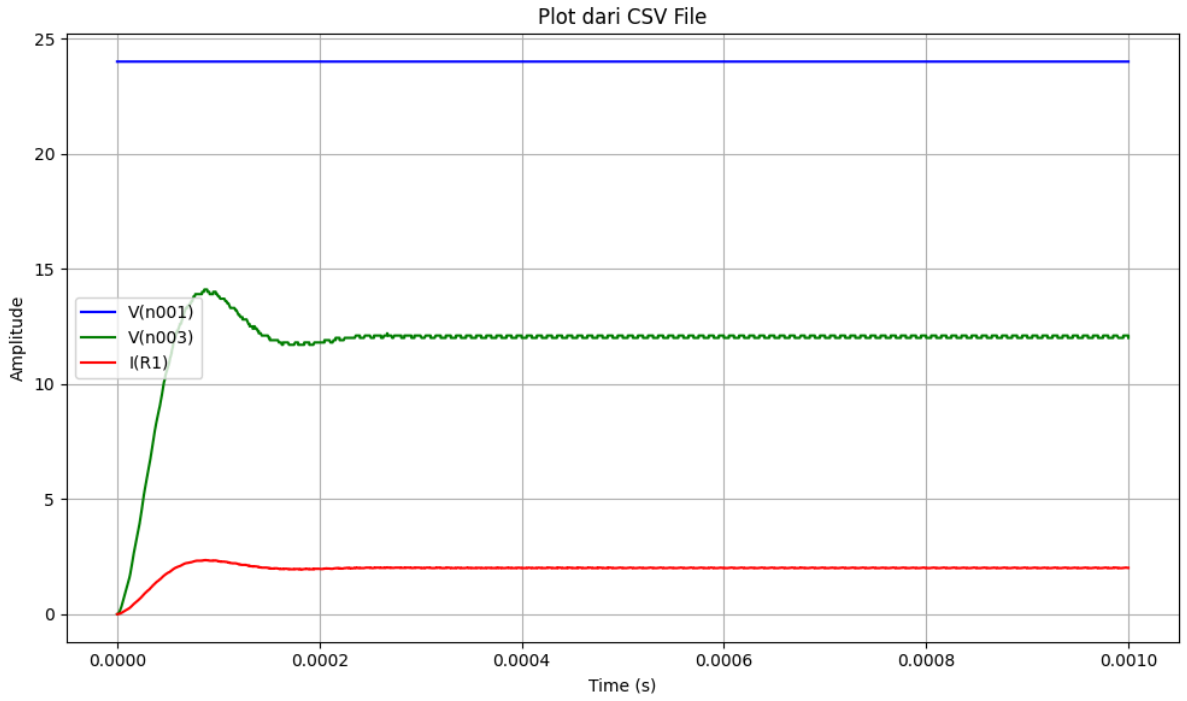
    Using the capacitor ripple formula:

$$C = \frac{\Delta I_L}{8 \cdot f_{sw} \cdot \Delta V_o} = \frac{0.4}{8 \cdot 100{,}000 \cdot 0.12} = \frac{0.4}{96{,}000} \approx 4.17$$

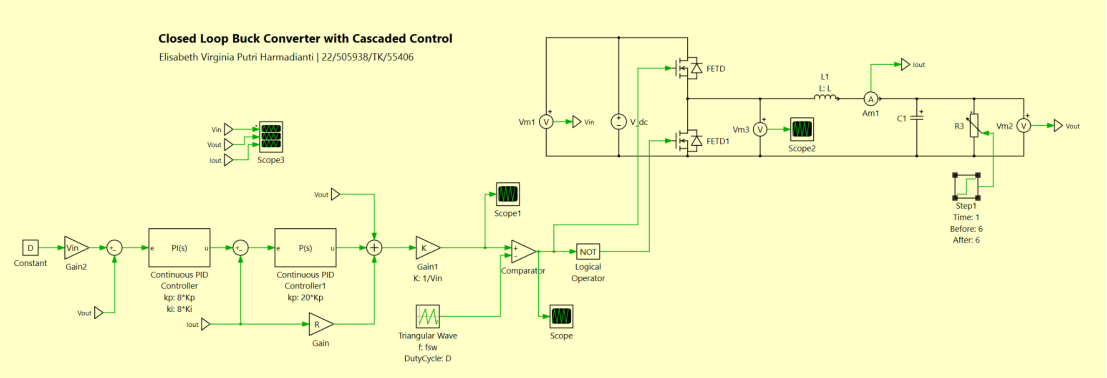
3. **Develop and simulate the open-loop operation**

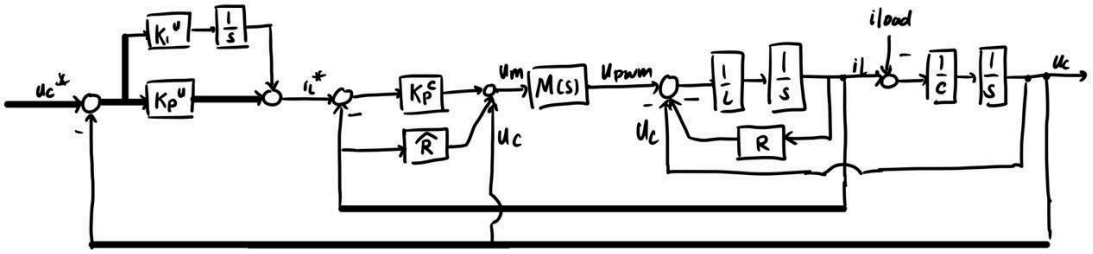






4. **Design a cascaded control system** for voltage regulation of the buck converter.
    - Include a complete block diagram of your control architecture.





    - Provide detailed calculations or tuning procedures for determining the control gains (e.g., Kp and Ki).

      To regulate the output voltage of the buck converter, we use a Proportional-Integral (PI) controller in the outer voltage loop of a cascaded control architecture. Parameters are tuned using a frequency-based design method, considering the converter's output capacitor and the desired bandwidths of the control loops.

      a. Selection of Bandwidth

         The bandwidth of the voltage loop is set significantly lower than the switching frequency to ensure proper separation between the power stage dynamics and the control loop:

         - Voltage loop bandwidth (breakpoint):

$$f_{bp} = \frac{f_{sw}}{20} = \frac{100{,}000}{20} = 5000$$

         - Integral action corner frequency:

$$f_{bi} = \frac{f_{bp}}{10} = \frac{5000}{10} = 500$$

b. Calculating Kp

$$K_p = 2\pi f_{bp} \cdot C = 2\pi \cdot 5000 \cdot 4.17 \times 10^{-6} = 0.131$$

c. Calculating Ki

$$K_i = 2\pi f_{bi} \cdot K_p = 2\pi \cdot 500 \cdot 0.131 = 411.6$$

Parameters inputted on PLECS simulation:

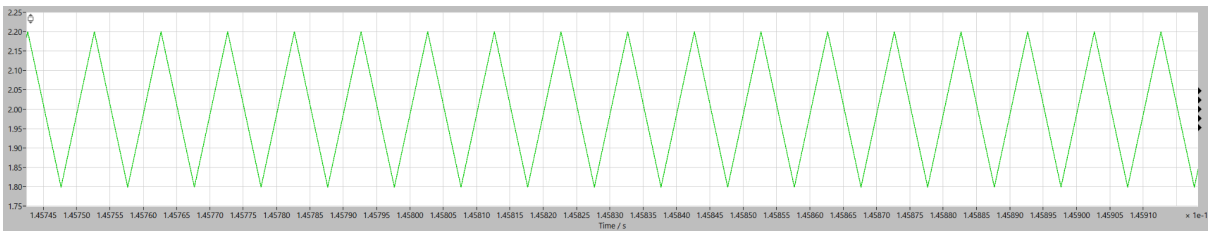
```
%parameter system
Vin = 24;
Vout = 12;
R = 6;
fsw = 100e3;
perc_I = 20;
perc_V = 1;
Iout=Vout/R;
dI = (perc_I/100)*Iout;
dV = (perc_V/100)*Vout;

%duty cycle
D = Vout/Vin;
Ts = 1/fsw;

%inductance and capacitance
L = Vout * (1 - D) / (dI * fsw);
C = Vout * (1 - D) / (8 * dV * L * fsw^2);

% Kp and Ki
Fbp = fsw/20;
Fbi = Fbp/10;
Kp  = 2*pi*Fbp*C;
Ki  = 2*pi*Fbi*Kp;
```

5. **Plot the inductor current waveform** and verify that the ripple meets your design criteria.

The inductor current waveform has been successfully plotted as shown in the figure. According to the design criteria, the peak-to-peak ripple current, is calculated as 20% of the output current:

$$I_o = \frac{V_{out}}{R_{load}} = \frac{12}{6} = 2$$

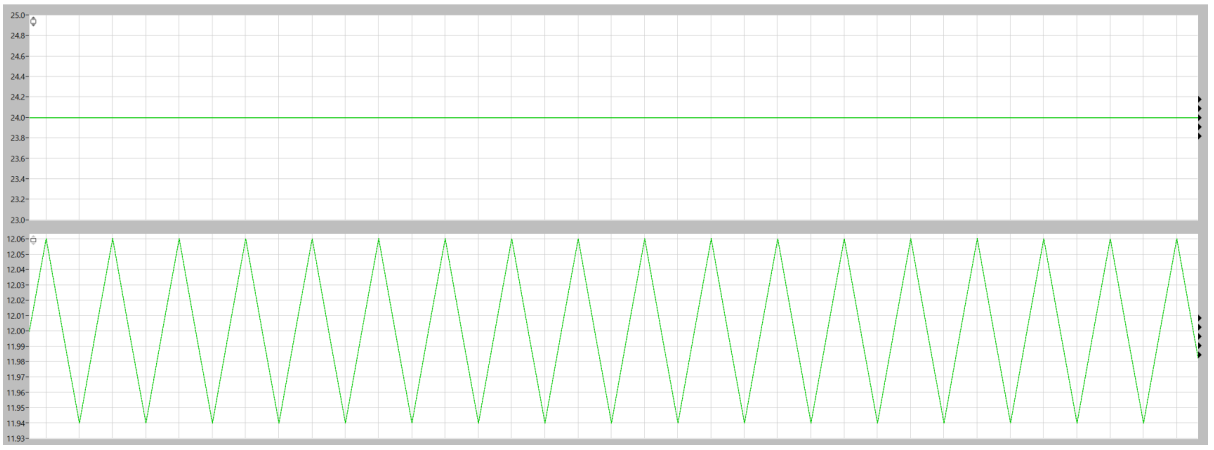
$$\Delta I_L = 0.2 \cdot I_o = 0.2 \cdot 2 = 0.4$$



From the waveform, it can be observed that the inductor current varies approximately between 1.8 A and 2.2 A, resulting in a peak-to-peak ripple of 0.4A. This confirms that the inductor ripple current meets the expected design target of 0.4 A, validating the proper operation of the converter.

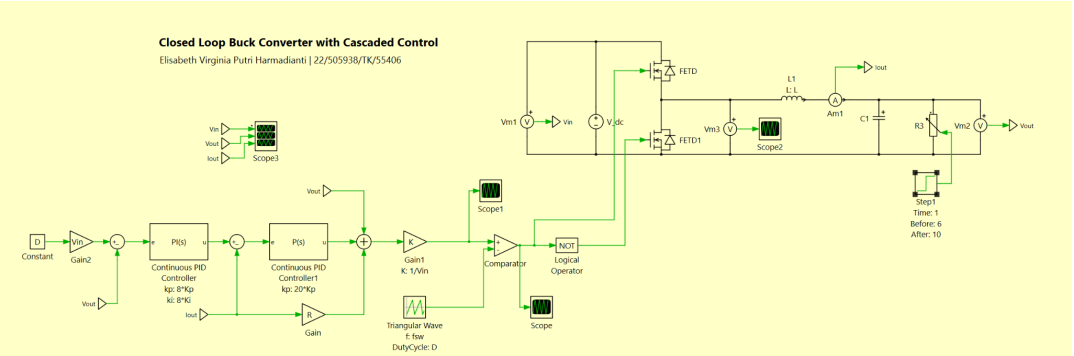
6. **Plot the output voltage waveform** and verify that the ripple is within the allowable range

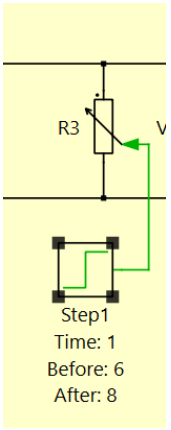
$$\Delta V_o = 0.01 \cdot V_{out} = 0.01 \cdot 12 = 0.12$$

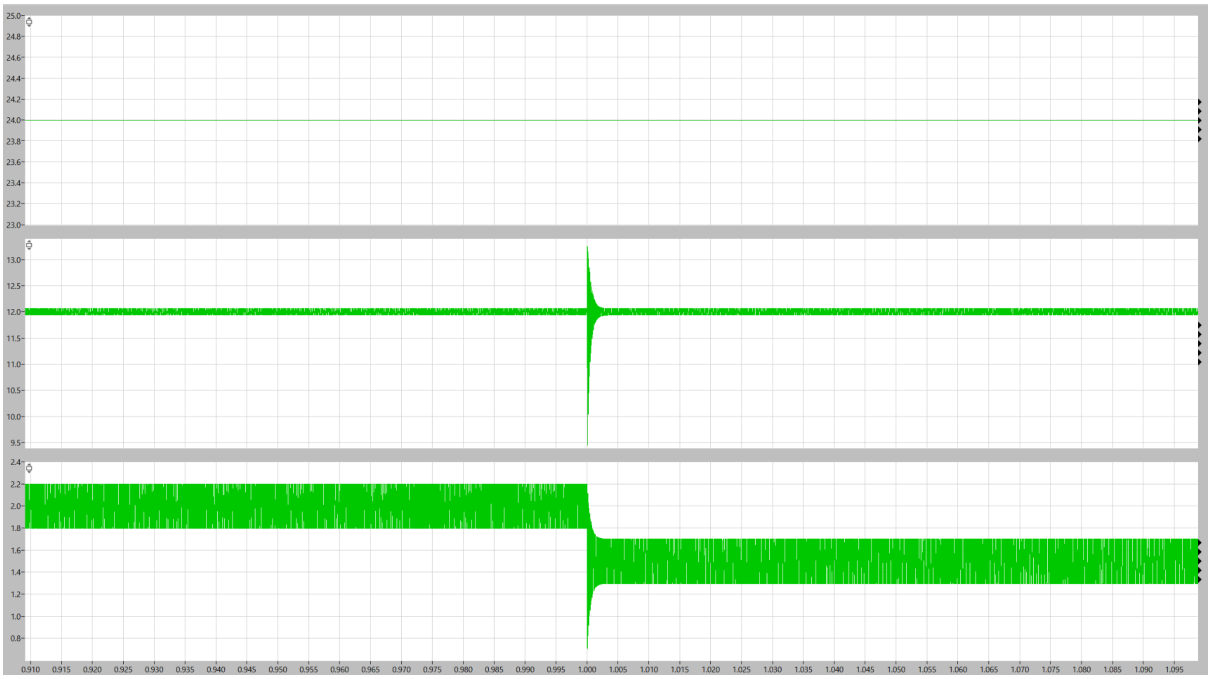


From the waveform, the output voltage fluctuates approximately between 11.94 V and 12.06 V, resulting in a total ripple of 0.12V. This confirms that the output voltage ripple is **exactly 0.12 V**, which is within the allowable range. Therefore, the output voltage meets the design requirement.

7. **Simulate a sudden load change** and analyze the converter's dynamic response. Demonstrate how the controller maintains stability and restores regulation.







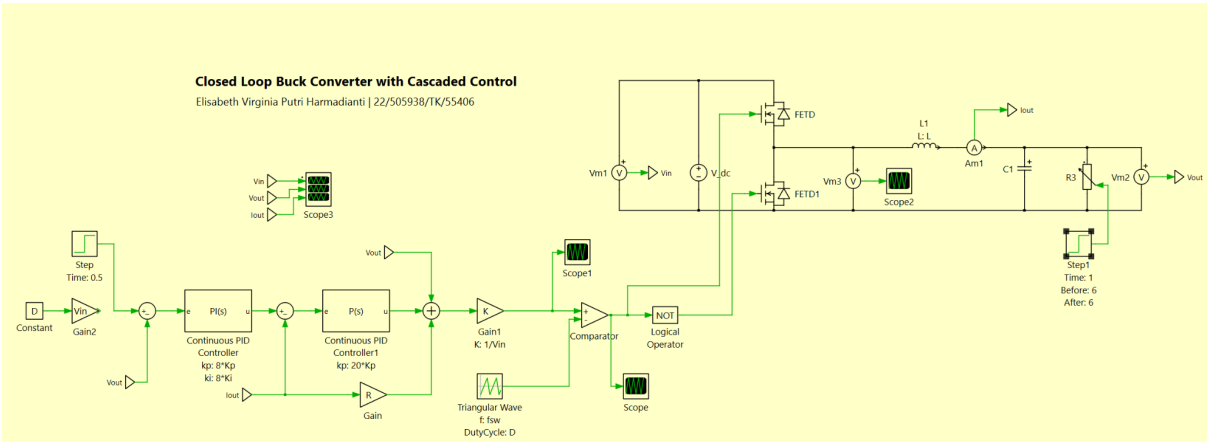
A sudden load change was simulated at **t = 1 s** to evaluate the dynamic performance and stability of the converter. The plots above illustrate the output voltage, the error signal, and the inductor current in response to this disturbance.

- Before the disturbance, the output voltage remained steady at approximately **12 V**, indicating proper regulation under nominal load conditions.

- At the moment of the load step, a **transient deviation** is observed in both the output voltage and inductor current. The output voltage briefly dips or overshoots, while the inductor current shows a sharp transient response.
- However, because of the feedback control mechanism, the converter quickly restores regulation. The output voltage settles back to 12 V within a short time, and the inductor current stabilizes at its new steady-state level.

This behavior demonstrates that the controller effectively maintains system **stability** and provides a fast **transient response** under sudden load changes. The overshoot and settling time are within acceptable limits, confirming that the converter design is robust and reliable.

8. **Simulate the system response to a step change** in the voltage reference. Show how effectively the controller tracks the new reference value.



9. 

A step change in the reference voltage was introduced at **t = 5.0 s** to evaluate the system's transient response and the tracking performance of the controller. The waveform plots above show the output voltage, the error signal, and the inductor current.

- The middle graph displays the **output voltage response**. Upon the reference change, the output voltage rises quickly with an initial **overshoot** reaching around 23–24 V before settling.
- The response exhibits **under-damped behavior** with a few oscillations, but it progressively converges to the new reference value, indicating the system's stability.
- The bottom graph shows the **inductor current**, which increases accordingly to meet the demand of the new voltage level and stabilizes with acceptable ripple.
- The top waveform remains steady, suggesting a regulated input or unaffected reference level.

This simulation demonstrates that the controller is **effective in tracking the new reference voltage**, successfully adjusting the output with a relatively fast **settling time** and maintaining regulation after a brief transient period. The control system is thus verified to have good dynamic performance under step reference changes.

Task 2: PV Grid-Connected Inverter

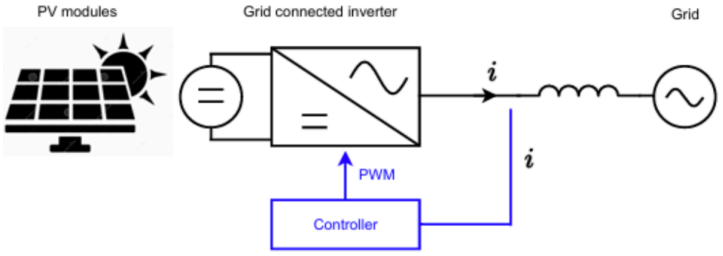


Figure 1: PV grid connected inverter

You are assigned to design a PV grid-connected inverter system as illustrated in the figure. The task includes determining the inverter and PV module specifications, selecting system components, and designing a control strategy to regulate both active and reactive power injected into the grid. Follow the detailed instructions below:

1. **Define the configuration of the photovoltaic (PV) array**. Specify key parameters such as module voltage, current, and how modules are arranged (series/parallel).
   - **4 arrays in parallel**
   - Each array: 2 strings of 20 modules in series → **40 modules total per array**
   - Total modules: 4×40=160
   - Total power: 160×65=10,400 W=10.4kW
   - Under practical irradiance (0.7–1.0 kW/m²), output ~2.6–3.2 kW
2. **Determine the PV module configuration and its rating** such as voltage and current.
   a. **PV Rating (BP365)**:
   - Voltage at maximum power point (Vmp): 17.5 V
   - Current at maximum power point (Imp): 3.7 A
   - Power per module: Pmp=65W
3. **Determine the specifications of the inverter**. At a minimum, include:

Parameter	Value	Notes
DC-link voltage	800 VDC	Output of the boost converter
Grid type	3-phase, 230 V (line-line RMS), 50 Hz	Low-voltage European grid
Power rating	3 kW	Target nominal inverter power
Switching frequency	10 kHz	Used for SVPWM modulation
Inverter type	3-level NPC	Better waveform quality
Modulation technique	3-Level SVPWM	With symmetrical & alternating zero vector modes

4. **Calculate the value of the inductor (L)** connecting the inverter to the grid (three-phase voltage of 380 V).
(Support your answer with a phasor (vector) analysis diagram showing voltage and current relationships.)

To limit switching ripple and reduce grid current THD, we use an **LCL filter**. It consists of:

- L1: inverter-side inductance
- L2: grid-side inductance
- Cf : filter capacitor (between L1 and L2)

a. Assumptions:

- Grid frequency: 50 Hz
- Switching frequency: 10 kHz
- Voltage per phase: 220 V (RMS)
- Peak voltage: Vpeak = $\sqrt{2} \times 220 = 311$ V
- Target current ripple: 10%

b. Output Current Estimate

$$I_{rms} = \frac{P}{3 \cdot V_{phase}} = \frac{3000}{3 \cdot 133} \approx 7.52$$

$$I_{peak} = \sqrt{2} \cdot I_{rms} \approx 10.63$$

$$\Delta I = 0.1 \cdot I_{peak} \approx 1.063$$

c. Inverter-Side Inductance

$$L_1 = \frac{V_{dc}}{4 \cdot f_{sw} \cdot \Delta I} = \frac{800}{4 \cdot 10{,}000 \cdot 1.063} \approx 1.88 \text{ mH}$$

d. Grid Side Inductance

$$L_2 = 0.5 \cdot L_1 = 1 \text{ mH}$$

e. Filter Capacitance

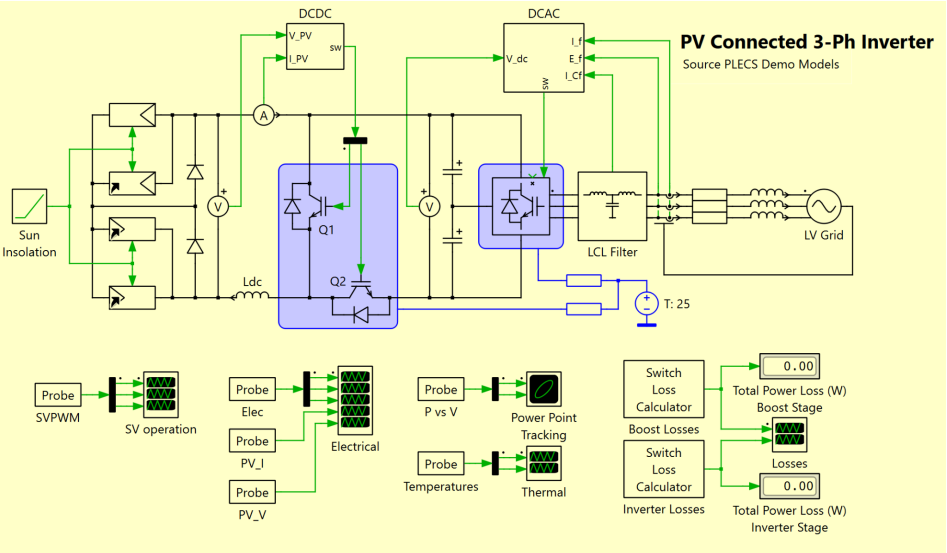
$$C_f = \frac{1}{10 \cdot 2\pi f_{grid} \cdot (L_1 + L_2)} = \frac{1}{10 \cdot 2\pi \cdot 50 \cdot 3 \times 10^{-3}} \approx 106 \text{ F}$$

f. Controller PI Tuning

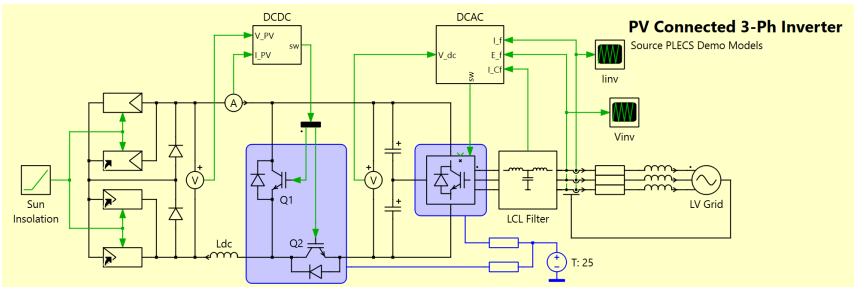
$$K_p = 2\pi f_{bp} \cdot L = 2\pi \cdot 1000 \cdot 0.002 = 12.57$$

$$K_i = 2\pi f_{bi} \cdot K_p = 2\pi \cdot 100 \cdot 12.57 = 789.6$$

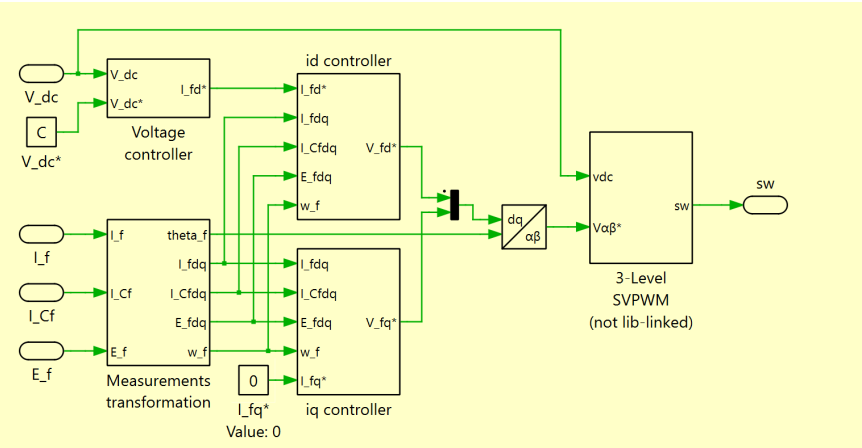
5. **Design a control system** capable of regulating both active and reactive power.
    - Present your control design using block diagrams.
    - Explain the method used to determine controller gain parameters.

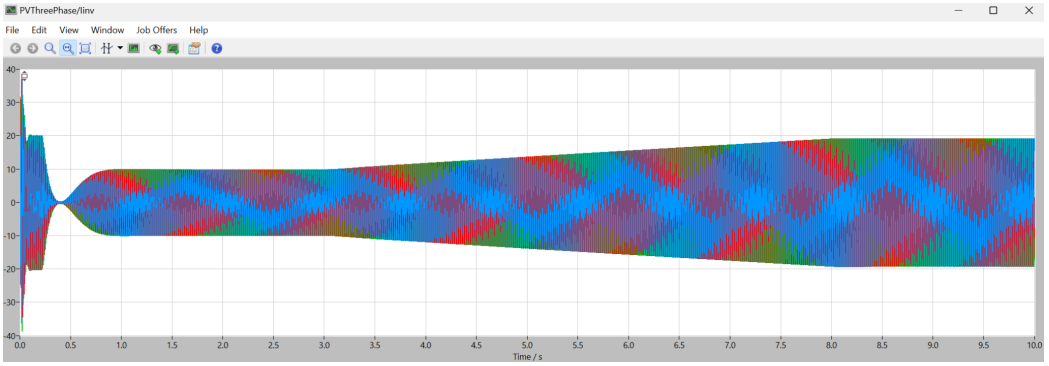


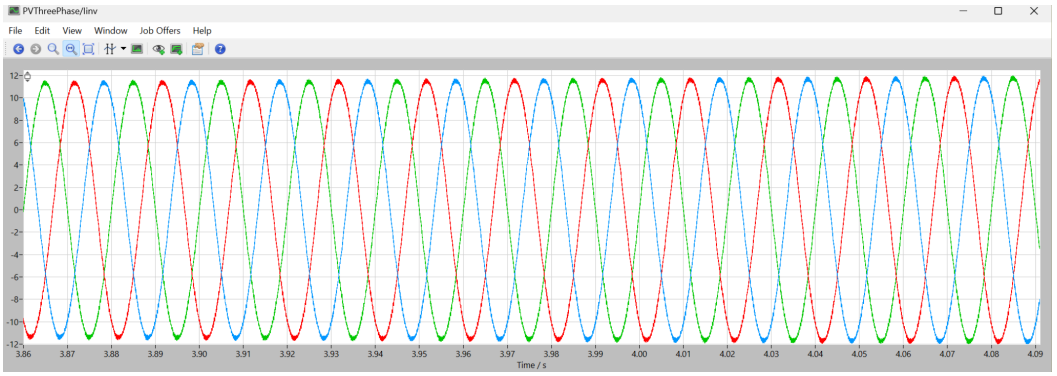
6. **Simulate and plot inverter currents** in the dq-reference frame.
    - Compare reference and measured currents
    - Demonstrate three operating conditions:



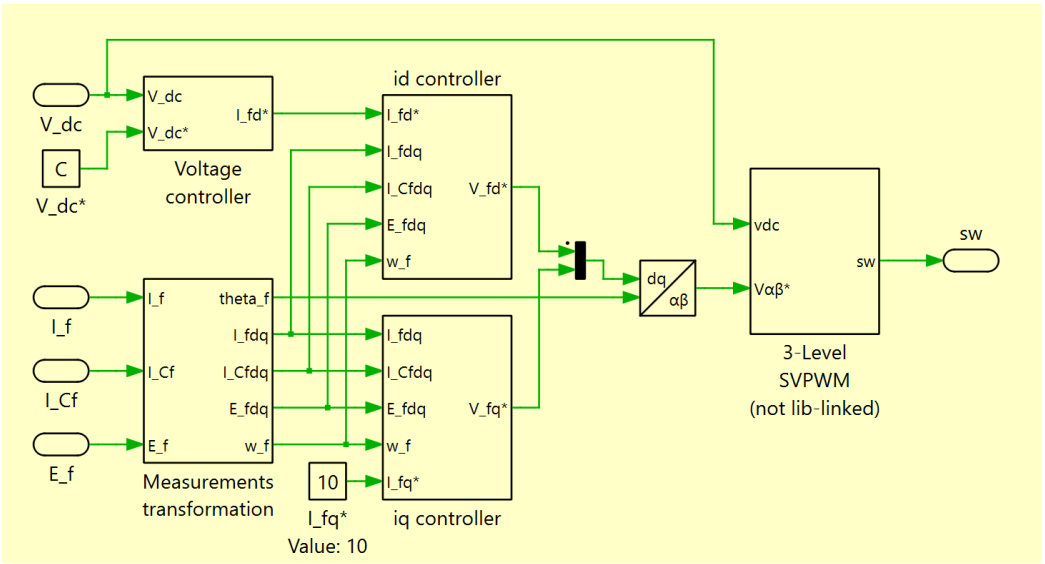
– In-phase current (unity power factor

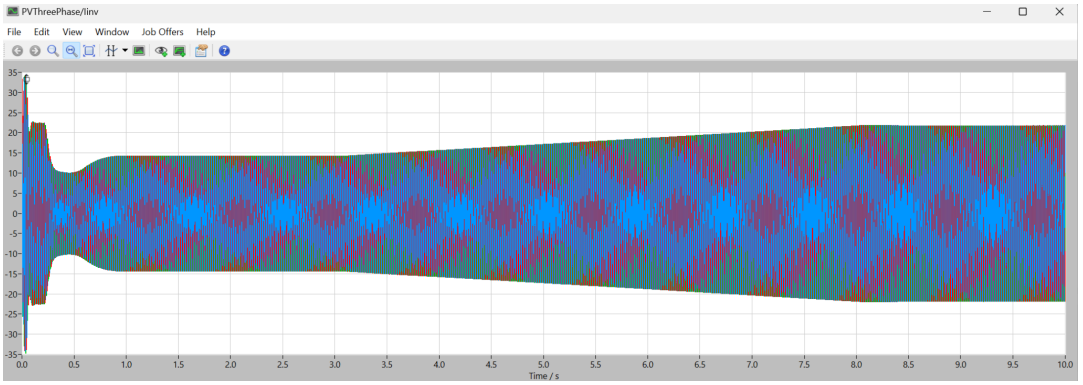


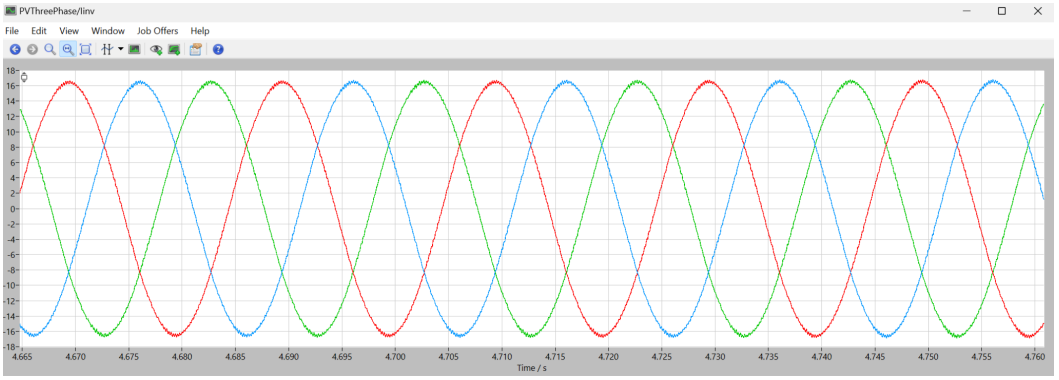




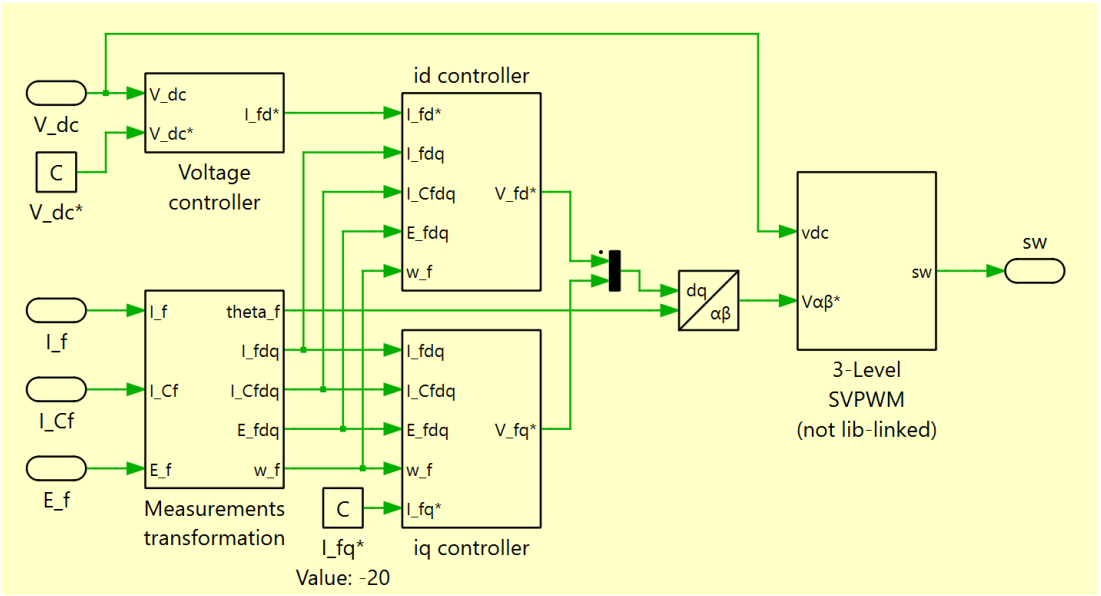
– Lagging current

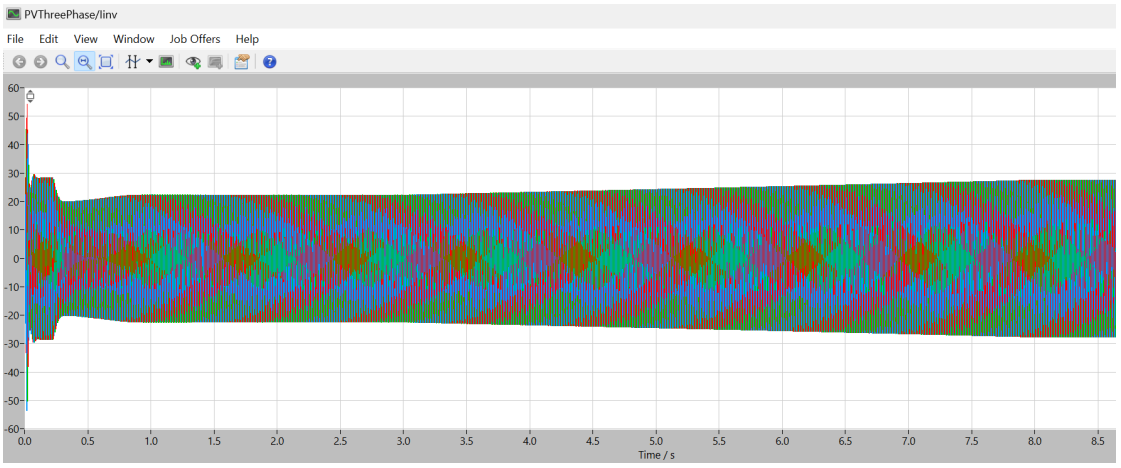


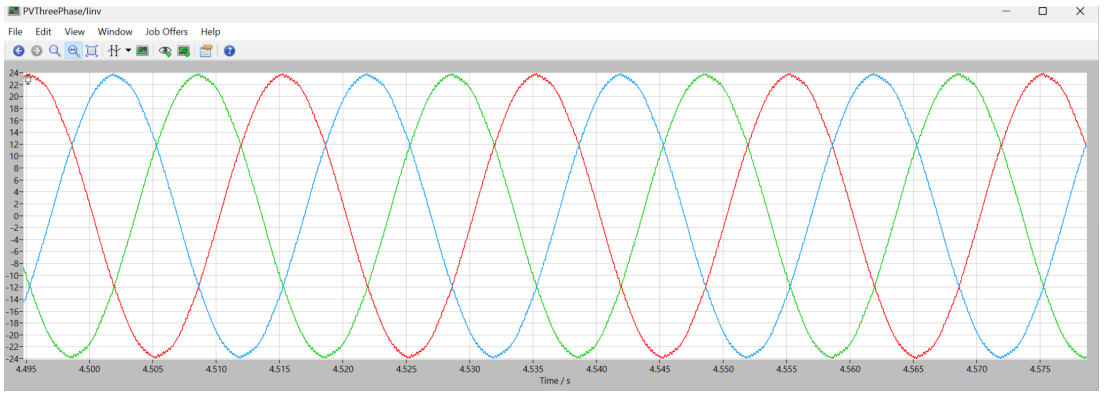




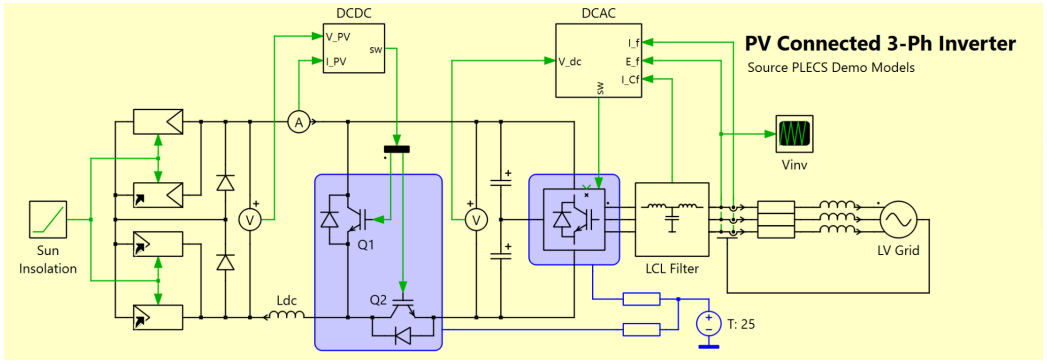
– Leading current

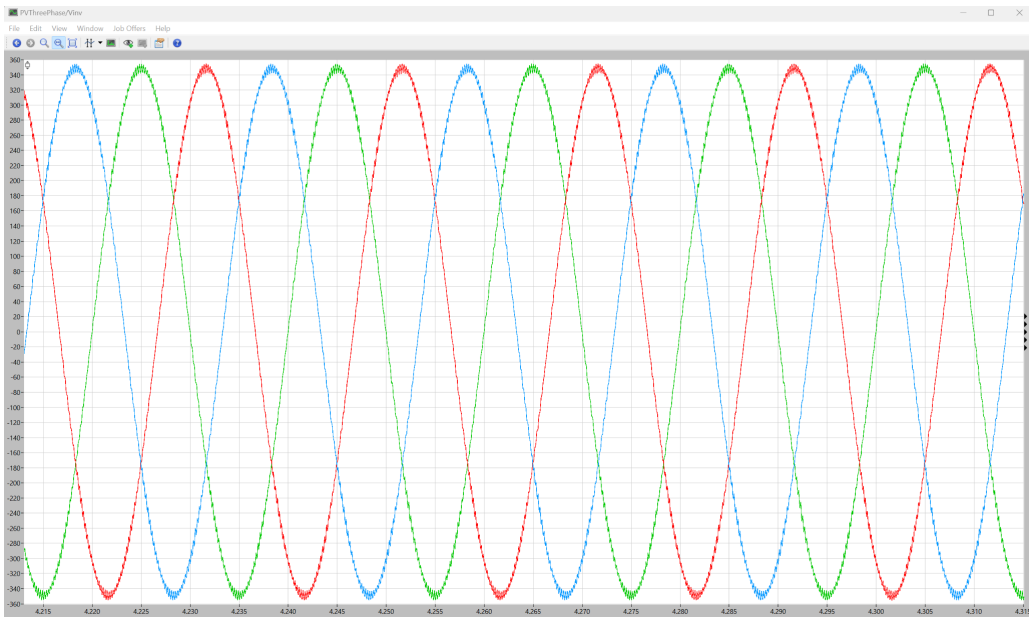


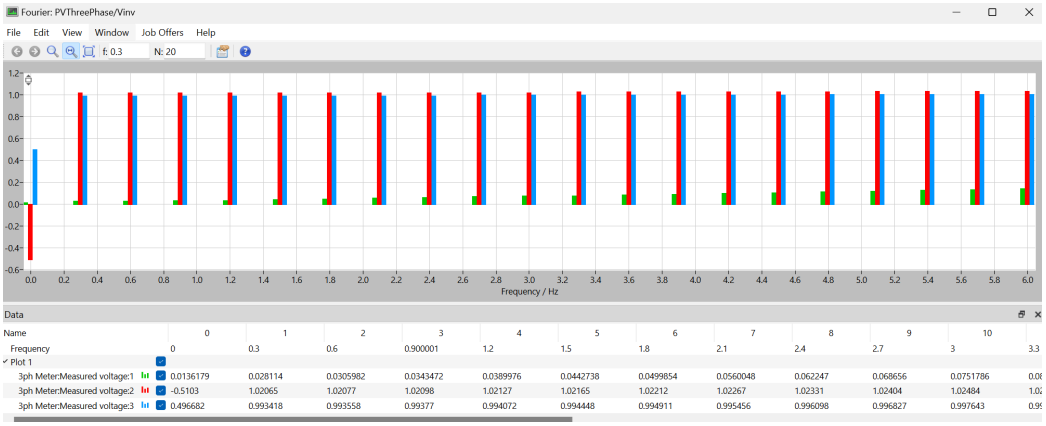




7. **Plot the inverter output voltage** (phase and line) in both time domain and frequency domain.
    - Perform FFT analysis on the time-domain waveform to evaluate harmonic content.







8. **Analyze the system behavior under overmodulation conditions**.
    - Show the effect of overmodulation on waveform distortion and control performance.
    - Support your analysis with simulation results.