

Elit Sobyak
A00314 177

24-Nov-2014
Digital Logic: Ass 5

Problem set:

Chapter 5: 1-11

Counter	Increment	Load	Out
0x2E	0xBF	0	0x2E
0010 1110	1011 1111	Load 0	Counter t Counter t+1 0x2E 0x2E

The next state of the machine

time	Counter	Increment	Load	Output	action
0	0x2E	0xBF	0	0x2E	inc(Counter)
1	0x2F	-	-	0x2F	

2) DFF @ t+1 output:
time t vs 1

Load	A	DFF _t	DFF _{t+1} = Out
1	a	b	a

- Load value of 1 jams the input in to the DFF
- The DFF changes the state at the rising edge of a clock cycle

3) $\frac{\text{Input}}{A}$

* If Input A is 1, no matter what Nor₆ Nor₅ together

6) The Control Code for the above
B

sci	OP	Label
11	11	0111

7) and 8)

time	Register Values				Control Code			Action
	A	B	C	D	Sel	OP	L1L2L3L4	
t	0x2F	0xED	0xF	0xA	00	01	0111	inc(A) → B, C, D
t+1	0x2F	0x30	0x30	0x30	01	01	0011	inc(B) → C, D
t+2	0x2F	0x30	0x31	0x31	10	00	1100	C → A, B
t+3	0x31	0x31	0x31	0x31	-	-	-	-

8) Control Codes for above

time	Control Code		
	Sel	OP	L1L2L3L4
t	00	01	0111
t+1	01	01	0011
t+2	10	00	1100

9) see 7

10)

time	Register Values				Control Code			Action
	A	B	C	D	DMax	RMax	Sub	
t	0x2F	0xED	0xF	0xA	00	10	0	add(A, C) → A
t+1	0x4E	0xED	0xF	0xA	10	01	1	Sub(C, B) → C
t+2	0x4E	0xED	0xCE	0xA	-	-	-	-

11)

time	Register Values					Control Code				Action
	A	B	C	D	Acc	RMax	DMax	Acc	Sub	
t	0x2F	0xED	0xF	0xA	-	11	1	1	0	0 → Acc
t+1	0x2F	0xED	0xF	0xA	0xA	01	10	1	1	Sub(Acc, B) → C
t+2	0x2F	0xED	0x4C	0xA	0xA	11	00	1	0	add(Acc, 0) → A
t+3	0x24	0xED	0x4C	0xA	0xA	-	-	-	-	-