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Digital Logic: 10/14

Problem Set:

Chapter 4: 1-8, 10-12

1)

Binary
$$\begin{array}{r} 10110 \\ + 0011 \\ \hline 1001 \\ 1001 \end{array}$$

Decimal
$$\begin{array}{r} 6 \\ + 3 \\ \hline 9 \end{array}$$

2)

Binary
$$\begin{array}{r} 1110 \\ + 0111 \\ \hline 0101 \end{array}$$

Decimal
$$\begin{array}{r} - 142 \\ + 7 \\ \hline - 135 \end{array}$$

3)

no overflow, 5 is within range of 4 bits

No, when there is an overflow the output is not correct. The front bit gets lobbed off and goes to the overflow indicator. The processor should tell the user that an overflow has occurred.

0100 0001
0011 0000
1100 1111
17 17

4) Hex

$$\begin{array}{r} 0x\ BA \\ + 0x\ 7F \\ \hline 0x\ 29 \end{array}$$

Decimal

$$\begin{array}{r} -86 \\ +127 \\ \hline 41 \end{array}$$

DA

$$\begin{array}{r} 1011\ 1010 \\ 0100\ 0101 \\ 0101\ 0110 \\ \hline 5\ 6 \\ 00\ 16 = -86 \end{array}$$

7F

$$\begin{array}{r} 0111\ 1111 \\ 1000\ 0000 \\ 1001\ 0001 \\ \hline 9\ 1 \end{array}$$

No PMS does not result in an overflow

5) Binary

$$\begin{array}{r} 1110 \\ +1001 \\ \hline 1\ 0111 \end{array}$$

Decimal

$$\begin{array}{r} -2 \\ + -7 \\ \hline -9 \end{array}$$

~~Yes! overflow~~

Yes! PMS did result in an overflow. The number -9 cannot be expressed with 4 bits in 2's complement.

6) Function table for Signed addition

X	Y	C _{in}	Sum
x	y	c _{in}	(x+y+c _{in}) mod 2 ⁷

~~Yes~~

1001 0110
0111 0001
0010 0010
0110 0111

Log2 table

7)

S_a	S_b	C_m	C_{out}	S_s	$Overflow$
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

Log2 Expression

$C_m \oplus C_{out}$

8)

10) The Subtraction Code is linked to the Carry-on line because we can force a carry in on the least significant number to accomplish the add-one the performs the negation.

11) It doesn't save any gates! They are the same.

12) The borrow signal tells you when the result is underflowed. This means the bit pattern representing the sum is not correct as it appears.