E.J. Sobylak
A00314177

8-Dec-2014
Digital Logic: Ass 8

Problem set:
Chapter 8: 1-10

1) Instruction Set Architecture
Registers that are visible:
Acc, Out, and PC

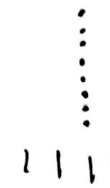
2) RTA
The components are:
PC, Inc, Amux, MAR, MBR, IR, Dmux, Acc, Out, SAB
Yes, the RTA includes the FSM

3) There are (4) four RT state transitions for each SAM instruction

4) The IR is loaded, always, in RTA state t_2.

5) The Hlt instruction is and-ed (&) together with the clock. When the Hlt instruction is executed it actually just disconnects the clock from the machine. The clock continues to run.

6) because the OP codes for the SAM are 4 bits (1 nibble) this means we can have; 0000



1111

15 total OP codes

7) FSA of SAM.V2

Word size: one byte (8 bits)

Memory: 32 bytes

Instruction Format Meaning

Lda M

10) The Logic expression I used in my SAM for the JAZ instruction was:

$PC = t_3 \wedge (JMPV(JAZ \wedge Acc \neq Zero))$

Also added the condition necessary for the JAZ instruction to preform a jump when the Acc is all zeroes.