

**DUE DATE:** See Canvas

**Problem 1** (12 points) Recall the various deadlock detection and prevention algorithms we've discussed in this course, and consider the following snapshot of a system with five processes (P1, P2, P3, P4, P5) and four resources (R1, R2, R3, R4).

There are no current outstanding queued unsatisfied requests.

Currently Available Resources

R1	R2	R3	R4
0	1	2	2

	Current Allocation				Max Need				Still Needs			
Process	R1	R2	R3	R4	R1	R2	R3	R4	R1	R2	R3	R4
P1	2	0	1	0	2	0	3	0				
P2	0	0	0	2	0	7	5	2				
P3	4	0	3	0	6	6	5	6				
P4	4	3	5	2	6	3	5	4				
P5	2	3	3	0	2	6	5	0				

- i) Is this system currently deadlocked, or can any process become deadlocked? Why or why not? If not deadlocked, give an execution order.

The execution order that does not become deadlocked is P1, P4, P5, P2, P3.

- ii) If a request from a process P1 arrives for (0, 4, 2, 0), can the request be immediately granted? Why or why not? If yes, show an execution order.
- iii) If a request from a process P2 arrives for (0, 1, 2, 0), can the request be immediately granted? Why or why not? If yes, show an execution order.

**Problem 2** (12 points) A process has these page accesses: 3 2 1 4 2 1 4 3 2 3 3 1 3 4 and there are three frames within the system. Using the **FIFO** replacement algorithm, what will be the final contents of the

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three frames after the execution of the given reference string? Show the successive contents of the frames in the table below. When there is no page faults, leave the column blank.

**Answer:**

	3	2	1	4	2	1	4	3	2	3	3	1	3	4	
F1	3	3	3	4				4	4			1		1	
F2		2	2	2				3	3			3		4	
F3			1	1				1	2			2		2	

**Problem 3** (12 points) Given the reference string of page accesses: 1 2 4 3 2 4 3 1 2 1 1 4 1 3 and a system with three page frames, what is the final configuration of the three frames after the **LRU** algorithm is applied? Use the table below to the successive contents of the frames. When there is no page faults, leave the column blank.

**Answer:**

	1	2	4	3	2	4	3	1	2	1	1	4	1	3	
F0	1	1	1	3				3	3			4		4	
F1		2	2	2				1	1			1		1	
F2			4	4				4	2			2		3	

**Problem 4** (13 points) In a demand-paged system, the TLB hit rate is 100% and accessing the TLB takes negligible time. It requires 8 milliseconds to service a page fault if an empty page is available or the replaced page is not dirty, and 16 milliseconds if the replaced page is dirty. Memory access time is 150 nanoseconds. = 0.000150ms  
The page to be replaced is dirty 60 percent of the time. The page fault rate is 1%. What is the effective access time in milliseconds?

Work:  $\text{avg page fault } t = 0.4 \times 8 + 0.6 \times 16 = 12.8 \text{ ms}$   
 $\text{avg page access } t = 0.99 \times 0.00015 + .01 (12.8 + .00015) = 0.12815 \text{ ms}$

Answer:  $\text{EAT} = 0(0 + 0.12815) + 1(0 + .00015 + .12815) = 0.1283 \text{ ms}$

**Problem 5** (13 points) The following page table is for a system with 16-bit virtual and physical addresses and with 4,096-byte pages. The reference bit is set to 1 when the page has been referenced. Periodically, a thread zeroes out all values of the reference bit. A dash for a page frame indicates the page is not in memory. The page-replacement algorithm is localized LRU, and all numbers are provided in decimal.

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Page	PageFrame	ReferenceBit
0	9	0
1	2	1
2	13	0
3	-	0
4	10	0
5	14	0
6	8	0
7	15	0
8	-	0
9	0	0
10	5	1
11	4	0
12	-	0
13	-	0
14	1	1
15	3	0

A. Convert the following virtual addresses (in hexadecimal) to the equivalent physical addresses(hex). [6 pts]

Virtual Address	Physical Address
0xE13C	x113C
0x5A9D	xE49D
0xF9D9	x39D9
0x7011	xF011
0xACA2	x5CA2

page offset = 12

B. Using the above addresses as a guide, provide an example of two logical address in different pages (in hexadecimal) that will result in a page fault.

Answer: 0xD18A 0x81BC

C. From what set of page frames will the LRU page-replacement algorithm will **not** choose in resolving a page fault?

Answer: page frames: 3, 8, 12, 13

**Problem 6** (12 points) Consider a demand-paging system with a paging disk that has an average access and transfer time of 15 milliseconds. Addresses are translated through a page table in main memory, with an access time of 1 microsecond. To improve this time, there is a TLB with negligible access time. Assume that 85

$$EAT = \frac{TLB \text{ miss ratio} (TLB \text{ lookup} + \text{page access } t) + TLB \text{ hit ratio} (TLB \text{ lookup} + MAT + \text{page access } t)}{15}$$

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percent of the accesses are in the associative memory and that, of those remaining, 10 percent (or 1.5 percent of the total) cause page faults.

What fraction of the references use the page table in memory? What is the effective memory access time?

**Answer:**

Fraction of the references use the page table in memory =

Effective Access Time =

**Problem 7 (9)** Consider the following page reference string:

7, 2, 3, 1, 2, 5, 3, 4, 6, 7, 7, 1, 0, 5, 4, 6, 2, 3..

Assuming demand paging with three frames, how many page faults would occur for the following replacement algorithms?

- LRU replacement
- Optimal replacement

	7	2	3	1	2	5	3	4	6	7	7	1	0	5	4	6	2	3
F0	7	7	7	1		1	3	3	3	7		7	7	5	5	5	2	2
F1		2	2	2		2	2	4	4	4		1	1	1	4	4	4	3
F2			3	3		5	5	5	6	6		6	0	0	0	6	6	6

LRU: Answer:

16 page faults

	7	2	3	1	2	5	3	4	6	7	7	1	0	5	4	6	2	3
F0	7	7	7	1		1		1	1	1			0		4	6	2	3
F1		2	2	2		5		5	5	5			5		5	5	5	5
F2			3	3		3		4	6	7			7		7	7	7	7

Optimal: Answer:

13 page faults

**Problem 8 (6 points)** Consider a disk queue holding requests to the following cylinders in the listed order: 116, 22, 3, 11, 75, 185, 99, 87. Using the C-SCAN scheduling algorithm, what is the order in

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which the requests are serviced, assuming the disk head is at cylinder 85 and moving upward through the cylinders? The cylinders are 0 to 199.

Use the graph below for a diagram. Assume each column includes 10 cylinders (i.e first one included 0-9 etc)

87, 99, 116, 185, 3, 11, 22, 75

Answer:

	0-19	20-39	40-59	60-79	80-99	100-119	120-139	140-159	160-179	180-199
1					Initial: 85					
2					87					
3					99					
4						116				
5										185
6	3									
7	11									
8		22								
9				75						

### Problem 9 (4 points)

- a. A system uses 32-bit logical addresses, a 16K byte ( $2^{14}$ ) page size, and 36-bit physical addresses (64 GB memory). What is the size of the page table?:

☒  $2^{22}$  entries ( $2^{36-14}$ ).

☐  $2^4$  entries ( $2^{36-32}$ ).

☐  $2^{18}$  entries ( $2^{32-14}$ ).

☐  $2^{14}$  entries

- b. Fill in the blanks:

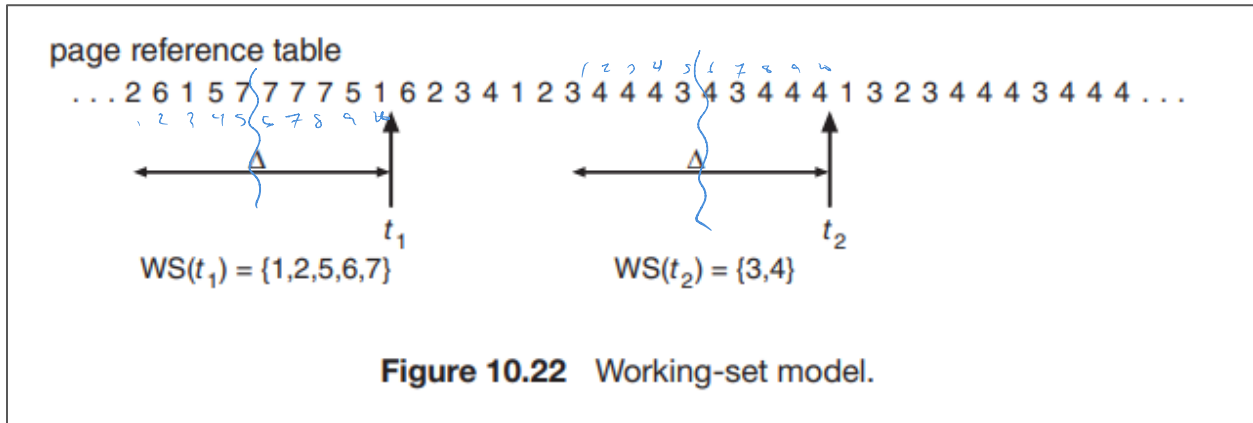
In Linux, the per-file File Control Block is termed FCB which contains details about the file such as permissions, size, dates etc.

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**Problem 10** (7 points)

a. Here's a **Working-Set model** from page 422 of your book:



For that example, obtain the value of  $WS(t_1)$  and  $WS(t_2)$  if  $\Delta = 5$  instead of 10.

Answer:  $WS(t_1) = \{1, 2, 5, 6, 7\}$   $WS(t_2) = \{3, 4\}$

b. Give a block diagram of a TLB. Mention where the input comes from and where does the output go. Identify where the page numbers are stored and where the corresponding frame numbers are stored.



The input comes from the logical address generated by the CPU. If the page # is found the frame # is available as output to the physical memory.

c. A system has 32 bit logical and physical addresses. The frames are 4096 bytes each. What is number of bits in the TLB input and output.

32 bit - 12 bit offset = 20 bits for input & output