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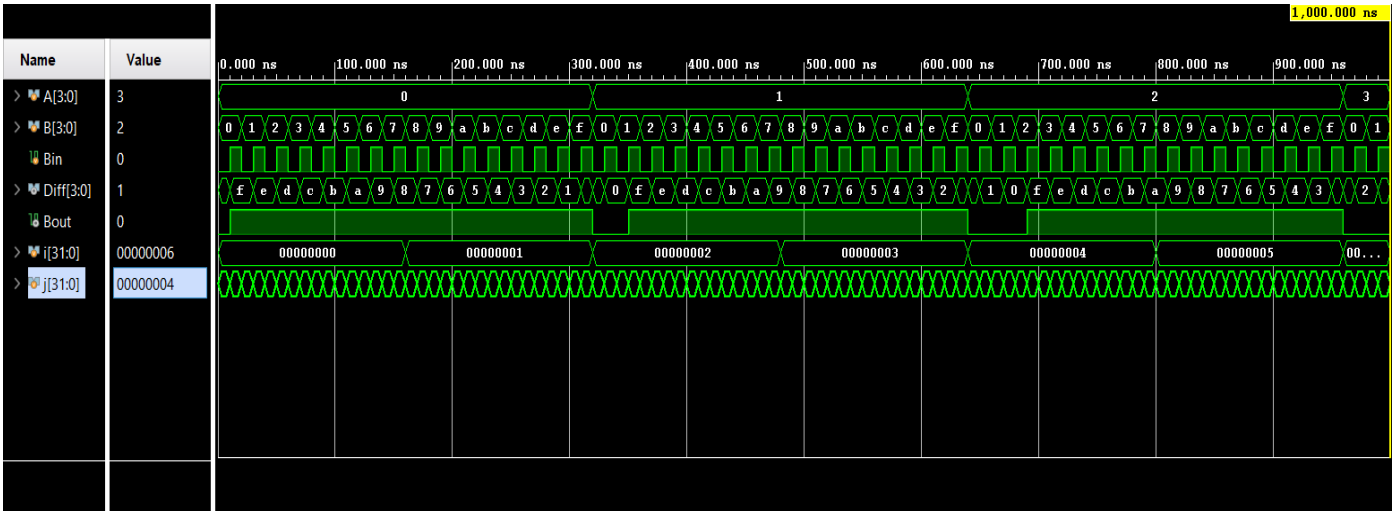

Lab-4.v

```
`timescale 1ns / 1ps

module full_sub_1b( input a, b, Bin, output Diff, Bout );
    assign Diff = a ^ b ^ Bin;
    assign Bout = ~a & ( b ^ Bin ) | b & Bin;

endmodule

module full_sub_4b( a, b, Bin, Diff, Bout );
    input [3:0] a, b;
    input Bin;
    output [3:0] Diff;
    output Bout;

    wire [2:0] Carry;

    full_sub_1b sub1( a[0], b[0], Bin, Diff[0], Carry[0] );
    full_sub_1b sub2( a[1], b[1], Carry[0], Diff[1], Carry[1] );
    full_sub_1b sub3( a[2], b[2], Carry[1], Diff[2], Carry[2] );
    full_sub_1b sub4( a[3], b[3], Carry[2], Diff[3], Bout );

endmodule

```

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Lab4_tb.v

```
`timescale 1ns / 1ps

module lab4_tb();
    reg [3:0] A, B;
    reg Bin;
    wire [3:0] Diff;
    wire Bout;

    full_sub_4b sub_4b( A, B, Bin, Diff, Bout );

    integer i, j;
    initial begin

        A = 4'b0000;
        B = 4'b0000;
        Bin = 1'b0;

        for ( i = 0; i < 16 ; i = i + 1 ) begin
            for ( j = 0; j < 16 ; j = j + 1 ) begin
                #10
                $monitor( "A: %b | B: %b | Bin: %b\nDiff: %b, Bout: %b\n\n", A, B, Bin, Diff, Bout );
                { A, B, Bin } = { A, B, Bin } + 1;

            end

        end

    end

endmodule
```