

## Lab5.v

```
module PFA( A, B, Cin, G, P, S );

    input A, B, Cin;
    output G, P, S;

    assign G = A & B;
    assign P = A ^ B;
    assign S = P ^ Cin;

endmodule

module CLA_Assign_Carries ( G, P, Cin, Carry, Cout );

    input [3:0] G, P;
    input Cin;
    output [2:0] Carry;
    output Cout;

    assign Carry[0] = G[0] / P[0] & Cin;
    assign Carry[1] = G[1] / P[1] & G[0] / P[1] & P[0] & Cin;
    assign Carry[2] = G[2] / P[2] & G[1] / P[1] & P[0] & G[0] / P[2] & P[1] & P[0] & Cin;
    assign Cout = G[3] / P[3] & G[2] / P[3] & P[2] & G[1] / P[3] & P[2] & P[1] & G[0] / P[3] & P[2] & P[1] & P[0] & Cin;

endmodule

module CLA_4b( A, B, Cin, Sum, Cout );

    input [3:0] A, B;
    input Cin;
    output [3:0] Sum;
    output Cout;

    wire [2:0] Carry;
    wire [3:0] G, P;

    PFA pfa_1( A[0], B[0], Cin, G[0], P[0], Sum[0] );
    PFA pfa_2( A[1], B[1], Carry[0], G[1], P[1], Sum[1] );
    PFA pfa_3( A[2], B[2], Carry[1], G[2], P[2], Sum[2] );
    PFA pfa_4( A[3], B[3], Carry[2], G[3], P[3], Sum[3] );

    CLA_Assign_Carries carry_logic( G, P, Cin, Carry, Cout );

endmodule
```

## Lab5\_tb.v

```
module CLA_4b_tb();

    reg [3:0] A, B;
    reg Cin;

    wire [3:0] Sum;
    wire Cout;

    CLA_4b cla( A, B, Cin, Sum, Cout );

    initial begin

        // Test 1
        Cin = 1'b0;
        A = 4'b0101;
        B = 4'b1001;

        $monitor( "A: %b\nB: %b\nCin: %b\n\nSum: %b\nCout: %b\n\n-----\n", A, B, Cin, Sum, Cout );
        #100;

        // Test 2
        Cin = 1'b1;
        A = 8'b0011;
        B = 8'b1001;

        $monitor( "A: %b\nB: %b\nCin: %b\n\nSum: %b\nCout: %b\n\n-----\n", A, B, Cin, Sum, Cout );
        #100;

        // Test 3
        Cin= 1'b1;
        A = 8'b0110;
        B = 8'b1011;

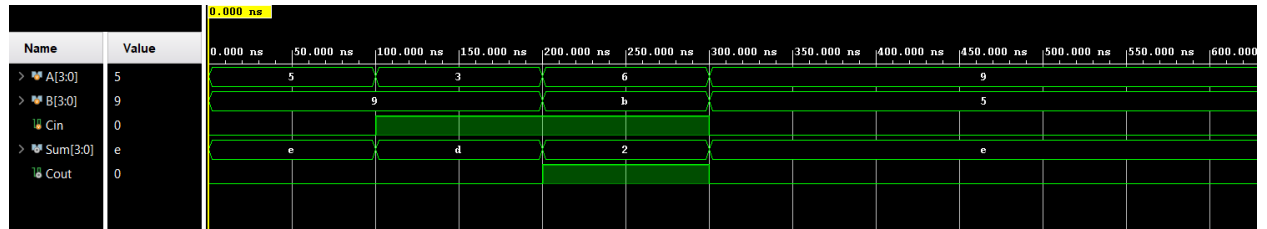
        $monitor( "A: %b\nB: %b\nCin: %b\n\nSum: %b\nCout: %b\n\n-----\n", A, B, Cin, Sum, Cout );
        #100;

        // Test 4
        Cin=1'b0;
        A = 8'b1001;
        B = 8'b0101;

        $monitor( "A: %b\nB: %b\nCin: %b\n\nSum: %b\nCout: %b\n\n-----\n", A, B, Cin, Sum, Cout );

    end
```

## Timing Chart



## TCL Console

A: 0101

B: 1001

Cin: 0

Sum: 1110

Cout: 0

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A: 0011

B: 1001

Cin: 1

Sum: 1101

Cout: 0

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A: 0011

B: 1001

Cin: 1

Sum: 1101

Cout: 0

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A: 0110

B: 1011

Cin: 1

Sum: 0010

Cout: 1

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A: 0110

B: 1011

Cin: 1

Sum: 0010

Cout: 1

-----

A: 0110

B: 1011

Cin: 1

Sum: 0010

Cout: 1

-----

A: 1001

B: 0101

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Cin: 0

Sum: 1110

Cout: 0

-----

A: 1001

B: 0101

Cin: 0

Sum: 1110

Cout: 0

-----

A: 1001

B: 0101

Cin: 0

Sum: 1110

Cout: 0

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A: 1001

B: 0101

Cin: 0

Abhi Rangarajan uxs876

Sum: 1110

Cout: 0

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