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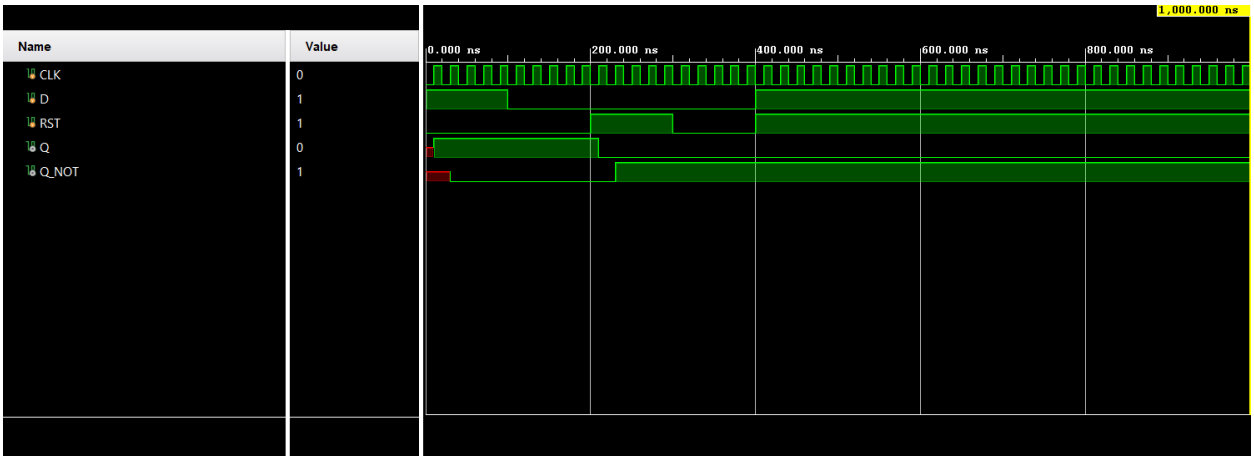
D-FF



TCL-Console:

D: 1

RST: 0

Q: x

Q_NOT: x

D: 1

RST: 0

Q: 1

Q_NOT: x

D: 1

RST: 0

Q: 1

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Q_NOT: 0

D: 0

RST: 0

Q: 1

Q_NOT: 0

D: 0

RST: 0

Q: 1

Q_NOT: 0

D: 0

RST: 1

Q: 1

Q_NOT: 0

D: 0

RST: 1

Q: 1

Q_NOT: 0

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D: 0

RST: 1

Q: 1

Q_NOT: 0

D: 0

RST: 1

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D: 0

RST: 1

Q: 0

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Q: 0

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Q: 0

Q_NOT: 1

D: 0

RST: 0

Q: 0

Q_NOT: 1

D: 1

RST: 1

Q: 0

Q_NOT: 1

D: 1

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RST: 1

Q: 0

Q_NOT: 1

D: 1

RST: 1

Q: 0

Q_NOT: 1

D: 1

RST: 1

Q: 0

Q_NOT: 1

D: 1

RST: 1

Q: 0

Q_NOT: 1

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Lab-3.v

```
`timescale 1ns / 1ps

module D_FF( CLK, D, RST, Q, Q_NOT );

  input CLK, D, RST;
  output reg Q, Q_NOT;

  always @ ( posedge CLK ) begin

    if ( RST ) begin

      Q <= 1'b0;

    end

    else if ( D ) begin

      Q <= 1'b1;

    end

    Q_NOT = !Q;

  end

endmodule
```

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Lab-3_tb.v

```
`timescale 1ns / 1ps


module D_FF_tb();

  reg CLK, D, RST;
  wire Q, Q_NOT;

  D_FF ff( CLK, D, RST, Q, Q_NOT );

  initial begin

    CLK = 1'b0;

    forever begin

      #10;
      CLK = !CLK; //This will generate a positive edge every 10ns

    end

  end

  initial begin

    // Test 1
    D = 1'b1;
    RST = 1'b0;
```

```
    $monitor( "D: %b\nRST: %b\n\nQ: %b\nQ_NOT: %b\n--------------------\n", D, RST, Q, Q_NOT );
    #100;

    // Test 2
    D = 1'b0;
    RST = 1'b0;
    $monitor( "D: %b\nRST: %b\n\nQ: %b\nQ_NOT: %b\n--------------------\n", D, RST, Q, Q_NOT );
    #100;

    // Test 3
    D = 1'b0;
    RST = 1'b1;
    $monitor( "D: %b\nRST: %b\n\nQ: %b\nQ_NOT: %b\n--------------------\n", D, RST, Q, Q_NOT );
    #100;

    // Test 4
    D = 1'b0;
    RST = 1'b0;
    $monitor( "D: %b\nRST: %b\n\nQ: %b\nQ_NOT: %b\n--------------------\n", D, RST, Q, Q_NOT );
    #100;

    // Test 5
    D = 1'b1;
    RST = 1'b1;
    $monitor( "D: %b\nRST: %b\n\nQ: %b\nQ_NOT: %b\n--------------------\n", D, RST, Q, Q_NOT );
    #100;

  end
endmodule
```