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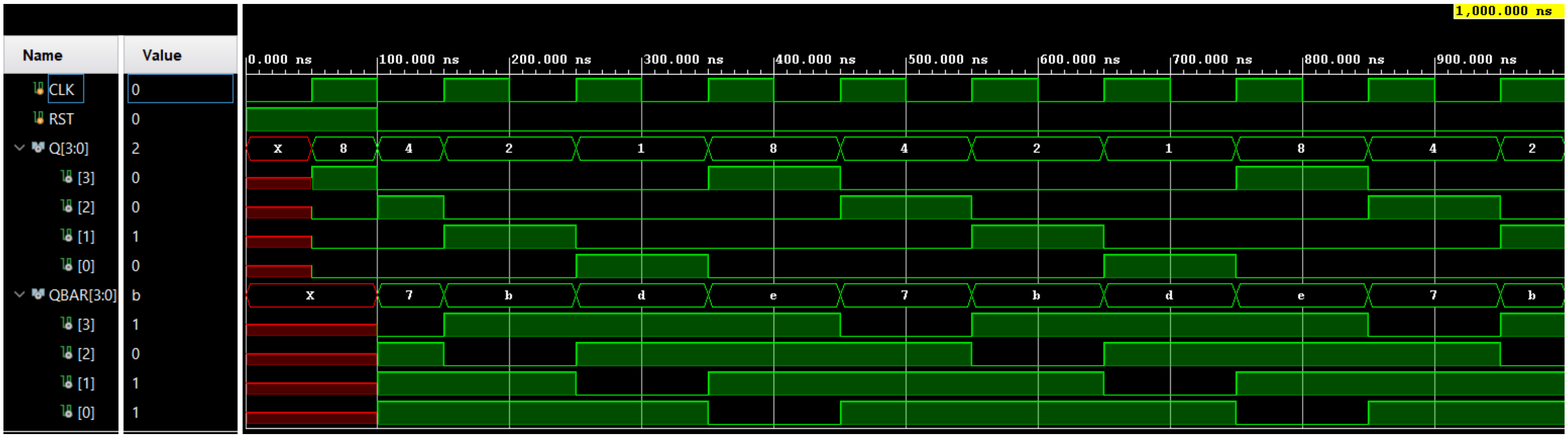
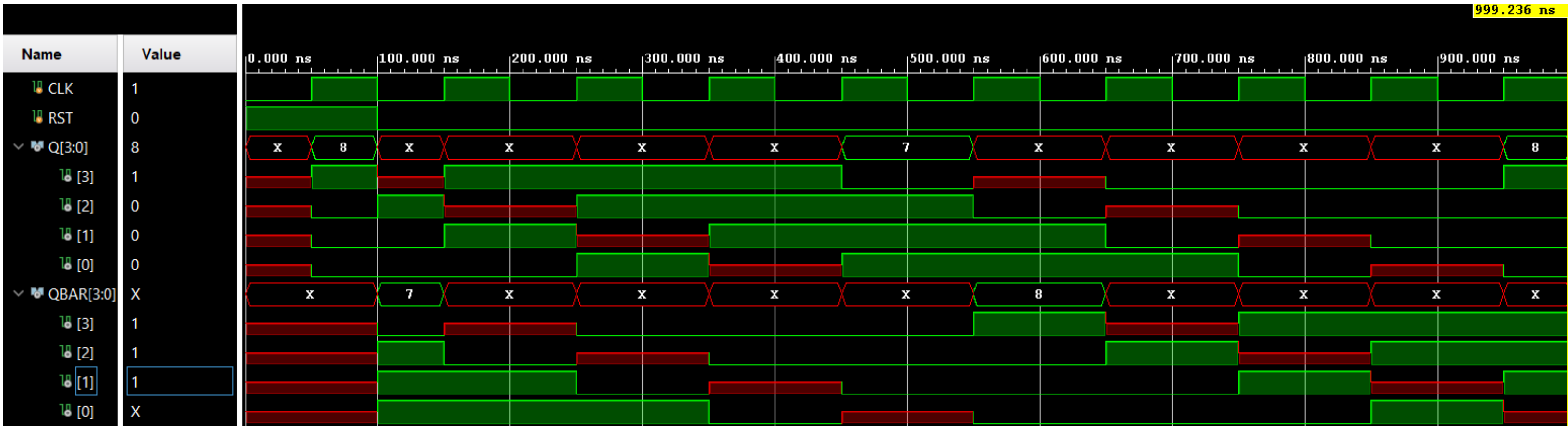
Ring Counter Timing Chart



Johnson Ring Counter Timing Chart



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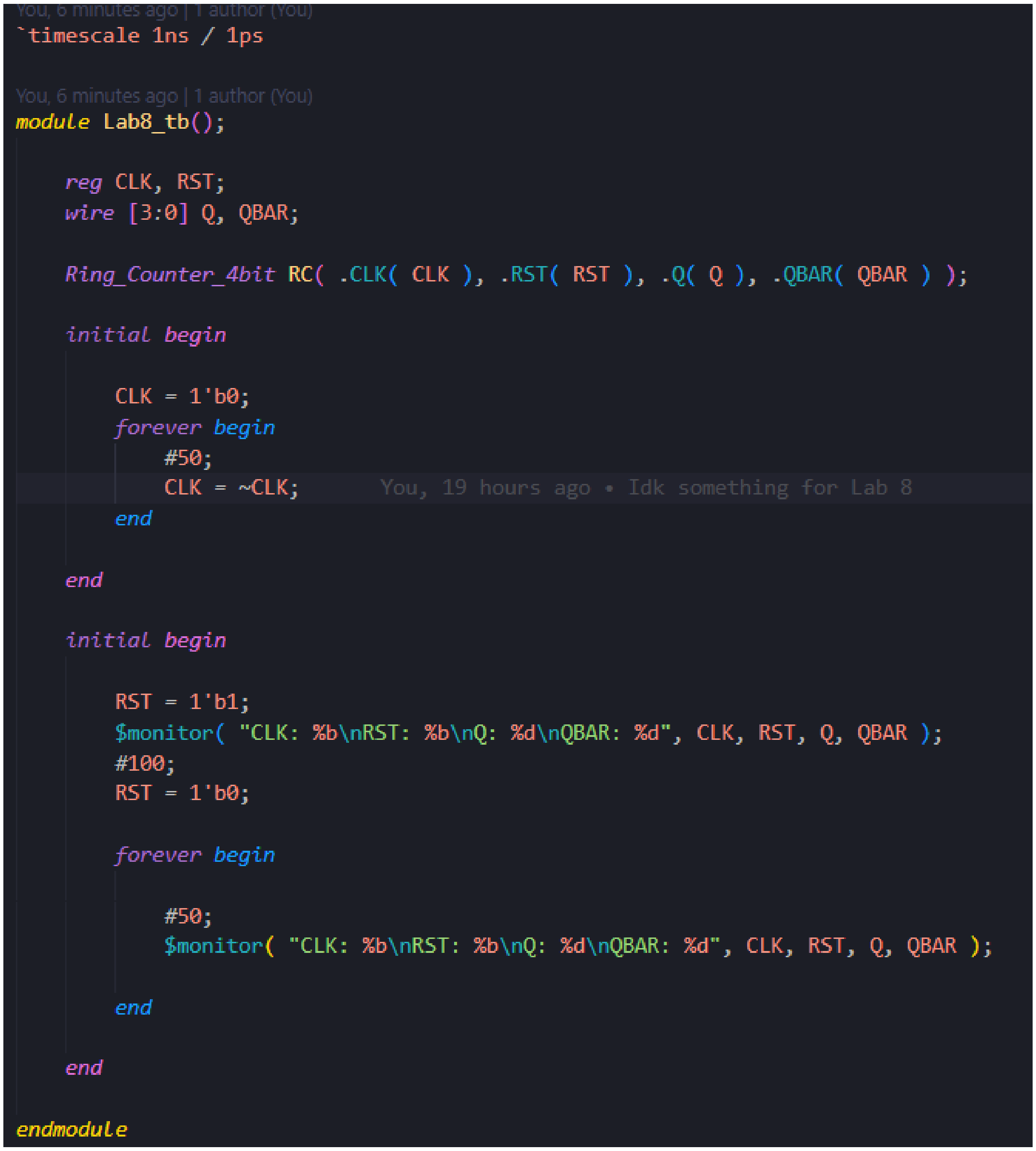
Lab8_tb.v



```
You, 6 minutes ago | 1 author (You)
`timescale 1ns / 1ps

You, 6 minutes ago | 1 author (You)
module Lab8_tb();

    reg CLK, RST;
    wire [3:0] Q, QBAR;

    Ring_Counter_4bit RC( .CLK( CLK ), .RST( RST ), .Q( Q ), .QBAR( QBAR ) );

    initial begin

        CLK = 1'b0;
        forever begin
            #50;
            CLK = ~CLK;       You, 19 hours ago • Idk something for Lab 8
        end

    end

    initial begin

        RST = 1'b1;
        $monitor( "CLK: %b\nRST: %b\nQ: %d\nQBAR: %d", CLK, RST, Q, QBAR );
        #100;
        RST = 1'b0;

        forever begin

            #50;
            $monitor( "CLK: %b\nRST: %b\nQ: %d\nQBAR: %d", CLK, RST, Q, QBAR );

        end

    end

endmodule
```

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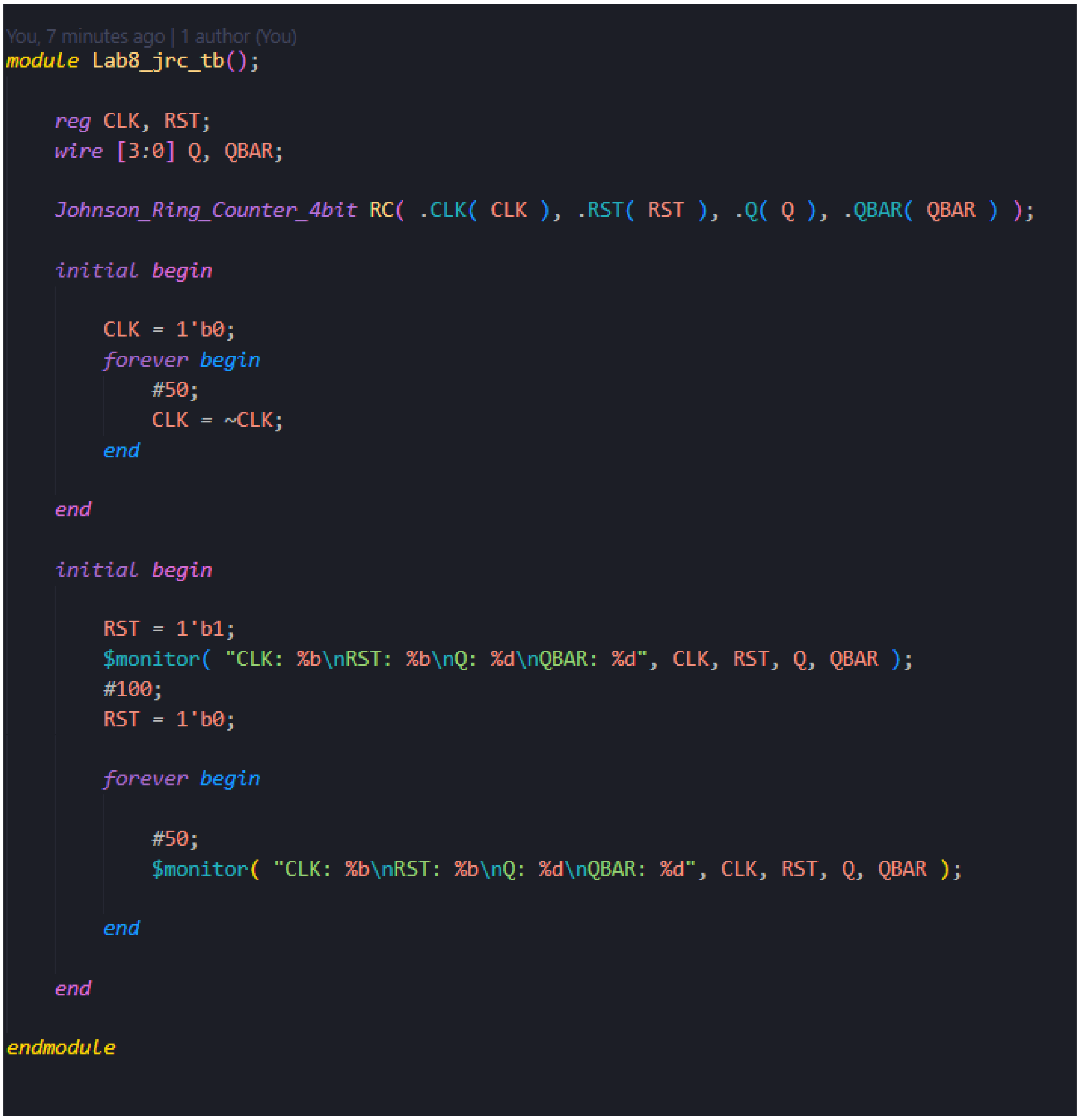

You, 7 minutes ago | 1 author (You)

```
module Lab8_jrc_tb();

    reg CLK, RST;
    wire [3:0] Q, QBAR;

    Johnson_Ring_Counter_4bit RC( .CLK( CLK ), .RST( RST ), .Q( Q ), .QBAR( QBAR ) );

    initial begin

        CLK = 1'b0;
        forever begin
            #50;
            CLK = ~CLK;
        end

    end

    initial begin

        RST = 1'b1;
        $monitor( "CLK: %b\nRST: %b\nQ: %d\nQBAR: %d", CLK, RST, Q, QBAR );
        #100;
        RST = 1'b0;

        forever begin

            #50;
            $monitor( "CLK: %b\nRST: %b\nQ: %d\nQBAR: %d", CLK, RST, Q, QBAR );

        end

    end

endmodule
```

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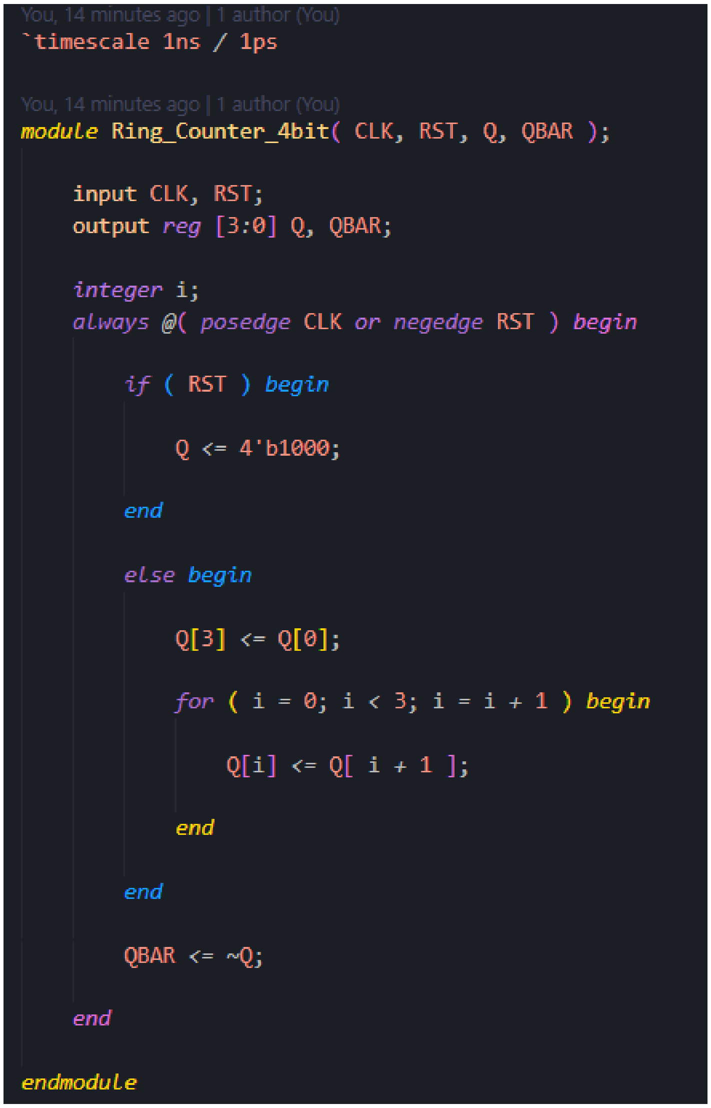
Lab8.v



```
You, 14 minutes ago | 1 author (You)
`timescale 1ns / 1ps

You, 14 minutes ago | 1 author (You)
module Ring_Counter_4bit( CLK, RST, Q, QBAR );

    input CLK, RST;
    output reg [3:0] Q, QBAR;

    integer i;
    always @( posedge CLK or negedge RST ) begin

        if ( RST ) begin

            Q <= 4'b1000;

        end

        else begin

            Q[3] <= Q[0];

            for ( i = 0; i < 3; i = i + 1 ) begin

                Q[i] <= Q[ i + 1 ];

            end

        end

        QBAR <= ~Q;

    end

endmodule
```

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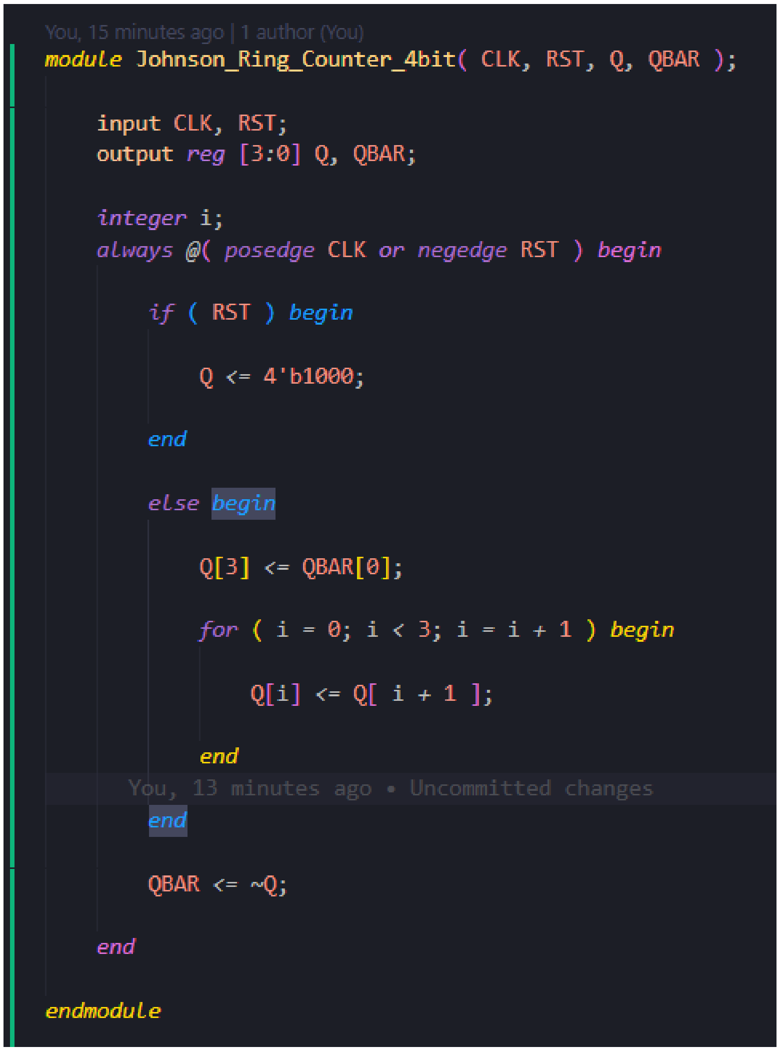

```
You, 15 minutes ago | 1 author (You)
module Johnson_Ring_Counter_4bit( CLK, RST, Q, QBAR );

    input CLK, RST;
    output reg [3:0] Q, QBAR;

    integer i;
    always @( posedge CLK or negedge RST ) begin

        if ( RST ) begin

            Q <= 4'b1000;

        end

        else begin

            Q[3] <= QBAR[0];

            for ( i = 0; i < 3; i = i + 1 ) begin

                Q[i] <= Q[ i + 1 ];

            end
      You, 13 minutes ago • Uncommitted changes
        end

        QBAR <= ~Q;

    end

endmodule
```