ELL-201

Table 20 Monday Batch

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Experiment 7 / Lab Project

Aim:- To simulate a Synchronous 4-bit Gray-Code Counter

Procedure:-

Knowing the properties of a S-R Latch. We created truth tables and Karnaugh Maps and deduced logic of S_n and R_n in terms of q_n & $\bar{q}_n$ for $n = 0, 1, 2, 3$. Then we wrote the verilog code in Quartus Software and simulated it on the CPLD module

The module sr_flip_flop is the instantiation for a SR Flip Flop. The always block has the condition for set and reset. The other two conditions are not defined since one of them will be memory state which need not be defined and the other one is invalid and won't occur in our case.

The module gcount is the instantiation for the grey code counter. It uses 4 SR Flip flops, and the values of S & R are derived using K maps. It's a Synchronous counter, so all of them are connected to the same clock.

Observations:-

The Output pins 24, 25, 26, 27 were connected to g0, g1, g2, g3 respectively, and the observation was noted in the table.

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```
module gcount(input gclock, output g0, output g1,output g2, output g3);
    sr_flip_flop sr0(~(g1^g2^g3),g1^g2^g3,gclock,g0);
    sr_flip_flop sr1((g0)&(~(g2^g3)),g0&(g2^g3),gclock,g1);
    sr_flip_flop sr2((~g0)&(g1)&(~g3),(~g0)&(g1)&(g3),gclock,g2);
    sr_flip_flop sr3((~g0)&(~g1)&(g2),(~g0)&(~g1)&(~g2),gclock,g3);
endmodule


module sr_flip_flop( input s, input r, input srclk, output reg srQ);
    always@(posedge srclk)
        begin
            if(s && (~r))
            srQ<=1;
            else if((~s) && r)
            srQ<=0;
        end
endmodule
```

Exp 7

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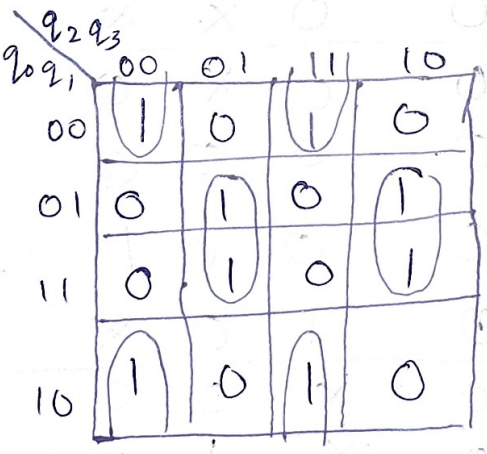
$q_3\ q_2\ q_1\ q_0$		$d_3\ d_2\ d_1\ d_0$
0 0 0 0	→	0 0 0 1
0 0 0 1	→	0 0 1 1
0 0 1 1	→	0 0 1 0
0 0 1 0	→	0 1 1 0
0 1 1 0	→	0 1 1 1
0 1 1 1	→	0 1 0 1
0 1 0 1	→	0 1 0 0
0 1 0 0	→	1 1 0 0
1 1 0 0	→	1 1 0 1
1 1 0 1	→	1 1 1 1
1 1 1 1	→	1 1 1 0
1 1 1 0	→	1 0 1 0
1 0 1 0	→	1 0 1 1
1 0 1 1	→	1 0 0 1
1 0 0 1	→	1 0 0 0
1 0 0 0	→	0 0 0 0

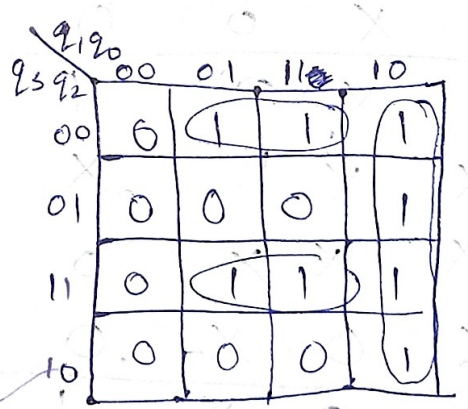
6/11 Shakti

For d_0



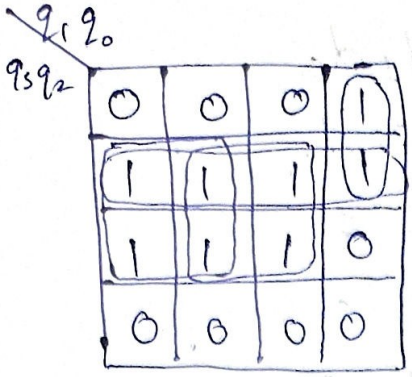
$$d_0 = \bar{q}_1\bar{q}_2\bar{q}_3 + q_1\bar{q}_2q_3 + \bar{q}_1q_2q_3 + q_1q_2\bar{q}_3$$

For d_1



$$d_1 = q_1\bar{q}_0 + q_0\bar{q}_2\bar{q}_3 + q_0q_2q_3$$

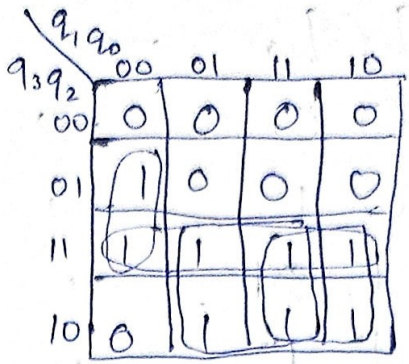
For d_2



$$d_2 = q_2\bar{q}_3 + \bar{q}_1q_2 + q_0q_2 + \bar{q}_0q_1q_3$$

$0 \to 1$	$S=1$	$R=0$
$1 \to 0$	$S=0$	$R=1$
$0 \to 0$	$S=0$	$R=X$
$1 \to 1$	$S=X$	$R=0$

For d_3



$$d_3 = q_2q_3 + q_0q_3 + q_1q_3 + \bar{q}_0\bar{q}_1q_2$$

S_3	S_2	S_1	S_0	R_3	R_2	R_1	R_0
0	0	0	1	X	X	X	0
0	0	1	X	X	X	0	0
0	0	X	0	X	X	0	1
0	1	X	0	X	0	0	X
0	X	X	1	X	0	0	0
0	X	0	X	X	0	1	0
0	X	0	0	X	0	X	1
1	X	0	0	0	0	X	X
X	X	0	1	0	0	X	0
X	X	1	X	0	0	0	0
X	X	X	0	0	0	0	1
X	0	X	0	0	1	0	X
X	0	X	1	0	X	0	0
X	0	0	X	0	X	1	0
X	0	0	0	0	X	X	1
0	0	0	0	1	X	X	X

For S_3

q_3q_2 \ q_1q_0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	X	X	X	X
10	0	X	X	X

$S_3 = \bar{q}_0 \bar{q}_1 q_2$

For S_2

q_3q_2 \ q_1q_0	00	01	11	10
00	0	0	0	1
01	X	X	X	X
11	X	X	X	0
10	0	0	0	0

$S_2 = \bar{q}_0 q_1 \bar{q}_3$

For S_1

q_3q_2 \ q_1q_0	00	01	11	10
00	0	1	X	X
01	0	0	0	X
11	0	1	X	X
10	0	0	0	X

$S_1 = q_0 \bar{q}_2 \bar{q}_3 + q_0 q_2 q_3$

$= q_0 \overline{(q_2 \oplus q_3)}$

For S_0

q_3q_2 \ q_1q_0	00	01	11	10
00	1	X	0	0
01	0	0	X	1
11	1	X	0	0
10	0	0	X	1

$S_0 = \bar{q}_1 \bar{q}_2 \bar{q}_3 + q_1 q_2 \bar{q}_3 + \bar{q}_1 q_2 q_3 + q_1 \bar{q}_2 q_3$

$= \overline{(q_1 \oplus q_2 \oplus q_3)}$

For R_3

q_3q_2 \ q_1q_0	00	01	11	10
00	X	X	X	X
01	0	X	X	X
11	0	0	0	0
10	1	0	0	0

$R_3 = \bar{q}_0 \bar{q}_1 \bar{q}_2$

For R_2

q_3q_2 \ q_1q_0	00	01	11	10
00	X	X	X	0
01	0	0	0	0
11	0	0	0	1
10	X	X	X	X

$R_2 = \bar{q}_0 q_1 q_3$

For R_1

q_3q_2 \ q_1q_0	00	01	11	10
00	X	0	0	0
01	X	X	1	0
11	X	0	0	0
10	X	X	1	0

$R_1 = q_0 q_2 \bar{q}_3 + q_0 \bar{q}_2 q_3 + q_0 (q_2 \oplus q_3)$

For R_0

q_3q_2 \ q_1q_0	00	01	11	10
00	0	0	1	X
01	X	1	0	0
11	0	0	1	X
10	X	1	0	0

$R_0 = q_1 \bar{q}_2 \bar{q}_3 + \bar{q}_1 q_2 \bar{q}_3 + q_1 q_2 q_3 + \bar{q}_1 \bar{q}_2 \bar{q}_3 = \bar{q}_1 (q_2 \oplus q_3) + q_1 (q_2 \oplus q_3)$

$R_0 = q_1 \oplus q_2 \oplus q_3$

Observation Table

Led 4 (27)	Led 3 (26)	Led 2 (25)	Led 1 (Pin 24)
q_3	q_2	q_1	q_0
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0

Circuit Diagram