

Name: Ningyuan Zhang

Section: A

Date: 4/25/2017

Instructor: Akhilesh Tyagi

Project B Lab Report

Tests without Hazard and Forwarding(Part 2 and 3):

The out put of U:\cpre381\projectB\ASM Files\Pipeline Test\test.asm:

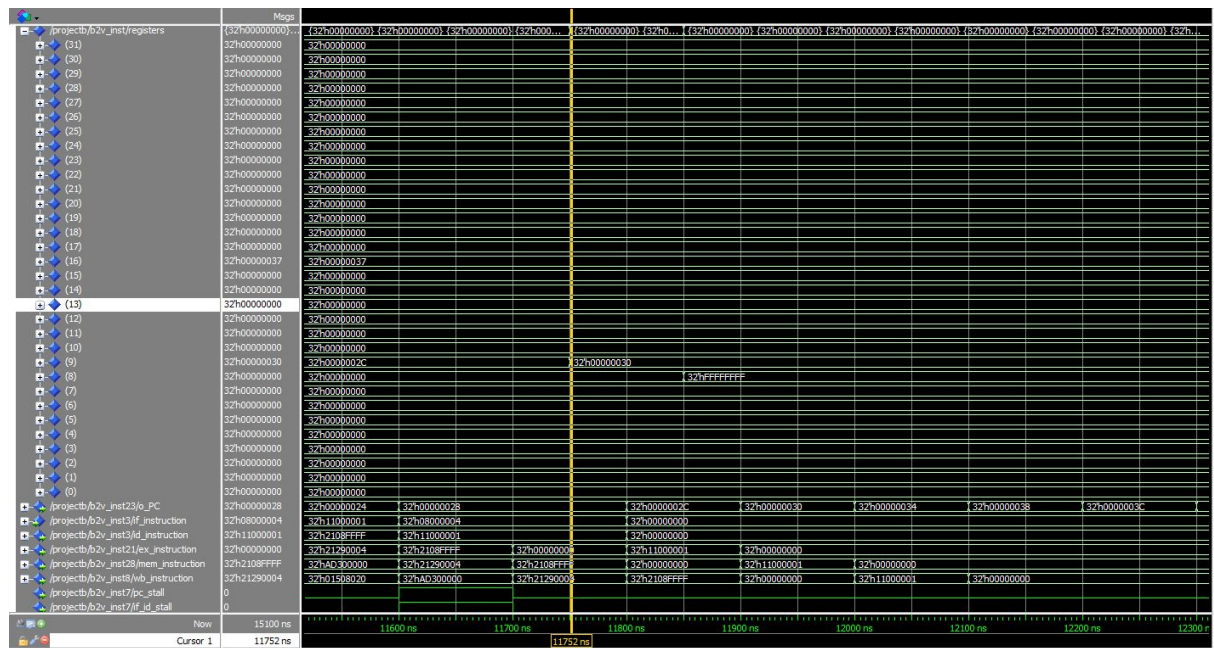
Registers	Coproc 1	Coproc 0	
Name	Number	Value	
\$zero	0	0x00000000	
\$at	1	0x10010000	
\$v0	2	0x00000000	
\$v1	3	0x00000000	
\$a0	4	0x00000000	
\$a1	5	0x00000000	
\$a2	6	0x00000000	
\$a3	7	0x00000000	
\$t0	8	0x00000000	
\$t1	9	0x1001002c	
\$t2	10	0x0000000a	
\$t3	11	0x00000000	
\$t4	12	0x00000000	
\$t5	13	0x10010000	
\$t6	14	0x00000000	
\$t7	15	0x00000000	
\$s0	16	0x00000037	
\$s1	17	0x00000000	
\$s2	18	0x00000000	
\$s3	19	0x00000000	
\$s4	20	0x00000000	
\$s5	21	0x00000000	
\$s6	22	0x00000000	
\$s7	23	0x00000000	
\$t8	24	0x00000000	
\$t9	25	0x00000000	
\$k0	26	0x00000000	
\$k1	27	0x00000000	
\$gp	28	0x10008000	
\$sp	29	0x7ffffeffc	
\$fp	30	0x00000000	
\$ra	31	0x00000000	
pc		0x00400038	
hi		0x00000000	
lo		0x00000000	

The result of my 5-stage-pipeline without hazard and forwarding:

Instance	Design unit	Design
- projectb	projectb(b...	Arch
+ b2v_inst	register_fil...	Arch
+ b2v_inst15	branch_co...	Arch
+ b2v_inst19	alu(mixed)	Arch
+ b2v_inst21	id_ex(mixed)	Arch
+ b2v_inst22	mux21_5bi...	Arch
+ b2v_inst23	pc_reg(mix...	Arch
+ b2v_inst24	and_2(mixed)	Arch
+ b2v_inst28	ex_mem(mi...	Arch
+ b2v_inst29	mux21_32...	Arch
+ b2v_inst3	if_id(mixed)	Arch
+ b2v_inst30	mux21_32...	Arch
+ b2v_inst31	adder_32(...	Arch
+ b2v_inst33	sll_2(mixed)	Arch
+ b2v_inst34	jumpaddrg...	Arch
+ b2v_inst35	sll_2(mixed)	Arch
+ b2v_inst36	sign_exten...	Arch
+ b2v_inst37	main_contr...	Arch
+ b2v_inst39	sign_exten...	Arch
+ b2v_inst4	mux21_32...	Arch
+ b2v_inst40	adder_32(...	Arch
+ b2v_inst44	dmem(beh...	Arch
+ b2v_inst45	imem(beh...	Arch
+ b2v_inst46	mux31_32...	Arch
+ b2v_inst47	mux31_32...	Arch
+ b2v_inst6	mux21_32...	Arch
+ b2v_inst8	mem_wb(m...	Arch
standard	standard	Pack
textio	textio	Pack
std_logic_1164	std_logic_1...	Pack
numeric_std	numeric_std	Pack
std_logic_arith	std_logic_a...	Pack
std_logic_unsigned	std_logic_u...	Pack

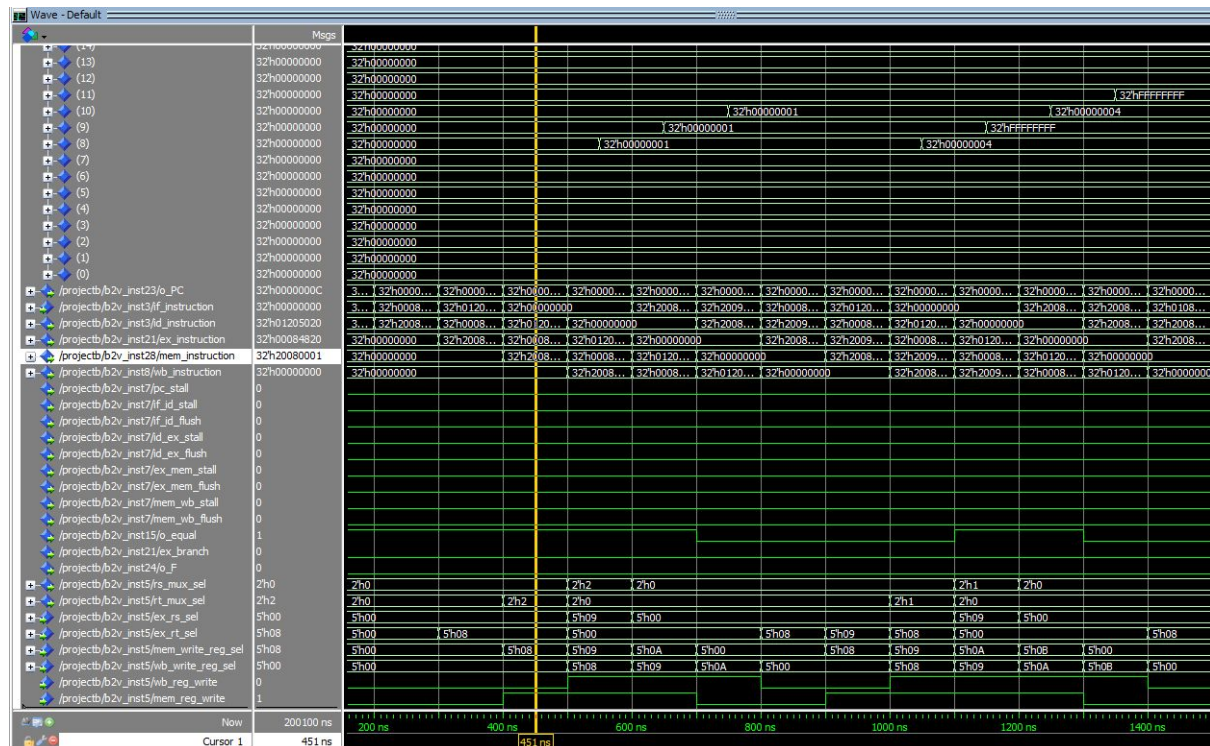
In this part, I originally put the `ex_branch` into the and gate after comparator, but because the comparators' signals were from id stage which is 1 cycle quicker than ex stage that sent `ex_branch`, and this caused that the branch will never achieve, so I switched the `ex_branch` with `id_branch` and it worked as it should.

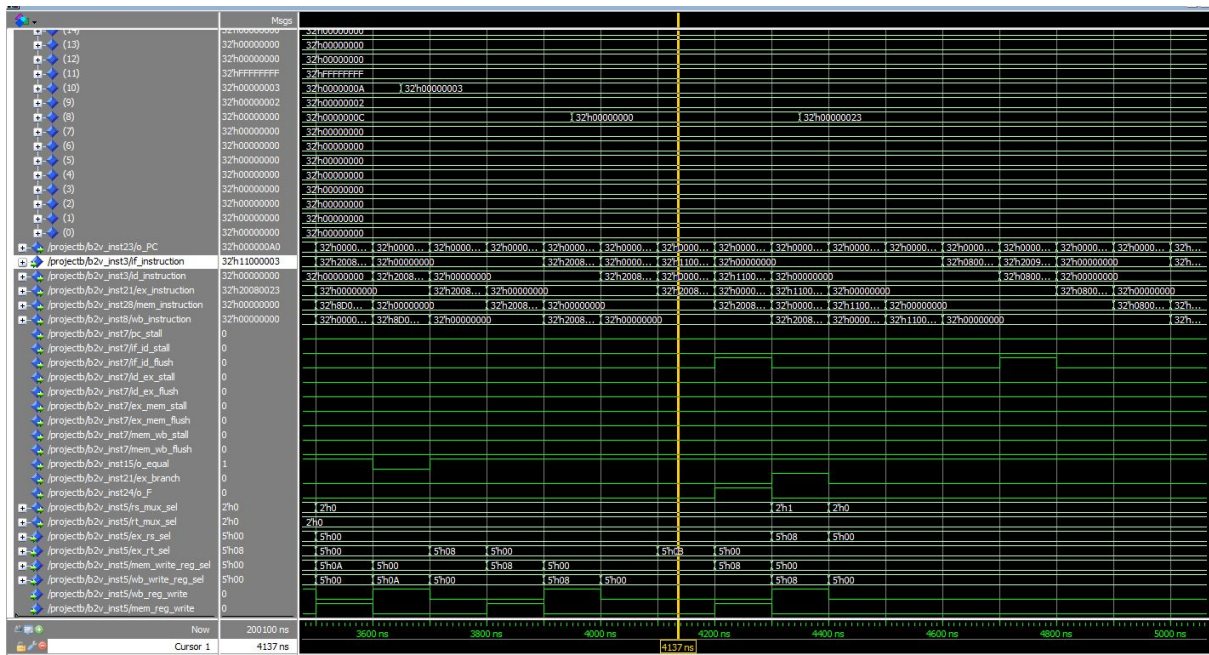
The result of running summation with all correct forwarding and hazard detection:



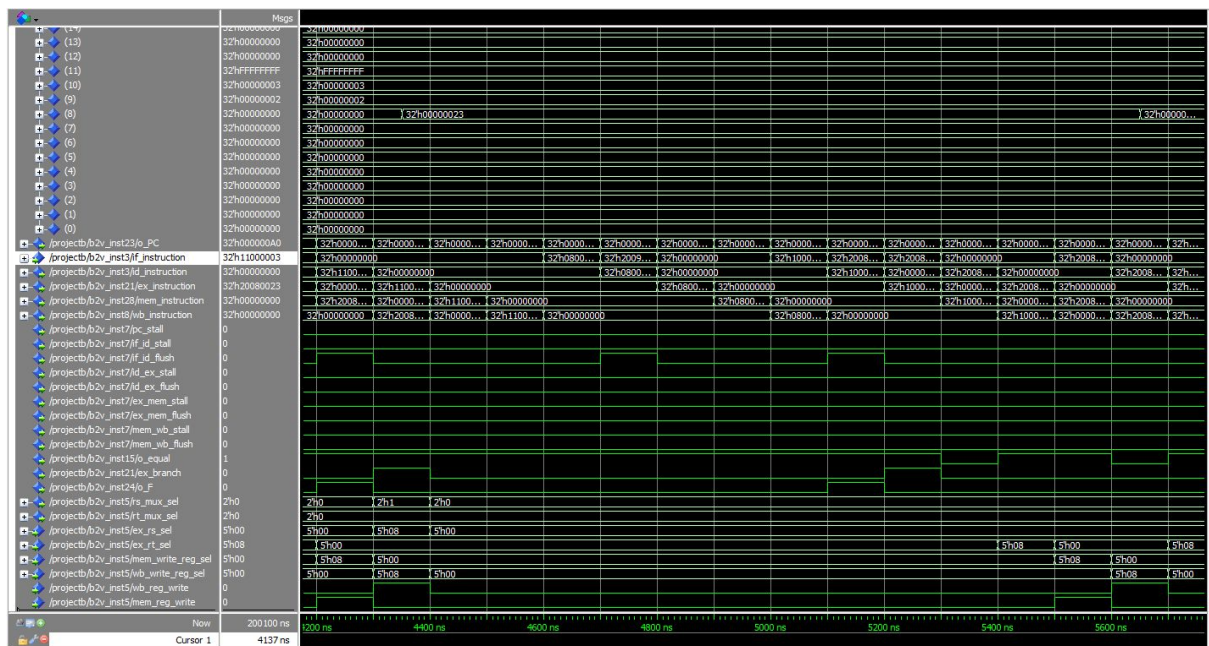
In this part, I actually used the HDandFUtest first to test my forwarding and hazard. with the help of TAs, I corrected all logic mistakes and errors inside the forwarding unit and hazard detection unit.

The result from HDandFUtest.asm (Part 4 and 5):





and this is the branch test of forwarding



other branch and jump test of hazard

projectb	projectb(bdf_type)
+ b2v_inst	register_file(mixed)
+ b2v_inst15	branch_comparator(mixed)
+ b2v_inst19	alu(mixed)
+ b2v_inst21	id_ex(mixed)
+ b2v_inst22	mux21_5bit(mixed)
+ b2v_inst23	pc_reg(mixed)
+ b2v_inst24	and_2(mixed)
+ b2v_inst28	ex_mem(mixed)
+ b2v_inst29	mux21_32bit(mixed)
+ b2v_inst3	if_id(mixed)
+ b2v_inst30	mux21_32bit(mixed)
+ b2v_inst31	adder_32(mixed)
+ b2v_inst33	sll_2(mixed)
+ b2v_inst34	jumpaddrgrnt(mixed)
+ b2v_inst35	sll_2(mixed)
+ b2v_inst36	sign_extender_26_32(mixed)
+ b2v_inst37	main_control(mixed)
+ b2v_inst39	sign_extender_16_32(mixed)
+ b2v_inst4	mux21_32bit(mixed)
+ b2v_inst40	adder_32(mixed)
+ b2v_inst44	dmem(behavioral)
+ b2v_inst45	imem(behavioral)
+ b2v_inst46	mux31_32bit(mixed)
+ b2v_inst47	mux31_32bit(mixed)
+ b2v_inst5	forwarding(mixed)
+ b2v_inst6	mux21_32bit(mixed)
+ b2v_inst7	hazard(mixed)
+ b2v_inst8	mem_wb(mixed)
standard	standard
textio	textio
std_logic_1164	std_logic_1164
numeric_std	numeric_std
std_logic_arith	std_logic_arith
std_logic_unsigned	std_logic_unsigned

this is the signal matches of waveforms of summation and HDandFUtest asm test files when I do the tests.

Conclusion:

All files and circuits are included in my zip. This is a really hard project for me, especially with the ideas of stalls and flushes between different pipeline registers. But with several weeks efforts, I finally finished the lab.

