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Section: A

Date: 2/21/2017

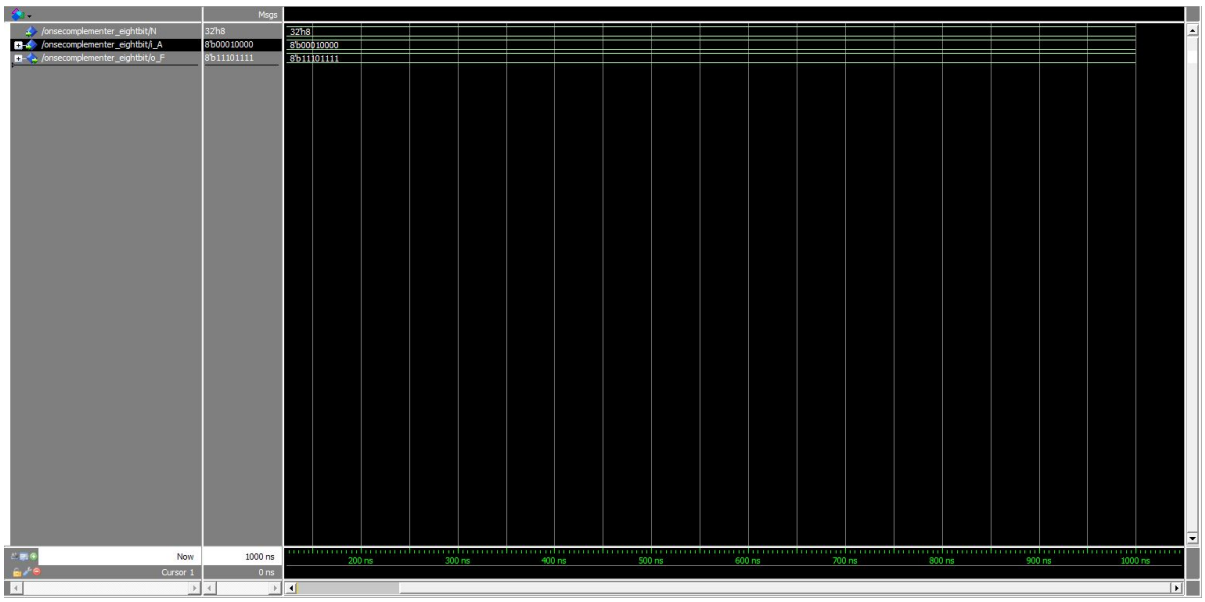
Instructor: Akhilesh Tyagi

Lab-5

1). One's Complimenter

The code was included in file onescomplimenter_eightbit.vhd

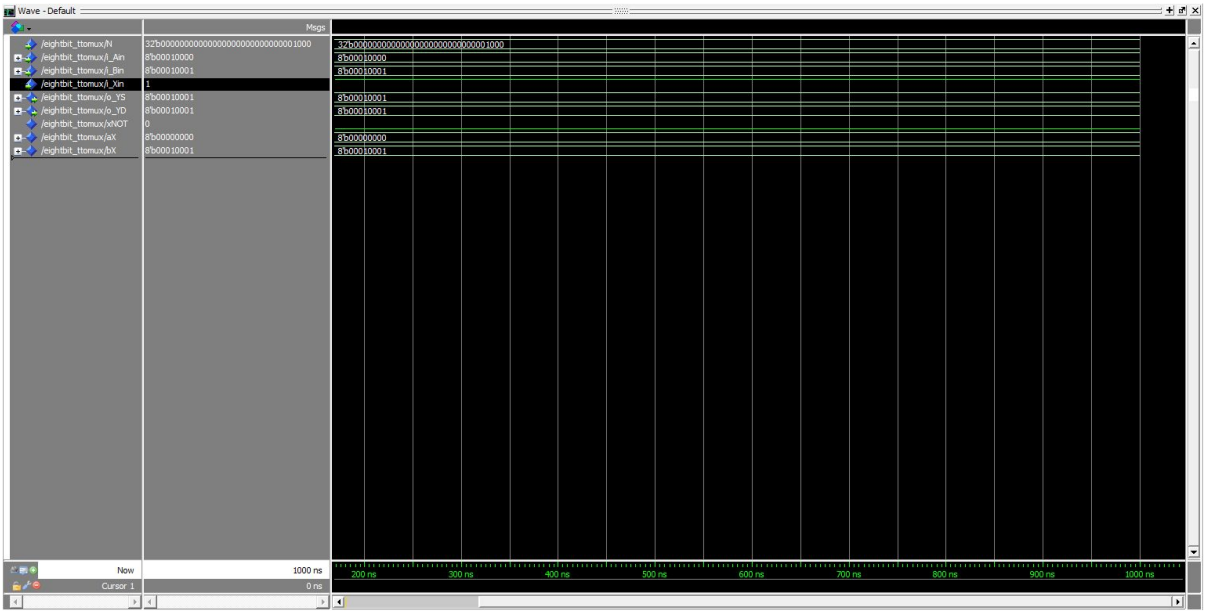
The wave form for the one's complimenter:



2). Two-Input Multiplexer

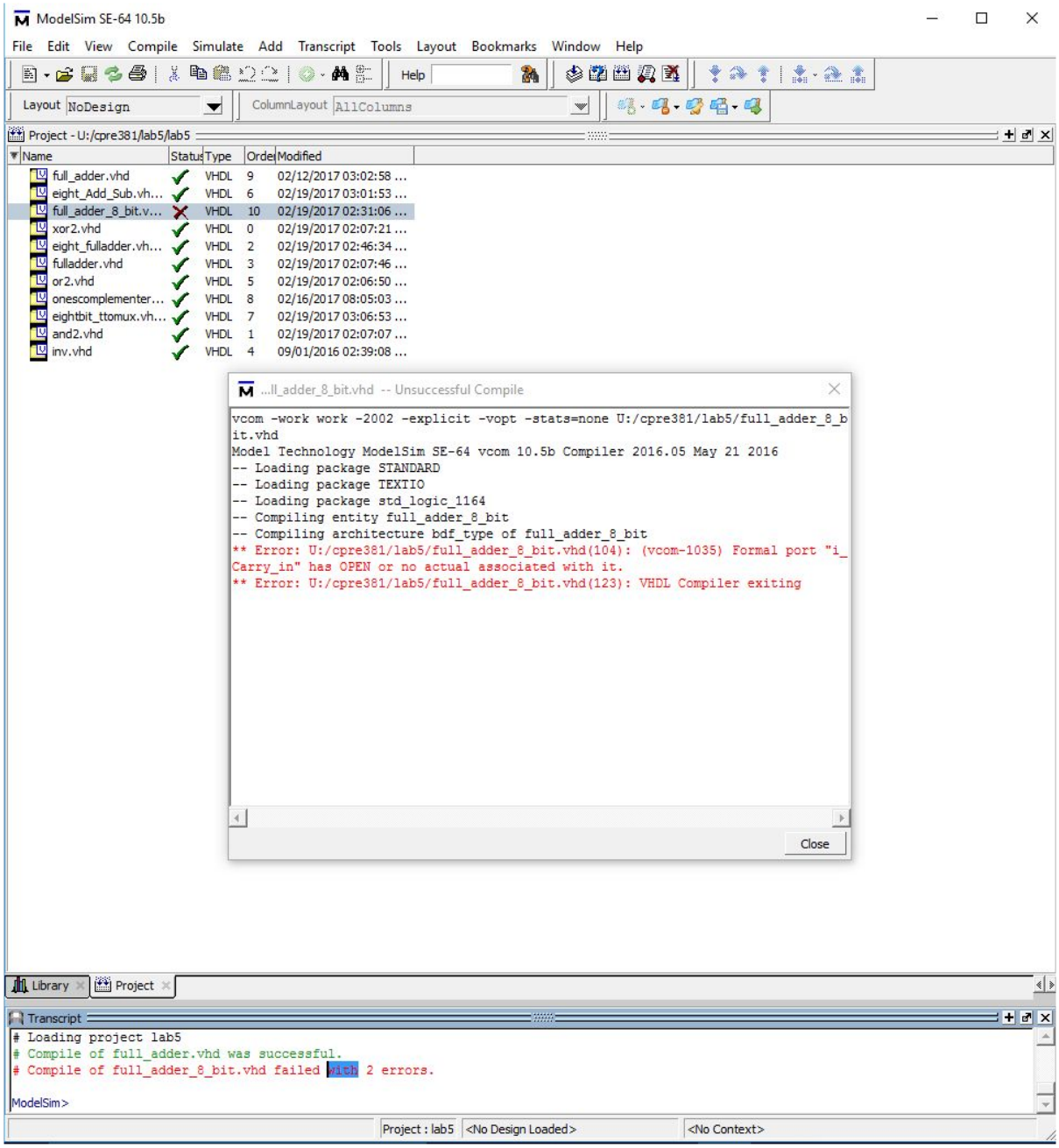
The code was included in file eightbit_ttomux.vhd

The wave form of the ttomux is:



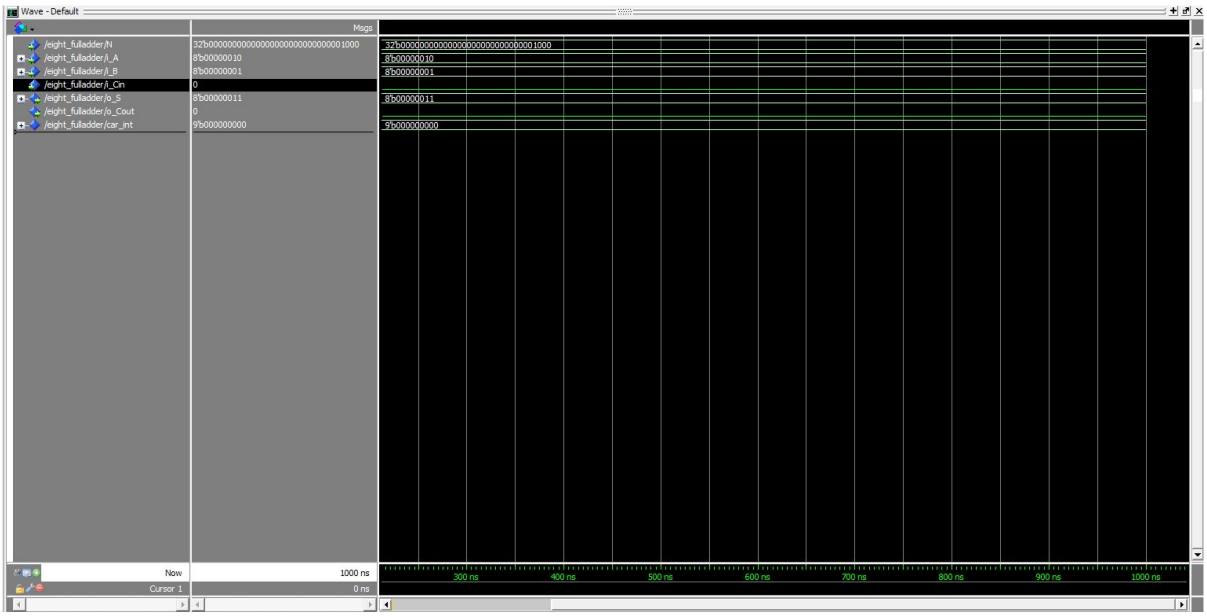
3) Full Adder

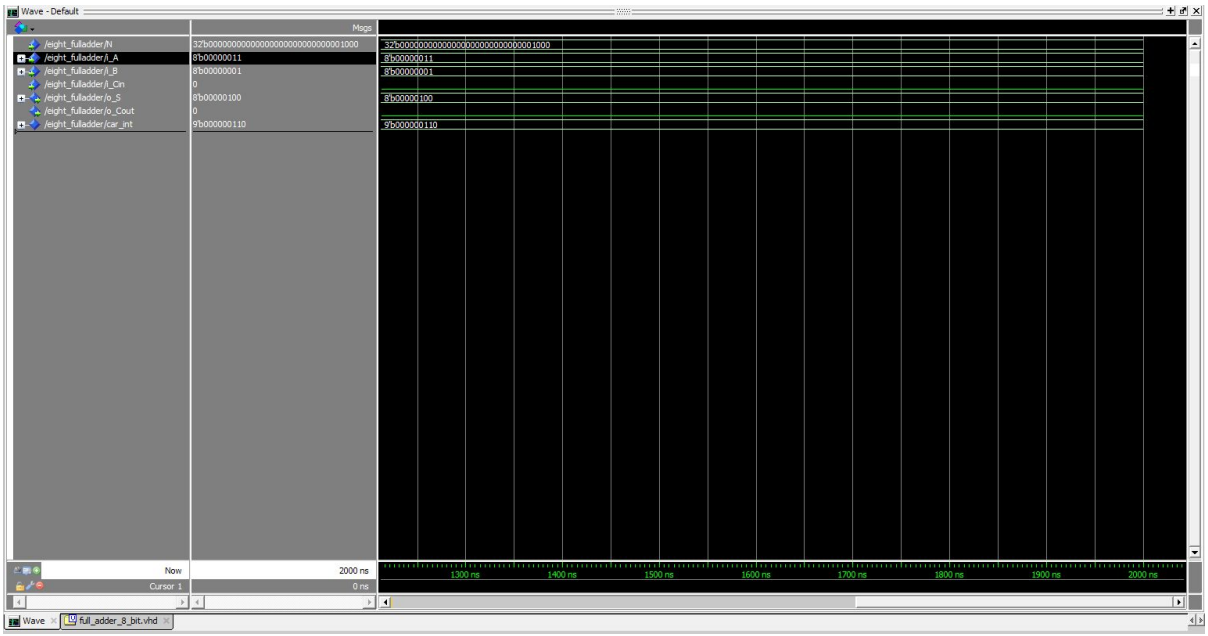
In this part, I failed to create VHDL file by my block diagram. I finished my Diagram and compiled it successfully, and did created the VHDL. the block diagram was named full_adder_8_bit.bdf, and the vhdl file was named full_adder_8_bit.vhd. but when I tried to simulate with modelsim, the vhdl file got error when compiling the file:

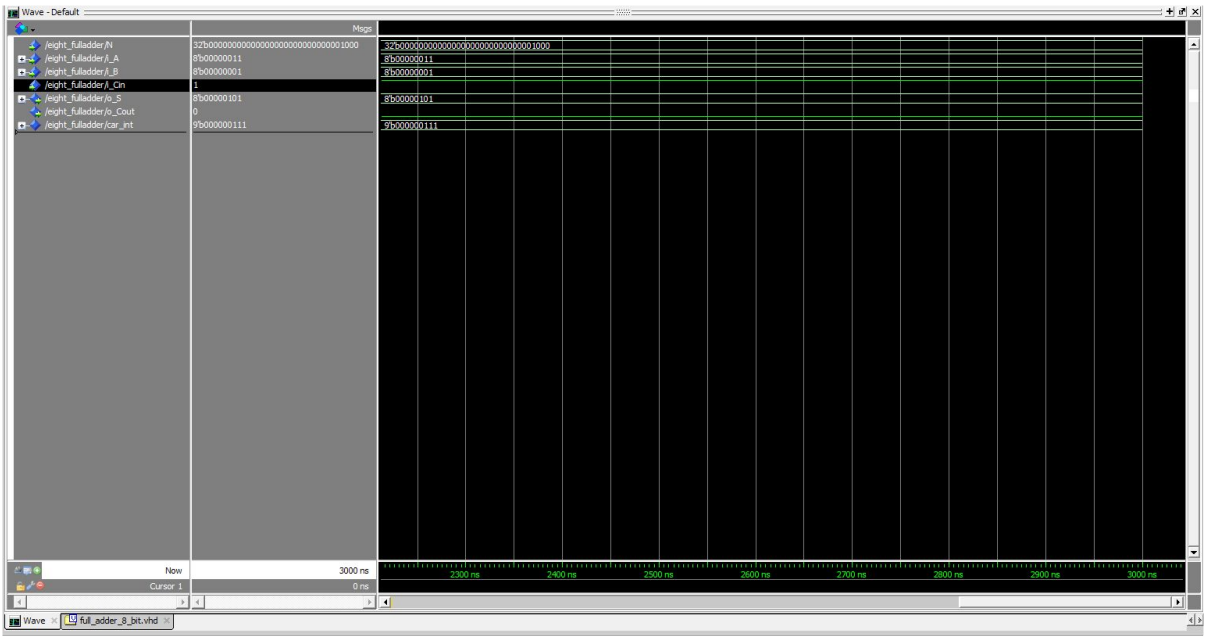


due to this problem, I used my own vhdl-only based file that I created which was named eight_fulladder.vhd and generated a block named eight_fulladder.bsf.

the tests of the program with waveforms:

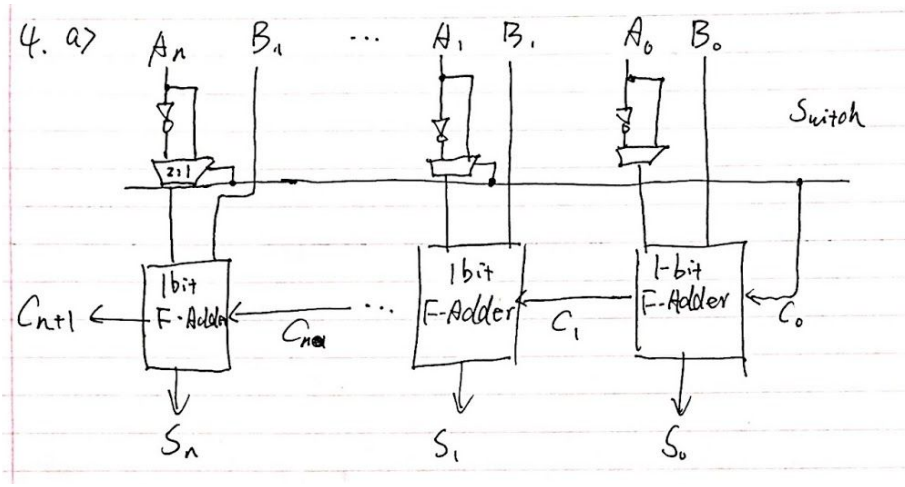

Wave - Default
Msgs
/eight_fulladder/N
/eight_fulladder/i_A
/eight_fulladder/i_B
/eight_fulladder/i_Cin
/eight_fulladder/o_S
/eight_fulladder/o_Cout
/eight_fulladder/car_int
32'b00000000000000000000000000001000
8'b00000010
8'b00000001
0
8'b00000011
0
9'b000000000
Now
1000 ns
Cursor 1
0 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
1000 ns


Wave - Default
Msgs
/eight_fulladder/N
/eight_fulladder/i_A
/eight_fulladder/i_B
/eight_fulladder/i_Cin
/eight_fulladder/o_S
/eight_fulladder/o_Cout
/eight_fulladder/car_int
32'b00000000000000000000000000001000
8'b00000011
8'b00000001
0
8'b00000100
0
9'b000000110
Now
2000 ns
Cursor 1
0 ns
1300 ns
1400 ns
1500 ns
1600 ns
1700 ns
1800 ns
1900 ns
2000 ns
Wave
full_adder_8_bit.vhd



4). Adder/Subtractor with Control

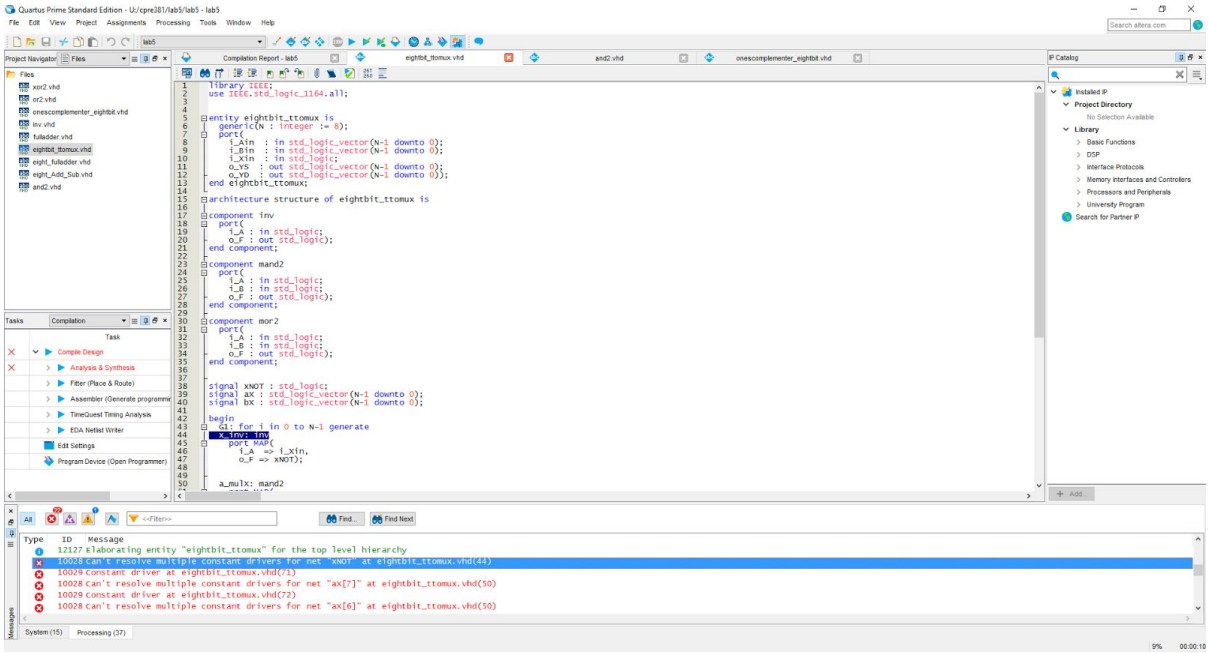
due to the problem happened in last part, I decided to write the vhdl instead of draw blocks. but I do have the block diagram drawn by hand:

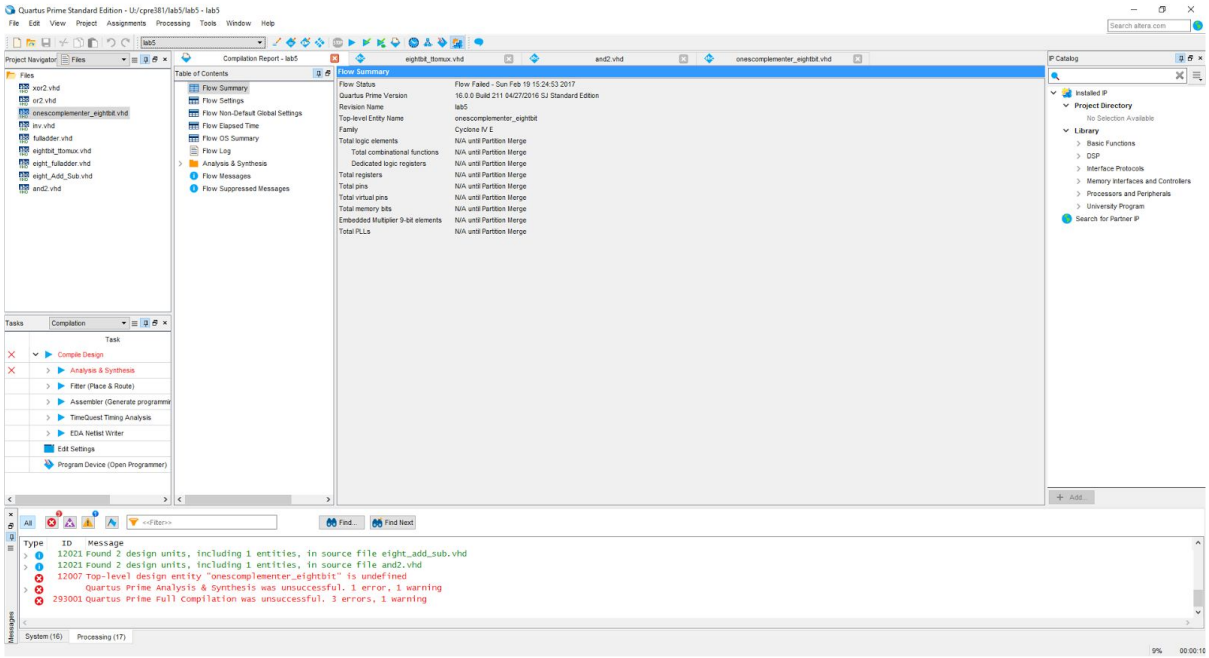


where n = 7, switch is the control signal and when it is 1, it will perform sub, 0 it will perform add. because I am using loops in vhdl, so if we want to enhance a n bit version, we only need to simply change the number of loops.

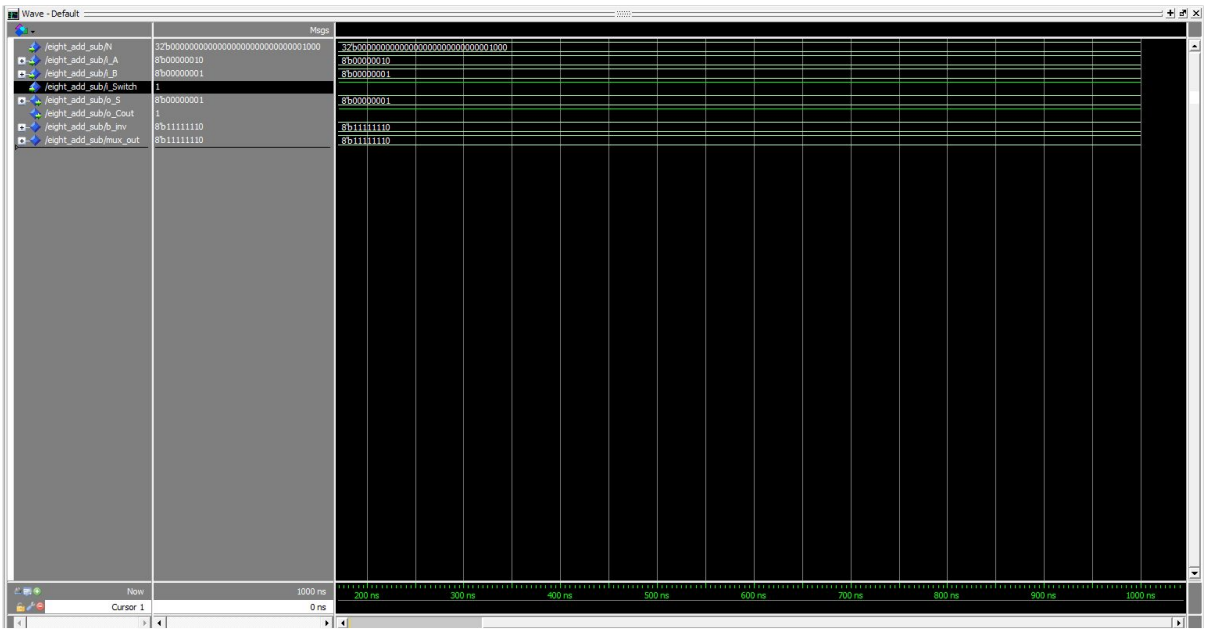
the vhdl file was named eight_Add_Sub.vhd.

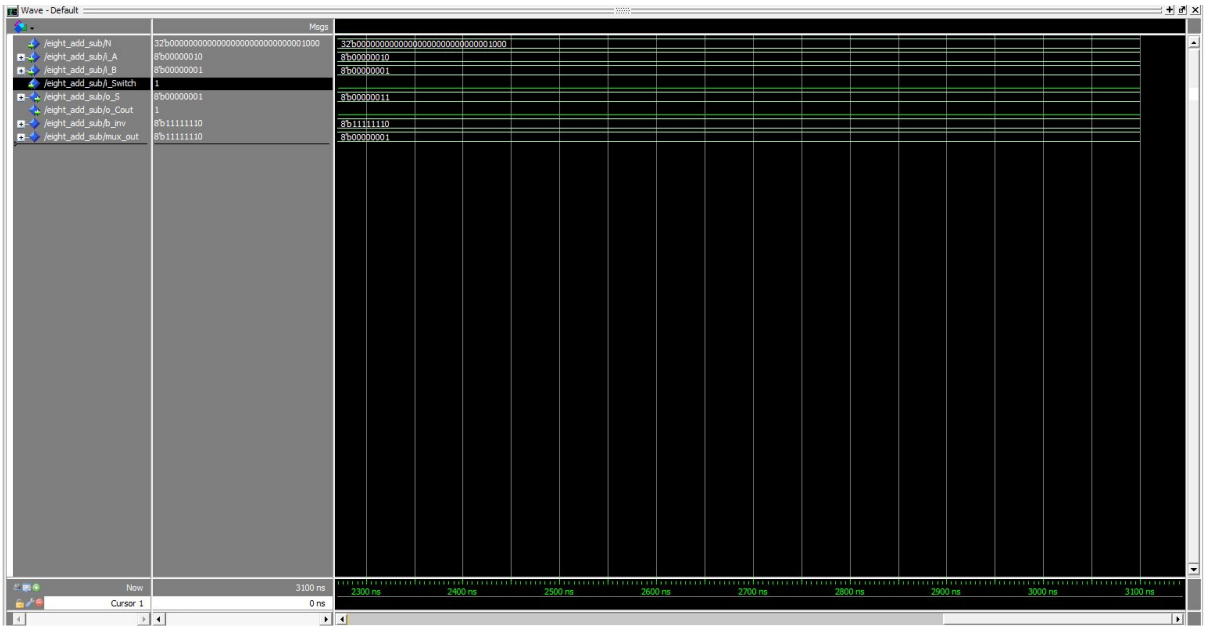
I did tried to generate a block of this program, but got errors:

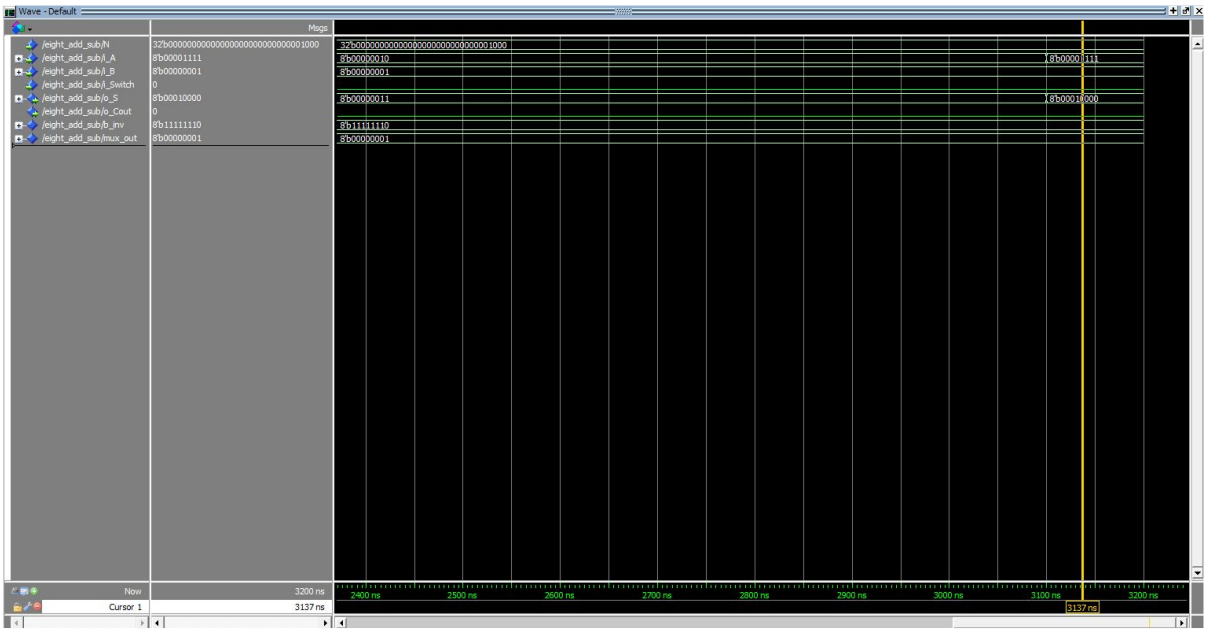


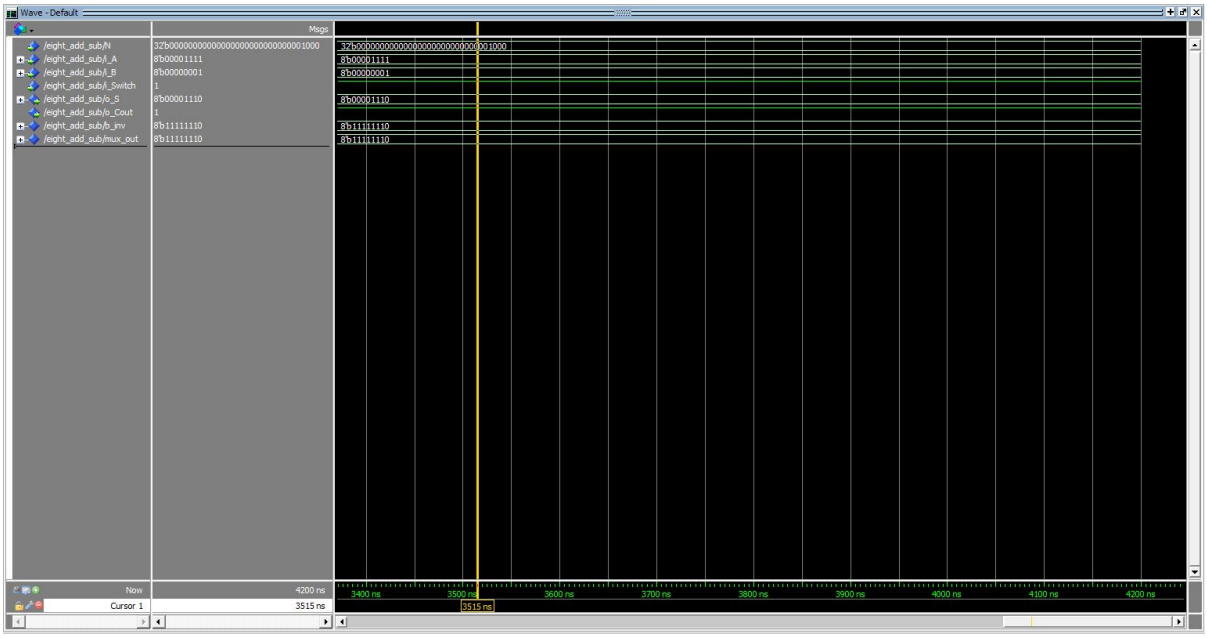


and the multi tests of waveforms:


Wave - Default
Msgs
/eight_add_sub/N
/eight_add_sub/i_A
/eight_add_sub/i_B
/eight_add_sub/i_Switch
/eight_add_sub/o_S
/eight_add_sub/o_Cout
/eight_add_sub/b_inv
/eight_add_sub/mux_out
32'b00000000000000000000000000001000
8'b00000010
8'b00000001
1
8'b00000001
1
8'b11111110
8'b11111110
Now
1000 ns
Cursor 1
0 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
1000 ns


Wave - Default
Msgs
/eight_add_sub/N
/eight_add_sub/i_A
/eight_add_sub/i_B
/eight_add_sub/i_Switch
/eight_add_sub/o_S
/eight_add_sub/o_Cout
/eight_add_sub/b_inv
/eight_add_sub/mux_out
32'b00000000000000000000000000001000
8'b00000010
8'b00000001
1
8'b00000011
1
8'b11111110
8'b00000001
Now
3100 ns
Cursor 1
0 ns
2300 ns
2400 ns
2500 ns
2600 ns
2700 ns
2800 ns
2900 ns
3000 ns
3100 ns





I chose these tests because it includes all situations include add, sub, with carry and without carry.