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Section: A

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Project A

outputs of main control:

o_reg_dest; -- '1' write to rd, '0' will not

o jump; -- '1'jump flag as selector of 2 to 1 mux, '0' select 0 value

o branch; -- '1'jump flag as selector of 2 to 1 mux, '0' select 0 value, will and with ALU zero flag

o mem to reg; -- write ALU output to reg file or not

o ALU op; -- operation code in ALU

o mem write; -- write to memory or not

o ALU src; -- select immidiate data as second input to ALU or rt data

o reg write; -- write enable to write register file (write rd)

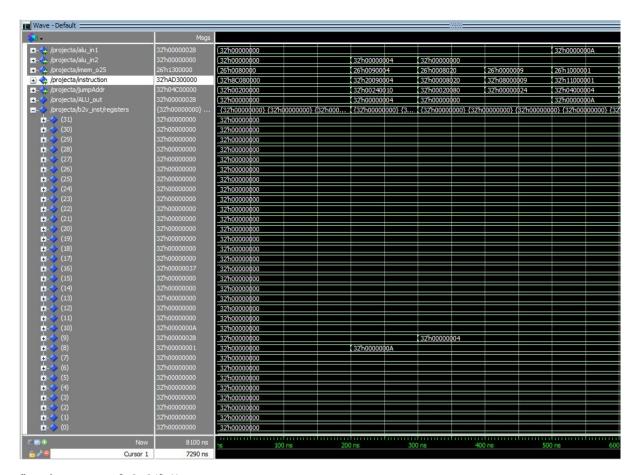
load \$t0, 0(\$zero):

≨ 1.	Msgs		
💶 📤 /projecta/alu_in1	32'h00000028	(32'h00000000	
💶 👆 /projecta/alu_in2	32'h00000000	(32'h00000000	32'h00000004
+-4 /projecta/imem_o25	26'h1300000	(26'h0080000	26'h0090004
+- /projecta/instruction	32'hAD300000	(32'h8C080000	32'h20090004
🛨 🚣 /projecta/jumpAddr	32'h04C00000	(32'h00200000	32'h00240010
∓ - ♦ /projecta/ALU_out	32'h00000028	(32'h00000000	32'h00000004
=	{32'h000000000}	{32'h00000000} {32'h00000000} {32'h000	{32'h00000000} {3
±- > (31)	32'h00000000	32'h00000000	
±- ◇ (30)	32'h00000000	32'h00000000	
+	32'h00000000	32'h00000000	
+-> (28)	32'h00000000	32'h00000000	
<u> </u>	32'h00000000	32'h00000000	
+> (26)	32'h00000000	32'h00000000	
+> (25)	32'h00000000	32'h00000000	
+- (24)	32'h00000000	32'h00000000	
∓- → (23)	32'h00000000	32'h00000000	
∓- → (22)	32'h00000000	32'h00000000	
→ - ◇ (21)	32'h00000000	32'h00000000	
∓- → (20)	32'h00000000	32'h00000000	
±- → (19)	32'h00000000	32'h00000000	
+- (18)	32'h00000000	32'h00000000	
<u> </u>	32'h00000000	32'h00000000	
+ (16)	32'h00000037	32'h00000000	
+> (15)	32'h00000000	32'h00000000	
1 - ◇ (14)	32'h00000000	32'h00000000	
1 → (13)	32'h00000000	32'h00000000	
1- (12)	32'h00000000	32'h00000000	
±- ♦ (11)	32'h00000000	32'h00000000	
+- (10)	32'h0000000A	32'h00000000	
↓ → (9)	32'h00000028	32'h00000000	
<u>∓</u> - → (8)	32'h00000001	32'h00000000	, 32'h0000000A
∓- → (7)	32'h00000000	32'h00000000	
+- (6)	32'h00000000	32'h00000000	
- → (5)	32'h00000000	32'h00000000	
+-→ (4)	32'h00000000	32'h00000000	
1 → (3)	32'h00000000	32'h00000000	
. (2)	32'h00000000	32'h00000000	
±→ (1)	32'h00000000	32'h00000000	
±- → (0)	32'h00000000	32'h00000000	
23W W 60%			
	ow 8100 ns	ns 100 ns 20	00 ns 30
Curson	r 1 7290 ns		

addi \$t1, \$zero, 4:

1.	Msgs			
- /projecta/alu_in1	32'h00000028	(32'h00000000		
⊢ <mark>人</mark> /projecta/alu_in2	32'h00000000	(32'h00000000	(32'h00000004	32'h00000000
⊢ <mark>4.</mark> /projecta/imem_o25	26'h 1300000	(26'h0080000	26'h0090004	26'h0008020
-🚣 /projecta/instruction	32'hAD300000	(32'h8C080000	32'h20090004	32'h00008020
-🚣 /projecta/jumpAddr	32'h04C00000	(32'h00200000	32'h00240010	32'h00020080
-🄷 /projecta/ALU_out	32'h00000028	(32'h00000000	32'h0000004	32'h00000000
/projecta/b2v_inst/registers	{32'h000000000}	{32'h00000000} {32'h00000000} {32'h000	\ {32'h000000000} {3.	(32'h00000000)
±- → (31)	32'h00000000	32'h00000000		
+ - \checkmark (30)	32'h00000000	32'h00000000		
±	32'h00000000	32'h00000000		
±> (28)	32'h00000000	32'h00000000		
±- ♦ (27)	32'h00000000	32'h00000000		
±	32'h00000000	32'h00000000		
±> (25)	32'h00000000	32'h00000000		
+- (24)	32'h00000000	32'h00000000		
±- (23)	32'h00000000	32'h00000000		
+- (22)	32'h00000000	32'h00000000		
+- (21)	32'h00000000	32'h00000000		
±> (20)	32'h00000000	32'h00000000		
<u>+</u> - $\langle \rangle$ (19)	32'h00000000	32'h00000000		
<u>+</u> - \checkmark (18)	32'h00000000	32'h00000000		
±- → (17)	32'h00000000	32'h00000000		
→ (16)	32'h00000037	32'h00000000		
±- → (15)	32'h00000000	32'h00000000		
±- → (14)	32'h00000000	32'h00000000		
± - ◇ (13)	32'h00000000	32'h00000000		
± - → (12)	32'h00000000	32'h00000000		
	32'h00000000	32'h00000000		
± - ◇ (10)	32'h0000000A	32'h00000000		
± - → (9)	32'h00000028	32'h00000000		32'h00000004
± - ♦ (8)	32'h00000001	32'h00000000	32'h0000000A	
	32'h00000000	32'h00000000		
‡ - ♦ (6)	32'h00000000	32'h00000000		
.	32'h00000000	32'h00000000		
± - → (4)	32'h00000000	32'h00000000		
± - ◇ (3)	32'h00000000	32'h00000000		
±- → (2)	32'h00000000	32'h00000000		
± - ◇ (1)	32'h00000000	32'h00000000		
<u>+</u> > (0)	32'h00000000	32'h00000000		
1 ⊕	low 8100 ns	ns 100 ns		300 ns
Curso		ns 100 ns	200 NS	300 TIS

add \$s0, \$zero, \$zero; j check:



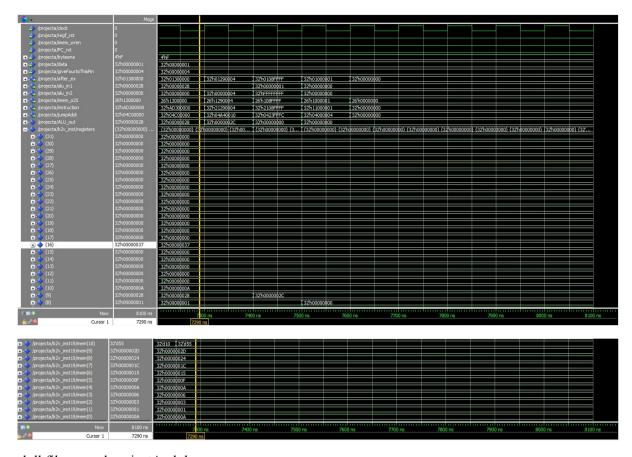
first time run sw \$s0, 0(\$t1):

Wave - Default ======							9	
(%) →	Msgs							
✓ /projecta/dock	1					ه در ا		
/projecta/regf_rst	0							
/projecta/imem_wren	0							
/projecta/PC_rst	0							
	4'hF	4'hF						
	32'h00000001	32'h00000001						
/projecta/giveFourtoThisPin	32'h00000004	32'h00000004						
	32'h01300000	32'h01000001	32'h000000	04	32'h012A0000	32'h015080)20 32'h	01300000 (3:
	32'h00000008	32'h00000009	32'h000000	00	32'h00000008	32'h000000	02 (32h	00000008
	32'h00000000	32'h00000000			32'h00000000	32'h000000	01 (32'h	00000000 (3:
	26'h1300000	26'h1000001	26'h000000	4	26'h12A0000	26'h150802	20 (26'h	300000 (26
	32'hAD300000	32'h11000001	32'h080000		32'h8D2A0000	32'h015080		AD300000 (3:
- /projecta/jumpAddr	32'h04C00000	32'h04000004	32'h000000	10	32'h04A80000	32'h054200)80 (32'h	04C00000 (3
	32'h00000008	32'h00000009	32'h000000	00	32'h00000008	32'h000000	003 (32'h	00000008 (3:
	{32'h000000000}	{32'h000000000}	{32'h00000000} {:	32'h0000000	0} {32'h000000000}	【{32'h00000	000} {3 {32	D00000000} {32'h000
+-> /projecta/b2v_inst19/mem(10)	32'd10	32'd10						
+-> /projecta/b2v_inst19/mem(9)	32'h00000009	32'h00000009						
+-> /projecta/b2v_inst19/mem(8)	32'h00000008	32'h00000008						
	32'h00000007	32'h00000007						
+ /projecta/b2v_inst19/mem(6)	32'h00000006	32'h00000006						
→ /projecta/b2v_inst19/mem(5)	32'h00000005	32'h00000005						
→ /projecta/b2v_inst19/mem(4)	32'h00000004	32'h00000004						
	32'h00000003	32'h00000003						
	32'h00000002	32'h00000002						(32'h00000003
	32'h00000001	32'h00000001						
projecta/b2v_inst19/mem(0)	32'h0000000A	32'h0000000A						
Now	8100 ns	ndumum hum						
		200 ns	1300 ns	1400	ns	1500 ns	1600 ns	1700 n
Cursor 1	1625 ns						162	25 ns

result from mars:

Registers Coproc	Coproc 0	
Name	Number	Value
\$zero	0	0x00000000
\$at	1	0x10010000
\$v0	2	0x00000000
\$v1	3	0x00000000
\$a0	4	0x00000000
\$a1	5	0x00000000
\$a2	6	0x00000000
\$a3	7	0x00000000
\$t0	8	0x00000000
\$t1	9	0x1001002c
\$t2	10	0x0000000a
\$t3	11	0x00000000
\$t4	12	0x00000000
\$t5	13	0x10010000
\$t6	14	0x00000000
\$t7	15	0x00000000
\$30	16	0x00000037
\$31	17	0x00000000
\$32	18	0x00000000
\$33	19	0x00000000
\$34	20	0x00000000
\$85	21	0x00000000
\$36	22	0x00000000
\$87	23	0x00000000
\$t8	24	0x00000000
\$t9	25	0x00000000
\$k0	26	0x00000000
\$k1	27	0x00000000
\$gp	28	0x10008000
\$sp	29	0x7fffeffc
\$fp	30	0x00000000
\$ra	31	0x00000000
рс		0x00400038
hi		0x00000000
10		0x00000000

result in wave form:



vhdl file named projectA.vhd

during this lab I created the component jumpAddrGnrt and 26 to 32 bit extender. I also added monitoring signal outputs to monitor the values.