Name: Ningyuan Zhang

Section: A

Date: 3/30/2017

Instructor: Akhilesh Tyagi

Project A

outputs of main control:

o_reg_dest; -- ‘1’ write to rd, ‘0’ will not

o_jump; -- ‘1’jump flag as selector of 2 to 1 mux, ‘0’ select 0 value

o_branch; -- ‘1’jump flag as selector of 2 to 1 mux, ‘0’ select 0 value, will and with ALU zero flag

o_mem_to_reg; -- write ALU output to reg file or not

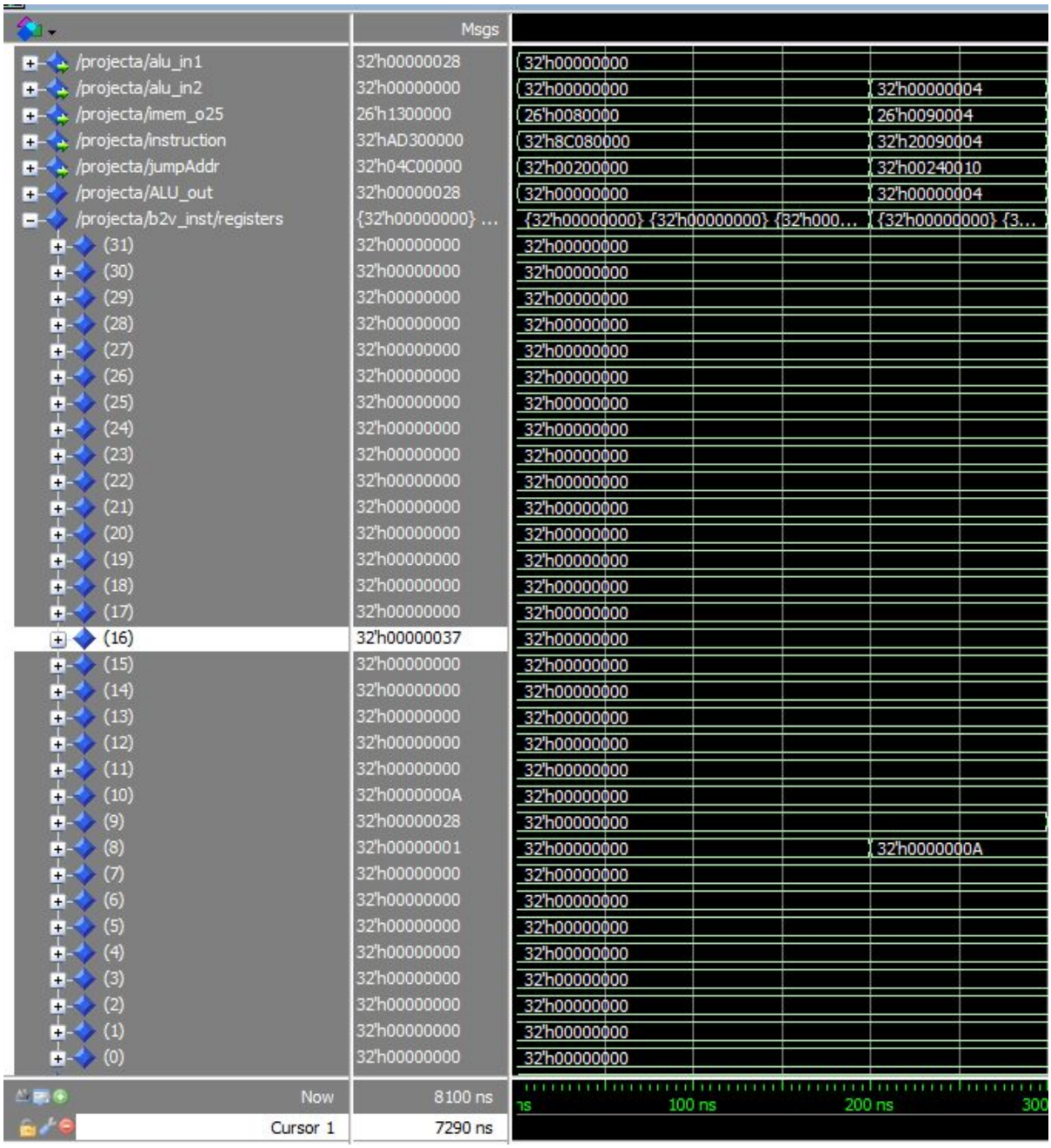
o_ALU_op; -- operation code in ALU

o_mem_write; -- write to memory or not

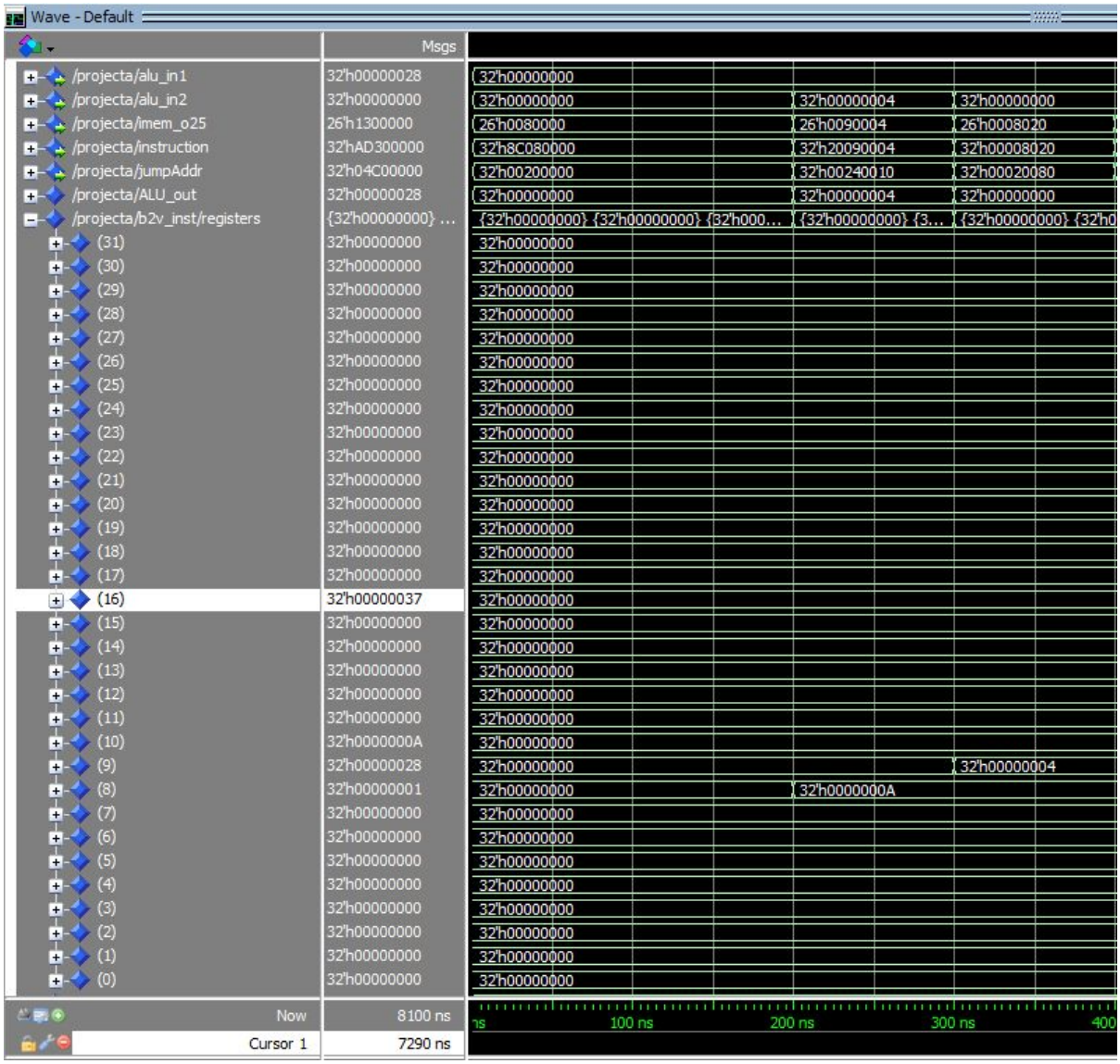
o_ALU_src; -- select immidiate data as second input to ALU or rt data

o_reg_write; -- write enable to write register file (write rd)

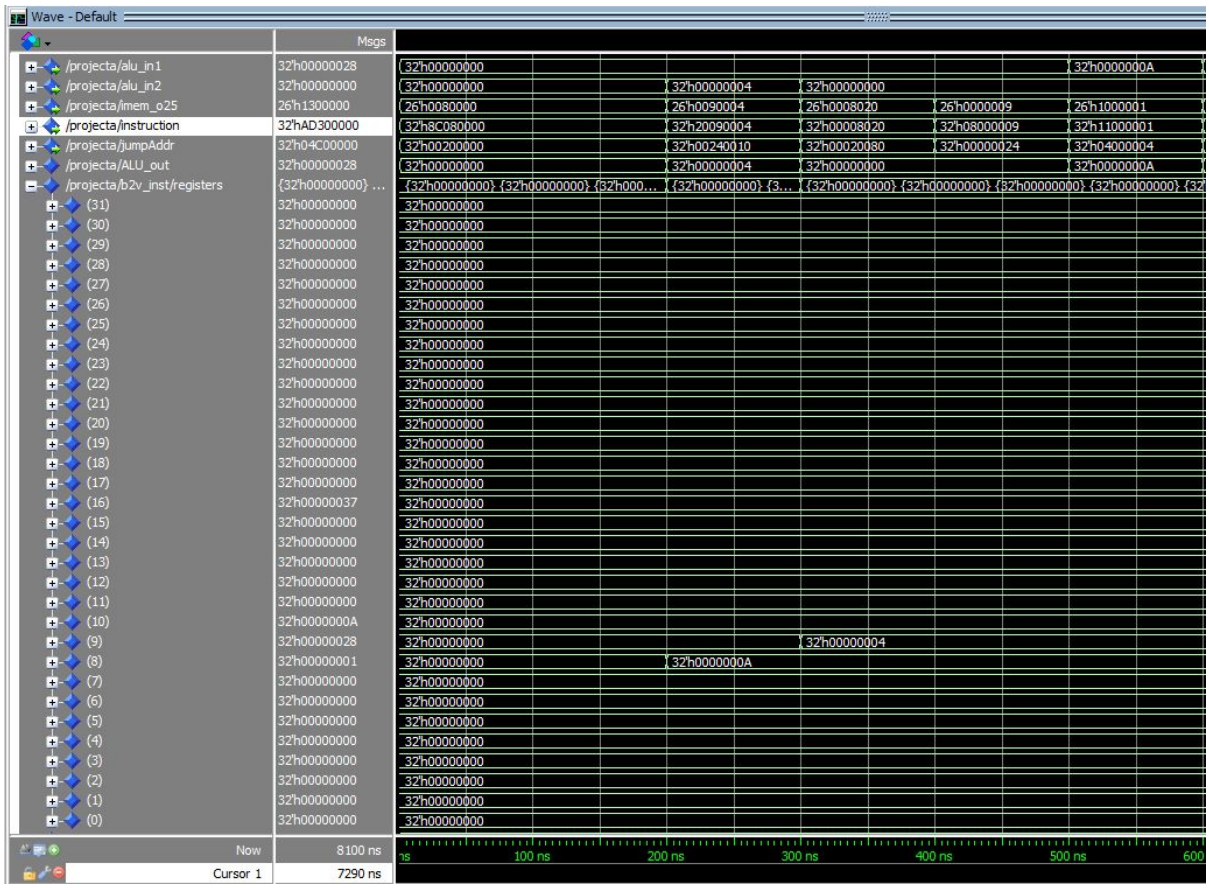
load $t0, 0($zero):



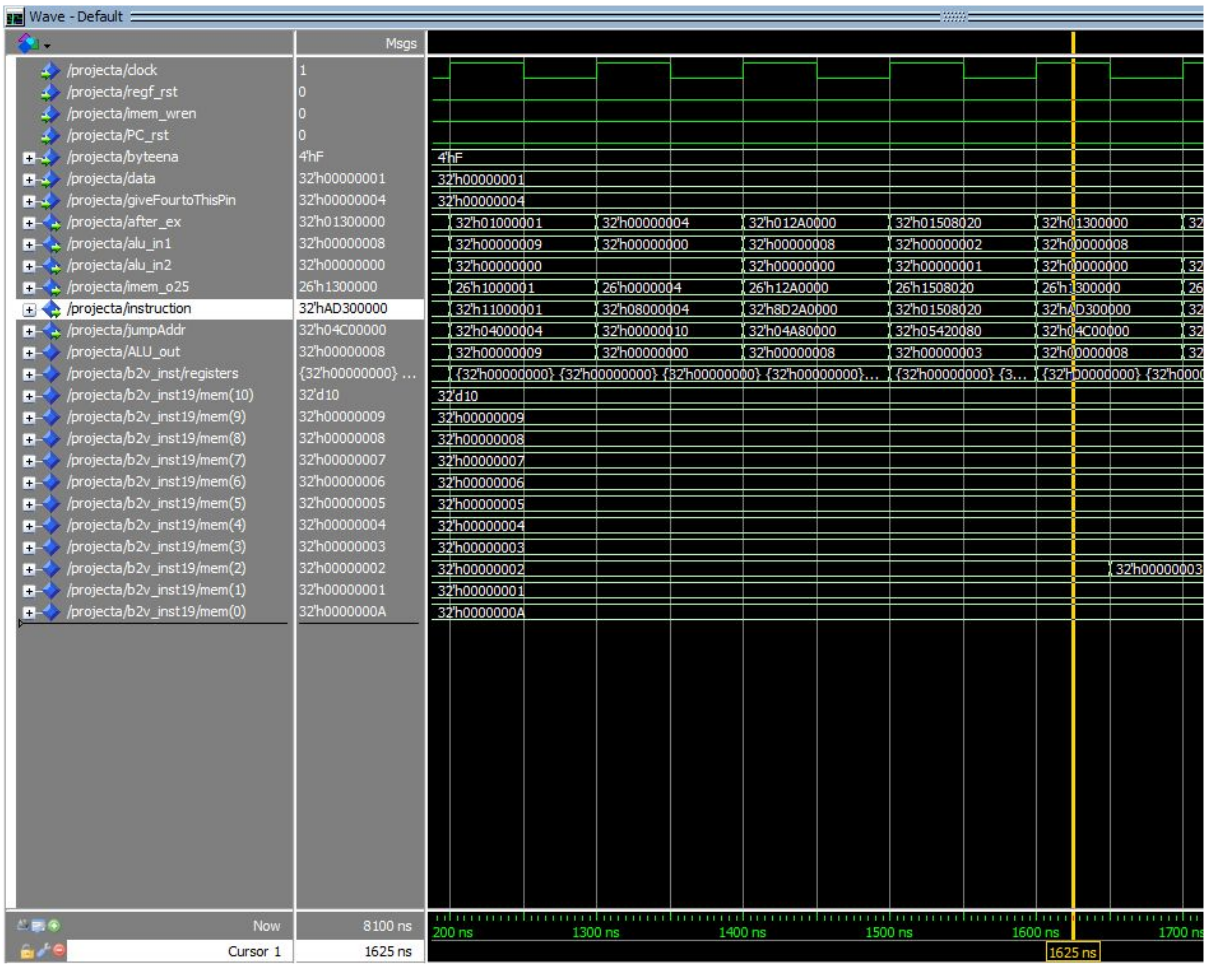
addi $t1, $zero, 4:



add $s0, $zero, $zero; j check:



first time run sw $s0, 0($t1):

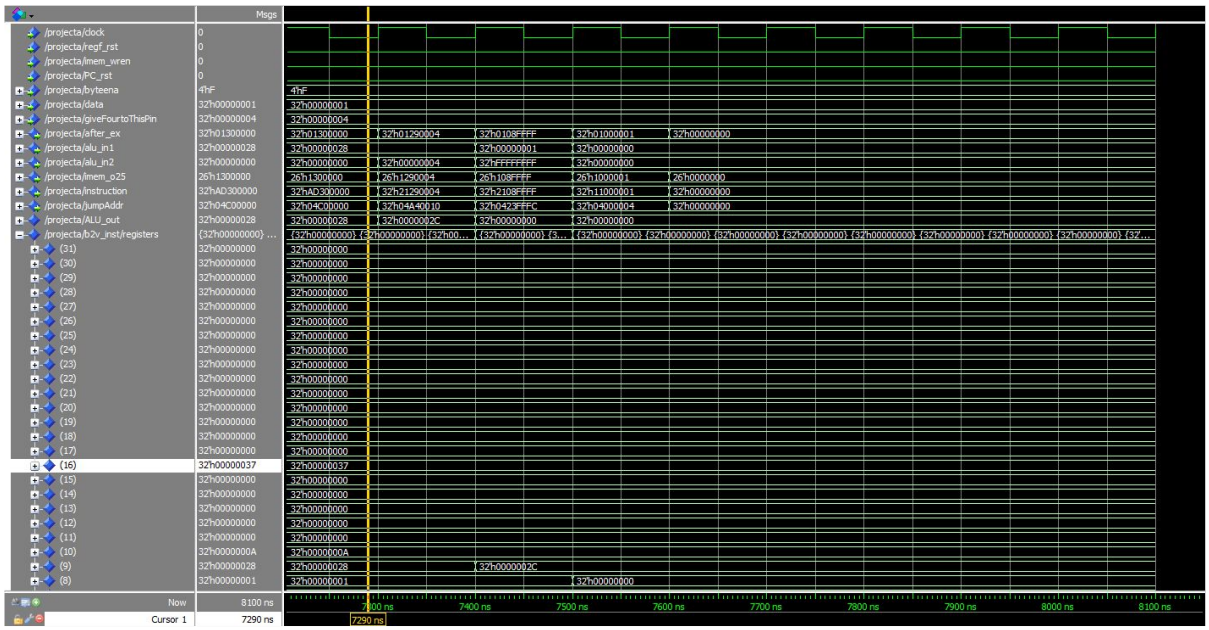


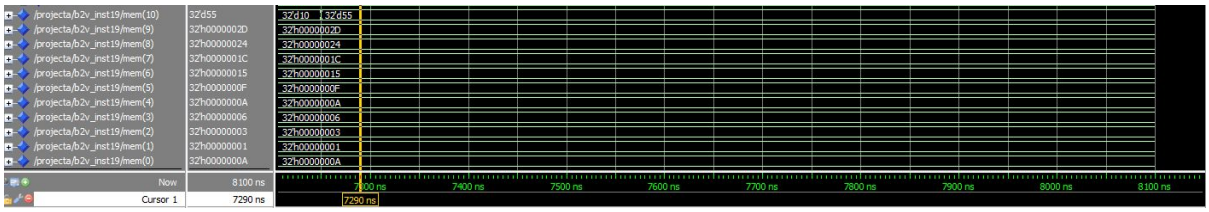
result from mars:

Registers | Coproc 1 | Coproc 0

Name	Number	Value
$zero	0	0x00000000
$at	1	0x10010000
$v0	2	0x00000000
$v1	3	0x00000000
$a0	4	0x00000000
$a1	5	0x00000000
$a2	6	0x00000000
$a3	7	0x00000000
$t0	8	0x00000000
$t1	9	0x1001002c
$t2	10	0x0000000a
$t3	11	0x00000000
$t4	12	0x00000000
$t5	13	0x10010000
$t6	14	0x00000000
$t7	15	0x00000000
$s0	16	0x00000037
$s1	17	0x00000000
$s2	18	0x00000000
$s3	19	0x00000000
$s4	20	0x00000000
$s5	21	0x00000000
$s6	22	0x00000000
$s7	23	0x00000000
$t8	24	0x00000000
$t9	25	0x00000000
$k0	26	0x00000000
$k1	27	0x00000000
$gp	28	0x10008000
$sp	29	0x7fffeffc
$fp	30	0x00000000
$ra	31	0x00000000
pc		0x00400038
hi		0x00000000
lo		0x00000000

result in wave form:





vhdl file named projectA.vhd

during this lab I created the component jumpAddrGnrt and 26 to 32 bit extender. I also added monitoring signal outputs to monitor the values.