Name: Ningyuan Zhang

Course: Cpr E 381

Section: K

Date: 9/15/2016

Group: K-3

TA: Taewoon Kim

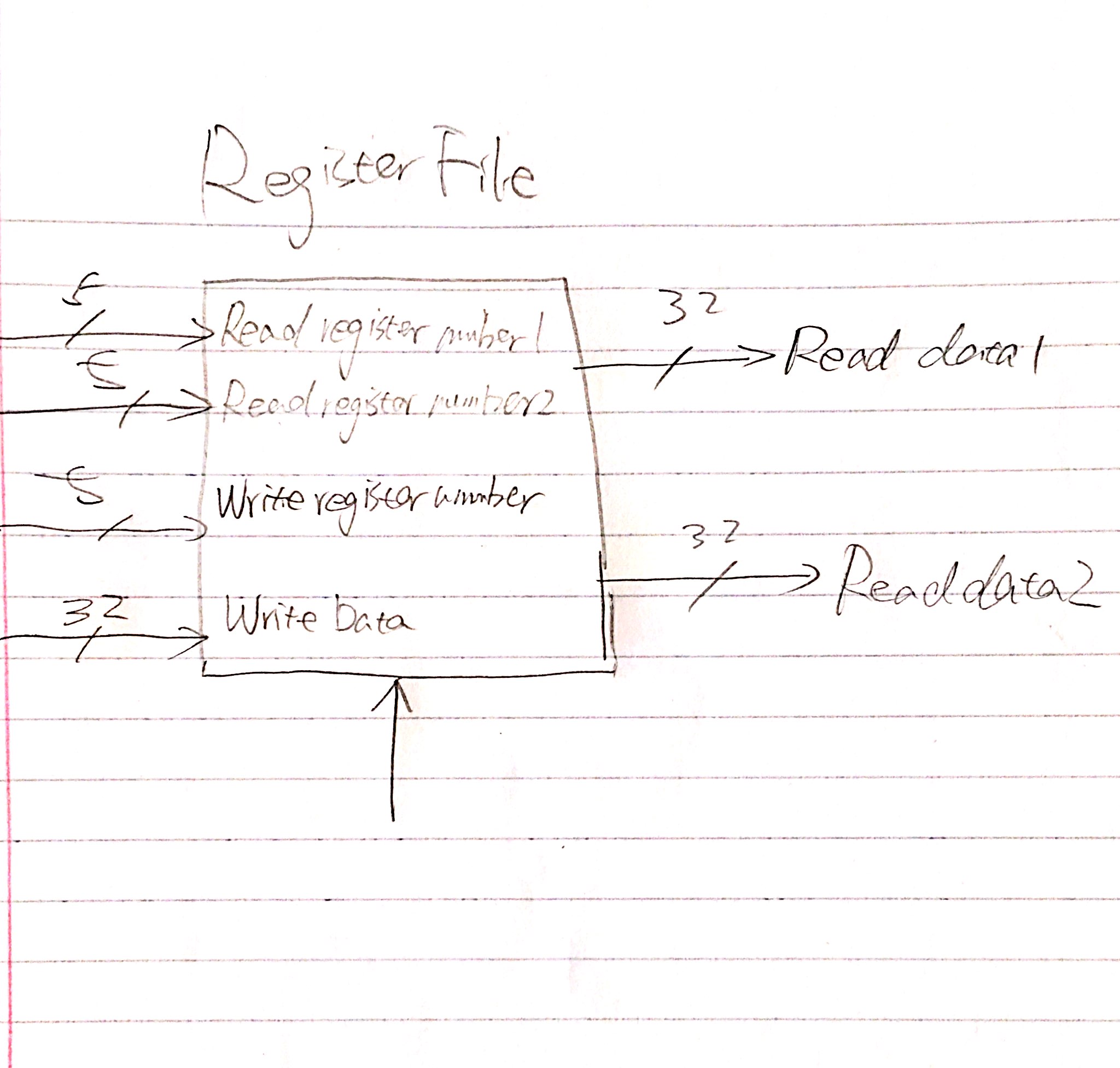
Lab 3 Report

VHDL level: Ningyuan Zhang: 8

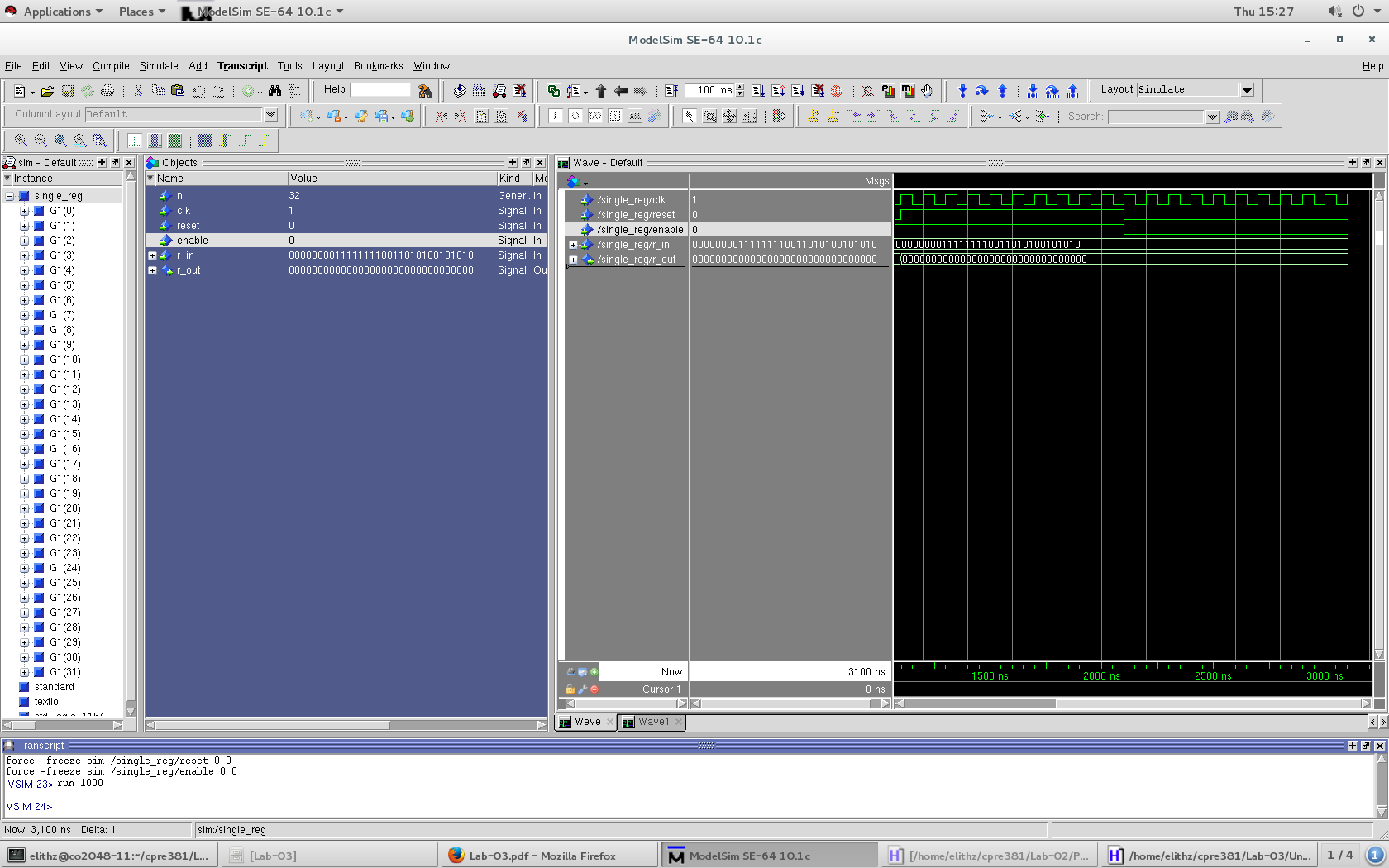
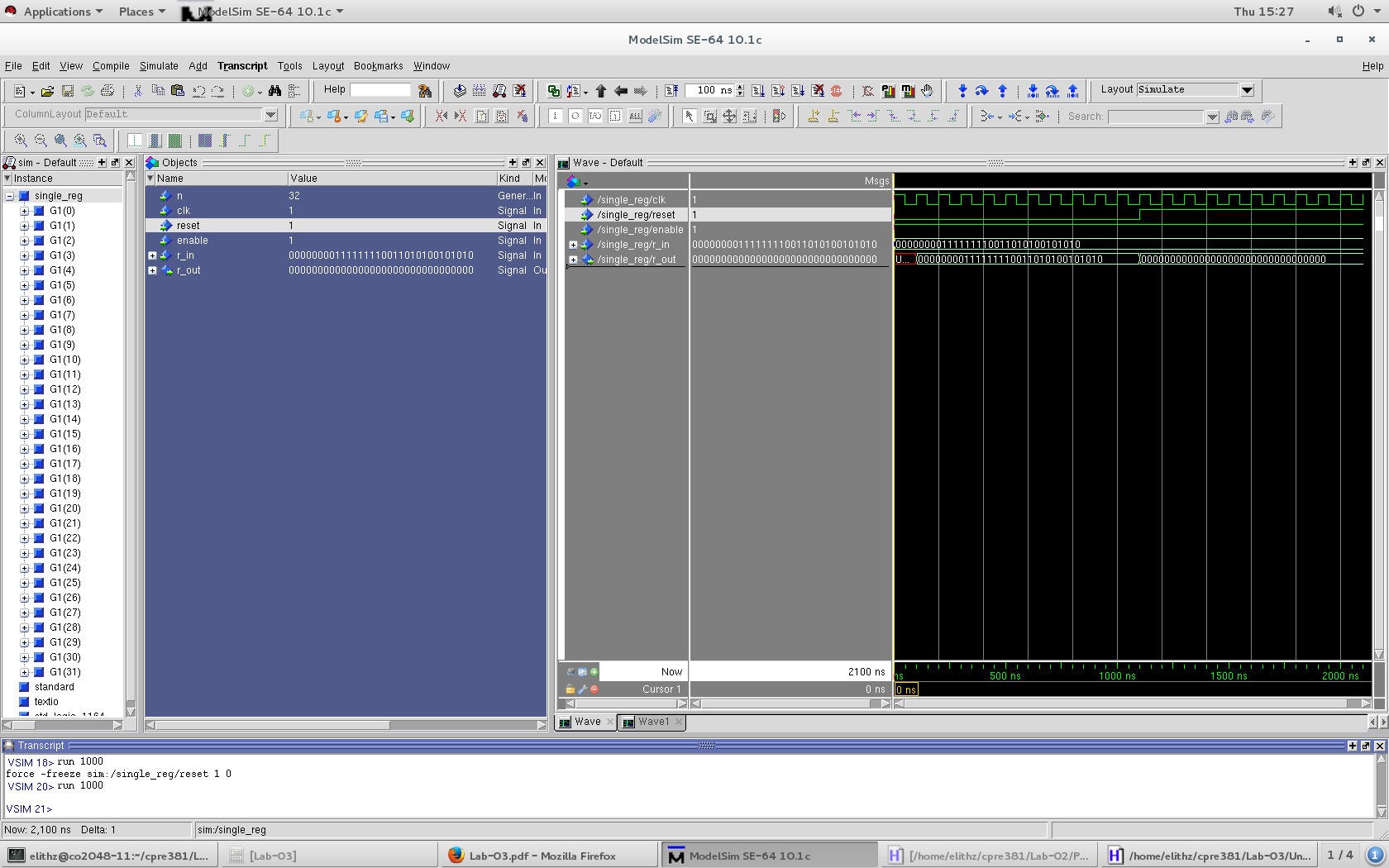
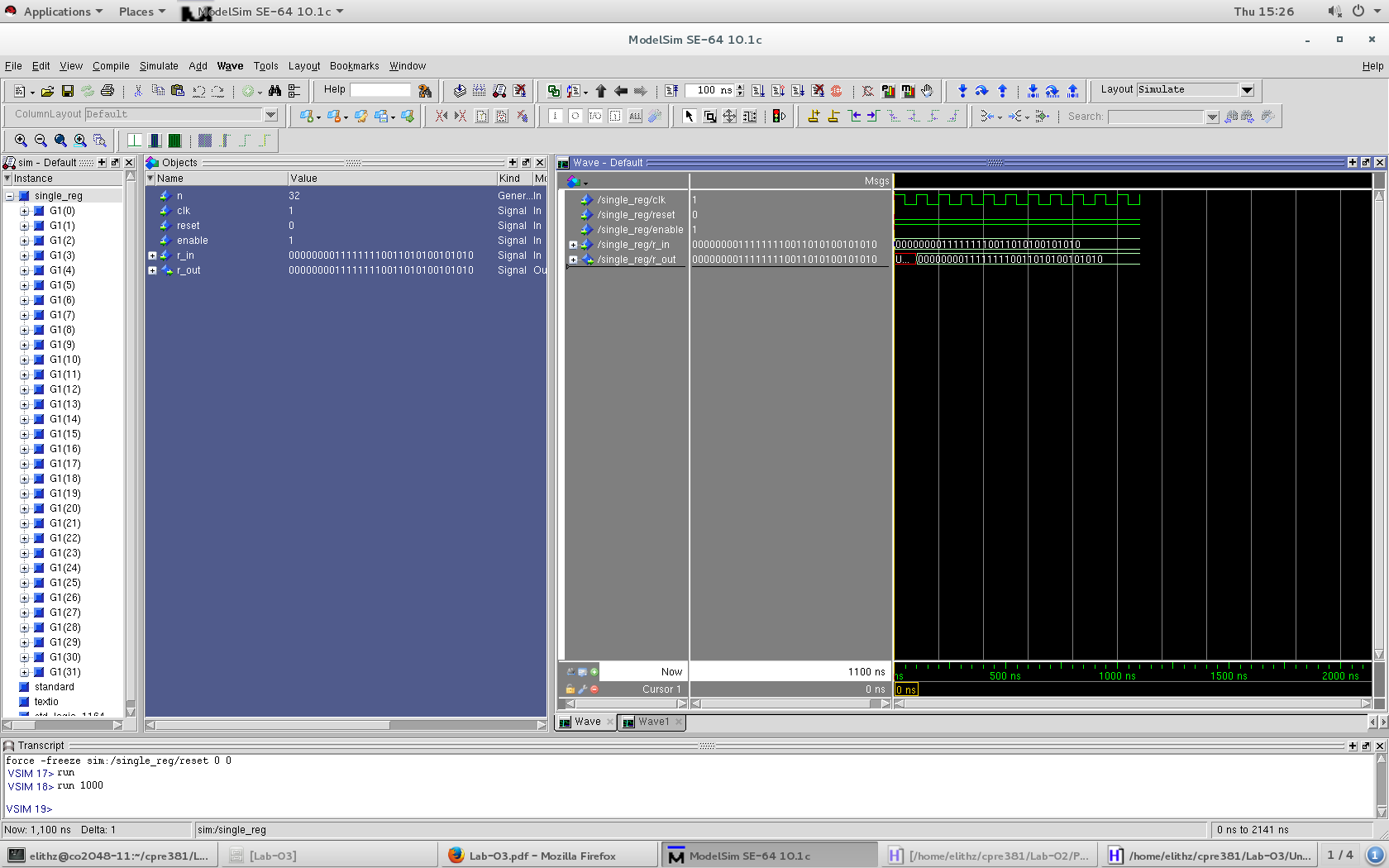
Daiyuan Ding: 8

Part 1.

a.) The instruction for MIPS 32 32-bit Register File is shown below:

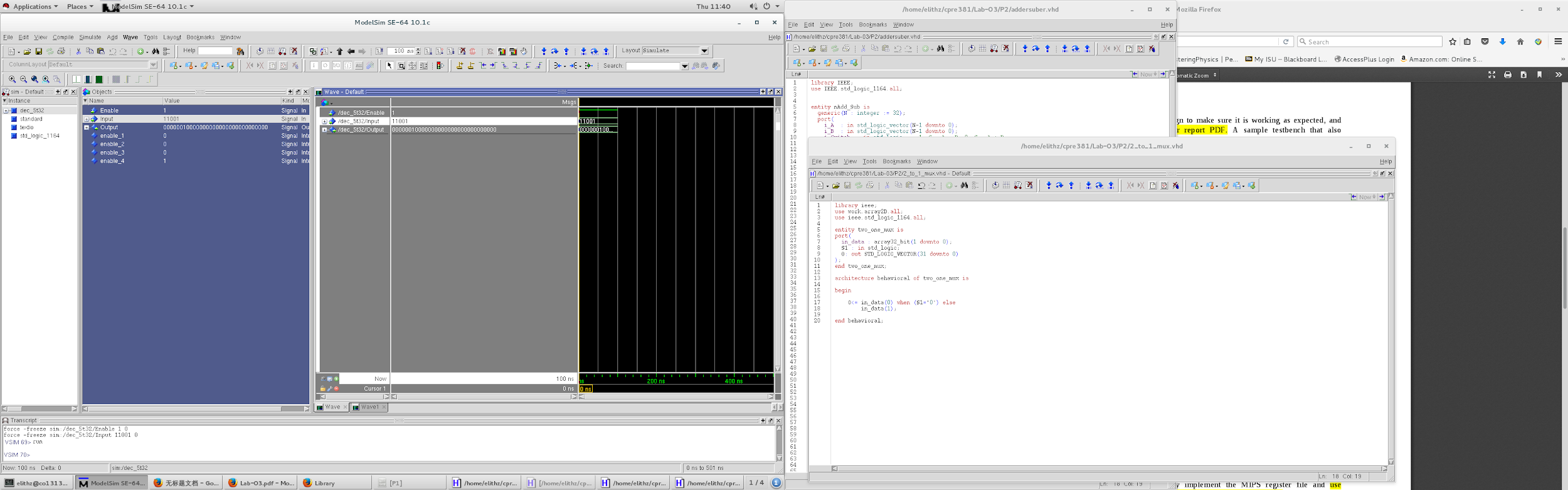


b.) The single 32-bit register was mad by a dff, which was already provided in the zip file, all I had to implement is just the register with clock, reset (which is always 0 in this lab) and inable.

c.) 

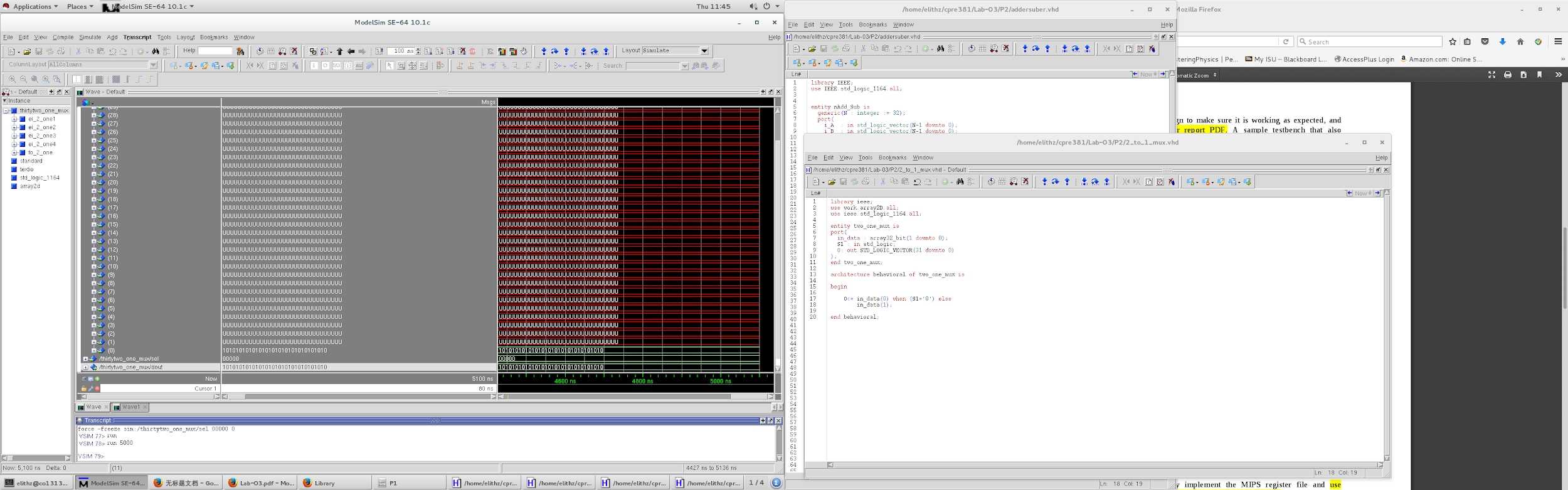
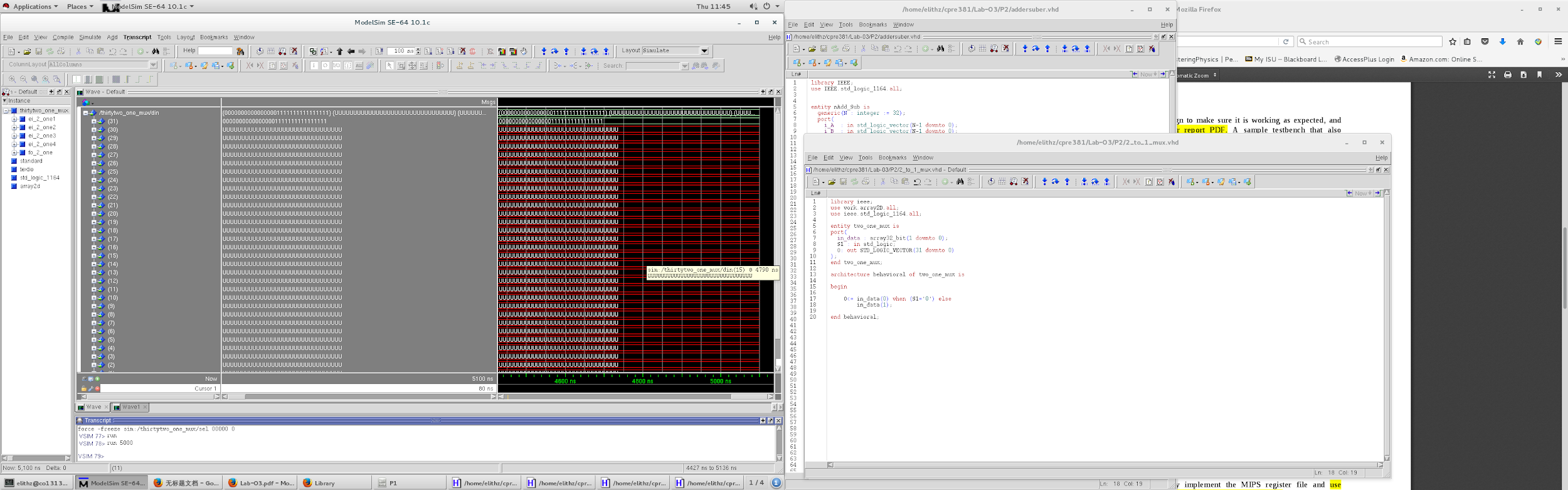
d.) We need 5:32 decoder because 32 is 2^5. This decoder was implemented by a 2:4 decoder and 4 3:8 decoder.

e.)

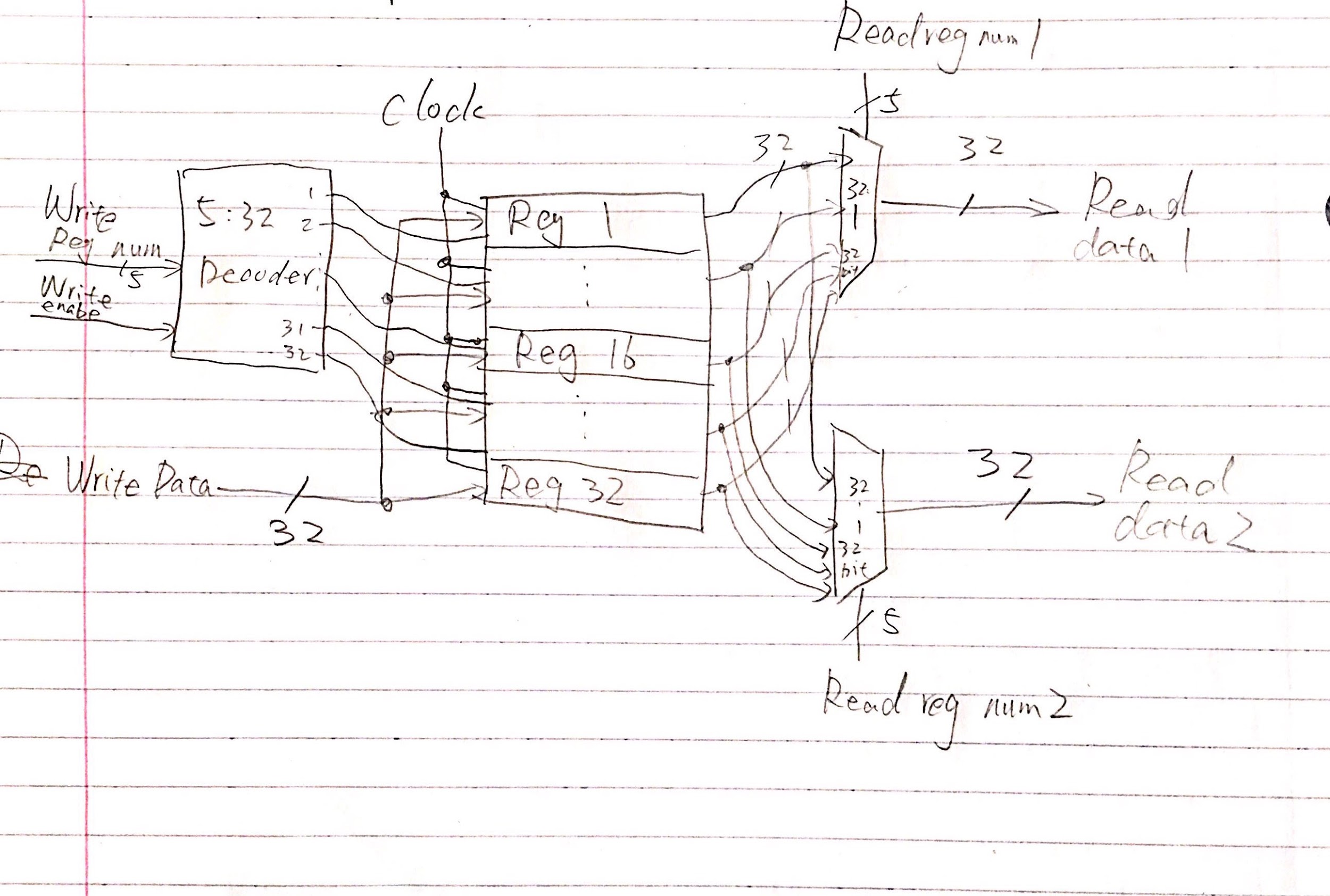


f.) For the 32-bit 32:1 MUX, I used 4 8:1 MUXes and a 4:1 MUX, and I set all of these MUXes’ input to a 32-bit value which was implemented by aD array provided with anouncement on BB.

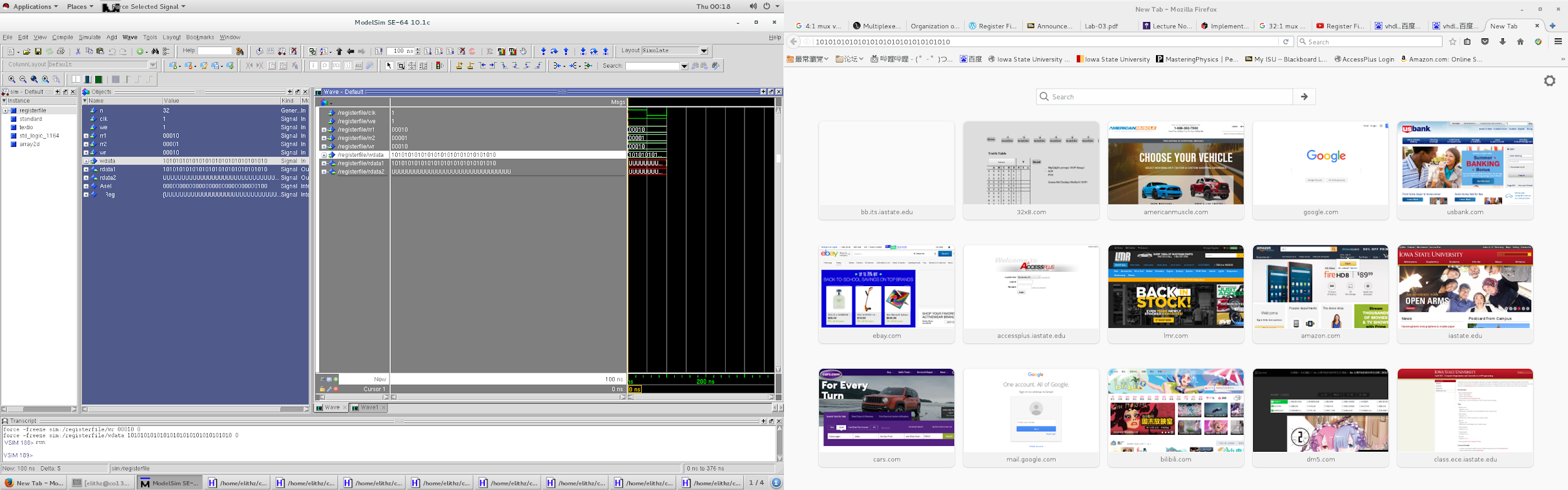
g.)

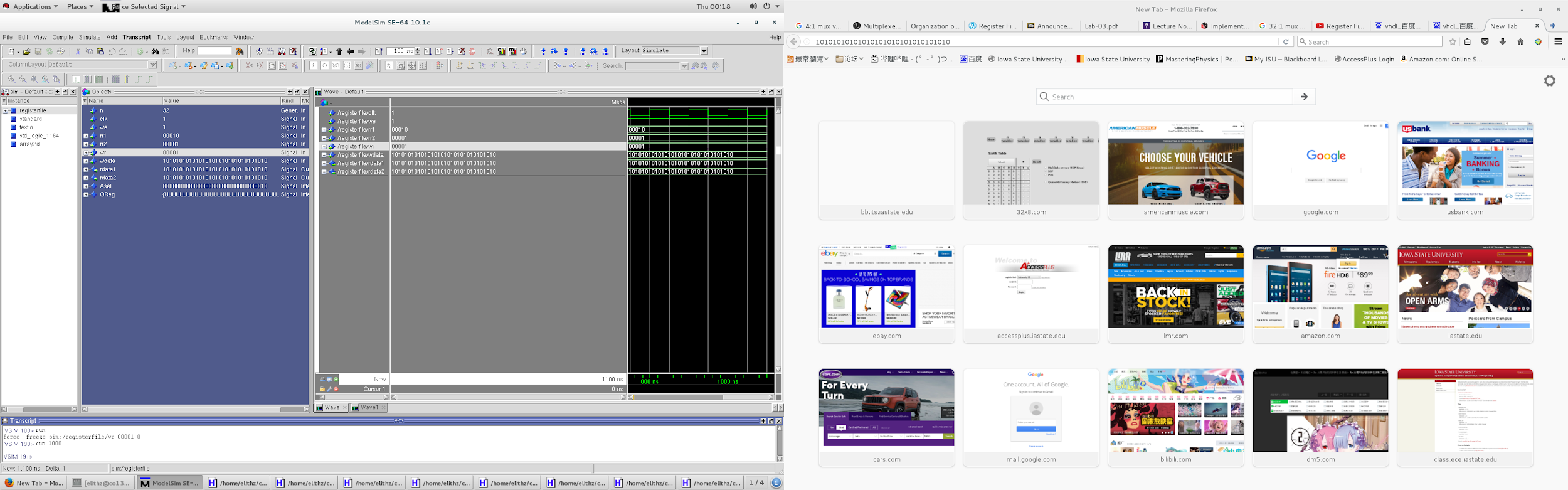


h.) The schematic for MIPS Register File was shown below:



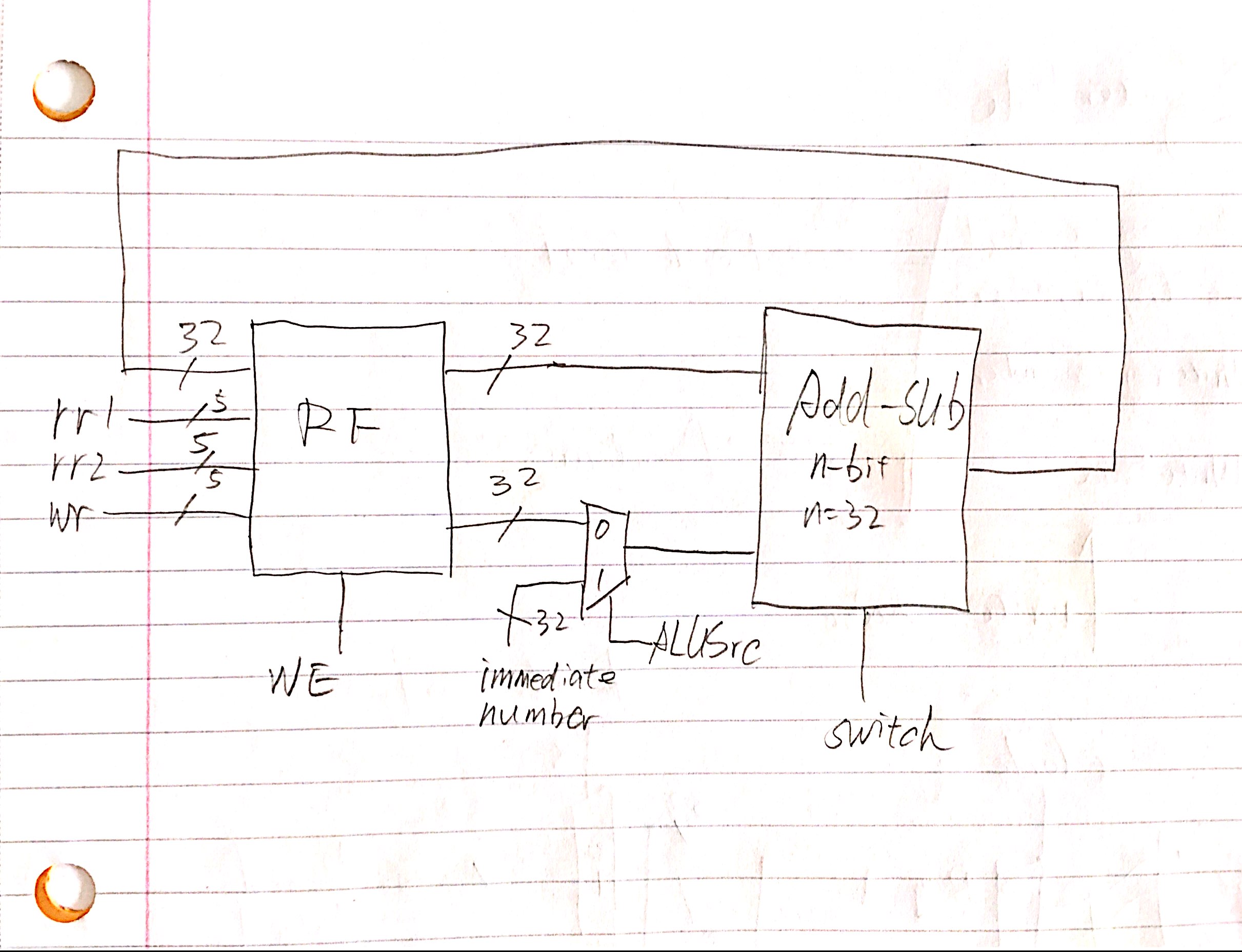
i.)





Part 2.

This application’s schematic was shown below:



For this part, because I don’t have enough time to finish the testbench, but instesd testbench, I did a simple test to get the result of sub and add with write data into registers. And below is my screen shot of this test:

