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Section: A

Date: 4/25/2017

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Project B Lab Report

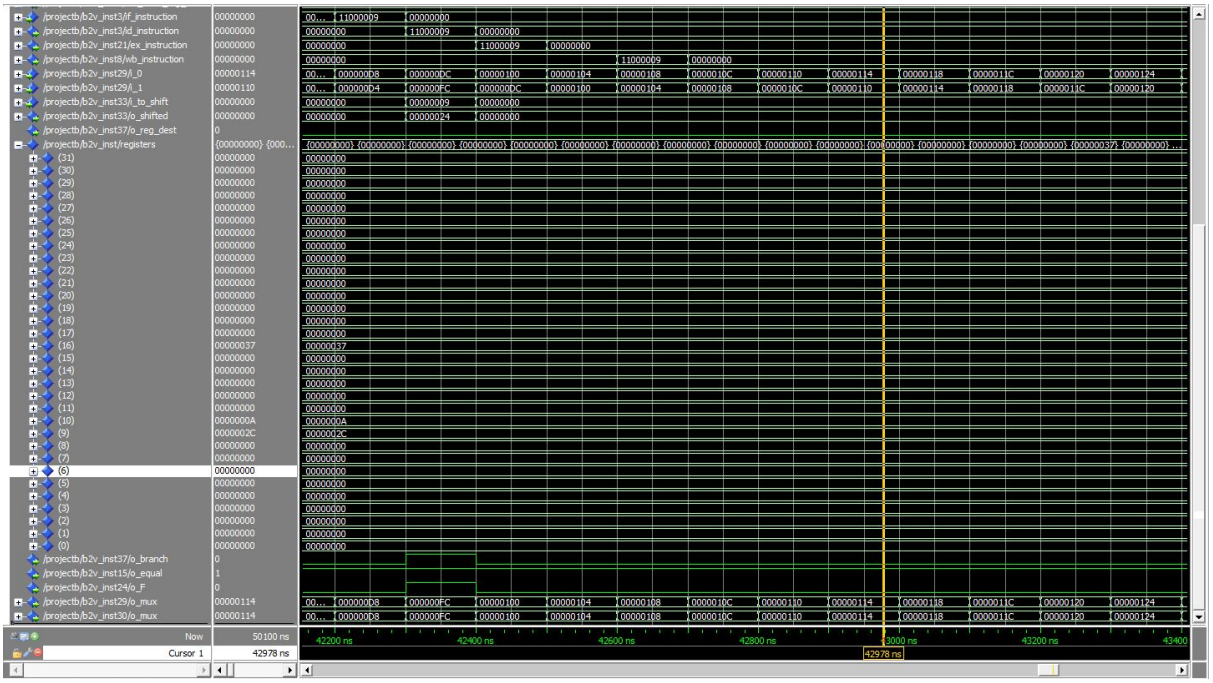
Tests without Hazard and Forwarding(Part 2 and 3):

The out put of U:\cpre381\projectB\ASM Files\Pipeline Test\test.asm:

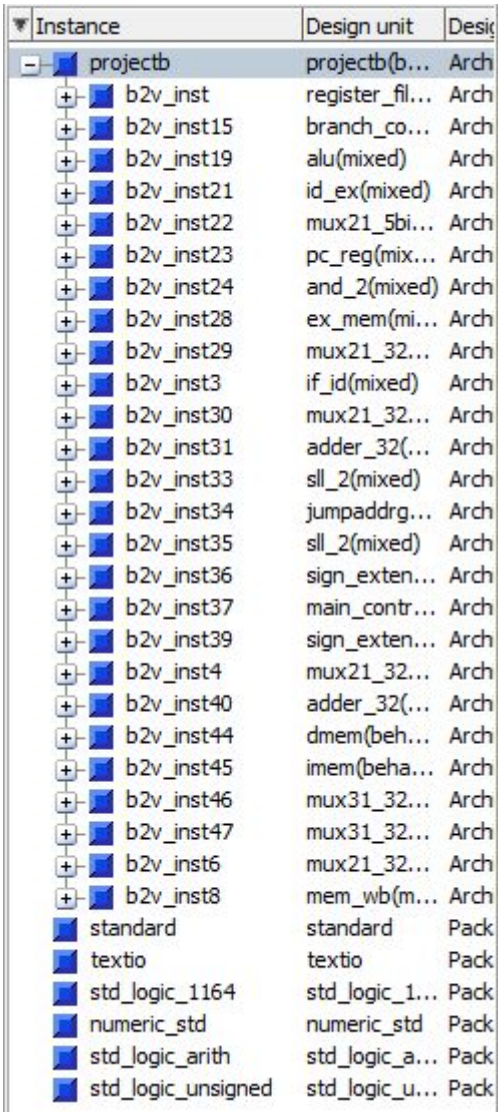
Registers | Coproc 1 | Coproc 0

Name	Number	Value
$zero	0	0x00000000
$at	1	0x10010000
$v0	2	0x00000000
$v1	3	0x00000000
$a0	4	0x00000000
$a1	5	0x00000000
$a2	6	0x00000000
$a3	7	0x00000000
$t0	8	0x00000000
$t1	9	0x1001002c
$t2	10	0x0000000a
$t3	11	0x00000000
$t4	12	0x00000000
$t5	13	0x10010000
$t6	14	0x00000000
$t7	15	0x00000000
$s0	16	0x00000037
$s1	17	0x00000000
$s2	18	0x00000000
$s3	19	0x00000000
$s4	20	0x00000000
$s5	21	0x00000000
$s6	22	0x00000000
$s7	23	0x00000000
$t8	24	0x00000000
$t9	25	0x00000000
$k0	26	0x00000000
$k1	27	0x00000000
$gp	28	0x10008000
$sp	29	0x7fffeffc
$fp	30	0x00000000
$ra	31	0x00000000
pc		0x00400038
hi		0x00000000
lo		0x00000000

The result of my 5-stage-pipeline without hazard and forwarding:

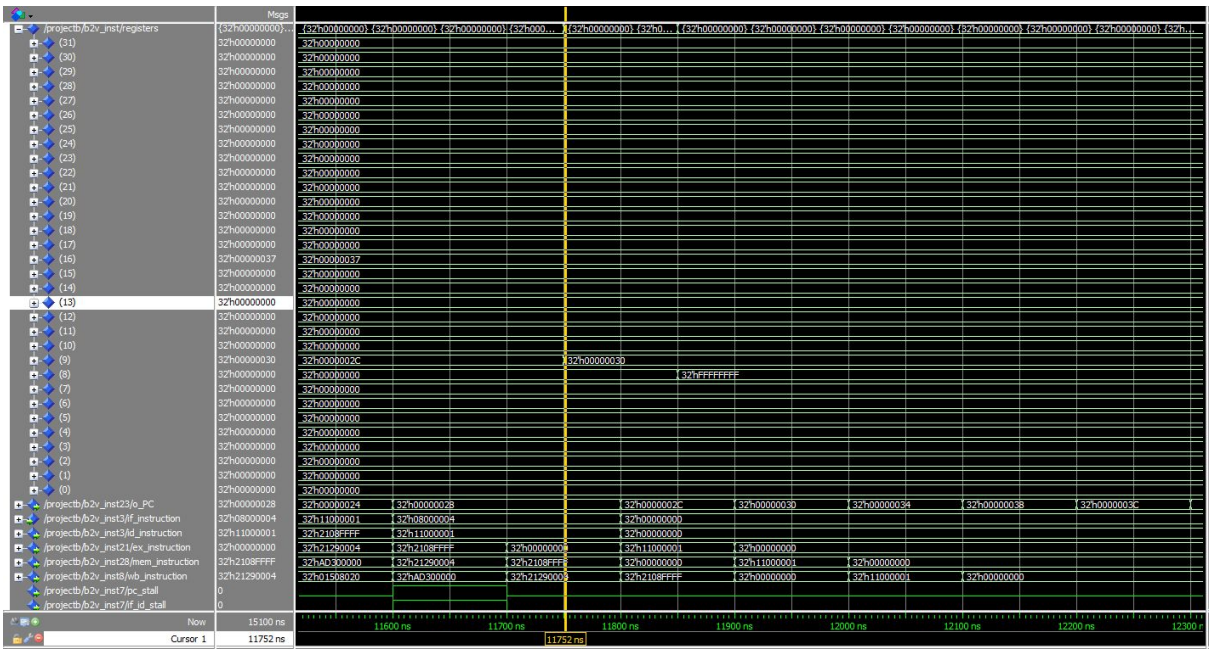


A signal match for different signals:



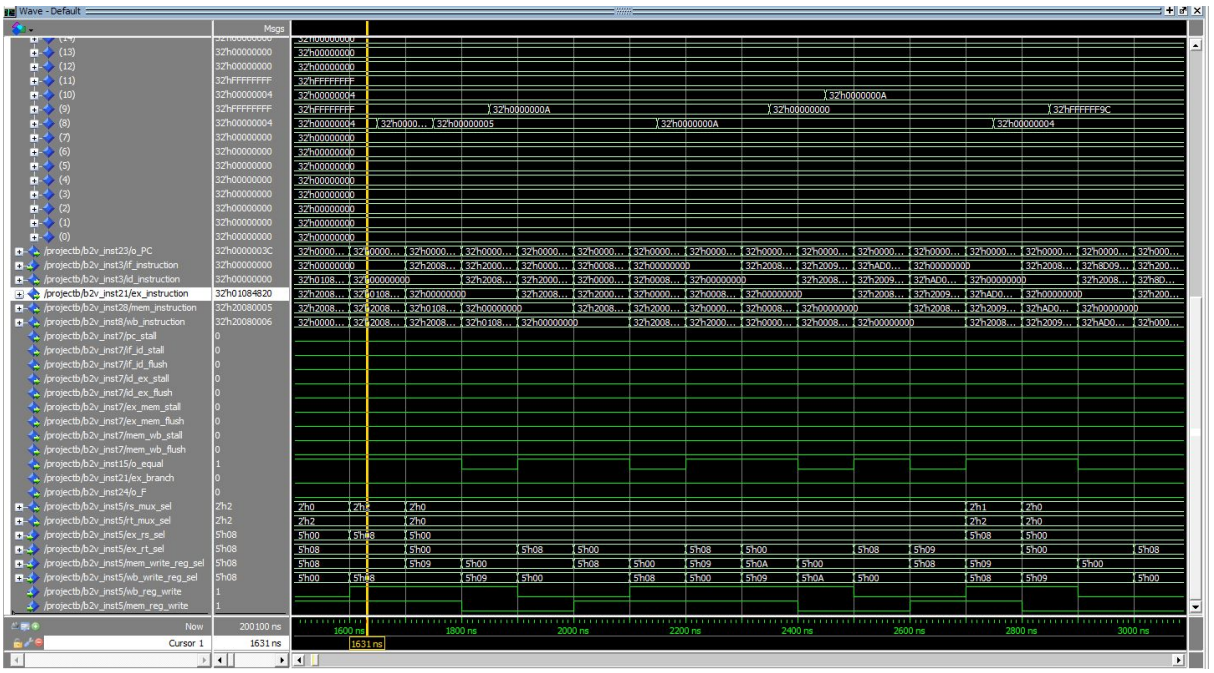
In this part, I originally put the ex_branch into the and gate after comparator, but because the comparators' signals were from id stage which is 1 cycle quicker than ex stage that sent ex_branch, and this caused that the branch will never achieve, so I switched the ex_branch with id_branch and it worked as it should.

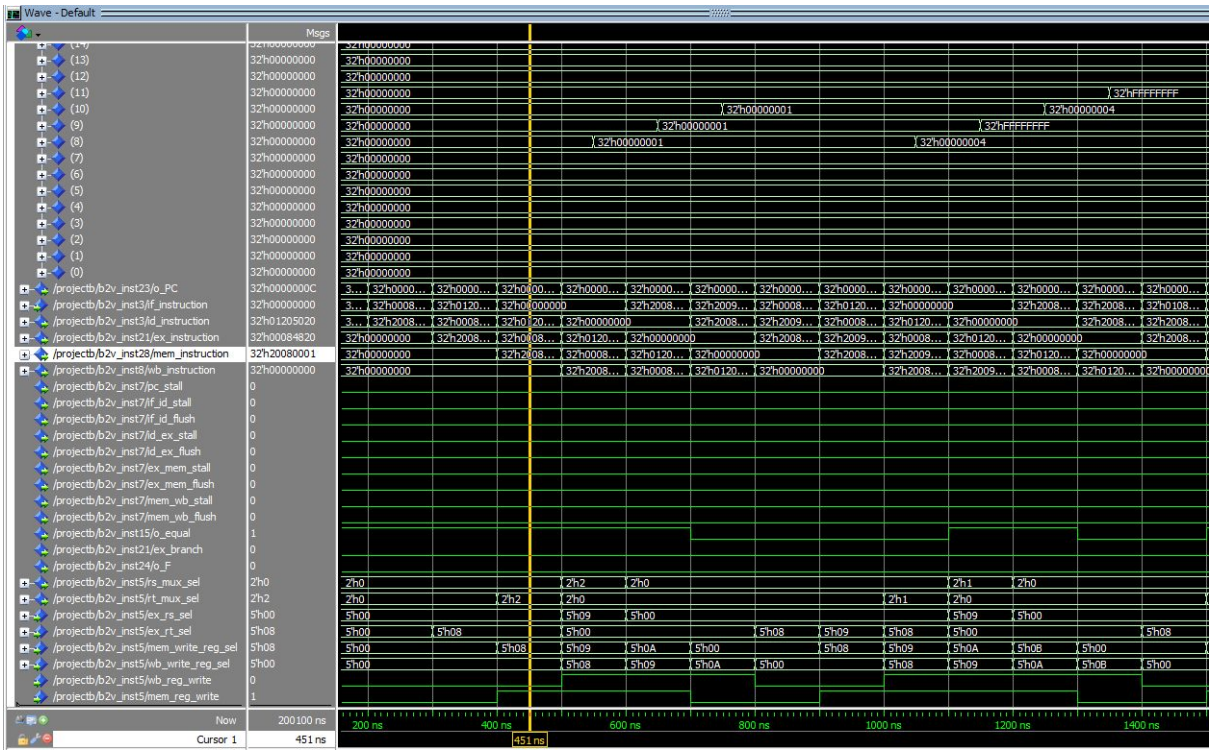
The result of running summation with all correct forwarding and hazard detection:



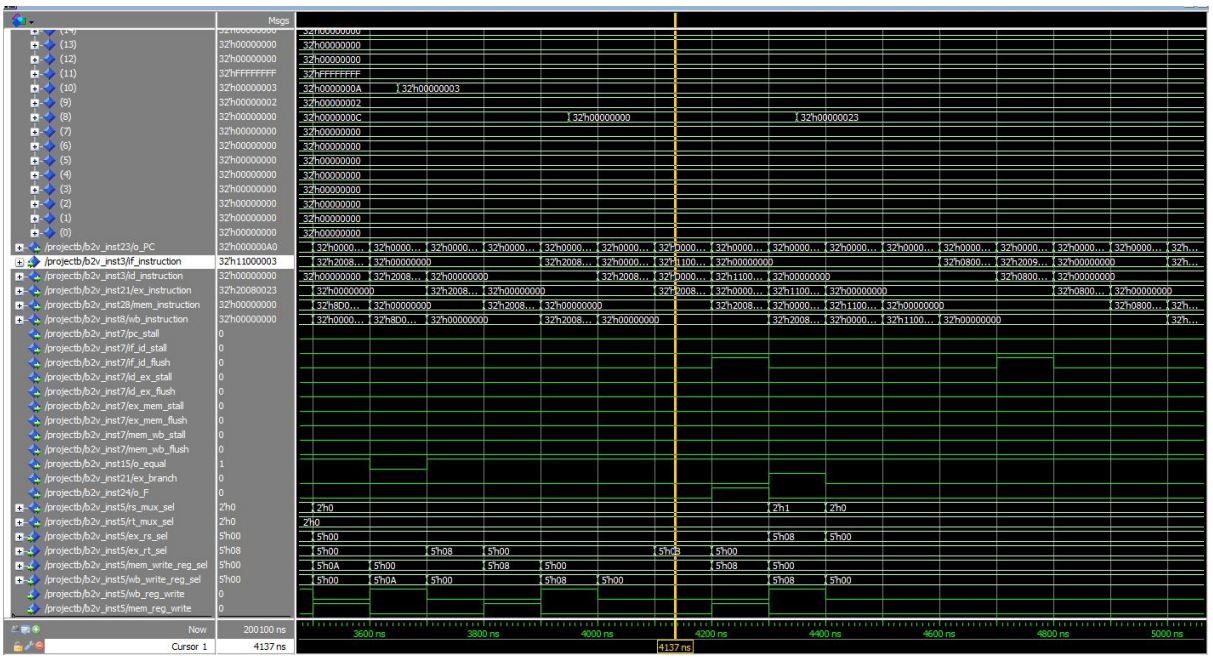
In this part, I actually used the HDandFUtest first to test my forwarding and hazard. with the help of TAs, I corrected all logic mistakes and errors inside the forwarding unit and hazard detection unit.

The result from HDandFUtest.asm (Part 4 and 5):

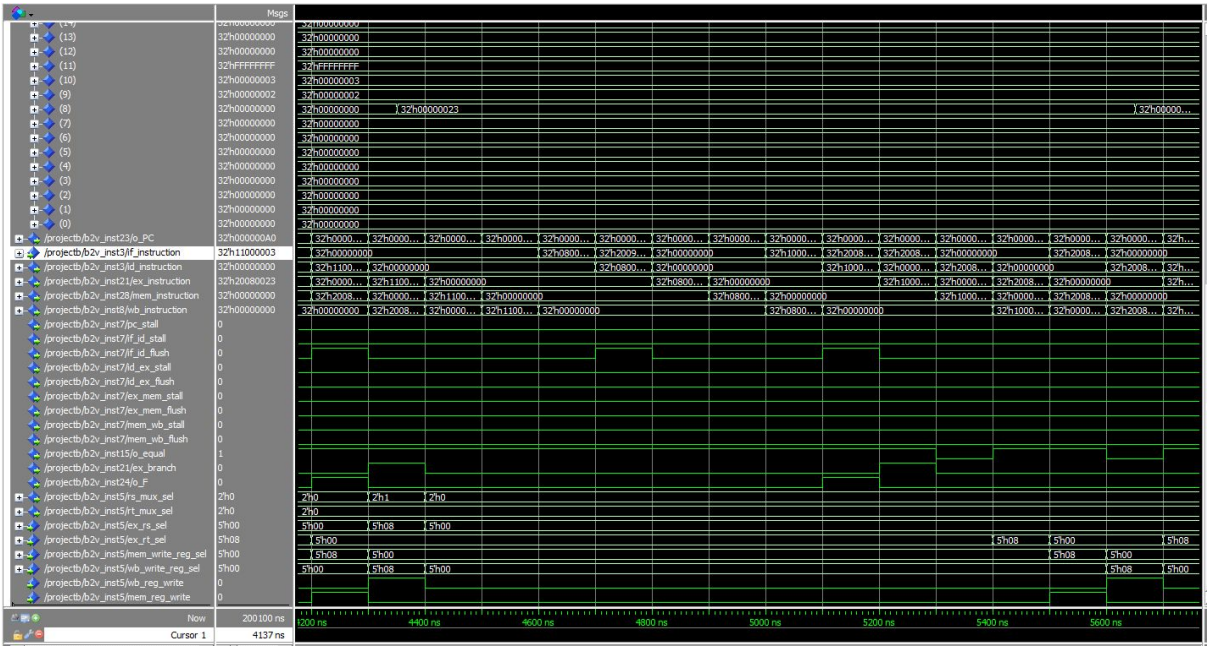




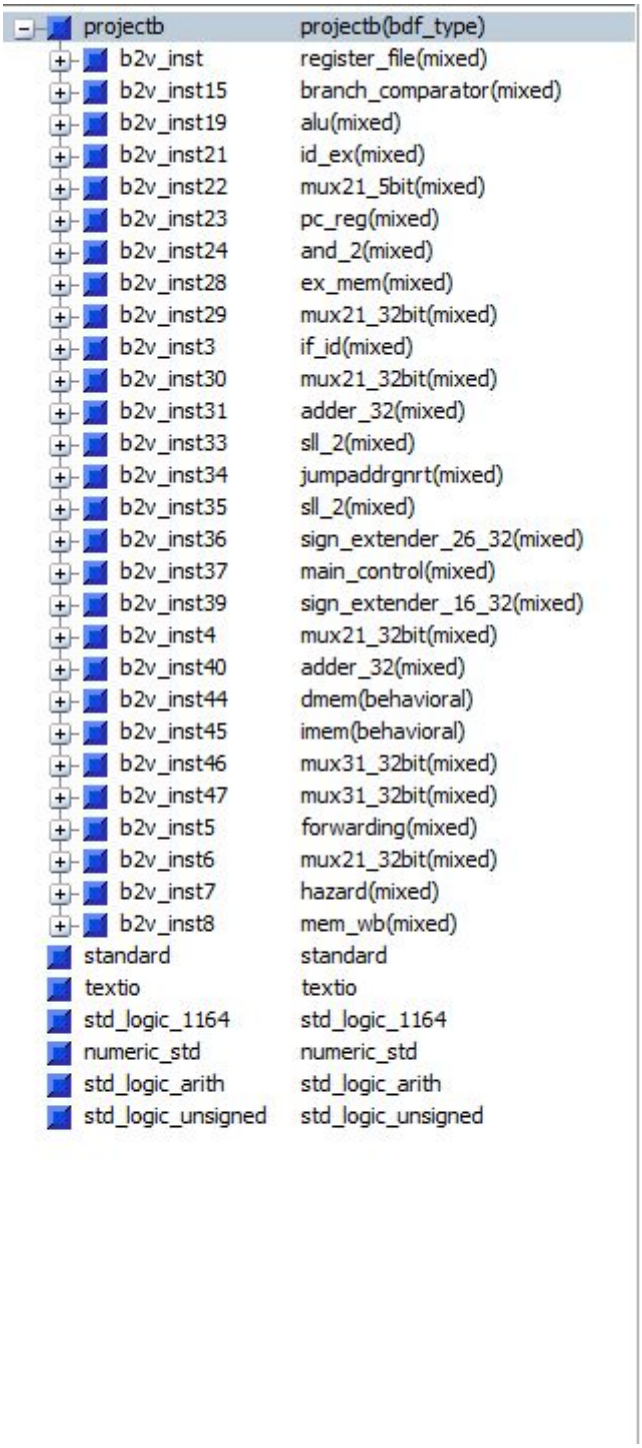
these are the reult of forwarding tests



and this is the branch test of forwarding



other branch and jump test of hazard



this is the signal matches of waveforms of summation and HDandFUtest asm test files when I do the tests.

Conclusion:

All files and circuits are included in my zip. This is a really hard project for me, especially with the ideas of stalls and flushes between different pipeline registers. But with several weeks efforts, I finally finished the lab.