GF-45RFSOI Single-Port Static RAM

(spram_1024x16m8b1pm2re1)

Datasheet

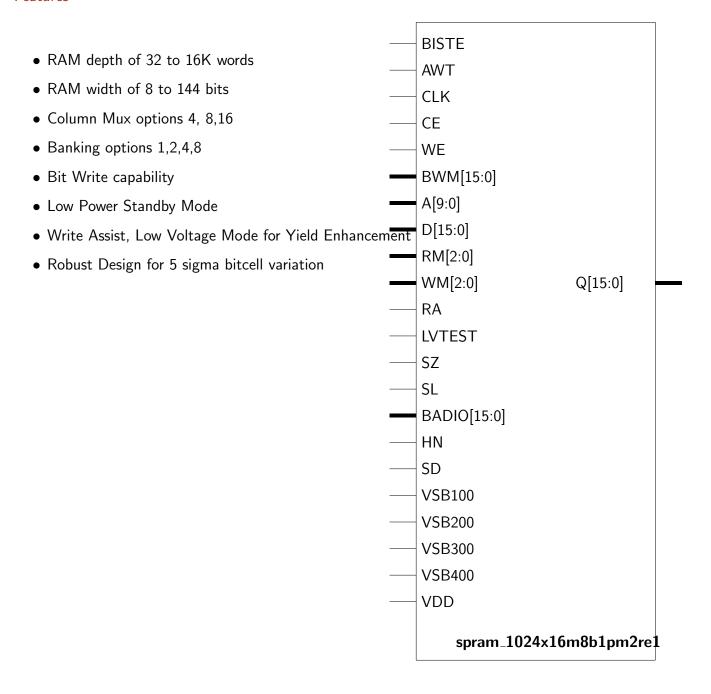
Version: 1.71



Introduction

The SpectralRAM IP Random Access Memory (RAM) core is a fully verified memory unit that uses state of the art power saving techniques to reduce standby power in deep sub-micron process nodes. The width, depth, memory type, and other optional features of the RAM core can be customized based on specifications.

Features





Software	MemoryTime 2.2.1
Compiler Name	Single-Port
Platform	Linux-CentOS
Date of Generation	07/11/19
Technology	GF-45RFSOI
Description	High Density Low Power RAM

Table 1: Compiler Information

Number of Words	1024
Number of Bits	16
Column-Mux	8
Width(um)	89.774
Height(um)	195.084
Area(square um)	17513.5
Frequency(MHz)	1106.67
Top Metal Layer	Metal 4

Table 2: Instance Information



Pin Information

Signal Name	In/Out	Description
BISTE	input	Test Enable: When High Memory operates in test mode else
		if low Memory operates in Normal Mode
AWT	input	
CLK	clock	Clock: All normal read/write operations are synchronous to
		the rising edge of the clock
TCLK	clock	Test Clock: All test read/write operations are synchronous to
		the rising edge of the clock
CE	input	Control signal used to select the macro. When the macro is
		deselected, primary inputs like address data are inhibited from
		accessing the memory array. If the power savings mode is
		selected, this pin will have no impact on the leakage savings
		operations
TCE	input	Test Control signal used to select the macro. When the macro
		is deselected, primary inputs like address data are inhibited
		from accessing the memory array. If the power savings mode
		is selected, this pin will have no impact on the leakage savings
		operations
WE	input	Read/Write Enable(Active High): Control signal used to se-
		lect between read and write operation
TWE	input	Test-Read/Write Enable(Active High): Control signal used to
		select between read and write operation
BWM[15:0]	input	Write Mask(Active High): Bitwise control signal to mask se-
		lected write locations of a word during the write operation.
		The selected word would retain the previous data for all the
		masked bits. The output latches for the masked bits would
		also retain the data read from the prior read operation. This
		bus is a don't care during the read operation
TBWM[15:0]	input	Test Write Mask(Active High): Bitwise control signal to mask
		selected write locations of a word during the write operation.
		The selected word would retain the previous data for all the
		masked bits. The output latches for the masked bits would
		also retain the data read from the prior read operation. This
2.50.01		bus is a don't care during the read operation
A[9:0]	input	Address: Address bus Specifies read and write Locations
TA[9:0]	input	Test Address: Address bus Specifies read and write Locations
D[15:0]	input	Data In: Data bus specifies the contents that get written into
		the Memory for an address specified
TD[15:0]	input	Test Data In: Data bus specifies the contents that get written
		into the Memory for an address specified
Q[15:0]	output	Data out: Data bus used to read contents of the Memory
RM[2:0]	input	Read Margin: this pin is used to control internal timer
WM[2:0]	input	Write Margin: this pin is used to control internal write boost

Table 3: Pin Information



RA	input	Read Assist: Please refer to the Compiler User Guide for the		
		details		
LVTEST	input	Low Voltage Mode for Yield: WL follows Clock High. Please		
		refer to the Compiler User Guide for the details		
SZ	input	SNOOZE: Array Source Bias (Data Retained)		
SL	input	SLUMBER: Periphery Shutdown (Data Retained)		
BADIO[15:0]	input	BADIO: Repair Shifting Signal		
HN	input	HIBERNATE: Array Source Bias + Periphery Shutdown (Data		
		Retained)		
SD	input	SHUTDOWN: Array $+$ Periphery Shutdown (Data Lost)		
VSB100	input	Source Bias (Lowest Level). Please refer to the Compiler User		
		Guide for the details		
VSB200	input	Source Bias (Med-Low Level). Please refer to the Compiler		
		User Guide for the details		
VSB300	input	Source Bias (Med-High Level). Please refer to the Compiler		
		User Guide for the details		
VSB400	input	Source Bias (Highest Level). Please refer to the Compiler		
		User Guide for the details		
VDD	input	Array Power Supply		

Table 3: Pin Information



Truth Table

	WRITE	READ	STANDBY	SNOOZE	SLUMBER	HIBERNATE	SHUTDOWN	TEST
A/TA [9:0]	ADDRESS	ADDRESS	Χ	X	X	X	X	TADDRESS
D/TD[15:0]	DATA	X	X	X	X	X	X	TDATA
BWM/TBWM[15:0]	MASK	X	X	X	X	X	X	TMASK
CLK/TCLK	^CLOCK	^CLOCK	X	X	X	X	X	^TCLOCK
WE/TWE	1	0	X	X	X	X	X	TREAD/TWRIT
CE/TCE	1	1	0	X	X	X	X	TCHIPENABLE
SZ	0	0	0	1	X	X	X	0
SL	0	0	0	0	1	X	X	0
HN	0	0	0	0	0	1	X	0
SD	0	0	0	0	0	0	1	0
Q[15:0]	DATA	DATA	Prev DATA	Prev DATA	Prev DATA	Prev DATA	0	TDATA
BISTE	0	0	X	X	X	X	X	1
MemoryCore	Retained	Retained	Retained	Retained	Retained	Retained	Not Retained	Retained

Table 4: Logic Truth Table

- * ^CLOCK/^TCLOCK: Positive Edge of Clock
- * MemoryCore : State of the stored Memory Contents
- * Each subsequent power down state reduces leakage more than the previous state

 SNOOZE Leakage > SLUMBER Leakage > HIBERNATE Leakage > SHUTDOWN Leakage
- * Each subsequent power down state consumes higher wake-up power than the previous state SNOOZE Power < SLUMBER Power < HIBERNATE Power < SHUTDOWN Power
- * Each subsequent power down state has a higher recovery time than the previous state

 SNOOZE Rec Time < SLUMBER Rec Time < HIBERNATE Rec Time < SHUTDOWN Rec Time



Look Up Table

Index	1	2	3	4	5	6	7
Input Slope(ns)	0.0021	0.0142	0.08	0.1359	0.2311	0.3467	0.52
Input Clock Slope(ns)	0.0021	0.0142	0.08	0.1359	0.2311	0.3467	0.52
Output Load(pF)	0.004	0.009	0.018	0.035	0.075	0.15	0.3

Table 5: Input slope & Output Load

Table shows the Input slews and Output loads that were used to characterize the memory

Operating Conditions

#	PVT Corner	Process	Voltage(V)	Temperature(C)
1	TT_1p00v_25c	TT	1	25
2	FF_1p10v_n40c	FF	1.1	-40
3	FF_1p10v_n55c		1.1	-55
4	FF_1p10v_125c	FF	1.1	125
5	SS_0p90v_n40c	SS	0.9	-40
6	SS_0p90v_n55c		0.9	-55
7	SS_0p90v_125c	SS	0.9	125

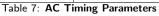
Table 6: **PVT Corners**

Table Depicts different process, voltage and temperature corners that were characterized for this memory.



AC Timing Parameters

#	Parameter(ns)	Description	TT_1p00v_25c	FF_1p10v_n40c	FF_1p10v_n55c
1	Ttens_rise	CLK to BISTE rise	0.138	0.096	0.096
		Setup time			
2	Ttens_fall	CLK to BISTE fall	0.138	0.096	0.096
		Setup time			
3	Ttenh_rise	CLK to BISTE rise Hold	0.576	0.387	0.386
		time			
4	Ttens_fall	CLK to BISTE fall Hold	0.576	0.387	0.386
		time			
5	Ttens_rise	TCLK to BISTE rise	0.138	0.096	0.096
		Setup time			
6	Ttens_fall	TCLK to BISTE fall	0.138	0.096	0.096
7	Ttenh_rise	Setup time TCLK to BISTE rise	0.576	0.207	0.200
7	i tenn_rise	Hold time	0.576	0.387	0.386
8	Ttens_fall	TCLK to BISTE fall	0.576	0.387	0.386
0	i tens_ian	Hold time	0.570	0.307	0.300
9	Tbms	CLK to AWT rise Setup	0.069	0.048	0.048
	l bills	time	0.003	0.010	0.010
10	Tbmx	CLK to AWT fall Setup	0.069	0.048	0.048
		time			
11	Tbms	CLK to AWT rise Hold	0.022	0.020	0.020
		time			
12	Tbmx	CLK to AWT fall Hold	0.022	0.020	0.020
		time			
13	Tbms	TCLK to AWT rise	0.069	0.048	0.048
		Setup time			
14	Tbmx	TCLK to AWT fall	0.069	0.048	0.048
		Setup time			
15	Tbms	TCLK to AWT rise Hold	0.022	0.020	0.020
16	Tbmx	time TCLK to AWT fall Hold	0.022	0.020	0.020
10	I DMX	time	0.022	0.020	0.020
17	Тсс	CLK Cycle Time	0.576	0.387	0.386
18	Tch	CLK Cycle Time CLK Pulse Width High	0.161	0.153	0.152
19	Tcl	CLK Pulse Width Low	0.140	0.098	0.098
20	Tcc	TCLK Cycle Time	0.576	0.387	0.386
21	Tch	TCLK Pulse Width High	0.161	0.153	0.152
22	Tcl	TCLK Pulse Width Low	0.140	0.098	0.098
23	Tces_rise	CLK to CE rise Setup	0.140	0.098	0.098
		time			
24	Tces_fall	CLK to CE fall Setup	0.140	0.098	0.098
		time			
25	Tceh_rise	CLK to CE rise Hold	0.015	0.013	0.013
		time			
26	Tceh_fall	CLK to CE fall Hold	0.015	0.013	0.013
		time	0.110	0.000	0.000
27	Tces_rise	TCLK to TCE rise Setup	0.140	0.098	0.098
20	Toos f-II	time	0.140	0.000	0.098
28	Tces_fall	TCLK to TCE fall Setup	0.140	0.098	υ.09δ
29	Tceh_rise	TCLK to TCE rise Hold	0.015	0.013	0.013
29	i cen_nse	time	0.013	0.013	0.013
30	Tceh_fall	TCLK to TCE fall Hold	0.015	0.013	0.013
	. con_iaii	time	3.013	0.010	5.015
31	Trwcs_rise	CLK to WE rise Setup	0.083	0.056	0.055
		time			
32	Trwcs_fall	CLK to WE fall Setup	0.083	0.056	0.055
L		time			
33	Trwch_rise	CLK to WE rise Hold	0.021	0.022	0.022
		time			
34	Trwch_fall	CLK to WE fall Hold	0.021	0.022	0.022
	_	time			
35	Trwcs_rise	TCLK to TWE rise	0.083	0.056	0.055
		Setup time	iming Parameters		





36	Trwcs_fall	TCLK to TWE fall Setup time	0.083	0.056	0.055		
37	Trwch_rise	TCLK to TWE rise Hold	0.021	0.022	0.022		
38	Trwch_fall	TCLK to TWE fall Hold time	0.021	0.022	0.022		
39	Tbyms_rise	CLK to BWM rise Setup	0.019	0.012	0.012		
40	Tbyms_fall	CLK to BWM fall Setup	0.019	0.012	0.012		
41	Tbymh_rise	CLK to BWM rise Hold time	0.041	0.036	0.036		
42	Tbymh ₋ fall	CLK to BWM fall Hold time	0.041	0.036	0.036		
43	Tbyms_rise	TCLK to TBWM rise Setup time	0.019	0.012	0.012		
44	Tbyms_fall	TCLK to TBWM fall Setup time	0.019	0.012	0.012		
45	Tbymh_rise	TCLK to TBWM rise Hold time	0.041	0.036	0.036		
46	Tbymh_fall	TCLK to TBWM fall Hold time	0.041	0.036	0.036		
47	Tacs_rise	CLK to A rise Setup	0.069	0.048	0.048		
48	Tacs_fall	CLK to A fall Setup time	0.069	0.048	0.048		
49	Tach_rise	CLK to A rise Hold time	0.022	0.020	0.020		
50	Tach_fall	CLK to A fall Hold time	0.022	0.020	0.020		
51	Tacs_rise	TCLK to TA rise Setup time	0.069	0.048	0.048		
52	Tacs_fall	TCLK to TA fall Setup	0.069	0.048	0.048		
53	Tach_rise	TCLK to TA rise Hold time	0.022	0.020	0.020		
54 55	Tach_fall Tdcs_rise	TCLK to TA fall Hold time CLK to D rise Setup	0.022	0.020	0.020		
56	Tdcs_fise Tdcs_fall	time CLK to D rise Setup time	0.001	0.001	0.001		
57	Tdch_rise	time CLK to D rise Hold time	0.001	0.001	0.001		
58	Tdch_fall	CLK to D rise Hold time	0.041	0.036	0.036		
59	Tdcs_rise	TCLK to TD rise Setup	0.001	0.001	0.001		
60	Tdcs_fall	time TCLK to TD fall Setup	0.001	0.001	0.001		
61	Tdch rise	time TCLK to TD rise Hold	0.041	0.036	0.036		
62	Tdch_fall	time TCLK to TD fall Hold	0.041	0.036	0.036		
63	Tcqh	time CLK to Q rise Delay	0.536	0.348	0.346		
64	Tcql	CLK to Q fall Delay	0.544	0.366	0.365		
65	Tcqxh	CLK to Q rise Retain	0.449	0.291	0.290		
66	Tcqxl	CLK to Q fall Retain	0.449	0.291	0.290		
67	Tcqh	D to Q rise Delay	0.536	0.348	0.346		
68	Tcql	D to Q fall Delay	0.544	0.366	0.365		
69	Tcqxh	D to Q rise Retain	0.449	0.291	0.290		
70	Tcqxl	D to Q fall Retain	0.449	0.291	0.290		
71	Tcqh	TD to Q rise Delay	0.536	0.348	0.346		
72	Tcql	TD to Q fall Delay	0.544	0.366	0.365		
73 74	Tcqxh Tcqxl	TD to Q rise Retain TD to Q fall Retain	0.449 0.449	0.291 0.291	0.290 0.290		
75	Tcqxi	TCLK to Q rise Delay	0.536	0.291	0.290		
76	Tcqf	TCLK to Q rise Delay TCLK to Q fall Delay	0.544	0.366	0.365		
77	Tcqxh	TCLK to Q rise Retain	0.449	0.291	0.290		
78	TcqxI	TCLK to Q fall Retain	0.449	0.291	0.290		
79	Trmcs_rise	CLK to RM rise Setup	0.138	0.096	0.096		
80	Trmcs_fall	CLK to RM fall Setup time	0.138	0.096	0.096		
Table 7: AC Timing Parameters							

Table 7: AC Timing Parameters



81	Trmch_rise	CLK to RM rise Hold	0.576	0.387	0.386
82	Trmch_fall	time CLK to RM fall Hold	0.576	0.387	0.386
83	Trmcs_rise	time TCLK to RM rise Setup	0.138	0.096	0.096
84	Trmcs_fall	time TCLK to RM fall Setup	0.138	0.096	0.096
85	Trmch₋rise	time TCLK to RM rise Hold	0.576	0.387	0.386
86	Trmch_fall	time TCLK to RM fall Hold	0.576	0.387	0.386
87	Twmcs_rise	time CLK to WM rise Setup	0.138	0.096	0.096
88	Twmcs_fall	time CLK to WM fall Setup	0.138	0.096	0.096
		time			
89	Twmch₋rise	CLK to WM rise Hold time	0.576	0.387	0.386
90	Twmch_fall	CLK to WM fall Hold time	0.576	0.387	0.386
91	Twmcs_rise	TCLK to WM rise Setup time	0.138	0.096	0.096
92	Twmcs_fall	TCLK to WM fall Setup time	0.138	0.096	0.096
93	Twmch_rise	TCLK to WM rise Hold time	0.576	0.387	0.386
94	Twmch_fall	TCLK to WM fall Hold time	0.576	0.387	0.386
95	Tracs_rise	CLK to RA rise Setup	0.138	0.096	0.096
96	Tracs_fall	CLK to RA fall Setup	0.138	0.096	0.096
97	Trach_rise	time CLK to RA rise Hold	0.576	0.387	0.386
98	Trach_fall	time CLK to RA fall Hold	0.576	0.387	0.386
99	Tracs_rise	time TCLK to RA rise Setup	0.138	0.096	0.096
100	Tracs_fall	time TCLK to RA fall Setup	0.138	0.096	0.096
101	Trach_rise	time TCLK to RA rise Hold	0.576	0.387	0.386
102	Trach_fall	time TCLK to RA fall Hold	0.576	0.387	0.386
103	Tlvcs₋rise	time CLK to LVTEST rise	0.138	0.096	0.096
104	Tlvcs_fall	Setup time CLK to LVTEST fall	0.138	0.096	0.096
105	Tlvch_rise	Setup time CLK to LVTEST rise	0.576	0.387	0.386
106	Tlvch_fall	Hold time CLK to LVTEST fall	0.576	0.387	0.386
107	Tlvcs_rise	Hold time TCLK to LVTEST rise	0.570	0.096	0.096
		Setup time			
108	Tlvcs_fall	TCLK to LVTEST fall Setup time	0.138	0.096	0.096
109	Tlvch_rise	TCLK to LVTEST rise Hold time	0.576	0.387	0.386
110	Tlvch₋fall	TCLK to LVTEST fall Hold time	0.576	0.387	0.386
111	Tszrch	CLK to SZ rise Setup time	0.276	0.193	0.191
112	Tszrcl	CLK to SZ fall Setup	0.276	0.193	0.191
113	Tszrmh	CLK to SZ rise Hold time	0.576	0.387	0.386
114	Tszrml	CLK to SZ fall Hold time	9.309	7.450	7.430
115	Tszrch	TCLK to SZ rise Setup	0.276	0.193	0.191
		time Table 7: AC T	 Iming Parameters		

Table 7: AC Timing Parameters



116	Tszrcl	TCLK to SZ fall Setup	0.276	0.193	0.191
117	Tszrmh	TCLK to SZ rise Hold time	0.576	0.387	0.386
118	Tszrml	TCLK to SZ fall Hold time	9.309	7.450	7.430
119	Tslrch	CLK to SL rise Setup	0.276	0.193	0.191
120	Tslrcl	CLK to SL fall Setup	0.276	0.193	0.191
121	Tslrmh	CLK to SL rise Hold time	0.576	0.387	0.386
122	Tslrml	CLK to SL fall Hold time	9.309	7.450	7.430
				0.193	0.191
123	Tslrch	TCLK to SL rise Setup time	0.276	0.193	0.191
124	Tslrcl	TCLK to SL fall Setup	0.276	0.193	0.191
125	Tslrmh	TCLK to SL rise Hold time	0.576	0.387	0.386
126	Tslrml	TCLK to SL fall Hold time	9.309	7.450	7.430
127	Tbiosh	CLK to BADIO rise Setup time	1.343	1.024	1.018
128	Tbiosl	CLK to BADIO fall Setup time	1.343	1.024	1.018
129	Tbiohh	CLK to BADIO rise Hold time	1.343	1.024	1.018
130	Tbiohl	CLK to BADIO fall Hold time	1.343	1.024	1.018
131	Tbiosh	TCLK to BADIO rise Setup time	1.343	1.024	1.018
132	Tbiosl	TCLK to BADIO fall Setup time	1.343	1.024	1.018
133	Tbiohh	TCLK to BADIO rise Hold time	1.343	1.024	1.018
134	Tbiohl	TCLK to BADIO fall Hold time	1.343	1.024	1.018
135	Thnrch	CLK to HN rise Setup time	0.276	0.193	0.191
136	Thnrcl	CLK to HN fall Setup time	0.276	0.193	0.191
137	Thnrmh	CLK to HN rise Hold time	0.576	0.387	0.386
138	Thnrml	CLK to HN fall Hold time	9.309	7.450	7.430
139	Thnrch	TCLK to HN rise Setup time	0.276	0.193	0.191
140	Thnrcl	TCLK to HN fall Setup time	0.276	0.193	0.191
141	Thnrmh	TCLK to HN rise Hold time	0.576	0.387	0.386
142	Thnrml	TCLK to HN fall Hold time	9.309	7.450	7.430
143	Tsdrch	CLK to SD rise Setup time	0.276	0.193	0.191
144	Tsdrcl	CLK to SD fall Setup time	0.276	0.193	0.191
145	Tsdrmh	CLK to SD rise Hold time	0.576	0.387	0.386
146	Tsdrml	CLK to SD fall Hold time	9.309	7.450	7.430
147	Tsdrch	TCLK to SD rise Setup time	0.276	0.193	0.191
148	Tsdrcl	TCLK to SD fall Setup time	0.276	0.193	0.191
149	Tsdrmh	TCLK to SD rise Hold time	0.576	0.387	0.386
150	Tsdrml	TCLK to SD fall Hold time	9.309	7.450	7.430
		Table 7. AC T	iming Parameters		

Table 7: AC Timing Parameters



151	Tvbcs_rise	CLK to VSB100 rise	0.138	0.096	0.096
152	Tvbcs_fall	Setup time CLK to VSB100 fall	0.138	0.096	0.096
102	T V D CO _ T C III	Setup time	0.130	0.030	0.030
153	Tvbch_rise	CLK to VSB100 rise	0.576	0.387	0.386
		Hold time			
154	Tvbch_fall	CLK to VSB100 fall	0.576	0.387	0.386
155	Tvbcs_rise	Hold time TCLK to VSB100 rise	0.138	0.096	0.096
133	I VDCS_FISE	Setup time	0.136	0.090	0.090
156	Tvbcs_fall	TCLK to VSB100 fall	0.138	0.096	0.096
		Setup time			
157	Tvbch_rise	TCLK to VSB100 rise	0.576	0.387	0.386
158	Tvbch_fall	Hold time TCLK to VSB100 fall	0.576	0.387	0.386
136	i vocn_taii	Hold time	0.576	0.387	0.380
159	Tvbcs_rise	CLK to VSB200 rise	0.138	0.096	0.096
		Setup time			
160	Tvbcs_fall	CLK to VSB200 fall	0.138	0.096	0.096
		Setup time			
161	Tvbch_rise	CLK to VSB200 rise Hold time	0.576	0.387	0.386
162	Tvbch₋fall	CLK to VSB200 fall	0.576	0.387	0.386
-0-		Hold time			1.000
163	Tvbcs₋rise	TCLK to VSB200 rise	0.138	0.096	0.096
		Setup time			
164	Tvbcs_fall	TCLK to VSB200 fall	0.138	0.096	0.096
165	Tvbch_rise	Setup time TCLK to VSB200 rise	0.576	0.387	0.386
103	1 VDCII_IISC	Hold time	0.570	0.507	0.500
166	Tvbch_fall	TCLK to VSB200 fall	0.576	0.387	0.386
		Hold time			
167	Tvbcs_rise	CLK to VSB300 rise	0.138	0.096	0.096
168	Tvbcs_fall	Setup time CLK to VSB300 fall	0.138	0.096	0.096
100	I VDC3_IAII	Setup time	0.130	0.090	0.090
169	Tvbch_rise	CLK to VSB300 rise	0.576	0.387	0.386
		Hold time			
170	Tvbch_fall	CLK to VSB300 fall	0.576	0.387	0.386
171	Tvbcs_rise	Hold time TCLK to VSB300 rise	0.138	0.096	0.096
111	I VDCS_HSE	Setup time	0.130	0.090	0.090
172	Tvbcs_fall	TCLK to VSB300 fall	0.138	0.096	0.096
		Setup time			
173	Tvbch_rise	TCLK to VSB300 rise	0.576	0.387	0.386
174	Tvbch_fall	Hold time TCLK to VSB300 fall	0.576	0.387	0.386
1.7		Hold time	3.3.3	3.301	3.333
175	Tvbcs_rise	CLK to VSB400 rise	0.138	0.096	0.096
4=4		Setup time	0.100	0.005	0.005
176	Tvbcs_fall	CLK to VSB400 fall	0.138	0.096	0.096
177	Tvbch_rise	Setup time CLK to VSB400 rise	0.576	0.387	0.386
1	. VDCII_II3C	Hold time	0.570	0.507	0.500
178	Tvbch₋fall	CLK to VSB400 fall	0.576	0.387	0.386
		Hold time			
179	Tvbcs_rise	TCLK to VSB400 rise Setup time	0.138	0.096	0.096
180	Tvbcs_fall	TCLK to VSB400 fall	0.138	0.096	0.096
100	i voca_iaii	Setup time	0.130	3.030	3.030
181	Tvbch_rise	TCLK to VSB400 rise	0.576	0.387	0.386
		Hold time			
182	Tvbch ₋ fall	TCLK to VSB400 fall	0.576	0.387	0.386
		Hold time	<u> </u>		

Table 7: AC Timing Parameters

^{*} This table shows values only for the nominal slews and output loads.



#	Parameter(ns)	Description	FF_1p10v_125c	SS_0p90v_n40c	SS_0p90v_n55c		
1	Ttens_rise	CLK to BISTE rise	0.104	0.217	0.219		
		Setup time					
2	Ttens_fall	CLK to BISTE fall	0.104	0.217	0.219		
		Setup time					
3	Ttenh_rise	CLK to BISTE rise Hold	0.460	0.848	0.850		
4	Ttens_fall	time CLK to BISTE fall Hold	0.460	0.848	0.850		
4	i tens_faii	time	0.400	0.848	0.850		
5	Ttens_rise	TCLK to BISTE rise	0.104	0.217	0.219		
	1 0011021100	Setup time	0.10	0.217	0.225		
6	Ttens_fall	TCLK to BISTE fall	0.104	0.217	0.219		
		Setup time					
7	Ttenh_rise	TCLK to BISTE rise	0.460	0.848	0.850		
_	T : 6 !!	Hold time	0.460	0.040	0.050		
8	Ttens_fall	TCLK to BISTE fall Hold time	0.460	0.848	0.850		
9	Tbms	CLK to AWT rise Setup	0.052	0.108	0.110		
	1 Dillis	time	0.032	0.100	0.110		
10	Tbmx	CLK to AWT fall Setup	0.052	0.108	0.110		
		time					
11	Tbms	CLK to AWT rise Hold	0.020	0.026	0.028		
1.0	<u> </u>	time	0.000	0.005			
12	Tbmx	CLK to AWT fall Hold	0.020	0.026	0.028		
13	Tbms	time TCLK to AWT rise	0.052	0.108	0.110		
13	I DITIS	Setup time	0.052	0.106	0.110		
14	Tbmx	TCLK to AWT fall	0.052	0.108	0.110		
	1 Dillix	Setup time	0.002	0.100	0.110		
15	Tbms	TCLK to AWT rise Hold	0.020	0.026	0.028		
		time					
16	Tbmx	TCLK to AWT fall Hold	0.020	0.026	0.028		
		time	0.450	0.040	0.050		
17 18	Tcc Tch	CLK Cycle Time CLK Pulse Width High	0.460 0.152	0.848 0.178	0.850 0.178		
19	Tcl	CLK Pulse Width Low	0.152	0.178	0.178		
20	Tcc	TCLK Cycle Time	0.460	0.848	0.850		
21	Tch	TCLK Pulse Width High	0.152	0.178	0.178		
22	Tcl	TCLK Pulse Width Low	0.112	0.204	0.203		
23	Tces_rise	CLK to CE rise Setup	0.112	0.204	0.203		
		time					
24	Tces_fall	CLK to CE fall Setup	0.112	0.204	0.203		
	_	time	0.015	0.010	0.010		
25	Tceh_rise	CLK to CE rise Hold	0.015	0.019	0.019		
26	Tceh_fall	time CLK to CE fall Hold	0.015	0.019	0.019		
20	i con_iaii	time	0.013	0.013	0.013		
27	Tces_rise	TCLK to TCE rise Setup	0.112	0.204	0.203		
		time					
28	Tces_fall	TCLK to TCE fall Setup	0.112	0.204	0.203		
		time					
29	Tceh_rise	TCLK to TCE rise Hold	0.015	0.019	0.019		
20	Took f-II	time	0.015	0.010	0.010		
30	Tceh_fall	TCLK to TCE fall Hold time	0.015	0.019	0.019		
31	Trwcs_rise	CLK to WE rise Setup	0.067	0.120	0.119		
31	111103_1136	time	3.001	3.123	3.113		
32	Trwcs_fall	CLK to WE fall Setup	0.067	0.120	0.119		
		time					
33	Trwch_rise	CLK to WE rise Hold	0.021	0.024	0.024		
	<u> </u>	time					
34	Trwch ₋ fall	CLK to WE fall Hold	0.021	0.024	0.024		
35	Trwcs_rise	time TCLK to TWE rise	0.067	0.120	0.119		
33	i i wcs_rise	Setup time	0.007	U.12U	0.119		
36	Trwcs_fall	TCLK to TWE fall	0.067	0.120	0.119		
		Setup time					
37	Trwch_rise	TCLK to TWE rise Hold	0.021	0.024	0.024		
		time					
_	Table 8: AC Timing Parameters						

Table 8: AC Timing Parameters



38	Trwch_fall	TCLK to TWE fall Hold	0.021	0.024	0.024
		time			
39	Tbyms_rise	CLK to BWM rise Setup	0.013	0.029	0.029
		time			
40	Tbyms_fall	CLK to BWM fall Setup	0.013	0.029	0.029
		time			
41	Tbymh_rise	CLK to BWM rise Hold	0.037	0.051	0.051
		time			
42	Tbymh_fall	CLK to BWM fall Hold	0.037	0.051	0.051
40		time	0.010	2.222	2.000
43	Tbyms_rise	TCLK to TBWM rise	0.013	0.029	0.029
44	T1 . C.11	Setup time	0.012	0.029	0.000
44	Tbyms ₋ fall	TCLK to TBWM fall Setup time	0.013	0.029	0.029
45	Tbymh_rise	TCLK to TBWM rise	0.037	0.051	0.051
43	i byiiii_iise	Hold time	0.037	0.031	0.031
46	Tbymh_fall	TCLK to TBWM fall	0.037	0.051	0.051
		Hold time	0.007	0.001	0.001
47	Tacs_rise	CLK to A rise Setup	0.052	0.108	0.110
		time			
48	Tacs_fall	CLK to A fall Setup time	0.052	0.108	0.110
49	Tach_rise	CLK to A rise Hold time	0.020	0.026	0.028
50	Tach_fall	CLK to A fall Hold time	0.020	0.026	0.028
51	Tacs_rise	TCLK to TA rise Setup	0.052	0.108	0.110
		time			
52	Tacs_fall	TCLK to TA fall Setup	0.052	0.108	0.110
	<u> </u>	time			
53	Tach_rise	TCLK to TA rise Hold	0.020	0.026	0.028
F-4	T. I. C. "	time	0.000	0.006	0.000
54	Tach_fall	TCLK to TA fall Hold time	0.020	0.026	0.028
55	Tdcs_rise	CLK to D rise Setup	0.001	0.004	0.004
33	1 003_1136	time	0.001	J.00 7	0.007
56	Tdcs_fall	CLK to D fall Setup	0.001	0.004	0.004
"		time	0.001	5.001	0.001
57	Tdch_rise	CLK to D rise Hold time	0.037	0.051	0.051
58	Tdch_fall	CLK to D fall Hold time	0.037	0.051	0.051
59	Tdcs_rise	TCLK to TD rise Setup	0.001	0.004	0.004
		time			
60	Tdcs_fall	TCLK to TD fall Setup	0.001	0.004	0.004
		time			
61	Tdch_rise	TCLK to TD rise Hold	0.037	0.051	0.051
		time			
62	Tdch_fall	TCLK to TD fall Hold	0.037	0.051	0.051
	 	time	0.400	0.770	0.775
63	Tcqh	CLK to Q rise Delay	0.430	0.773	0.775
64	Tcql	CLK to Q fall Delay	0.435	0.801	0.803
65 66	Tcqxh	CLK to Q rise Retain	0.360	0.648	0.649
67	Tcqxl Tcqh	CLK to Q fall Retain D to Q rise Delay	0.360 0.430	0.648 0.773	0.649 0.775
68	Tcql	D to Q rise Delay D to Q fall Delay	0.435	0.801	0.775
69	Tcqxh	D to Q fall Delay D to Q rise Retain	0.435	0.648	0.803
70	TcqxII	D to Q fise Retain	0.360	0.648	0.649
71	Tcqh	TD to Q rise Delay	0.430	0.773	0.775
72	Tcql	TD to Q fall Delay	0.435	0.801	0.803
73	Tcqxh	TD to Q rise Retain	0.360	0.648	0.649
74	Tcqxl	TD to Q fall Retain	0.360	0.648	0.649
75	Tcqh	TCLK to Q rise Delay	0.430	0.773	0.775
76	Tcql	TCLK to Q fall Delay	0.435	0.801	0.803
77	Tcqxh	TCLK to Q rise Retain	0.360	0.648	0.649
78	Tcqxl	TCLK to Q fall Retain	0.360	0.648	0.649
79	Trmcs_rise	CLK to RM rise Setup	0.104	0.217	0.219
1		time			
		CLK to RM fall Setup	0.104	0.217	0.219
80	Trmcs_fall	-			l .
		time	0.460	0.040	0.050
80	Trmcs_fall Trmch_rise	time CLK to RM rise Hold	0.460	0.848	0.850
81	Trmch_rise	time CLK to RM rise Hold time			
		time CLK to RM rise Hold	0.460	0.848	0.850

Table 8: AC Timing Parameters



83	Trmcs_rise	TCLK to RM rise Setup	0.104	0.217	0.219
84	Trmcs_fall	TCLK to RM fall Setup	0.104	0.217	0.219
85	Trmch_rise	TCLK to RM rise Hold	0.460	0.848	0.850
86	Trmch_fall	TCLK to RM fall Hold time	0.460	0.848	0.850
87	Twmcs₋rise	CLK to WM rise Setup	0.104	0.217	0.219
88	Twmcs_fall	CLK to WM fall Setup	0.104	0.217	0.219
89	Twmch_rise	CLK to WM rise Hold	0.460	0.848	0.850
90	Twmch_fall	CLK to WM fall Hold	0.460	0.848	0.850
91	Twmcs₋rise	TCLK to WM rise Setup	0.104	0.217	0.219
92	Twmcs_fall	TCLK to WM fall Setup	0.104	0.217	0.219
93	Twmch_rise	TCLK to WM rise Hold time	0.460	0.848	0.850
94	Twmch_fall	TCLK to WM fall Hold time	0.460	0.848	0.850
95	Tracs_rise	CLK to RA rise Setup time	0.104	0.217	0.219
96	Tracs_fall	CLK to RA fall Setup	0.104	0.217	0.219
97	Trach_rise	CLK to RA rise Hold time	0.460	0.848	0.850
98	Trach ₋ fall	CLK to RA fall Hold time	0.460	0.848	0.850
99	Tracs_rise	TCLK to RA rise Setup time	0.104	0.217	0.219
100	Tracs_fall	TCLK to RA fall Setup time	0.104	0.217	0.219
101	Trach_rise	TCLK to RA rise Hold time	0.460	0.848	0.850
102	Trach_fall	TCLK to RA fall Hold time	0.460	0.848	0.850
103	Tlvcs_rise	CLK to LVTEST rise Setup time	0.104	0.217	0.219
104	Tlvcs_fall	CLK to LVTEST fall Setup time	0.104	0.217	0.219
105	Tlvch₋rise	CLK to LVTEST rise Hold time	0.460	0.848	0.850
106	Tlvch_fall	CLK to LVTEST fall Hold time	0.460	0.848	0.850
107	Tlvcs₋rise	TCLK to LVTEST rise Setup time	0.104	0.217	0.219
108	Tlvcs_fall	TCLK to LVTEST fall Setup time	0.104	0.217	0.219
109	Tlvch_rise	TCLK to LVTEST rise Hold time	0.460	0.848	0.850
110	Tlvch₋fall	TCLK to LVTEST fall Hold time	0.460	0.848	0.850
111	Tszrch	CLK to SZ rise Setup time	0.208	0.433	0.439
112	Tszrcl	CLK to SZ fall Setup time	0.208	0.433	0.439
113	Tszrmh	CLK to SZ rise Hold time	0.460	0.848	0.850
114	Tszrml	CLK to SZ fall Hold time	7.635	14.254	14.502
115	Tszrch	TCLK to SZ rise Setup time	0.208	0.433	0.439
116	Tszrcl	TCLK to SZ fall Setup time	0.208	0.433	0.439
117	Tszrmh	TCLK to SZ rise Hold time	0.460	0.848	0.850

Table 8: AC Timing Parameters



118	Tszrml	TCLK to SZ fall Hold time	7.635	14.254	14.502
119	Tslrch	CLK to SL rise Setup	0.208	0.433	0.439
120	Tslrcl	CLK to SL fall Setup	0.208	0.433	0.439
121	Tslrmh	CLK to SL rise Hold time	0.460	0.848	0.850
122	Tslrml	CLK to SL fall Hold time	7.635	14.254	14.502
123	Tslrch	TCLK to SL rise Setup	0.208	0.433	0.439
124	Tslrcl	TCLK to SL fall Setup	0.208	0.433	0.439
125	Tslrmh	TCLK to SL rise Hold time	0.460	0.848	0.850
126	Tslrml	TCLK to SL fall Hold time	7.635	14.254	14.502
127	Tbiosh	CLK to BADIO rise Setup time	1.101	1.871	1.868
128	Tbiosl	CLK to BADIO fall Setup time	1.101	1.871	1.868
129	Tbiohh	CLK to BADIO rise Hold time	1.101	1.871	1.868
130	Tbiohl	CLK to BADIO fall Hold time	1.101	1.871	1.868
131	Tbiosh	TCLK to BADIO rise Setup time	1.101	1.871	1.868
132	Tbiosl	TCLK to BADIO fall Setup time	1.101	1.871	1.868
133	Tbiohh	TCLK to BADIO rise Hold time	1.101	1.871	1.868
134	Tbiohl	TCLK to BADIO fall Hold time	1.101	1.871	1.868
135	Thnrch	CLK to HN rise Setup time	0.208	0.433	0.439
136	Thnrcl	CLK to HN fall Setup time	0.208	0.433	0.439
137	Thnrmh	CLK to HN rise Hold time	0.460	0.848	0.850
138	Thnrml	CLK to HN fall Hold time	7.635	14.254	14.502
139	Thnrch	TCLK to HN rise Setup time	0.208	0.433	0.439
140	Thnrcl	TCLK to HN fall Setup	0.208	0.433	0.439
141	Thnrmh	TCLK to HN rise Hold time	0.460	0.848	0.850
142	Thnrml	TCLK to HN fall Hold time	7.635	14.254	14.502
143	Tsdrch	CLK to SD rise Setup time	0.208	0.433	0.439
144	Tsdrcl	CLK to SD fall Setup time	0.208	0.433	0.439
145	Tsdrmh	CLK to SD rise Hold time	0.460	0.848	0.850
146	Tsdrml	CLK to SD fall Hold time	7.635	14.254	14.502
147	Tsdrch	TCLK to SD rise Setup	0.208	0.433	0.439
148	Tsdrcl	TCLK to SD fall Setup	0.208	0.433	0.439
149	Tsdrmh	TCLK to SD rise Hold time	0.460	0.848	0.850
150	Tsdrml	TCLK to SD fall Hold time	7.635	14.254	14.502
151	Tvbcs_rise	CLK to VSB100 rise Setup time	0.104	0.217	0.219
152	Tvbcs_fall	CLK to VSB100 fall	0.104	0.217	0.219
		Setup time	iming Parameters		

Table 8: AC Timing Parameters



153	Tvbch_rise	CLK to VSB100 rise	0.460	0.848	0.850
		Hold time			
154	Tvbch_fall	CLK to VSB100 fall Hold time	0.460	0.848	0.850
155	Tvbcs_rise	TCLK to VSB100 rise	0.104	0.217	0.219
		Setup time			
156	Tvbcs_fall	TCLK to VSB100 fall	0.104	0.217	0.219
1==		Setup time	0.460	0.040	0.050
157	Tvbch_rise	TCLK to VSB100 rise Hold time	0.460	0.848	0.850
158	Tvbch_fall	TCLK to VSB100 fall	0.460	0.848	0.850
		Hold time			
159	Tvbcs₋rise	CLK to VSB200 rise	0.104	0.217	0.219
160	T 1 6 11	Setup time	0.104	0.017	0.010
160	Tvbcs_fall	CLK to VSB200 fall Setup time	0.104	0.217	0.219
161	Tvbch_rise	CLK to VSB200 rise	0.460	0.848	0.850
		Hold time	0.100	0.0.0	0.000
162	Tvbch_fall	CLK to VSB200 fall	0.460	0.848	0.850
100		Hold time	0.104	0.017	0.010
163	Tvbcs_rise	TCLK to VSB200 rise Setup time	0.104	0.217	0.219
164	Tvbcs_fall	TCLK to VSB200 fall	0.104	0.217	0.219
		Setup time			0.220
165	Tvbch_rise	TCLK to VSB200 rise	0.460	0.848	0.850
166	T 1 -1 C-11	Hold time TCLK to VSB200 fall	0.460	0.040	0.050
166	Tvbch ₋ fall	Hold time	0.460	0.848	0.850
167	Tvbcs_rise	CLK to VSB300 rise	0.104	0.217	0.219
		Setup time			
168	Tvbcs_fall	CLK to VSB300 fall	0.104	0.217	0.219
169	Tvbch_rise	Setup time CLK to VSB300 rise	0.460	0.848	0.850
109	I VDCII_IISE	Hold time	0.400	0.040	0.030
170	Tvbch_fall	CLK to VSB300 fall	0.460	0.848	0.850
		Hold time			
171	Tvbcs_rise	TCLK to VSB300 rise	0.104	0.217	0.219
172	Tvbcs_fall	Setup time TCLK to VSB300 fall	0.104	0.217	0.219
		Setup time	0.20	0.21,	0.213
173	Tvbch₋rise	TCLK to VSB300 rise	0.460	0.848	0.850
174	T	Hold time	0.460	0.040	0.050
174	Tvbch_fall	TCLK to VSB300 fall Hold time	0.460	0.848	0.850
175	Tvbcs_rise	CLK to VSB400 rise	0.104	0.217	0.219
L		Setup time			
176	Tvbcs_fall	CLK to VSB400 fall	0.104	0.217	0.219
177	Tvbch_rise	Setup time CLK to VSB400 rise	0.460	0.848	0.850
111	I VDCII_FISE	Hold time	0.400	0.040	0.000
178	Tvbch_fall	CLK to VSB400 fall	0.460	0.848	0.850
		Hold time			
179	Tvbcs_rise	TCLK to VSB400 rise	0.104	0.217	0.219
180	Tvbcs_fall	Setup time TCLK to VSB400 fall	0.104	0.217	0.219
100	I VDC3_IdII	Setup time	0.104	0.211	0.213
181	Tvbch_rise	TCLK to VSB400 rise	0.460	0.848	0.850
		Hold time			
182	Tvbch₋fall	TCLK to VSB400 fall	0.460	0.848	0.850
		Hold time	iming Parameters		

Table 8: AC Timing Parameters



^{*} This table shows values only for the nominal slews and output loads.

#	Parameter(ns)	Description	SS_0p90v_125c
1	Ttens_rise	CLK to BISTE rise	0.195
		Setup time	
2	Ttens_fall	CLK to BISTE fall Setup time	0.195
3	Ttenh_rise	CLK to BISTE rise Hold	0.904
4	Ttens_fall	time CLK to BISTE fall Hold	0.904
		time	
5	Ttens_rise	TCLK to BISTE rise Setup time	0.195
6	Ttens_fall	TCLK to BISTE fall	0.195
7	Ttenh_rise	Setup time TCLK to BISTE rise	0.904
8	Ttens_fall	Hold time TCLK to BISTE fall	0.904
		Hold time	
9	Tbms	CLK to AWT rise Setup time	0.098
10	Tbmx	CLK to AWT fall Setup	0.098
11	Tbms	time CLK to AWT rise Hold	0.028
		time	
12	Tbmx	CLK to AWT fall Hold time	0.028
13	Tbms	TCLK to AWT rise Setup time	0.098
14	Tbmx	TCLK to AWT fall	0.098
15	Tbms	Setup time TCLK to AWT rise Hold	0.028
		time	
16	Tbmx	TCLK to AWT fall Hold time	0.028
17	Тсс	CLK Cycle Time	0.904
18	Tch	CLK Pulse Width High	0.184
19	Tcl	CLK Pulse Width Low	0.213
20	Tcc	TCLK Cycle Time	0.904
21	Tch	TCLK Pulse Width High	0.184
22	Tcl	TCLK Pulse Width Low	0.213
23	Tces₋rise	CLK to CE rise Setup	0.213
24	Tces_fall	time CLK to CE fall Setup	0.213
		time	
25	Tceh_rise	CLK to CE rise Hold time	0.023
26	Tceh_fall	CLK to CE fall Hold	0.023
27	Tces_rise	time TCLK to TCE rise Setup	0.213
		time	
28	Tces_fall	TCLK to TCE fall Setup time	0.213
29	Tceh_rise	TCLK to TCE rise Hold time	0.023
30	Tceh_fall	TCLK to TCE fall Hold	0.023
31	Trwcs_rise	time CLK to WE rise Setup	0.125
		time	
32	Trwcs_fall	CLK to WE fall Setup	0.125
33	Trwch_rise	CLK to WE rise Hold time	0.027
34	Trwch_fall	CLK to WE fall Hold	0.027
35	Trwcs_rise	time TCLK to TWE rise	0.125
33	11 WC3_(15E	Setup time	0.123
36	Trwcs_fall	TCLK to TWE fall	0.125
37	Trwch_rise	Setup time TCLK to TWE rise Hold	0.027
		time	
	Table	9: AC Timing Parameters	

Table 9: AC Timing Parameters



38	Trwch_fall	TCLK to TWE fall Hold	0.027
39	Tbyms_rise	CLK to BWM rise Setup	0.029
		time	
40	Tbyms_fall	CLK to BWM fall Setup	0.029
41	Tbymh_rise	CLK to BWM rise Hold	0.060
42	Tbymh ₋ fall	time CLK to BWM fall Hold	0.060
		time	
43	Tbyms_rise	TCLK to TBWM rise Setup time	0.029
44	Tbyms_fall	TCLK to TBWM fall Setup time	0.029
45	Tbymh_rise	TCLK to TBWM rise Hold time	0.060
46	Tbymh_fall	TCLK to TBWM fall	0.060
		Hold time	
47	Tacs_rise	CLK to A rise Setup time	0.098
48	Tacs_fall	CLK to A fall Setup time	0.098
49	Tach_rise	CLK to A rise Hold time	0.028
50	Tach_fall	CLK to A fall Hold time	0.028
51	Tacs_rise	TCLK to TA rise Setup	0.098
		time	
52	Tacs_fall	TCLK to TA fall Setup time	0.098
53	Tach_rise	TCLK to TA rise Hold time	0.028
54	Tach ₋ fall	TCLK to TA fall Hold time	0.028
55	Tdcs_rise	CLK to D rise Setup	0.001
56	Tdcs₋fall	CLK to D fall Setup	0.001
		time	
57	Tdch_rise	CLK to D rise Hold time	0.060
58	Tdch_fall	CLK to D rise Hold time CLK to D fall Hold time	0.060 0.060
		CLK to D rise Hold time	
58	Tdch_fall	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup	0.060
58 59	Tdch_fall Tdcs_rise	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD fall Setup time TCLK to TD rise Hold	0.060 0.001
58 59 60	Tdch_fall Tdcs_rise Tdcs_fall	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD rise Hold	0.060 0.001 0.001
58 59 60 61	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD rise Hold time TCLK to TD fall Hold time	0.060 0.001 0.001 0.060 0.060
58 59 60 61	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay	0.060 0.001 0.001 0.060
58 59 60 61	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay	0.060 0.001 0.001 0.060 0.060
58 59 60 61 62 63	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689
58 59 60 61 62 63 64	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay CLK to Q fall Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854
58 59 60 61 62 63 64 65	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay CLK to Q fall Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689
58 59 60 61 62 63 64 65 66	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.689
58 59 60 61 62 63 64 65 66 67 68	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxl Tcqt	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay CLK to Q fall Retain D to Q rise Delay D to Q fall Delay	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.689 0.822 0.854
58 59 60 61 62 63 64 65 66 67 68 69	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxl Tcqt Tcqt	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay CLK to Q fall Retain D to Q rise Delay D to Q fall Delay	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.689 0.822 0.854 0.689
58 59 60 61 62 63 64 65 66 67 68 69 70	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxl Tcqt Tcqt Tcqt	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q fall Delay	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.689 0.689
58 59 60 61 62 63 64 65 66 67 68 69 70 71	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxl Tcqt Tcqt Tcqt Tcqt Tcqt Tcqt Tcqt Tcqt	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay D to Q rise Retain TD to Q rise Delay	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.689 0.689 0.689
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqxh Tcqxl Tcqxl Tcqt Tcqxh Tcqt Tcqt Tcqt Tcqt Tcqt Tcqct	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay D to Q rise Delay D to Q rise Retain D to Q rise Retain D to Q rise Retain TD to Q rise Delay TD to Q fall Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.689 0.689 0.689
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqxh Tcqxh Tcqxl Tcqyh Tcqt Tcqcyh Tcqcyh Tcqcyh Tcqcyh Tcqcyh Tcqcyh Tcqcyh Tcqcyh Tcqxh Tcqcyh Tcqxh	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay D to Q rise Retain D to Q rise Retain D to Q rise Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Delay	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.822 0.854 0.689 0.689 0.689 0.822 0.854 0.689
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqxh Tcqxl Tcqxl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Retain D to Q rise Delay D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Delay	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.689 0.689 0.689 0.689 0.822 0.854 0.689 0.689 0.0822 0.854
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqxh Tcqxl Tcqxh Tcqyl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q fall Retain TD to Q rise Delay TD to Q fall Retain TD to Q fall Retain TD to Q fall Retain TD to Q rise Retain TD to Q fall Retain TD to Q fall Retain TD to Q fall Retain TD to Q rise Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.689 0.689 0.689 0.822 0.854 0.689 0.689 0.0822 0.854 0.689
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxh Tcqyl Tcqxh Tcqyl Tcqxh Tcqcyl Tcqxh Tcqcyl Tcqxh Tcqcyl Tcqxh Tcqcyl Tcqxh Tcqcyl Tcqxh Tcqcyl	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q rise Retain D to Q rise Delay D to Q fall Delay D to Q fall Retain TD to Q rise Delay TD to Q fall Retain TD to Q rise Retain TD to Q fall Retain TD to Q rise Retain TD to Q rise Delay TD to Q rise Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.689 0.822 0.854
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxh Tcql Tcqxh Tcqyl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqcyl Tcqxh	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q rise Retain D to Q rise Delay D to Q fall Delay D to Q fall Retain TD to Q rise Delay TD to Q rise Delay TD to Q rise Retain TD to Q rise Retain TD to Q rise Retain TD to Q rise Delay TD to Q rise Retain TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q rise Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.822 0.854
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqcyl Tcqxh Tcqxl	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q rise Retain D to Q rise Delay D to Q fall Delay D to Q fall Retain TD to Q rise Delay TD to Q rise Delay TD to Q rise Delay TD to Q fall Retain TD to Q rise Retain TD to Q rise Delay TD to Q rise Retain TD to Q rise Delay TD to Q rise Retain TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q rise Retain TCLK to Q rise Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.822 0.854 0.689 0.689 0.689 0.689 0.689 0.689 0.689 0.689 0.689 0.689
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxh Tcql Tcqxh Tcqyl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqcyl Tcqxh	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay D to Q fall Delay D to Q rise Retain D to Q rise Retain TD to Q rise Delay TD to Q rise Delay TD to Q rise Delay TD to Q fall Retain TD to Q rise Retain TD to Q rise Delay TD to Q rise Retain TD to Q rise Retain TCLK to Q rise Retain TCLK to Q rise Retain TCLK to Q rise Delay TCLK to Q rise Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.822 0.854
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqcyl Tcqxh Tcqxl	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q fall Retain D to Q rise Retain TD to Q rise Delay TD to Q rise Delay TD to Q fall Delay TD to Q rise Retain TD to Q rise Retain TCLK to Q rise Retain	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.822 0.854 0.689 0.689 0.689 0.689 0.689 0.689 0.689 0.689 0.689 0.689
58 59 60 61 62 63 64 65 66 67 70 71 72 73 74 75 76 77 78 79	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcql Tcqxh Tcql Tcqxh Tcql Tcqxh Tcql Tcqxh Tcqcl Tcqxh Tcqxl Tcqxh Tcqxl	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q rise Retain D to Q rise Delay D to Q fall Delay D to Q fall Pelay D to Q fall Retain TD to Q rise Delay TD to Q rise Delay TD to Q rise Retain TCLK to RM rise Setup time CLK to RM rise Setup time CLK to RM rise Hold	0.060 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.689 0.689 0.689 0.689
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqt Tcqxl Tcqxh Tcqt Tcqxh Tcqt Tcqxh Tcqxl Trqxh Tcqxl Trqxh Trqxl	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay CLK to Q fall Retain D to Q rise Delay D to Q fall Pelay D to Q fall Retain TD to Q rise Retain TD to Q fall Retain TD to Q fall Retain TD to Q fall Delay TD to Q fall Retain TCLK to Q rise Retain TCLK to Q rise Retain TCLK to Q rise Retain TCLK to Q fall Retain TCLK to Q fall Retain TCLK to Q rise Retain TCLK to Q fall Retain TCLK to RM rise Setup time CLK to RM rise Setup time CLK to RM fall Setup time CLK to RM rise Hold time	0.060 0.001 0.001 0.001 0.060 0.060 0.060 0.822 0.854 0.689 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.689 0.689 0.689 0.689 0.689 0.689 0.195
58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79	Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqcyl Tcqxh Tcqxl	CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q rise Retain D to Q rise Delay D to Q fall Delay D to Q fall Pelay D to Q fall Retain TD to Q rise Delay TD to Q rise Delay TD to Q rise Retain TCLK to RM rise Setup time CLK to RM rise Setup time CLK to RM rise Hold	0.060 0.001 0.001 0.001 0.060 0.060 0.822 0.854 0.689 0.822 0.854 0.689 0.689 0.822 0.854 0.689 0.689 0.689 0.689 0.689 0.689 0.689 0.689 0.195

Table 9: AC Timing Parameters



83	Trmcs_rise	TCLK to RM rise Setup	0.195
84	Trmcs_fall	TCLK to RM fall Setup	0.195
85	Trmch_rise	TCLK to RM rise Hold time	0.904
86	Trmch_fall	TCLK to RM fall Hold time	0.904
87	Twmcs₋rise	CLK to WM rise Setup	0.195
88	Twmcs_fall	CLK to WM fall Setup	0.195
89	Twmch₋rise	CLK to WM rise Hold time	0.904
90	Twmch_fall	CLK to WM fall Hold time	0.904
91	Twmcs_rise	TCLK to WM rise Setup	0.195
92	Twmcs_fall	TCLK to WM fall Setup	0.195
93	Twmch₋rise	TCLK to WM rise Hold	0.904
94	Twmch_fall	TCLK to WM fall Hold time	0.904
95	Tracs_rise	CLK to RA rise Setup	0.195
96	Tracs_fall	CLK to RA fall Setup	0.195
97	Trach_rise	CLK to RA rise Hold time	0.904
98	Trach_fall	CLK to RA fall Hold time	0.904
99	Tracs_rise	TCLK to RA rise Setup	0.195
100	Tracs_fall	TCLK to RA fall Setup	0.195
101	Trach_rise	TCLK to RA rise Hold time	0.904
102	Trach_fall	TCLK to RA fall Hold time	0.904
103	Tlvcs₋rise	CLK to LVTEST rise Setup time	0.195
104	Tlvcs_fall	CLK to LVTEST fall Setup time	0.195
105	Tlvch₋rise	CLK to LVTEST rise Hold time	0.904
106	Tlvch_fall	CLK to LVTEST fall Hold time	0.904
107	Tlvcs₋rise	TCLK to LVTEST rise Setup time	0.195
108	Tlvcs_fall	TCLK to LVTEST fall Setup time	0.195
109	Tlvch₋rise	TCLK to LVTEST rise Hold time	0.904
110	Tlvch₋fall	TCLK to LVTEST fall Hold time	0.904
111	Tszrch	CLK to SZ rise Setup time	0.391
112	Tszrcl	CLK to SZ fall Setup time	0.391
113	Tszrmh	CLK to SZ rise Hold time	0.904
114	Tszrml	CLK to SZ fall Hold time	14.427
115	Tszrch	TCLK to SZ rise Setup time	0.391
116	Tszrcl	TCLK to SZ fall Setup time	0.391
117	Tszrmh	TCLK to SZ rise Hold time 9: AC Timing Parameters	0.904

Table 9: AC Timing Parameters



TSZTMI				
119	118	Tszrml		14.427
120 Tsircl CLK to SL fall Setup 0.391 time 121 Tsirmh CLK to SL rise Hold 0.904 time 122 Tsirml CLK to SL fall Hold time 14.427 123 Tsirch TCLK to SL fall Setup 0.391 time 124 Tsircl TCLK to SL fall Setup 0.391 time 125 Tsirmh TCLK to SL fall Setup 0.391 time 126 Tsirml TCLK to SL fall Hold 14.427 time 127 Tbiosh CLK to BADIO rise Setup time 128 Tbiosl CLK to BADIO fall 2.013 Setup time 129 Tbiohh CLK to BADIO fall 2.013 Setup time 130 Tbiohl CLK to BADIO fall 2.013 Setup time 131 Tbiosh TCLK to BADIO fall 2.013 Setup time 132 Tbiosl TCLK to BADIO fall 2.013 Setup time 133 Tbiohh TCLK to BADIO fall 2.013 Setup time 134 Tbiohl TCLK to BADIO fall 2.013 Setup time 135 Thnrch TCLK to HN rise Setup 0.391 time 136 Thnrch CLK to HN fall Setup 0.391 time 137 Thnrmh CLK to HN rise Hold time 138 Thnrml CLK to HN fall Setup 0.391 time 138 Thnrml CLK to HN fall Setup 0.391 time 137 Thnrmh CLK to HN rise Hold 14.427 time 140 Thnrch TCLK to HN fall Setup 0.391 time 140 Thnrch TCLK to HN fall Setup 0.391 time 140 Thnrch TCLK to HN fall Setup 0.391 time 140 Thnrch TCLK to HN fall Setup 0.391 time 141 Thnrmh TCLK to HN fall Setup 0.391 time 142 Thnrml TCLK to HN fall Hold 14.427 time 144 Tsdrcl CLK to SD rise Setup 0.391 time 145 Tsdrmh CLK to SD rise Setup 0.391 time 146 Tsdrml TCLK to SD rise Setup 0.391 time 147 Tsdrch TCLK to SD rise Setup 0.391 time 148 Tsdrcl TCLK to SD rise Hold 0.904 time 144 Tsdrcl TCLK to SD rise Hold 0.904 time 145 Tsdrmh TCLK to SD rise Hold 0.904 time 146 Tsdrmh TCLK to SD rise Hold 0.904 time 150 Tsdrmh TCLK to SD rise Hold 0.904 time 150 Tsdrmh TCLK to SD rise Hold 0.904 time 150 Tsdrmh TCLK to SD rise Hold 0.905 TCLK to SD rise Ho	119	Tslrch	CLK to SL rise Setup	0.391
121 Tsirmh	120	Tslrcl	CLK to SL fall Setup	0.391
122 Tsirml CLK to SL fall Hold time 14.427 123 Tsirch TCLK to SL rise Setup 0.391 124 Tsircl TCLK to SL rise Setup 0.391 125 Tsirmh TCLK to SL rise Hold 0.904 126 Tsirml TCLK to SL rise Hold 0.904 127 Tbiosh CLK to BADIO rise 2.013 128 Tbiosl CLK to BADIO rise 2.013 129 Tbiohh CLK to BADIO rise 2.013 120 Tbiohh CLK to BADIO rise 2.013 121 Tbiosh TCLK to BADIO rise 2.013 122 Tbiosh TCLK to BADIO rise 2.013 130 Tbiohl CLK to BADIO rise 2.013 131 Tbiosh TCLK to BADIO rise 2.013 132 Tbiosl TCLK to BADIO rise 2.013 133 Tbiosh TCLK to BADIO rise 2.013 134 Tbiohh TCLK to BADIO rise 2.013 135 Thnrch TCLK to BADIO rise 2.013 136 Thnrcl TCLK to BADIO rise 0.391 137 Thnrmh CLK to HN rise Setup 0.391 138 Thnrmh CLK to HN rise Hold 0.904 139 Thnrch TCLK to HN fall Setup 0.391 130 Thnrch TCLK to HN fall Setup 0.391 131 Thorh TCLK to HN fall Setup 0.391 132 Thorh TCLK to HN rise Hold 0.904 133 Thnrmh TCLK to HN rise Setup 0.391 140 Thnrcl TCLK to HN fall Setup 0.391 141 Thnrmh TCLK to HN fall Setup 0.391 142 Thnrml TCLK to HN fall Hold 14.427 143 Tsdrch TCLK to SD rise Setup 0.391 144 Tsdrcl CLK to SD rise Setup 0.391 145 Tsdrmh TCLK to SD rise Setup 0.391 146 Tsdrml TCLK to SD rise Setup 0.391 147 Tsdrch TCLK to SD rise Setup 0.391 148 Tsdrcl TCLK to SD rise Setup 0.391 149 Tsdrml TCLK to SD rise Hold 0.904 150 Tsdrml TCLK to SD rise Hold 0.904 151 Tvbcs_rise CLK to SD rise Hold 0.904 152 Tvbcs_rise CLK to VSB100 rise 0.195 Setup time 150 TSdrml TCLK to VSB100 rise 0.195 152 Tvbcs_rise CLK to VSB100 rise 0.195 152 Tvbcs_rise CLK to VSB100 rise 0.195 154 Total Tclk to SD rise Iola 0.195 155 Tsdrml TCLK to	121	Tslrmh	CLK to SL rise Hold	0.904
123	100	Tolumal		14.407
124 Tsircl TCLK to SL fall Setup time 125 Tsirmh TCLK to SL rise Hold 0.904 time 126 Tsirmh TCLK to SL rise Hold 14.427 time 127 Tbiosh CLK to BADIO rise 2.013 Setup time 128 Tbiosl CLK to BADIO rise 2.013 Setup time 129 Tbiohh CLK to BADIO fall 2.013 Setup time 130 Tbiohl CLK to BADIO fall 4.013 CLK to BADIO rise 2.013 Hold time 131 Tbiosh TCLK to BADIO fall 2.013 Setup time 132 Tbiosl TCLK to BADIO rise 2.013 Setup time 133 Tbiohh TCLK to BADIO rise 2.013 Setup time 134 Tbiohl TCLK to BADIO rise 2.013 Hold time 134 Tbiohl TCLK to BADIO fall 2.013 Hold time 135 Thnrch CLK to HN rise Setup 0.391 time 136 Thnrcl CLK to HN rise Hold 0.904 time 137 Thnrmh CLK to HN rise Hold 0.904 time 138 Thnrml CLK to HN rise Setup 0.391 time 139 Thnrch TCLK to HN rise Setup 0.391 time 140 Thnrcl TCLK to HN rise Hold 0.904 time 140 Thnrcl TCLK to HN rise Hold 0.904 time 141 Thnrmh TCLK to HN rise Hold 0.904 time 142 Thnrml TCLK to HN rise Hold 0.904 time 143 Tsdrch CLK to SD rise Setup 0.391 time 145 Tsdrmh CLK to SD rise Setup 0.391 time 146 Tsdrml CLK to SD rise Hold 0.904 time 147 Tsdrch CLK to SD rise Hold 0.904 time 148 Tsdrch CLK to SD rise Hold 0.904 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 140 Tsdrml TCLK to SD rise Hold 0.904 time 140 Tsdrml TCLK to SD rise Hold 0.904 time 140 Tsdrml TCLK to SD rise Hold 0.904 time 140 Tsdrml TCLK to SD rise Hold 0.904 time 140 Tsdrml TCLK to SD rise Hold 0.904 time 140 Tsdrml TCLK to SD rise Hold 0.904 time 140 Tsdrml TCLK to SD rise Hold 0.904 time 140 Tsdrml TCLK to SD rise Hold 0.904 time 140 Tsdrml TCLK to SD rise Hold 0.904 time 140 Tsdrml TCLK to SD rise Hold				
125 Tslrmh			time	
126			time	
127 Tbiosh CLK to BADIO rise 2.013	125	Tslrmh	time	0.904
Setup time	126	Tslrml		14.427
128 Tbios CLK to BADIO fall Setup time 129 Tbiohh CLK to BADIO rise 2.013 Hold time 130 Tbiohl CLK to BADIO fall Hold 2.013 time 131 Tbiosh TCLK to BADIO rise 2.013 Setup time 132 Tbiosl TCLK to BADIO fall 2.013 Setup time 133 Tbiohl TCLK to BADIO rise 2.013 Setup time 134 Tbiohl TCLK to BADIO fall 2.013 Hold time 135 Thnrch CLK to HN rise Setup 0.391 time 136 Thnrch CLK to HN fall Setup 0.391 time 137 Thnrmh CLK to HN rise Hold 0.904 time 138 Thnrmh CLK to HN fall Hold 14.427 time 139 Thnrch TCLK to HN fall Setup 0.391 time 140 Thnrch TCLK to HN fall Setup 0.391 time 141 Thnrmh TCLK to HN fall Setup 0.391 time 142 Thnrmh TCLK to HN fall Setup 0.391 time 143 Tsdrch CLK to SD rise Setup 0.391 time 144 Tsdrcl CLK to SD rise Setup 0.391 time 145 Tsdrmh CLK to SD rise Setup 0.391 time 146 Tsdrml CLK to SD rise Hold 0.904 time 147 Tsdrch CLK to SD rise Setup 0.391 time 148 Tsdrcl CLK to SD rise Setup 0.391 time 148 Tsdrcl TCLK to SD rise Setup 0.391 time 148 Tsdrcl TCLK to SD rise Setup 0.391 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 148 Tsdrcl TCLK to SD rise Hold 0.904 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.905 Setup time 150 Tsdrml TCLK to VSB100 rise 0.195 Setup time 150 Tsdrml TCLK to VSB100 rise 0.195 Setup time 150 Tsdrml CLK to VSB100 rise 0.195 Setup time 150 Tybcs_fall CLK to VSB100 fall 0.195 Setup time 150 Tybcs_fall CLK to VSB100 rise 0.195 Setup time 150 Tybcs_fall CLK to VSB100 rise 0.195 Setup time 150 Tybcs_fall CLK to VSB100 rise 0.195 Setup time 150 Tybcs_fall CLK to VSB100 rise 0.195 Setup time 150 Tybcs_fall Tybcs_fall Tybcs_fall Tybcs_fall	127	Tbiosh		2.013
Setup time	128	Tbiosl		2.013
Hold time				
130 Tbiohl CLK to BADIO fall Hold time 131 Tbiosh TCLK to BADIO rise 2.013 Setup time 132 Tbiosl TCLK to BADIO rise 2.013 Setup time 133 Tbiohh TCLK to BADIO rise 2.013 Hold time 134 Tbiohl TCLK to BADIO fall 2.013 Hold time 135 Thnrch CLK to HN rise Setup 0.391 time 136 Thnrch CLK to HN rise Hold 0.904 time 137 Thnrmh CLK to HN rise Hold 0.904 time 138 Thnrml CLK to HN rise Setup 0.391 time 139 Thnrch TCLK to HN rise Setup 0.391 time 140 Thnrch TCLK to HN rise Hold 0.904 time 141 Thnrmh TCLK to HN rise Hold 0.904 time 142 Thnrmh TCLK to HN rise Hold 0.904 time 143 Tsdrch CLK to SD rise Setup 0.391 time 144 Tsdrch CLK to SD rise Setup 0.391 time 145 Tsdrmh CLK to SD rise Hold 0.904 time 145 Tsdrmh CLK to SD rise Setup 0.391 time 146 Tsdrml TCLK to SD rise Setup 0.391 time 147 Tsdrch TCLK to SD rise Setup 0.391 time 148 Tsdrch TCLK to SD rise Setup 0.391 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise 0.195 Setup time 0.195 Setup ti	129	Tbiohh	CLK to BADIO rise	2.013
131 Tbiosh TCLK to BADIO rise 2.013 Setup time 132 Tbiosl TCLK to BADIO rise 2.013 Setup time 133 Tbiohh TCLK to BADIO rise 2.013 Hold time 134 Tbiohl TCLK to BADIO fall 2.013 Hold time 135 Thnrch CLK to HN rise Setup 0.391 time 136 Thnrch CLK to HN rise Hold 0.904 time 137 Thnrmh CLK to HN rise Hold 0.904 time 138 Thnrmh CLK to HN rise Setup 0.391 time 139 Thnrch TCLK to HN rise Setup 0.391 time 140 Thnrch TCLK to HN rise Setup 0.391 time 141 Thnrmh TCLK to HN rise Hold 0.904 time 142 Thnrml TCLK to HN rise Hold 0.904 time 143 Tsdrch CLK to SD rise Setup 0.391 time 144 Tsdrcl CLK to SD rise Setup 0.391 time 145 Tsdrmh CLK to SD rise Hold 0.904 time 146 Tsdrml CLK to SD rise Setup 0.391 time 147 Tsdrch TCLK to SD rise Setup 0.391 time 148 Tsdrcl TCLK to SD rise Setup 0.391 time 149 Tsdrmh TCLK to SD rise Setup 0.391 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.904 time 151 Tvbcs.rise CLK to VSB100 rise 0.195 Setup time 152 Tvbcs.fall CLK to VSB100 rise 0.195 Setup time 152 Tvbcs.fall CLK to VSB100 rise 0.195 Setup time 152 Tvbcs.fall CLK to VSB100 rise 0.195 Setup time 152 Tvbcs.fall CLK to VSB100 rise 0.195 Setup time 152 Tvbcs.fall CLK to VSB100 rise 0.195 Setup time 150 Tsdrml CLK to VSB100 rise 0.195 Setup time	130	Tbiohl		2.013
Setup time 132 Tbiosl TCLK to BADIO fall 2.013 Setup time 133 Tbiohh TCLK to BADIO rise 2.013 Hold time 134 Tbiohl TCLK to BADIO fall 2.013 Hold time 135 Thnrch CLK to HN rise Setup time 136 Thnrcl CLK to HN fall Setup time 137 Thnrmh CLK to HN fall Setup time 138 Thnrml CLK to HN fall Hold 14.427 time 139 Thnrch TCLK to HN fall Setup time 139 Thnrch TCLK to HN fall Setup time 140 Thnrcl TCLK to HN fall Setup time 141 Thnrmh TCLK to HN fall Hold 14.427 time 142 Thnrml TCLK to HN fall Hold 14.427 time 143 Tsdrch CLK to SD rise Setup time 144 Tsdrcl CLK to SD fall Setup time 145 Tsdrmh CLK to SD fall Setup time 146 Tsdrml CLK to SD fall Hold 14.427 time 147 Tsdrch TCLK to SD fall Setup time 148 Tsdrch TCLK to SD fall Setup time 149 Tsdrmh TCLK to SD fall Setup time 149 Tsdrmh TCLK to SD fall Hold 14.427 time 150 Tsdrml TCLK to SD fall Hold 14.427 time 150 Tsdrml TCLK to SD fall Hold 14.427 time 150 Tsdrml TCLK to SD fall Hold 14.427 time 150 Tsdrml TCLK to SD fall Hold 14.427 time 150 Tsdrml TCLK to VSB100 rise 0.195 Setup time 150 Tvbcs_fall CLK to VSB100 fall 0.195 Setup time 150 Tvbcs_fall CLK to VSB100 fall 0.195 Setup time 150 Tvbcs_fall CLK to VSB100 fall 0.195 Setup time 150 Tsdrml TCLK to VSB100 fall 0.195 Setup time 150 Tsdrml TCLK to VSB100 fall 0.195 Setup time 150 Tsdrml TCLK to VSB100 fall 0.195 Setup time 150 Tsdrml TCLK to VSB100 fall 0.195 Setup time 150 Tsdrml TCLK to VSB100 fall 0.195 Setup time 150 Tsdrml TCLK to VSB100 fall 0.195 Setup time 150 Tsdrml TCLK to VSB100 fall 0.195 Setup time 150 Tsdrml TcLK to VSB100 fall 0.195 Setup time 150 Tsdrml TcLK to VSB100 fall 0.195 TcLK to VSB100 fall 0.195 TcLK to VSB100 fall 0.195 TcLK to VSB100 fall			time	
Setup time 133 Tbiohh TCLK to BADIO rise 2.013 Hold time 134 Tbiohl TCLK to BADIO fall 2.013 Hold time 135 Thnrch CLK to HN rise Setup 0.391 time 136 Thnrch CLK to HN fall Setup time 137 Thnrmh CLK to HN rise Hold 0.904 time 138 Thnrml CLK to HN fall Hold 14.427 time 139 Thnrch TCLK to HN rise Setup time 140 Thnrcl TCLK to HN fall Setup time 141 Thnrmh TCLK to HN rise Hold 14.427 time 142 Thnrml TCLK to HN fall Hold 14.427 time 143 Tsdrch CLK to SD rise Setup 0.391 time 144 Tsdrcl CLK to SD rise Setup time 145 Tsdrmh CLK to SD rise Hold 0.904 time 146 Tsdrml TCLK to SD rise Setup 0.391 time 147 Tsdrch TCLK to SD rise Setup 0.391 time 148 Tsdrcl TCLK to SD rise Setup 0.391 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD rise Hold 0.905 time 150 Tsdrml TCLK to SD rise Hold 0.905 Setup time 151 Tvbcs_rise CLK to VSB100 rise 0.195 Setup time 152 Tvbcs_fall CLK to VSB100 fall 0.195 Setup time 150 Setup time			Setup time	
Hold time 134			Setup time	
134	133	Tbiohh		2.013
135	134	Tbiohl	TCLK to BADIO fall	2.013
136	135	Thnrch	CLK to HN rise Setup	0.391
137 Thnrmh CLK to HN rise Hold time 138 Thnrml CLK to HN fall Hold time 139 Thnrch TCLK to HN rise Setup time 140 Thnrcl TCLK to HN fall Setup time 141 Thnrmh TCLK to HN rise Hold time 142 Thnrml TCLK to HN fall Hold time 143 Tsdrch CLK to SD rise Setup time 144 Tsdrcl CLK to SD rise Setup time 145 Tsdrmh CLK to SD rise Hold time 146 Tsdrml TCLK to SD rise Setup time 147 Tsdrch CLK to SD rise Setup time 148 Tsdrcl TCLK to SD rise Setup time 149 Tsdrmh TCLK to SD rise Hold time 150 Tsdrml TCLK to SD rise Hold time 151 Tvbcs_rise CLK to VSB100 rise 152 Tvbcs_fall CLK to VSB100 fall CLK to VSB100 fall	136	Thnrcl	CLK to HN fall Setup	0.391
138 Thnrml CLK to HN fall Hold 14.427 time 139 Thnrch TCLK to HN rise Setup 0.391 time 140 Thnrcl TCLK to HN fall Setup 0.391 time 141 Thnrmh TCLK to HN rise Hold 0.904 time 142 Thnrml TCLK to HN fall Hold 14.427 time 143 Tsdrch CLK to SD rise Setup 0.391 time 144 Tsdrcl CLK to SD fall Setup 0.391 time 145 Tsdrmh CLK to SD rise Hold 0.904 time 146 Tsdrml CLK to SD fall Hold 14.427 time 147 Tsdrch TCLK to SD rise Setup 0.391 time 148 Tsdrcl TCLK to SD fall Setup 0.391 time 149 Tsdrmh TCLK to SD fall Setup 0.391 time 150 Tsdrml TCLK to SD fall Hold 14.427 time 151 Tvbcs_rise CLK to VSB100 rise 0.195 Setup time 152 Tvbcs_fall CLK to VSB100 fall 0.195 Setup time	137	Thnrmh		0.904
Thurch			time	
140 Thnrcl TCLK to HN fall Setup 0.391			time	
Thurmh	139	-	time	
141 Thnrmh TCLK to HN rise Hold time 0.904 142 Thnrml TCLK to HN fall Hold time 14.427 143 Tsdrch CLK to SD rise Setup 0.391 0.391 144 Tsdrcl CLK to SD fall Setup 0.391 0.391 145 Tsdrmh CLK to SD rise Hold 0.904 0.427 146 Tsdrml CLK to SD rise Setup 0.391 0.391 147 Tsdrch TCLK to SD rise Setup 0.391 0.391 148 Tsdrcl TCLK to SD fall Setup 0.391 0.391 149 Tsdrmh TCLK to SD rise Hold 0.904 0.904 150 Tsdrml TCLK to SD fall Hold 14.427 14.427 150 Tsdrml TCLK to VSB100 rise 0.195 0.195 Setup time CLK to VSB100 fall 0.195 0.195	140	Thnrcl	-	0.391
142 Thnrml TCLK to HN fall Hold time 14.427 143 Tsdrch CLK to SD rise Setup time 0.391 144 Tsdrcl CLK to SD fall Setup time 0.391 145 Tsdrmh CLK to SD rise Hold time 0.904 146 Tsdrml CLK to SD fall Hold time 14.427 147 Tsdrch TCLK to SD rise Setup time 0.391 148 Tsdrcl TCLK to SD fall Setup time 0.391 149 Tsdrmh TCLK to SD rise Hold time 0.904 150 Tsdrml TCLK to SD fall Hold time 14.427 151 Tvbcs_rise CLK to VSB100 rise time 0.195 152 Tvbcs_fall CLK to VSB100 fall time 0.195	141	Thnrmh	TCLK to HN rise Hold	0.904
time 143 Tsdrch CLK to SD rise Setup 0.391 time 144 Tsdrcl CLK to SD fall Setup 0.391 time 145 Tsdrmh CLK to SD rise Hold 0.904 time 146 Tsdrml CLK to SD fall Hold 14.427 time 147 Tsdrch TCLK to SD rise Setup 0.391 time 148 Tsdrcl TCLK to SD fall Setup 0.391 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD fall Hold 14.427 time 151 Tvbcs_rise CLK to VSB100 rise 0.195 Setup time 152 Tvbcs_fall CLK to VSB100 fall 0.195 Setup time 155 Setup time	140	Thomas		14.427
time			time	-
time 145 Tsdrmh CLK to SD rise Hold 0.904 time 146 Tsdrml CLK to SD fall Hold 14.427 time 147 Tsdrch TCLK to SD rise Setup 0.391 time 148 Tsdrcl TCLK to SD fall Setup 0.391 time 149 Tsdrmh TCLK to SD rise Hold 0.904 time 150 Tsdrml TCLK to SD fall Hold 14.427 time 151 Tvbcs_rise CLK to VSB100 rise 0.195 Setup time 152 Tvbcs_fall CLK to VSB100 fall 0.195 Setup time 155 Setup time 156 Setup time 157 Setup time 158 Setup time 159 Setup time 150 Setup time 150	143	Tsdrch	time	0.391
145 Tsdrmh CLK to SD rise Hold time 0.904 146 Tsdrml CLK to SD fall Hold time 14.427 147 Tsdrch TCLK to SD rise Setup time 0.391 148 Tsdrcl TCLK to SD fall Setup time 0.391 149 Tsdrmh TCLK to SD rise Hold time 0.904 150 Tsdrml TCLK to SD fall Hold time 14.427 151 Tvbcs_rise CLK to VSB100 rise Setup time 0.195 152 Tvbcs_fall CLK to VSB100 fall to 0.195 Setup time 0.195	144	Tsdrcl		0.391
146 Tsdrml CLK to SD fall Hold time 14.427 147 Tsdrch TCLK to SD rise Setup time 0.391 148 Tsdrcl TCLK to SD fall Setup time 0.391 149 Tsdrmh TCLK to SD rise Hold time 0.904 150 Tsdrml TCLK to SD fall Hold time 14.427 151 Tvbcs_rise CLK to VSB100 rise Setup time 0.195 152 Tvbcs_fall CLK to VSB100 fall to 0.195 Setup time 0.195	145	Tsdrmh	CLK to SD rise Hold	0.904
147 Tsdrch TCLK to SD rise Setup time 0.391 148 Tsdrcl TCLK to SD fall Setup time 0.391 149 Tsdrmh TCLK to SD rise Hold time 0.904 150 Tsdrml TCLK to SD fall Hold time 14.427 151 Tvbcs_rise CLK to VSB100 rise Setup time 0.195 152 Tvbcs_fall CLK to VSB100 fall Setup time 0.195	146	Tsdrml	CLK to SD fall Hold	14.427
148 Tsdrcl TCLK to SD fall Setup time 0.391 149 Tsdrmh TCLK to SD rise Hold 0.904 time 0.904 150 Tsdrml TCLK to SD fall Hold 14.427 time 14.427 151 Tvbcs_rise CLK to VSB100 rise Setup time 0.195 Setup time 152 Tvbcs_fall CLK to VSB100 fall 0.195 Setup time	147	Tsdrch	TCLK to SD rise Setup	0.391
149 Tsdrmh TCLK to SD rise Hold time 0.904 150 Tsdrml TCLK to SD fall Hold time 14.427 151 Tvbcs_rise CLK to VSB100 rise Setup time 0.195 152 Tvbcs_fall CLK to VSB100 fall Setup time 0.195	148	Tsdrcl	TCLK to SD fall Setup	0.391
TSdrml	149	Tsdrmh	TCLK to SD rise Hold	0.904
151 Tvbcs_rise CLK to VSB100 rise Setup time 0.195 152 Tvbcs_fall CLK to VSB100 fall Setup time 0.195	150	Tsdrml	TCLK to SD fall Hold	14.427
Setup time 152 Tvbcs_fall CLK to VSB100 fall 0.195 Setup time	1=1	-		0.105
Setup time			Setup time	
	152	Tvbcs_fall		0.195
		Table		

Table 9: AC Timing Parameters



153	Tvbch_rise	CLK to VSB100 rise Hold time	0.904
154	Tvbch₋fall	CLK to VSB100 fall	0.904
155		Hold time	0.105
155	Tvbcs_rise	TCLK to VSB100 rise Setup time	0.195
156	Tvbcs_fall	TCLK to VSB100 fall	0.195
157	Tvbch_rise	Setup time TCLK to VSB100 rise	0.904
		Hold time	
158	Tvbch_fall	TCLK to VSB100 fall Hold time	0.904
159	Tvbcs_rise	CLK to VSB200 rise Setup time	0.195
160	Tvbcs_fall	CLK to VSB200 fall	0.195
161		Setup time	
161	Tvbch_rise	CLK to VSB200 rise Hold time	0.904
162	Tvbch_fall	CLK to VSB200 fall Hold time	0.904
163	Tvbcs₋rise	TCLK to VSB200 rise	0.195
164	Tvbcs_fall	Setup time TCLK to VSB200 fall	0.195
		Setup time	
165	Tvbch_rise	TCLK to VSB200 rise Hold time	0.904
166	Tvbch₋fall	TCLK to VSB200 fall	0.904
167	Tvbcs_rise	Hold time CLK to VSB300 rise	0.195
107	T VDCS_FISE	Setup time	0.195
168	Tvbcs_fall	CLK to VSB300 fall Setup time	0.195
169	Tvbch_rise	CLK to VSB300 rise	0.904
170	Tvbch_fall	Hold time CLK to VSB300 fall	0.904
170	I VDCII_Iaii	Hold time	0.904
171	Tvbcs_rise	TCLK to VSB300 rise Setup time	0.195
172	Tvbcs_fall	TCLK to VSB300 fall	0.195
		Setup time	
173	Tvbch₋rise	TCLK to VSB300 rise Hold time	0.904
174	Tvbch_fall	TCLK to VSB300 fall	0.904
175	Tvbcs_rise	Hold time CLK to VSB400 rise	0.195
173	T VDCS_FISE	Setup time	0.193
176	Tvbcs_fall	CLK to VSB400 fall Setup time	0.195
177	Tvbch₋rise	CLK to VSB400 rise Hold time	0.904
178	Tvbch_fall	CLK to VSB400 fall	0.904
179	Tvbcs_rise	Hold time TCLK to VSB400 rise	0.195
		Setup time	
180	Tvbcs_fall	TCLK to VSB400 fall Setup time	0.195
181	Tvbch_rise	TCLK to VSB400 rise Hold time	0.904
182	Tvbch_fall	TCLK to VSB400 fall	0.904
		Hold time	

Table 9: AC Timing Parameters



st This table shows values only for the nominal slews and output loads.

Leakage and Power

#	Parameter	Description	TT_1p00v_25c	FF_1p10v_n40c	FF_1p10v_n55c
1	sl_leak(uW)	Leakage Power::slumber	1697.	3633.	2633.
2	sz_leak(uW)	Leakage Power::snooze	1889.	3830.	2715.
3	hn_leak(uW)	Leakage Power::hibernate	1614.	3395.	2397.
4	sd_leak(uW)	Leakage Power::shutdown	1583.	3297.	2307.
5	static_leak(uW)	Leakage Power::standby	2002.	4154.	3015.
6	Power_WE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.09695	0.08931	0.08931
7	Power_WE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.09776	0.08535	0.08535
8	Power_TWE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.09695	0.08931	0.08931
9	Power_TWE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.09776	0.08535	0.08535
10	Power_A_r::chip_dis(uW/MHZ)	Pin Power Rise	0.09695	0.08931	0.08931
11	Power_A_f::chip_dis(uW/MHZ)	Pin Power Fall	0.09695	0.08931	0.08931
12	Power_TA_r::chip_dis(uW/MHZ)	Pin Power Rise	0.09695	0.08931	0.08931
13	Power_TA_f::chip_dis(uW/MHZ)	Pin Power Fall	0.09695	0.08931	0.08931
14	Power_WE_r::chip_en(uW/MHZ)	Pin Power Rise	1.619	1.720	1.720
15	Power_WE_f::chip_en(uW/MHZ)	Pin Power Fall	1.654	1.227	1.227
16	Power_TWE_r::chip_en(uW/MHZ)	Pin Power Rise	1.619	1.720	1.720
17	Power_TWE_f::chip_en(uW/MHZ)	Pin Power Fall	1.654	1.227	1.227
18	Power_A_r::chip_en(uW/MHZ)	Pin Power Rise	0.2742	0.2280	0.2280
19	Power_A_f::chip_en(uW/MHZ)	Pin Power Fall	0.7758	0.1439	0.1439
20	Power_TA_r::chip_en(uW/MHZ)	Pin Power Rise	0.2742	0.2280	0.2280
21	Power_TA_f::chip_en(uW/MHZ)	Pin Power Fall	0.7758	0.1439	0.1439
22	Pread(uW/MHZ)	Read Power Rise	3.846	4.918	4.918
23	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
24	Pwrite(uW/MHZ)	Write Power Rise	5.868	6.017	6.017
25	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
26	Power_CLK_r(uW/MHZ)	Pin Power Rise	1.546	1.139	1.139
27	$Power_CLK_f(uW/MHZ)$	Pin Power Fall	1.471	1.213	1.213
28	Pread(uW/MHZ)	Read Power Rise	3.846	4.918	4.918
29	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
30	Pwrite(uW/MHZ)	Write Power Rise	5.868	6.017	6.017
31	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
32	Power_TCLK_r(uW/MHZ)	Pin Power Rise	1.546	1.139	1.139
33	Power_TCLK_f(uW/MHZ)	Pin Power Fall	1.471	1.213	1.213
34	Power_SZ_r(uW/MHZ)	Pin Power Rise	0.2742	0.2280	0.2280
35	Power_SZ_f(uW/MHZ)	Pin Power Fall	0.7758	0.1439	0.1439
36	Power_SL_r(uW/MHZ)	Pin Power Rise	0.2742	0.2280	0.2280
37	Power_SL_f(uW/MHZ)	Pin Power Fall	0.7758	0.1439	0.1439
38	Power_HN_r(uW/MHZ)	Pin Power Rise	0.2742	0.2280	0.2280
39	Power_HN_f(uW/MHZ)	Pin Power Fall	0.7758	0.1439	0.1439
40	Power_SD_r(uW/MHZ)	Pin Power Rise	0.2742	0.2280	0.2280
41	Power_SD_f(uW/MHZ)	Pin Power Fall	0.7758	0.1439	0.1439
42	Power_VSB100_r(uW/MHZ)	Pin Power Rise	0.2742	0.2280	0.2280
43	Power_VSB100_f(uW/MHZ)	Pin Power Fall	0.7758	0.1439	0.1439
44	Power_VSB200_r(uW/MHZ)	Pin Power Rise	0.2742	0.2280	0.2280
45	Power_VSB200_f(uW/MHZ)	Pin Power Fall	0.7758	0.1439	0.1439
46	Power_VSB300_r(uW/MHZ)	Pin Power Rise Pin Power Fall	0.2742	0.2280	0.2280
	Power_VSB300_f(uW/MHZ)		0.7758	0.1439	0.1439
48 49	Power_VSB400_r(uW/MHZ)	Pin Power Rise	0.2742	0.2280	0.2280
49	Power_VSB400_f(uW/MHZ)	Pin Power Fall	0.7758	0.1439	0.1439

Table 10: Leakage & Dynamic Power

- * Read/Write power is due to the rising edge of the clock only.
- * Read/Write power is for the alternate active cycles
- * Read/Write power is measured with 50% data and address bus toggling.
- * Address/Data power is for each individual bit of the bus



Table 11: Leakage & Dynamic Power

#	Parameter	Description	FF_1p10v_125c	SS_0p90v_n40c	SS_0p90v_n55c
1	sl_leak(uW)	Leakage Power::slumber	3.786e+04	212.7	226.6
2	sz_leak(uW)	Leakage Power::snooze	4.153e+04	164.4	148.9
3	hn_leak(uW)	Leakage Power::hibernate	3.735e+04	184.9	197.9
4	sd_leak(uW)	Leakage Power::shutdown	3.718e+04	174.0	188.7
5	static_leak(uW)	Leakage Power::standby	4.302e+04	194.2	178.9
6	Power_WE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.08931	0.006689	0.006689
7	Power_WE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.08535	0.007980	0.007980
8	Power_TWE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.08931	0.006689	0.006689
9	Power_TWE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.08535	0.007980	0.007980
10	Power_A_r::chip_dis(uW/MHZ)	Pin Power Rise	0.08931	0.006689	0.006689
11	Power_A_f::chip_dis(uW/MHZ)	Pin Power Fall	0.08931	0.006689	0.006689
12	Power_TA_r::chip_dis(uW/MHZ)	Pin Power Rise	0.08931	0.006689	0.006689
13	Power_TA_f::chip_dis(uW/MHZ)	Pin Power Fall	0.08931	0.006689	0.006689
14	Power_WE_r::chip_en(uW/MHZ)	Pin Power Rise	1.720	0.2654	0.2654
15	Power_WE_f::chip_en(uW/MHZ)	Pin Power Fall	1.227	0.2669	0.2669
16	Power_TWE_r::chip_en(uW/MHZ)	Pin Power Rise	1.720	0.2654	0.2654
17	Power_TWE_f::chip_en(uW/MHZ)	Pin Power Fall	1.227	0.2669	0.2669
18	Power_A_r::chip_en(uW/MHZ)	Pin Power Rise	0.2280	0.05190	0.05190
19	Power_A_f::chip_en(uW/MHZ)	Pin Power Fall	0.1439	0.4384	0.4384
20	Power_TA_r::chip_en(uW/MHZ)	Pin Power Rise	0.2280	0.05190	0.05190
21	Power_TA_f::chip_en(uW/MHZ)	Pin Power Fall	0.1439	0.4384	0.4384
22	Pread(uW/MHZ)	Read Power Rise	4.918	1.751	1.751
23	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
24	Pwrite(uW/MHZ)	Write Power Rise	6.017	2.089	2.089
25	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
26	Power_CLK_r(uW/MHZ)	Pin Power Rise	1.139	0.07222	0.07222
27	$Power_CLK_f(uW/MHZ)$	Pin Power Fall	1.213	0.08803	0.08803
28	Pread(uW/MHZ)	Read Power Rise	4.918	1.751	1.751
29	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
30	Pwrite(uW/MHZ)	Write Power Rise	6.017	2.089	2.089
31	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
32	Power_TCLK_r(uW/MHZ)	Pin Power Rise	1.139	0.07222	0.07222
33	Power_TCLK_f(uW/MHZ)	Pin Power Fall	1.213	0.08803	0.08803
34	Power_SZ_r(uW/MHZ)	Pin Power Rise	0.2280	0.05190	0.05190
35	Power_SZ_f(uW/MHZ)	Pin Power Fall	0.1439	0.4384	0.4384
36	Power_SL_r(uW/MHZ)	Pin Power Rise	0.2280	0.05190	0.05190
37	Power_SL_f(uW/MHZ)	Pin Power Fall	0.1439	0.4384	0.4384
38	Power_HN_r(uW/MHZ)	Pin Power Rise	0.2280	0.05190	0.05190
39	Power_HN_f(uW/MHZ)	Pin Power Fall	0.1439	0.4384	0.4384
40	Power_SD_r(uW/MHZ)	Pin Power Rise	0.2280	0.05190	0.05190
41	Power_SD_f(uW/MHZ)	Pin Power Fall	0.1439	0.4384	0.4384
42	Power_VSB100_r(uW/MHZ)	Pin Power Rise	0.2280	0.05190	0.05190
43	Power_VSB100_f(uW/MHZ)	Pin Power Fall	0.1439	0.4384	0.4384
44	Power_VSB200_r(uW/MHZ)	Pin Power Rise	0.2280	0.05190	0.05190
45	Power_VSB200_f(uW/MHZ)	Pin Power Fall	0.1439	0.4384	0.4384
46	Power_VSB300_r(uW/MHZ)	Pin Power Rise	0.2280	0.05190	0.05190
47	Power_VSB300_f(uW/MHZ)	Pin Power Fall	0.1439	0.4384	0.4384
48	Power_VSB400_r(uW/MHZ)	Pin Power Rise	0.2280	0.05190	0.05190
49	Power_VSB400_f(uW/MHZ)	Pin Power Fall	0.1439	0.4384	0.4384

Table 11: Leakage & Dynamic Power

- * Read/Write power is due to the rising edge of the clock only.
- * Read/Write power is for the alternate active cycles
- * Read/Write power is measured with 50% data and address bus toggling.
- * Address/Data power is for each individual bit of the bus

#	Parameter	Description	SS_0p90v_125c
1	sl_leak(uW)	Leakage Power::slumber	1862.
2	sz_leak(uW)	Leakage Power::snooze	2158.
3	hn_leak(uW)	Leakage Power::hibernate	1833.
4	sd_leak(uW)	Leakage Power::shutdown	1829.
5	static_leak(uW)	Leakage Power::standby	2200.

Table 12: Leakage & Dynamic Power



6	Power_WE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.006689
7	Power_WE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.007980
8	Power_TWE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.006689
9	Power_TWE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.007980
10	Power_A_r::chip_dis(uW/MHZ)	Pin Power Rise	0.006689
11	Power_A_f::chip_dis(uW/MHZ)	Pin Power Fall	0.006689
12	Power_TA_r::chip_dis(uW/MHZ)	Pin Power Rise	0.006689
13	Power_TA_f::chip_dis(uW/MHZ)	Pin Power Fall	0.006689
14	Power_WE_r::chip_en(uW/MHZ)	Pin Power Rise	0.2654
15	Power_WE_f::chip_en(uW/MHZ)	Pin Power Fall	0.2669
16	Power_TWE_r::chip_en(uW/MHZ)	Pin Power Rise	0.2654
17	Power_TWE_f::chip_en(uW/MHZ)	Pin Power Fall	0.2669
18	Power_A_r::chip_en(uW/MHZ)	Pin Power Rise	0.05190
19	Power_A_f::chip_en(uW/MHZ)	Pin Power Fall	0.4384
20	Power_TA_r::chip_en(uW/MHZ)	Pin Power Rise	0.05190
21	Power_TA_f::chip_en(uW/MHZ)	Pin Power Fall	0.4384
22	Pread(uW/MHZ)	Read Power Rise	1.751
23	Pread(uW/MHZ)	Read Power Fall	0.000
24	Pwrite(uW/MHZ)	Write Power Rise	2.089
25	Pwrite(uW/MHZ)	Write Power Fall	0.000
26	Power_CLK_r(uW/MHZ)	Pin Power Rise	0.07222
27	Power_CLK_f(uW/MHZ)	Pin Power Fall	0.08803
28	Pread(uW/MHZ)	Read Power Rise	1.751
29	Pread(uW/MHZ)	Read Power Fall	0.000
30	Pwrite(uW/MHZ)	Write Power Rise	2.089
31	Pwrite(uW/MHZ)	Write Power Fall	0.000
32	Power_TCLK_r(uW/MHZ)	Pin Power Rise	0.07222
33	Power_TCLK_f(uW/MHZ)	Pin Power Fall	0.08803
34	$Power_SZ_r(uW/MHZ)$	Pin Power Rise	0.05190
35	$Power_SZ_f(uW/MHZ)$	Pin Power Fall	0.4384
36	Power_SL_r(uW/MHZ)	Pin Power Rise	0.05190
37	Power_SL_f(uW/MHZ)	Pin Power Fall	0.4384
38	Power_HN_r(uW/MHZ)	Pin Power Rise	0.05190
39	Power_HN_f(uW/MHZ)	Pin Power Fall	0.4384
40	Power_SD_r(uW/MHZ)	Pin Power Rise	0.05190
41	Power_SD_f(uW/MHZ)	Pin Power Fall	0.4384
42	Power_VSB100_r(uW/MHZ)	Pin Power Rise	0.05190
43	Power_VSB100_f(uW/MHZ)	Pin Power Fall	0.4384
44	Power_VSB200_r(uW/MHZ)	Pin Power Rise	0.05190
45	Power_VSB200_f(uW/MHZ)	Pin Power Fall	0.4384
46	Power_VSB300_r(uW/MHZ)	Pin Power Rise	0.05190
47	Power_VSB300_f(uW/MHZ)	Pin Power Fall	0.4384
48	Power_VSB400_r(uW/MHZ)	Pin Power Rise	0.05190
49	Power_VSB400_f(uW/MHZ)	Pin Power Fall	0.4384

Table 12: Leakage & Dynamic Power

- * Read/Write power is due to the rising edge of the clock only.
- * Read/Write power is for the alternate active cycles
- * Read/Write power is measured with 50% data and address bus toggling.
- * Address/Data power is for each individual bit of the bus



Input Pin Capacitance

#	PIN	Description(unit:pF)	TT_1p00v_25c	FF_1p10v_n40c	FF_1p10v_n55c
1	BISTE	Pin Capacitance	0.002	0.002	0.002
2	AWT	Pin Capacitance	0.002	0.002	0.002
3	CLK	Pin Capacitance	0.008	0.007	0.007
4	TCLK	Pin Capacitance	0.008	0.007	0.007
5	CE	Pin Capacitance	0.002	0.002	0.002
6	TCE	Pin Capacitance	0.002	0.002	0.002
7	WE	Pin Capacitance	0.002	0.002	0.002
8	TWE	Pin Capacitance	0.002	0.002	0.002
9	BWM	Pin Capacitance	0.002	0.002	0.002
10	TBWM	Pin Capacitance	0.002	0.002	0.002
11	Α	Pin Capacitance	0.002	0.002	0.002
12	TA	Pin Capacitance	0.002	0.002	0.002
13	D	Pin Capacitance	0.002	0.002	0.002
14	TD	Pin Capacitance	0.002	0.002	0.002
15	RM	Pin Capacitance	0.002	0.002	0.002
16	WM	Pin Capacitance	0.002	0.002	0.002
17	RA	Pin Capacitance	0.002	0.002	0.002
18	LVTEST	Pin Capacitance	0.002	0.002	0.002
19	SZ	Pin Capacitance	0.005	0.005	0.005
20	SL	Pin Capacitance	0.005	0.005	0.005
21	BADIO	Pin Capacitance	_	_	_
22	HN	Pin Capacitance	0.011	0.011	0.011
23	SD	Pin Capacitance	0.006	0.006	0.006
24	VSB100	Pin Capacitance	0.002	0.002	0.002
25	VSB200	Pin Capacitance	0.002	0.002	0.002
26	VSB300	Pin Capacitance	0.002	0.002	0.002
27	VSB400	Pin Capacitance	0.002	0.002	0.002
28	VDD	Pin Capacitance	-	_	_

Table 13: Capacitance

#	PIN	Description(unit:pF)	FF_1p10v_125c	SS_0p90v_n40c	SS_0p90v_n55c
1	BISTE	Pin Capacitance	0.002	0.002	0.002
2	AWT	Pin Capacitance	0.002	0.002	0.002
3	CLK	Pin Capacitance	0.007	0.009	0.009
4	TCLK	Pin Capacitance	0.007	0.009	0.009
5	CE	Pin Capacitance	0.002	0.002	0.002
6	TCE	Pin Capacitance	0.002	0.002	0.002
7	WE	Pin Capacitance	0.002	0.002	0.002
8	TWE	Pin Capacitance	0.002	0.002	0.002
9	BWM	Pin Capacitance	0.002	0.002	0.002
10	TBWM	Pin Capacitance	0.002	0.002	0.002
11	Α	Pin Capacitance	0.002	0.002	0.002
12	TA	Pin Capacitance	0.002	0.002	0.002
13	D	Pin Capacitance	0.002	0.002	0.002
14	TD	Pin Capacitance	0.002	0.002	0.002
15	RM	Pin Capacitance	0.002	0.002	0.002
16	WM	Pin Capacitance	0.002	0.002	0.002
17	RA	Pin Capacitance	0.002	0.002	0.002
18	LVTEST	Pin Capacitance	0.002	0.002	0.002
19	SZ	Pin Capacitance	0.005	0.005	0.005
20	SL	Pin Capacitance	0.005	0.005	0.005
21	BADIO	Pin Capacitance	_	_	_
22	HN	Pin Capacitance	0.011	0.011	0.011
23	SD	Pin Capacitance	0.006	0.005	0.005
24	VSB100	Pin Capacitance	0.002	0.002	0.002
25	VSB200	Pin Capacitance	0.002	0.002	0.002
26	VSB300	Pin Capacitance	0.002	0.002	0.002
27	VSB400	Pin Capacitance	0.002	0.002	0.002
28	VDD	Pin Capacitance	_	_	_

Table 14: Capacitance



#	PIN	Description(unit:pF)	SS_0p90v_125c
1	BISTE	Pin Capacitance	0.002
2	AWT	Pin Capacitance	0.002
3	CLK	Pin Capacitance	0.009
4	TCLK	Pin Capacitance	0.009
5	CE	Pin Capacitance	0.002
6	TCE	Pin Capacitance	0.002
7	WE	Pin Capacitance	0.002
8	TWE	Pin Capacitance	0.002
9	BWM	Pin Capacitance	0.002
10	TBWM	Pin Capacitance	0.002
11	Α	Pin Capacitance	0.002
12	TA	Pin Capacitance	0.002
13	D	Pin Capacitance	0.002
14	TD	Pin Capacitance	0.002
15	RM	Pin Capacitance	0.002
16	WM	Pin Capacitance	0.002
17	RA	Pin Capacitance	0.002
18	LVTEST	Pin Capacitance	0.002
19	SZ	Pin Capacitance	0.005
20	SL	Pin Capacitance	0.005
21	BADIO	Pin Capacitance	ı
22	HN	Pin Capacitance	0.011
23	SD	Pin Capacitance	0.005
24	VSB100	Pin Capacitance	0.002
25	VSB200	Pin Capacitance	0.002
26	VSB300	Pin Capacitance	0.002
27	VSB400	Pin Capacitance	0.002
28	VDD	Pin Capacitance	_

Table 15: Capacitance



Corruption Table

#	Parameter	Related Pin	CEM	CCL
1	Tcc(Violation)	CLK	YES	NO
2	Tcl(Violation)	CLK	YES	NO
3	Tch(Violation)	CLK	YES	NO
4	Tacs_rise(Violation)	Α	YES	NO
5	Tach_rise(Violation)	A	YES	NO
6	Trwcs_rise(Violation)	WE	NO	YES
7	Trwch_rise(Violation)	WE	NO	YES
8	Tbyms_rise(Violation)	BWM	NO	YES
9	Tbymh_rise(Violation)	BWM	NO	YES
10	Tces_rise(Violation)	CE	YES	NO
11	Tceh_rise(Violation)	CE	YES	NO
12	Tdcs_rise(Violation)	D	NO	YES
13	Tdch_rise(Violation)	D	NO	YES
14	Tsnzrc(Violation)	SZ	YES	NO
15	Tsnzrm(Violation)	SZ	YES	NO
16	Tslprc(Violation)	SL	YES	NO
17	Tslprm(Violation)	SL	YES	NO
18	Thbrntrc(Violation)	HN	YES	NO
19	Thbrntprm(Violation)	HN	YES	NO
20	Tdslprc(Violation)	SD	YES	NO
21	Tdslprm(Violation)	SD	YES	NO
	T 11 40 10 1 1	C 14/ 1:		

Table 16: Violation in case of Write Mode

* CEM : Corrupt Entire Memory

* CCL : Corrupt Current Location (Selected Word)

#	Parameter	Related Pin	CEM	CCL
1	Tcc(Violation)	CLK	YES	NO
2	Tcl(Violation)	CLK	YES	NO
3	Tch(Violation)	CLK	YES	NO
4	Tacs_rise(Violation)	A	YES	NO
5	Tach_rise(Violation)	A	YES	NO
6	Trwcs_rise(Violation)	WE	NO	YES
7	Trwch_rise(Violation)	WE	NO	YES
8	Tces_rise(Violation)	CE	YES	NO
9	Tceh_rise(Violation)	CE	YES	NO
10	Tsnzrc(Violation)	SZ	YES	NO
11	Tsnzrm(Violation)	SZ	YES	NO
12	Tslprc(Violation)	SL	YES	NO
13	Tslprm(Violation)	SL	YES	NO
14	Thbrntrc(Violation)	HN	YES	NO
15	Thbrntprm(Violation)	HN	YES	NO
16	Tdslprc(Violation)	SD	YES	NO
17	Tdslprm(Violation)	SD	YES	NO

Table 17: Violation in case of Read Mode

* CEM : Corrupt Entire Memory

* CCL : Corrupt Current Location (Selected Word)



Timing Diagrams

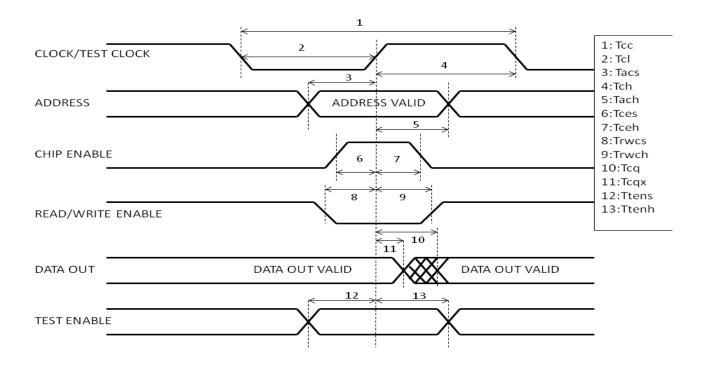


Figure 1: Read Timing



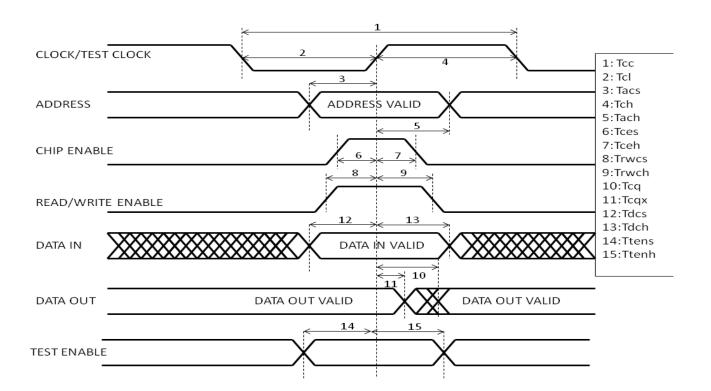
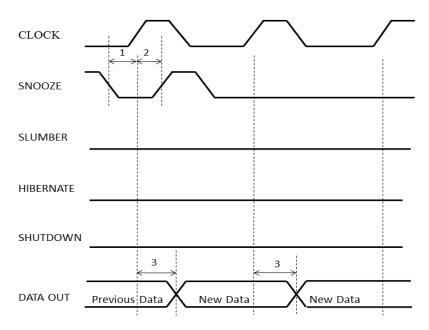


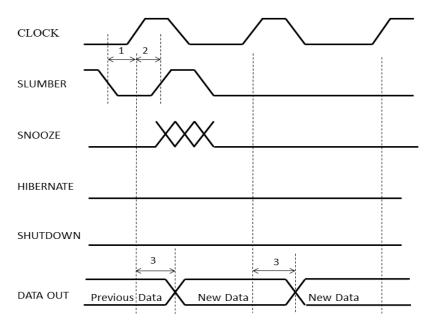
Figure 2: Write Timing



1 => Recovery Time; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

Figure 3: Snooze Timing





1 => Recovery Time; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

CLOCK

HIBERNATE

SHUTDOWN

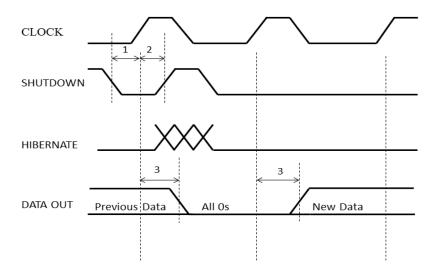
DATA OUT Previous Data All 0s New Data

Figure 4: Slumber Timing

1 => Recovery Time; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

Figure 5: Hibernate Timing





1 => Recovery Time; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

Figure 6: Shutdown Timing



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