GF-45RFSOI Single-Port Static RAM

(spram_4096x16m16b1pm2re1)

Datasheet

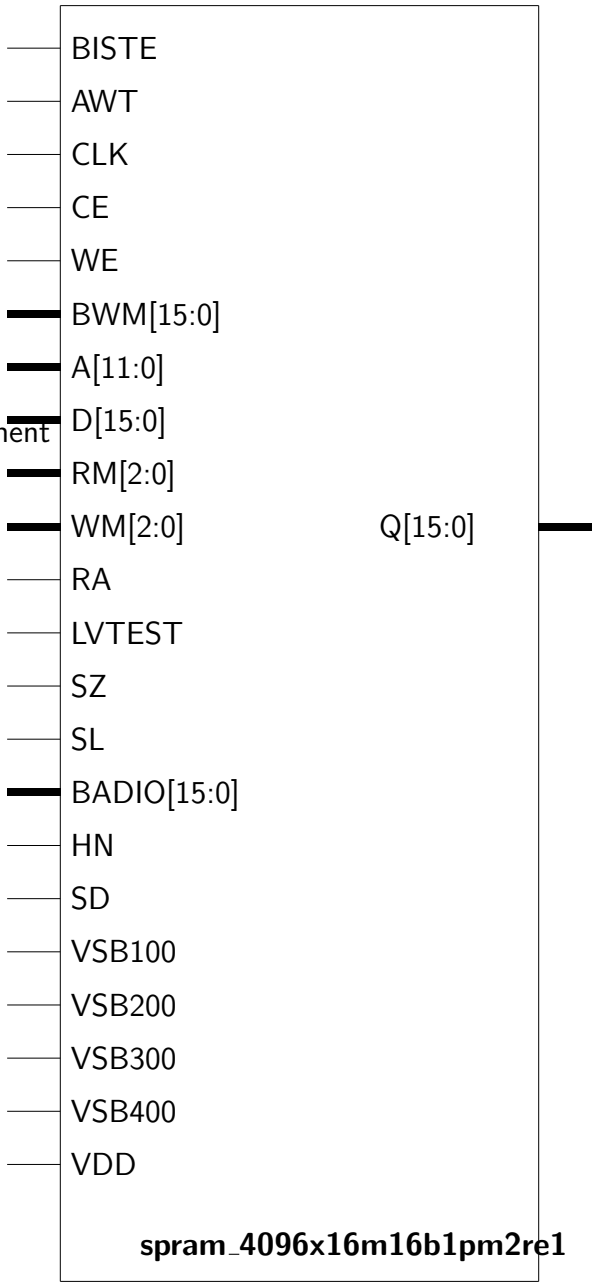
Version: 1.71

Introduction

The SpectralRAM IP Random Access Memory (RAM) core is a fully verified memory unit that uses state of the art power saving techniques to reduce standby power in deep sub-micron process nodes. The width, depth, memory type, and other optional features of the RAM core can be customized based on specifications.

Features

- RAM depth of 32 to 16K words
- RAM width of 8 to 144 bits
- Column Mux options 4, 8,16
- Banking options 1,2,4,8
- Bit Write capability
- Low Power Standby Mode
- Write Assist, Low Voltage Mode for Yield Enhancement
- Robust Design for 5 sigma bitcell variation



Software	MemoryTime 2.2.1
Compiler Name	Single-Port
Platform	Linux-CentOS
Date of Generation	06/14/19
Technology	GF-45RFSOI
Description	High Density Low Power RAM

Table 1: **Compiler Information**

Number of Words	4096
Number of Bits	16
Column-Mux	16
Width(um)	138.414
Height(um)	339.788
Area(square um)	47031.4
Frequency(MHz)	874.81
Top Metal Layer	Metal 4

Table 2: **Instance Information**

Pin Information

Signal Name	In/Out	Description
BISTE	input	Test Enable: When High Memory operates in test mode else if low Memory operates in Normal Mode
AWT	input	
CLK	clock	Clock: All normal read/write operations are synchronous to the rising edge of the clock
TCLK	clock	Test Clock: All test read/write operations are synchronous to the rising edge of the clock
CE	input	Control signal used to select the macro. When the macro is deselected, primary inputs like address data are inhibited from accessing the memory array. If the power savings mode is selected, this pin will have no impact on the leakage savings operations
TCE	input	Test Control signal used to select the macro. When the macro is deselected, primary inputs like address data are inhibited from accessing the memory array. If the power savings mode is selected, this pin will have no impact on the leakage savings operations
WE	input	Read/Write Enable(Active High): Control signal used to select between read and write operation
TWE	input	Test-Read/Write Enable(Active High): Control signal used to select between read and write operation
BWM[15:0]	input	Write Mask(Active High): Bitwise control signal to mask selected write locations of a word during the write operation. The selected word would retain the previous data for all the masked bits. The output latches for the masked bits would also retain the data read from the prior read operation. This bus is a don't care during the read operation
TBWM[15:0]	input	Test Write Mask(Active High): Bitwise control signal to mask selected write locations of a word during the write operation. The selected word would retain the previous data for all the masked bits. The output latches for the masked bits would also retain the data read from the prior read operation. This bus is a don't care during the read operation
A[11:0]	input	Address: Address bus Specifies read and write Locations
TA[11:0]	input	Test Address: Address bus Specifies read and write Locations
D[15:0]	input	Data In: Data bus specifies the contents that get written into the Memory for an address specified
TD[15:0]	input	Test Data In: Data bus specifies the contents that get written into the Memory for an address specified
Q[15:0]	output	Data out: Data bus used to read contents of the Memory
RM[2:0]	input	Read Margin: this pin is used to control internal timer
WM[2:0]	input	Write Margin: this pin is used to control internal write boost

Table 3: **Pin Information**

RA	input	Read Assist: Please refer to the Compiler User Guide for the details
LVTEST	input	Low Voltage Mode for Yield: WL follows Clock High. Please refer to the Compiler User Guide for the details
SZ	input	SNOOZE: Array Source Bias (Data Retained)
SL	input	SLUMBER: Periphery Shutdown (Data Retained)
BADIO[15:0]	input	BADIO: Repair Shifting Signal
HN	input	HIBERNATE: Array Source Bias + Periphery Shutdown (Data Retained)
SD	input	SHUTDOWN: Array + Periphery Shutdown (Data Lost)
VSB100	input	Source Bias (Lowest Level). Please refer to the Compiler User Guide for the details
VSB200	input	Source Bias (Med-Low Level). Please refer to the Compiler User Guide for the details
VSB300	input	Source Bias (Med-High Level). Please refer to the Compiler User Guide for the details
VSB400	input	Source Bias (Highest Level). Please refer to the Compiler User Guide for the details
VDD	input	Array Power Supply

Table 3: **Pin Information**

Truth Table

.	WRITE	READ	STANDBY	SNOOZE	SLUMBER	HIBERNATE	SHUTDOWN	TEST
A/TA [11:0]	ADDRESS	ADDRESS	X	X	X	X	X	TADDRESS
D/TD[15:0]	DATA	X	X	X	X	X	X	TDATA
BWM/TBWM[15:0]	MASK	X	X	X	X	X	X	TMASK
CLK/TCLK	^CLOCK	^CLOCK	X	X	X	X	X	^TCLOCK
WE/TWE	1	0	X	X	X	X	X	TREAD/TWRIT
CE/TCE	1	1	0	X	X	X	X	TCHIPENABLE
SZ	0	0	0	1	X	X	X	0
SL	0	0	0	0	1	X	X	0
HN	0	0	0	0	0	1	X	0
SD	0	0	0	0	0	0	1	0
Q[15:0]	DATA	DATA	Prev DATA	Prev DATA	Prev DATA	Prev DATA	0	TDATA
BISTE	0	0	X	X	X	X	X	1
MemoryCore	Retained	Retained	Retained	Retained	Retained	Retained	Not Retained	Retained

Table 4: **Logic Truth Table**

* ^CLOCK/^TCLOCK: Positive Edge of Clock
* MemoryCore : State of the stored Memory Contents
* Each subsequent power down state reduces leakage more than the previous state

  SNOOZE Leakage > SLUMBER Leakage > HIBERNATE Leakage > SHUTDOWN Leakage
* Each subsequent power down state consumes higher wake-up power than the previous state

  SNOOZE Power < SLUMBER Power < HIBERNATE Power < SHUTDOWN Power
* Each subsequent power down state has a higher recovery time than the previous state

  SNOOZE Rec Time < SLUMBER Rec Time < HIBERNATE Rec Time < SHUTDOWN Rec Time

Look Up Table

Index	1	2	3	4	5	6	7
Input Slope(ns)	0.0021	0.0142	0.08	0.1359	0.2311	0.3467	0.52
Input Clock Slope(ns)	0.0021	0.0142	0.08	0.1359	0.2311	0.3467	0.52
Output Load(pF)	0.004	0.009	0.018	0.035	0.075	0.15	0.3

Table 5: **Input slope & Output Load**

Table shows the Input slews and Output loads that were used to characterize the memory

Operating Conditions

#	PVT Corner	Process	Voltage(V)	Temperature(C)
1	**TT_1p00v_25c**	TT	1	25
2	**FF_1p10v_n40c**	FF	1.1	-40
3	**FF_1p10v_n55c**	FF	1.1	-55
4	**FF_1p10v_125c**	FF	1.1	125
5	**SS_0p90v_n40c**	SS	0.9	-40
6	**SS_0p90v_n55c**	SS	0.9	-55
7	**SS_0p90v_125c**	SS	0.9	125

Table 6: **PVT Corners**

Table Depicts different process,voltage and temperature corners that were characterized for this memory.

AC Timing Parameters

#	Parameter(ns)	Description	TT_1p00v_25c	FF_1p10v_n40c	FF_1p10v_n55c
1	**Ttens_rise**	CLK to BISTE rise Setup time	0.163	0.123	0.123
2	**Ttens_fall**	CLK to BISTE fall Setup time	0.163	0.123	0.123
3	**Ttenh_rise**	CLK to BISTE rise Hold time	0.723	0.415	0.415
4	**Ttens_fall**	CLK to BISTE fall Hold time	0.723	0.415	0.415
5	**Ttens_rise**	TCLK to BISTE rise Setup time	0.163	0.123	0.123
6	**Ttens_fall**	TCLK to BISTE fall Setup time	0.163	0.123	0.123
7	**Ttenh_rise**	TCLK to BISTE rise Hold time	0.723	0.415	0.415
8	**Ttens_fall**	TCLK to BISTE fall Hold time	0.723	0.415	0.415
9	**Tbms**	CLK to AWT rise Setup time	0.081	0.062	0.061
10	**Tbmx**	CLK to AWT fall Setup time	0.081	0.062	0.061
11	**Tbms**	CLK to AWT rise Hold time	0.022	0.020	0.020
12	**Tbmx**	CLK to AWT fall Hold time	0.022	0.020	0.020
13	**Tbms**	TCLK to AWT rise Setup time	0.081	0.062	0.061
14	**Tbmx**	TCLK to AWT fall Setup time	0.081	0.062	0.061
15	**Tbms**	TCLK to AWT rise Hold time	0.022	0.020	0.020
16	**Tbmx**	TCLK to AWT fall Hold time	0.022	0.020	0.020
17	**Tcc**	CLK Cycle Time	0.723	0.415	0.415
18	**Tch**	CLK Pulse Width High	0.160	0.153	0.152
19	**Tcl**	CLK Pulse Width Low	0.158	0.108	0.107
20	**Tcc**	TCLK Cycle Time	0.723	0.415	0.415
21	**Tch**	TCLK Pulse Width High	0.160	0.153	0.152
22	**Tcl**	TCLK Pulse Width Low	0.158	0.108	0.107
23	**Tces_rise**	CLK to CE rise Setup time	0.158	0.108	0.107
24	**Tces_fall**	CLK to CE fall Setup time	0.158	0.108	0.107
25	**Tceh_rise**	CLK to CE rise Hold time	0.015	0.013	0.013
26	**Tceh_fall**	CLK to CE fall Hold time	0.015	0.013	0.013
27	**Tces_rise**	TCLK to TCE rise Setup time	0.158	0.108	0.107
28	**Tces_fall**	TCLK to TCE fall Setup time	0.158	0.108	0.107
29	**Tceh_rise**	TCLK to TCE rise Hold time	0.015	0.013	0.013
30	**Tceh_fall**	TCLK to TCE fall Hold time	0.015	0.013	0.013
31	**Trwcs_rise**	CLK to WE rise Setup time	0.102	0.066	0.065
32	**Trwcs_fall**	CLK to WE fall Setup time	0.102	0.066	0.065
33	**Trwch_rise**	CLK to WE rise Hold time	0.019	0.021	0.021
34	**Trwch_fall**	CLK to WE fall Hold time	0.019	0.021	0.021
35	**Trwcs_rise**	TCLK to TWE rise Setup time	0.102	0.066	0.065

Table 7: **AC Timing Parameters**

36	**Trwcs_fall**	TCLK to TWE fall Setup time	0.102	0.066	0.065
37	**Trwch_rise**	TCLK to TWE rise Hold time	0.019	0.021	0.021
38	**Trwch_fall**	TCLK to TWE fall Hold time	0.019	0.021	0.021
39	**Tbyms_rise**	CLK to BWM rise Setup time	0.020	0.011	0.011
40	**Tbyms_fall**	CLK to BWM fall Setup time	0.020	0.011	0.011
41	**Tbymh_rise**	CLK to BWM rise Hold time	0.047	0.042	0.041
42	**Tbymh_fall**	CLK to BWM fall Hold time	0.047	0.042	0.041
43	**Tbyms_rise**	TCLK to TBWM rise Setup time	0.020	0.011	0.011
44	**Tbyms_fall**	TCLK to TBWM fall Setup time	0.020	0.011	0.011
45	**Tbymh_rise**	TCLK to TBWM rise Hold time	0.047	0.042	0.041
46	**Tbymh_fall**	TCLK to TBWM fall Hold time	0.047	0.042	0.041
47	**Tacs_rise**	CLK to A rise Setup time	0.081	0.062	0.061
48	**Tacs_fall**	CLK to A fall Setup time	0.081	0.062	0.061
49	**Tach_rise**	CLK to A rise Hold time	0.022	0.020	0.020
50	**Tach_fall**	CLK to A fall Hold time	0.022	0.020	0.020
51	**Tacs_rise**	TCLK to TA rise Setup time	0.081	0.062	0.061
52	**Tacs_fall**	TCLK to TA fall Setup time	0.081	0.062	0.061
53	**Tach_rise**	TCLK to TA rise Hold time	0.022	0.020	0.020
54	**Tach_fall**	TCLK to TA fall Hold time	0.022	0.020	0.020
55	**Tdcs_rise**	CLK to D rise Setup time	0.001	0.001	0.001
56	**Tdcs_fall**	CLK to D fall Setup time	0.001	0.001	0.001
57	**Tdch_rise**	CLK to D rise Hold time	0.047	0.042	0.041
58	**Tdch_fall**	CLK to D fall Hold time	0.047	0.042	0.041
59	**Tdcs_rise**	TCLK to TD rise Setup time	0.001	0.001	0.001
60	**Tdcs_fall**	TCLK to TD fall Setup time	0.001	0.001	0.001
61	**Tdch_rise**	TCLK to TD rise Hold time	0.047	0.042	0.041
62	**Tdch_fall**	TCLK to TD fall Hold time	0.047	0.042	0.041
63	**Tcqh**	CLK to Q rise Delay	0.654	0.374	0.371
64	**Tcql**	CLK to Q fall Delay	0.684	0.392	0.392
65	**Tcqxh**	CLK to Q rise Retain	0.548	0.313	0.311
66	**Tcqxl**	CLK to Q fall Retain	0.548	0.313	0.311
67	**Tcqh**	D to Q rise Delay	0.654	0.374	0.371
68	**Tcql**	D to Q fall Delay	0.684	0.392	0.392
69	**Tcqxh**	D to Q rise Retain	0.548	0.313	0.311
70	**Tcqxl**	D to Q fall Retain	0.548	0.313	0.311
71	**Tcqh**	TD to Q rise Delay	0.654	0.374	0.371
72	**Tcql**	TD to Q fall Delay	0.684	0.392	0.392
73	**Tcqxh**	TD to Q rise Retain	0.548	0.313	0.311
74	**Tcqxl**	TD to Q fall Retain	0.548	0.313	0.311
75	**Tcqh**	TCLK to Q rise Delay	0.654	0.374	0.371
76	**Tcql**	TCLK to Q fall Delay	0.684	0.392	0.392
77	**Tcqxh**	TCLK to Q rise Retain	0.548	0.313	0.311
78	**Tcqxl**	TCLK to Q fall Retain	0.548	0.313	0.311
79	**Trmcs_rise**	CLK to RM rise Setup time	0.163	0.123	0.123
80	**Trmcs_fall**	CLK to RM fall Setup time	0.163	0.123	0.123

Table 7: **AC Timing Parameters**

81	**Trmch_rise**	CLK to RM rise Hold time	0.723	0.415	0.415
82	**Trmch_fall**	CLK to RM fall Hold time	0.723	0.415	0.415
83	**Trmcs_rise**	TCLK to RM rise Setup time	0.163	0.123	0.123
84	**Trmcs_fall**	TCLK to RM fall Setup time	0.163	0.123	0.123
85	**Trmch_rise**	TCLK to RM rise Hold time	0.723	0.415	0.415
86	**Trmch_fall**	TCLK to RM fall Hold time	0.723	0.415	0.415
87	**Twmcs_rise**	CLK to WM rise Setup time	0.163	0.123	0.123
88	**Twmcs_fall**	CLK to WM fall Setup time	0.163	0.123	0.123
89	**Twmch_rise**	CLK to WM rise Hold time	0.723	0.415	0.415
90	**Twmch_fall**	CLK to WM fall Hold time	0.723	0.415	0.415
91	**Twmcs_rise**	TCLK to WM rise Setup time	0.163	0.123	0.123
92	**Twmcs_fall**	TCLK to WM fall Setup time	0.163	0.123	0.123
93	**Twmch_rise**	TCLK to WM rise Hold time	0.723	0.415	0.415
94	**Twmch_fall**	TCLK to WM fall Hold time	0.723	0.415	0.415
95	**Tracs_rise**	CLK to RA rise Setup time	0.163	0.123	0.123
96	**Tracs_fall**	CLK to RA fall Setup time	0.163	0.123	0.123
97	**Trach_rise**	CLK to RA rise Hold time	0.723	0.415	0.415
98	**Trach_fall**	CLK to RA fall Hold time	0.723	0.415	0.415
99	**Tracs_rise**	TCLK to RA rise Setup time	0.163	0.123	0.123
100	**Tracs_fall**	TCLK to RA fall Setup time	0.163	0.123	0.123
101	**Trach_rise**	TCLK to RA rise Hold time	0.723	0.415	0.415
102	**Trach_fall**	TCLK to RA fall Hold time	0.723	0.415	0.415
103	**Tlvcs_rise**	CLK to LVTEST rise Setup time	0.163	0.123	0.123
104	**Tlvcs_fall**	CLK to LVTEST fall Setup time	0.163	0.123	0.123
105	**Tlvch_rise**	CLK to LVTEST rise Hold time	0.723	0.415	0.415
106	**Tlvch_fall**	CLK to LVTEST fall Hold time	0.723	0.415	0.415
107	**Tlvcs_rise**	TCLK to LVTEST rise Setup time	0.163	0.123	0.123
108	**Tlvcs_fall**	TCLK to LVTEST fall Setup time	0.163	0.123	0.123
109	**Tlvch_rise**	TCLK to LVTEST rise Hold time	0.723	0.415	0.415
110	**Tlvch_fall**	TCLK to LVTEST fall Hold time	0.723	0.415	0.415
111	**Tszrch**	CLK to SZ rise Setup time	0.325	0.247	0.245
112	**Tszrcl**	CLK to SZ fall Setup time	0.325	0.247	0.245
113	**Tszrmh**	CLK to SZ rise Hold time	0.723	0.415	0.415
114	**Tszrml**	CLK to SZ fall Hold time	9.309	7.450	7.430
115	**Tszrch**	TCLK to SZ rise Setup time	0.325	0.247	0.245

Table 7: **AC Timing Parameters**

116	**Tszrcl**	TCLK to SZ fall Setup time	0.325	0.247	0.245
117	**Tszrmh**	TCLK to SZ rise Hold time	0.723	0.415	0.415
118	**Tszrml**	TCLK to SZ fall Hold time	9.309	7.450	7.430
119	**Tslrch**	CLK to SL rise Setup time	0.325	0.247	0.245
120	**Tslrcl**	CLK to SL fall Setup time	0.325	0.247	0.245
121	**Tslrmh**	CLK to SL rise Hold time	0.723	0.415	0.415
122	**Tslrml**	CLK to SL fall Hold time	9.309	7.450	7.430
123	**Tslrch**	TCLK to SL rise Setup time	0.325	0.247	0.245
124	**Tslrcl**	TCLK to SL fall Setup time	0.325	0.247	0.245
125	**Tslrmh**	TCLK to SL rise Hold time	0.723	0.415	0.415
126	**Tslrml**	TCLK to SL fall Hold time	9.309	7.450	7.430
127	**Tbiosh**	CLK to BADIO rise Setup time	1.343	1.024	1.018
128	**Tbiosl**	CLK to BADIO fall Setup time	1.343	1.024	1.018
129	**Tbiohh**	CLK to BADIO rise Hold time	1.343	1.024	1.018
130	**Tbiohl**	CLK to BADIO fall Hold time	1.343	1.024	1.018
131	**Tbiosh**	TCLK to BADIO rise Setup time	1.343	1.024	1.018
132	**Tbiosl**	TCLK to BADIO fall Setup time	1.343	1.024	1.018
133	**Tbiohh**	TCLK to BADIO rise Hold time	1.343	1.024	1.018
134	**Tbiohl**	TCLK to BADIO fall Hold time	1.343	1.024	1.018
135	**Thnrch**	CLK to HN rise Setup time	0.325	0.247	0.245
136	**Thnrcl**	CLK to HN fall Setup time	0.325	0.247	0.245
137	**Thnrmh**	CLK to HN rise Hold time	0.723	0.415	0.415
138	**Thnrml**	CLK to HN fall Hold time	9.309	7.450	7.430
139	**Thnrch**	TCLK to HN rise Setup time	0.325	0.247	0.245
140	**Thnrcl**	TCLK to HN fall Setup time	0.325	0.247	0.245
141	**Thnrmh**	TCLK to HN rise Hold time	0.723	0.415	0.415
142	**Thnrml**	TCLK to HN fall Hold time	9.309	7.450	7.430
143	**Tsdrch**	CLK to SD rise Setup time	0.325	0.247	0.245
144	**Tsdrcl**	CLK to SD fall Setup time	0.325	0.247	0.245
145	**Tsdrmh**	CLK to SD rise Hold time	0.723	0.415	0.415
146	**Tsdrml**	CLK to SD fall Hold time	9.309	7.450	7.430
147	**Tsdrch**	TCLK to SD rise Setup time	0.325	0.247	0.245
148	**Tsdrcl**	TCLK to SD fall Setup time	0.325	0.247	0.245
149	**Tsdrmh**	TCLK to SD rise Hold time	0.723	0.415	0.415
150	**Tsdrml**	TCLK to SD fall Hold time	9.309	7.450	7.430

Table 7: **AC Timing Parameters**

151	**Tvbcs_rise**	CLK to VSB100 rise Setup time	0.163	0.123	0.123
152	**Tvbcs_fall**	CLK to VSB100 fall Setup time	0.163	0.123	0.123
153	**Tvbch_rise**	CLK to VSB100 rise Hold time	0.723	0.415	0.415
154	**Tvbch_fall**	CLK to VSB100 fall Hold time	0.723	0.415	0.415
155	**Tvbcs_rise**	TCLK to VSB100 rise Setup time	0.163	0.123	0.123
156	**Tvbcs_fall**	TCLK to VSB100 fall Setup time	0.163	0.123	0.123
157	**Tvbch_rise**	TCLK to VSB100 rise Hold time	0.723	0.415	0.415
158	**Tvbch_fall**	TCLK to VSB100 fall Hold time	0.723	0.415	0.415
159	**Tvbcs_rise**	CLK to VSB200 rise Setup time	0.163	0.123	0.123
160	**Tvbcs_fall**	CLK to VSB200 fall Setup time	0.163	0.123	0.123
161	**Tvbch_rise**	CLK to VSB200 rise Hold time	0.723	0.415	0.415
162	**Tvbch_fall**	CLK to VSB200 fall Hold time	0.723	0.415	0.415
163	**Tvbcs_rise**	TCLK to VSB200 rise Setup time	0.163	0.123	0.123
164	**Tvbcs_fall**	TCLK to VSB200 fall Setup time	0.163	0.123	0.123
165	**Tvbch_rise**	TCLK to VSB200 rise Hold time	0.723	0.415	0.415
166	**Tvbch_fall**	TCLK to VSB200 fall Hold time	0.723	0.415	0.415
167	**Tvbcs_rise**	CLK to VSB300 rise Setup time	0.163	0.123	0.123
168	**Tvbcs_fall**	CLK to VSB300 fall Setup time	0.163	0.123	0.123
169	**Tvbch_rise**	CLK to VSB300 rise Hold time	0.723	0.415	0.415
170	**Tvbch_fall**	CLK to VSB300 fall Hold time	0.723	0.415	0.415
171	**Tvbcs_rise**	TCLK to VSB300 rise Setup time	0.163	0.123	0.123
172	**Tvbcs_fall**	TCLK to VSB300 fall Setup time	0.163	0.123	0.123
173	**Tvbch_rise**	TCLK to VSB300 rise Hold time	0.723	0.415	0.415
174	**Tvbch_fall**	TCLK to VSB300 fall Hold time	0.723	0.415	0.415
175	**Tvbcs_rise**	CLK to VSB400 rise Setup time	0.163	0.123	0.123
176	**Tvbcs_fall**	CLK to VSB400 fall Setup time	0.163	0.123	0.123
177	**Tvbch_rise**	CLK to VSB400 rise Hold time	0.723	0.415	0.415
178	**Tvbch_fall**	CLK to VSB400 fall Hold time	0.723	0.415	0.415
179	**Tvbcs_rise**	TCLK to VSB400 rise Setup time	0.163	0.123	0.123
180	**Tvbcs_fall**	TCLK to VSB400 fall Setup time	0.163	0.123	0.123
181	**Tvbch_rise**	TCLK to VSB400 rise Hold time	0.723	0.415	0.415
182	**Tvbch_fall**	TCLK to VSB400 fall Hold time	0.723	0.415	0.415

Table 7: **AC Timing Parameters**

* This table shows values only for the nominal slews and output loads.

#	Parameter(ns)	Description	FF_1p10v_125c	SS_0p90v_n40c	SS_0p90v_n55c
1	**Ttens_rise**	CLK to BISTE rise Setup time	0.134	0.226	0.304
2	**Ttens_fall**	CLK to BISTE fall Setup time	0.134	0.226	0.304
3	**Ttenh_rise**	CLK to BISTE rise Hold time	0.678	1.083	1.095
4	**Ttens_fall**	CLK to BISTE fall Hold time	0.678	1.083	1.095
5	**Ttens_rise**	TCLK to BISTE rise Setup time	0.134	0.226	0.304
6	**Ttens_fall**	TCLK to BISTE fall Setup time	0.134	0.226	0.304
7	**Ttenh_rise**	TCLK to BISTE rise Hold time	0.678	1.083	1.095
8	**Ttens_fall**	TCLK to BISTE fall Hold time	0.678	1.083	1.095
9	**Tbms**	CLK to AWT rise Setup time	0.067	0.113	0.152
10	**Tbmx**	CLK to AWT fall Setup time	0.067	0.113	0.152
11	**Tbms**	CLK to AWT rise Hold time	0.024	0.026	0.026
12	**Tbmx**	CLK to AWT fall Hold time	0.024	0.026	0.026
13	**Tbms**	TCLK to AWT rise Setup time	0.067	0.113	0.152
14	**Tbmx**	TCLK to AWT fall Setup time	0.067	0.113	0.152
15	**Tbms**	TCLK to AWT rise Hold time	0.024	0.026	0.026
16	**Tbmx**	TCLK to AWT fall Hold time	0.024	0.026	0.026
17	**Tcc**	CLK Cycle Time	0.678	1.083	1.095
18	**Tch**	CLK Pulse Width High	0.155	0.179	0.177
19	**Tcl**	CLK Pulse Width Low	0.126	0.228	0.236
20	**Tcc**	TCLK Cycle Time	0.678	1.083	1.095
21	**Tch**	TCLK Pulse Width High	0.155	0.179	0.177
22	**Tcl**	TCLK Pulse Width Low	0.126	0.228	0.236
23	**Tces_rise**	CLK to CE rise Setup time	0.126	0.228	0.236
24	**Tces_fall**	CLK to CE fall Setup time	0.126	0.228	0.236
25	**Tceh_rise**	CLK to CE rise Hold time	0.020	0.021	0.017
26	**Tceh_fall**	CLK to CE fall Hold time	0.020	0.021	0.017
27	**Tces_rise**	TCLK to TCE rise Setup time	0.126	0.228	0.236
28	**Tces_fall**	TCLK to TCE fall Setup time	0.126	0.228	0.236
29	**Tceh_rise**	TCLK to TCE rise Hold time	0.020	0.021	0.017
30	**Tceh_fall**	TCLK to TCE fall Hold time	0.020	0.021	0.017
31	**Trwcs_rise**	CLK to WE rise Setup time	0.081	0.145	0.138
32	**Trwcs_fall**	CLK to WE fall Setup time	0.081	0.145	0.138
33	**Trwch_rise**	CLK to WE rise Hold time	0.024	0.024	0.026
34	**Trwch_fall**	CLK to WE fall Hold time	0.024	0.024	0.026
35	**Trwcs_rise**	TCLK to TWE rise Setup time	0.081	0.145	0.138
36	**Trwcs_fall**	TCLK to TWE fall Setup time	0.081	0.145	0.138
37	**Trwch_rise**	TCLK to TWE rise Hold time	0.024	0.024	0.026

Table 8: **AC Timing Parameters**

38	**Trwch_fall**	TCLK to TWE fall Hold time	0.024	0.024	0.026
39	**Tbyms_rise**	CLK to BWM rise Setup time	0.010	0.027	0.030
40	**Tbyms_fall**	CLK to BWM fall Setup time	0.010	0.027	0.030
41	**Tbymh_rise**	CLK to BWM rise Hold time	0.048	0.065	0.055
42	**Tbymh_fall**	CLK to BWM fall Hold time	0.048	0.065	0.055
43	**Tbyms_rise**	TCLK to TBWM rise Setup time	0.010	0.027	0.030
44	**Tbyms_fall**	TCLK to TBWM fall Setup time	0.010	0.027	0.030
45	**Tbymh_rise**	TCLK to TBWM rise Hold time	0.048	0.065	0.055
46	**Tbymh_fall**	TCLK to TBWM fall Hold time	0.048	0.065	0.055
47	**Tacs_rise**	CLK to A rise Setup time	0.067	0.113	0.152
48	**Tacs_fall**	CLK to A fall Setup time	0.067	0.113	0.152
49	**Tach_rise**	CLK to A rise Hold time	0.024	0.026	0.026
50	**Tach_fall**	CLK to A fall Hold time	0.024	0.026	0.026
51	**Tacs_rise**	TCLK to TA rise Setup time	0.067	0.113	0.152
52	**Tacs_fall**	TCLK to TA fall Setup time	0.067	0.113	0.152
53	**Tach_rise**	TCLK to TA rise Hold time	0.024	0.026	0.026
54	**Tach_fall**	TCLK to TA fall Hold time	0.024	0.026	0.026
55	**Tdcs_rise**	CLK to D rise Setup time	0.001	0.001	0.006
56	**Tdcs_fall**	CLK to D fall Setup time	0.001	0.001	0.006
57	**Tdch_rise**	CLK to D rise Hold time	0.048	0.065	0.055
58	**Tdch_fall**	CLK to D fall Hold time	0.048	0.065	0.055
59	**Tdcs_rise**	TCLK to TD rise Setup time	0.001	0.001	0.006
60	**Tdcs_fall**	TCLK to TD fall Setup time	0.001	0.001	0.006
61	**Tdch_rise**	TCLK to TD rise Hold time	0.048	0.065	0.055
62	**Tdch_fall**	TCLK to TD fall Hold time	0.048	0.065	0.055
63	**Tcqh**	CLK to Q rise Delay	0.527	0.966	0.974
64	**Tcql**	CLK to Q fall Delay	0.549	1.024	1.035
65	**Tcqxh**	CLK to Q rise Retain	0.442	0.810	0.816
66	**Tcqxl**	CLK to Q fall Retain	0.442	0.810	0.816
67	**Tcqh**	D to Q rise Delay	0.527	0.966	0.974
68	**Tcql**	D to Q fall Delay	0.549	1.024	1.035
69	**Tcqxh**	D to Q rise Retain	0.442	0.810	0.816
70	**Tcqxl**	D to Q fall Retain	0.442	0.810	0.816
71	**Tcqh**	TD to Q rise Delay	0.527	0.966	0.974
72	**Tcql**	TD to Q fall Delay	0.549	1.024	1.035
73	**Tcqxh**	TD to Q rise Retain	0.442	0.810	0.816
74	**Tcqxl**	TD to Q fall Retain	0.442	0.810	0.816
75	**Tcqh**	TCLK to Q rise Delay	0.527	0.966	0.974
76	**Tcql**	TCLK to Q fall Delay	0.549	1.024	1.035
77	**Tcqxh**	TCLK to Q rise Retain	0.442	0.810	0.816
78	**Tcqxl**	TCLK to Q fall Retain	0.442	0.810	0.816
79	**Trmcs_rise**	CLK to RM rise Setup time	0.134	0.226	0.304
80	**Trmcs_fall**	CLK to RM fall Setup time	0.134	0.226	0.304
81	**Trmch_rise**	CLK to RM rise Hold time	0.678	1.083	1.095
82	**Trmch_fall**	CLK to RM fall Hold time	0.678	1.083	1.095

Table 8: **AC Timing Parameters**

83	**Trmcs_rise**	TCLK to RM rise Setup time	0.134	0.226	0.304
84	**Trmcs_fall**	TCLK to RM fall Setup time	0.134	0.226	0.304
85	**Trmch_rise**	TCLK to RM rise Hold time	0.678	1.083	1.095
86	**Trmch_fall**	TCLK to RM fall Hold time	0.678	1.083	1.095
87	**Twmcs_rise**	CLK to WM rise Setup time	0.134	0.226	0.304
88	**Twmcs_fall**	CLK to WM fall Setup time	0.134	0.226	0.304
89	**Twmch_rise**	CLK to WM rise Hold time	0.678	1.083	1.095
90	**Twmch_fall**	CLK to WM fall Hold time	0.678	1.083	1.095
91	**Twmcs_rise**	TCLK to WM rise Setup time	0.134	0.226	0.304
92	**Twmcs_fall**	TCLK to WM fall Setup time	0.134	0.226	0.304
93	**Twmch_rise**	TCLK to WM rise Hold time	0.678	1.083	1.095
94	**Twmch_fall**	TCLK to WM fall Hold time	0.678	1.083	1.095
95	**Tracs_rise**	CLK to RA rise Setup time	0.134	0.226	0.304
96	**Tracs_fall**	CLK to RA fall Setup time	0.134	0.226	0.304
97	**Trach_rise**	CLK to RA rise Hold time	0.678	1.083	1.095
98	**Trach_fall**	CLK to RA fall Hold time	0.678	1.083	1.095
99	**Tracs_rise**	TCLK to RA rise Setup time	0.134	0.226	0.304
100	**Tracs_fall**	TCLK to RA fall Setup time	0.134	0.226	0.304
101	**Trach_rise**	TCLK to RA rise Hold time	0.678	1.083	1.095
102	**Trach_fall**	TCLK to RA fall Hold time	0.678	1.083	1.095
103	**Tlvcs_rise**	CLK to LVTEST rise Setup time	0.134	0.226	0.304
104	**Tlvcs_fall**	CLK to LVTEST fall Setup time	0.134	0.226	0.304
105	**Tlvch_rise**	CLK to LVTEST rise Hold time	0.678	1.083	1.095
106	**Tlvch_fall**	CLK to LVTEST fall Hold time	0.678	1.083	1.095
107	**Tlvcs_rise**	TCLK to LVTEST rise Setup time	0.134	0.226	0.304
108	**Tlvcs_fall**	TCLK to LVTEST fall Setup time	0.134	0.226	0.304
109	**Tlvch_rise**	TCLK to LVTEST rise Hold time	0.678	1.083	1.095
110	**Tlvch_fall**	TCLK to LVTEST fall Hold time	0.678	1.083	1.095
111	**Tszrch**	CLK to SZ rise Setup time	0.268	0.451	0.607
112	**Tszrcl**	CLK to SZ fall Setup time	0.268	0.451	0.607
113	**Tszrmh**	CLK to SZ rise Hold time	0.678	1.083	1.095
114	**Tszrml**	CLK to SZ fall Hold time	7.635	14.254	14.502
115	**Tszrch**	TCLK to SZ rise Setup time	0.268	0.451	0.607
116	**Tszrcl**	TCLK to SZ fall Setup time	0.268	0.451	0.607
117	**Tszrmh**	TCLK to SZ rise Hold time	0.678	1.083	1.095

Table 8: **AC Timing Parameters**

118	**Tszrml**	TCLK to SZ fall Hold time	7.635	14.254	14.502
119	**Tslrch**	CLK to SL rise Setup time	0.268	0.451	0.607
120	**Tslrcl**	CLK to SL fall Setup time	0.268	0.451	0.607
121	**Tslrmh**	CLK to SL rise Hold time	0.678	1.083	1.095
122	**Tslrml**	CLK to SL fall Hold time	7.635	14.254	14.502
123	**Tslrch**	TCLK to SL rise Setup time	0.268	0.451	0.607
124	**Tslrcl**	TCLK to SL fall Setup time	0.268	0.451	0.607
125	**Tslrmh**	TCLK to SL rise Hold time	0.678	1.083	1.095
126	**Tslrml**	TCLK to SL fall Hold time	7.635	14.254	14.502
127	**Tbiosh**	CLK to BADIO rise Setup time	1.101	1.871	1.868
128	**Tbiosl**	CLK to BADIO fall Setup time	1.101	1.871	1.868
129	**Tbiohh**	CLK to BADIO rise Hold time	1.101	1.871	1.868
130	**Tbiohl**	CLK to BADIO fall Hold time	1.101	1.871	1.868
131	**Tbiosh**	TCLK to BADIO rise Setup time	1.101	1.871	1.868
132	**Tbiosl**	TCLK to BADIO fall Setup time	1.101	1.871	1.868
133	**Tbiohh**	TCLK to BADIO rise Hold time	1.101	1.871	1.868
134	**Tbiohl**	TCLK to BADIO fall Hold time	1.101	1.871	1.868
135	**Thnrch**	CLK to HN rise Setup time	0.268	0.451	0.607
136	**Thnrcl**	CLK to HN fall Setup time	0.268	0.451	0.607
137	**Thnrmh**	CLK to HN rise Hold time	0.678	1.083	1.095
138	**Thnrml**	CLK to HN fall Hold time	7.635	14.254	14.502
139	**Thnrch**	TCLK to HN rise Setup time	0.268	0.451	0.607
140	**Thnrcl**	TCLK to HN fall Setup time	0.268	0.451	0.607
141	**Thnrmh**	TCLK to HN rise Hold time	0.678	1.083	1.095
142	**Thnrml**	TCLK to HN fall Hold time	7.635	14.254	14.502
143	**Tsdrch**	CLK to SD rise Setup time	0.268	0.451	0.607
144	**Tsdrcl**	CLK to SD fall Setup time	0.268	0.451	0.607
145	**Tsdrmh**	CLK to SD rise Hold time	0.678	1.083	1.095
146	**Tsdrml**	CLK to SD fall Hold time	7.635	14.254	14.502
147	**Tsdrch**	TCLK to SD rise Setup time	0.268	0.451	0.607
148	**Tsdrcl**	TCLK to SD fall Setup time	0.268	0.451	0.607
149	**Tsdrmh**	TCLK to SD rise Hold time	0.678	1.083	1.095
150	**Tsdrml**	TCLK to SD fall Hold time	7.635	14.254	14.502
151	**Tvbcs_rise**	CLK to VSB100 rise Setup time	0.134	0.226	0.304
152	**Tvbcs_fall**	CLK to VSB100 fall Setup time	0.134	0.226	0.304

Table 8: **AC Timing Parameters**

153	**Tvbch_rise**	CLK to VSB100 rise Hold time	0.678	1.083	1.095
154	**Tvbch_fall**	CLK to VSB100 fall Hold time	0.678	1.083	1.095
155	**Tvbcs_rise**	TCLK to VSB100 rise Setup time	0.134	0.226	0.304
156	**Tvbcs_fall**	TCLK to VSB100 fall Setup time	0.134	0.226	0.304
157	**Tvbch_rise**	TCLK to VSB100 rise Hold time	0.678	1.083	1.095
158	**Tvbch_fall**	TCLK to VSB100 fall Hold time	0.678	1.083	1.095
159	**Tvbcs_rise**	CLK to VSB200 rise Setup time	0.134	0.226	0.304
160	**Tvbcs_fall**	CLK to VSB200 fall Setup time	0.134	0.226	0.304
161	**Tvbch_rise**	CLK to VSB200 rise Hold time	0.678	1.083	1.095
162	**Tvbch_fall**	CLK to VSB200 fall Hold time	0.678	1.083	1.095
163	**Tvbcs_rise**	TCLK to VSB200 rise Setup time	0.134	0.226	0.304
164	**Tvbcs_fall**	TCLK to VSB200 fall Setup time	0.134	0.226	0.304
165	**Tvbch_rise**	TCLK to VSB200 rise Hold time	0.678	1.083	1.095
166	**Tvbch_fall**	TCLK to VSB200 fall Hold time	0.678	1.083	1.095
167	**Tvbcs_rise**	CLK to VSB300 rise Setup time	0.134	0.226	0.304
168	**Tvbcs_fall**	CLK to VSB300 fall Setup time	0.134	0.226	0.304
169	**Tvbch_rise**	CLK to VSB300 rise Hold time	0.678	1.083	1.095
170	**Tvbch_fall**	CLK to VSB300 fall Hold time	0.678	1.083	1.095
171	**Tvbcs_rise**	TCLK to VSB300 rise Setup time	0.134	0.226	0.304
172	**Tvbcs_fall**	TCLK to VSB300 fall Setup time	0.134	0.226	0.304
173	**Tvbch_rise**	TCLK to VSB300 rise Hold time	0.678	1.083	1.095
174	**Tvbch_fall**	TCLK to VSB300 fall Hold time	0.678	1.083	1.095
175	**Tvbcs_rise**	CLK to VSB400 rise Setup time	0.134	0.226	0.304
176	**Tvbcs_fall**	CLK to VSB400 fall Setup time	0.134	0.226	0.304
177	**Tvbch_rise**	CLK to VSB400 rise Hold time	0.678	1.083	1.095
178	**Tvbch_fall**	CLK to VSB400 fall Hold time	0.678	1.083	1.095
179	**Tvbcs_rise**	TCLK to VSB400 rise Setup time	0.134	0.226	0.304
180	**Tvbcs_fall**	TCLK to VSB400 fall Setup time	0.134	0.226	0.304
181	**Tvbch_rise**	TCLK to VSB400 rise Hold time	0.678	1.083	1.095
182	**Tvbch_fall**	TCLK to VSB400 fall Hold time	0.678	1.083	1.095

Table 8: **AC Timing Parameters**

* This table shows values only for the nominal slews and output loads.

#	Parameter(ns)	Description	SS_0p90v_125c
1	**Ttens_rise**	CLK to BISTE rise Setup time	0.238
2	**Ttens_fall**	CLK to BISTE fall Setup time	0.238
3	**Ttenh_rise**	CLK to BISTE rise Hold time	1.143
4	**Ttens_fall**	CLK to BISTE fall Hold time	1.143
5	**Ttens_rise**	TCLK to BISTE rise Setup time	0.238
6	**Ttens_fall**	TCLK to BISTE fall Setup time	0.238
7	**Ttenh_rise**	TCLK to BISTE rise Hold time	1.143
8	**Ttens_fall**	TCLK to BISTE fall Hold time	1.143
9	**Tbms**	CLK to AWT rise Setup time	0.119
10	**Tbmx**	CLK to AWT fall Setup time	0.119
11	**Tbms**	CLK to AWT rise Hold time	0.032
12	**Tbmx**	CLK to AWT fall Hold time	0.032
13	**Tbms**	TCLK to AWT rise Setup time	0.119
14	**Tbmx**	TCLK to AWT fall Setup time	0.119
15	**Tbms**	TCLK to AWT rise Hold time	0.032
16	**Tbmx**	TCLK to AWT fall Hold time	0.032
17	**Tcc**	CLK Cycle Time	1.143
18	**Tch**	CLK Pulse Width High	0.182
19	**Tcl**	CLK Pulse Width Low	0.235
20	**Tcc**	TCLK Cycle Time	1.143
21	**Tch**	TCLK Pulse Width High	0.182
22	**Tcl**	TCLK Pulse Width Low	0.235
23	**Tces_rise**	CLK to CE rise Setup time	0.235
24	**Tces_fall**	CLK to CE fall Setup time	0.235
25	**Tceh_rise**	CLK to CE rise Hold time	0.023
26	**Tceh_fall**	CLK to CE fall Hold time	0.023
27	**Tces_rise**	TCLK to TCE rise Setup time	0.235
28	**Tces_fall**	TCLK to TCE fall Setup time	0.235
29	**Tceh_rise**	TCLK to TCE rise Hold time	0.023
30	**Tceh_fall**	TCLK to TCE fall Hold time	0.023
31	**Trwcs_rise**	CLK to WE rise Setup time	0.149
32	**Trwcs_fall**	CLK to WE fall Setup time	0.149
33	**Trwch_rise**	CLK to WE rise Hold time	0.028
34	**Trwch_fall**	CLK to WE fall Hold time	0.028
35	**Trwcs_rise**	TCLK to TWE rise Setup time	0.149
36	**Trwcs_fall**	TCLK to TWE fall Setup time	0.149
37	**Trwch_rise**	TCLK to TWE rise Hold time	0.028

Table 9: **AC Timing Parameters**

38	**Trwch_fall**	TCLK to TWE fall Hold time	0.028
39	**Tbyms_rise**	CLK to BWM rise Setup time	0.029
40	**Tbyms_fall**	CLK to BWM fall Setup time	0.029
41	**Tbymh_rise**	CLK to BWM rise Hold time	0.070
42	**Tbymh_fall**	CLK to BWM fall Hold time	0.070
43	**Tbyms_rise**	TCLK to TBWM rise Setup time	0.029
44	**Tbyms_fall**	TCLK to TBWM fall Setup time	0.029
45	**Tbymh_rise**	TCLK to TBWM rise Hold time	0.070
46	**Tbymh_fall**	TCLK to TBWM fall Hold time	0.070
47	**Tacs_rise**	CLK to A rise Setup time	0.119
48	**Tacs_fall**	CLK to A fall Setup time	0.119
49	**Tach_rise**	CLK to A rise Hold time	0.032
50	**Tach_fall**	CLK to A fall Hold time	0.032
51	**Tacs_rise**	TCLK to TA rise Setup time	0.119
52	**Tacs_fall**	TCLK to TA fall Setup time	0.119
53	**Tach_rise**	TCLK to TA rise Hold time	0.032
54	**Tach_fall**	TCLK to TA fall Hold time	0.032
55	**Tdcs_rise**	CLK to D rise Setup time	0.001
56	**Tdcs_fall**	CLK to D fall Setup time	0.001
57	**Tdch_rise**	CLK to D rise Hold time	0.070
58	**Tdch_fall**	CLK to D fall Hold time	0.070
59	**Tdcs_rise**	TCLK to TD rise Setup time	0.001
60	**Tdcs_fall**	TCLK to TD fall Setup time	0.001
61	**Tdch_rise**	TCLK to TD rise Hold time	0.070
62	**Tdch_fall**	TCLK to TD fall Hold time	0.070
63	**Tcqh**	CLK to Q rise Delay	1.032
64	**Tcql**	CLK to Q fall Delay	1.080
65	**Tcqxh**	CLK to Q rise Retain	0.865
66	**Tcqxl**	CLK to Q fall Retain	0.865
67	**Tcqh**	D to Q rise Delay	1.032
68	**Tcql**	D to Q fall Delay	1.080
69	**Tcqxh**	D to Q rise Retain	0.865
70	**Tcqxl**	D to Q fall Retain	0.865
71	**Tcqh**	TD to Q rise Delay	1.032
72	**Tcql**	TD to Q fall Delay	1.080
73	**Tcqxh**	TD to Q rise Retain	0.865
74	**Tcqxl**	TD to Q fall Retain	0.865
75	**Tcqh**	TCLK to Q rise Delay	1.032
76	**Tcql**	TCLK to Q fall Delay	1.080
77	**Tcqxh**	TCLK to Q rise Retain	0.865
78	**Tcqxl**	TCLK to Q fall Retain	0.865
79	**Trmcs_rise**	CLK to RM rise Setup time	0.238
80	**Trmcs_fall**	CLK to RM fall Setup time	0.238
81	**Trmch_rise**	CLK to RM rise Hold time	1.143
82	**Trmch_fall**	CLK to RM fall Hold time	1.143

Table 9: **AC Timing Parameters**

83	**Trmcs_rise**	TCLK to RM rise Setup time	0.238
84	**Trmcs_fall**	TCLK to RM fall Setup time	0.238
85	**Trmch_rise**	TCLK to RM rise Hold time	1.143
86	**Trmch_fall**	TCLK to RM fall Hold time	1.143
87	**Twmcs_rise**	CLK to WM rise Setup time	0.238
88	**Twmcs_fall**	CLK to WM fall Setup time	0.238
89	**Twmch_rise**	CLK to WM rise Hold time	1.143
90	**Twmch_fall**	CLK to WM fall Hold time	1.143
91	**Twmcs_rise**	TCLK to WM rise Setup time	0.238
92	**Twmcs_fall**	TCLK to WM fall Setup time	0.238
93	**Twmch_rise**	TCLK to WM rise Hold time	1.143
94	**Twmch_fall**	TCLK to WM fall Hold time	1.143
95	**Tracs_rise**	CLK to RA rise Setup time	0.238
96	**Tracs_fall**	CLK to RA fall Setup time	0.238
97	**Trach_rise**	CLK to RA rise Hold time	1.143
98	**Trach_fall**	CLK to RA fall Hold time	1.143
99	**Tracs_rise**	TCLK to RA rise Setup time	0.238
100	**Tracs_fall**	TCLK to RA fall Setup time	0.238
101	**Trach_rise**	TCLK to RA rise Hold time	1.143
102	**Trach_fall**	TCLK to RA fall Hold time	1.143
103	**Tlvcs_rise**	CLK to LVTEST rise Setup time	0.238
104	**Tlvcs_fall**	CLK to LVTEST fall Setup time	0.238
105	**Tlvch_rise**	CLK to LVTEST rise Hold time	1.143
106	**Tlvch_fall**	CLK to LVTEST fall Hold time	1.143
107	**Tlvcs_rise**	TCLK to LVTEST rise Setup time	0.238
108	**Tlvcs_fall**	TCLK to LVTEST fall Setup time	0.238
109	**Tlvch_rise**	TCLK to LVTEST rise Hold time	1.143
110	**Tlvch_fall**	TCLK to LVTEST fall Hold time	1.143
111	**Tszrch**	CLK to SZ rise Setup time	0.476
112	**Tszrcl**	CLK to SZ fall Setup time	0.476
113	**Tszrmh**	CLK to SZ rise Hold time	1.143
114	**Tszrml**	CLK to SZ fall Hold time	14.427
115	**Tszrch**	TCLK to SZ rise Setup time	0.476
116	**Tszrcl**	TCLK to SZ fall Setup time	0.476
117	**Tszrmh**	TCLK to SZ rise Hold time	1.143

Table 9: **AC Timing Parameters**

118	**Tszrml**	TCLK to SZ fall Hold time	14.427
119	**Tslrch**	CLK to SL rise Setup time	0.476
120	**Tslrcl**	CLK to SL fall Setup time	0.476
121	**Tslrmh**	CLK to SL rise Hold time	1.143
122	**Tslrml**	CLK to SL fall Hold time	14.427
123	**Tslrch**	TCLK to SL rise Setup time	0.476
124	**Tslrcl**	TCLK to SL fall Setup time	0.476
125	**Tslrmh**	TCLK to SL rise Hold time	1.143
126	**Tslrml**	TCLK to SL fall Hold time	14.427
127	**Tbiosh**	CLK to BADIO rise Setup time	2.013
128	**Tbiosl**	CLK to BADIO fall Setup time	2.013
129	**Tbiohh**	CLK to BADIO rise Hold time	2.013
130	**Tbiohl**	CLK to BADIO fall Hold time	2.013
131	**Tbiosh**	TCLK to BADIO rise Setup time	2.013
132	**Tbiosl**	TCLK to BADIO fall Setup time	2.013
133	**Tbiohh**	TCLK to BADIO rise Hold time	2.013
134	**Tbiohl**	TCLK to BADIO fall Hold time	2.013
135	**Thnrch**	CLK to HN rise Setup time	0.476
136	**Thnrcl**	CLK to HN fall Setup time	0.476
137	**Thnrmh**	CLK to HN rise Hold time	1.143
138	**Thnrml**	CLK to HN fall Hold time	14.427
139	**Thnrch**	TCLK to HN rise Setup time	0.476
140	**Thnrcl**	TCLK to HN fall Setup time	0.476
141	**Thnrmh**	TCLK to HN rise Hold time	1.143
142	**Thnrml**	TCLK to HN fall Hold time	14.427
143	**Tsdrch**	CLK to SD rise Setup time	0.476
144	**Tsdrcl**	CLK to SD fall Setup time	0.476
145	**Tsdrmh**	CLK to SD rise Hold time	1.143
146	**Tsdrml**	CLK to SD fall Hold time	14.427
147	**Tsdrch**	TCLK to SD rise Setup time	0.476
148	**Tsdrcl**	TCLK to SD fall Setup time	0.476
149	**Tsdrmh**	TCLK to SD rise Hold time	1.143
150	**Tsdrml**	TCLK to SD fall Hold time	14.427
151	**Tvbcs_rise**	CLK to VSB100 rise Setup time	0.238
152	**Tvbcs_fall**	CLK to VSB100 fall Setup time	0.238

Table 9: **AC Timing Parameters**

153	**Tvbch_rise**	CLK to VSB100 rise Hold time	1.143
154	**Tvbch_fall**	CLK to VSB100 fall Hold time	1.143
155	**Tvbcs_rise**	TCLK to VSB100 rise Setup time	0.238
156	**Tvbcs_fall**	TCLK to VSB100 fall Setup time	0.238
157	**Tvbch_rise**	TCLK to VSB100 rise Hold time	1.143
158	**Tvbch_fall**	TCLK to VSB100 fall Hold time	1.143
159	**Tvbcs_rise**	CLK to VSB200 rise Setup time	0.238
160	**Tvbcs_fall**	CLK to VSB200 fall Setup time	0.238
161	**Tvbch_rise**	CLK to VSB200 rise Hold time	1.143
162	**Tvbch_fall**	CLK to VSB200 fall Hold time	1.143
163	**Tvbcs_rise**	TCLK to VSB200 rise Setup time	0.238
164	**Tvbcs_fall**	TCLK to VSB200 fall Setup time	0.238
165	**Tvbch_rise**	TCLK to VSB200 rise Hold time	1.143
166	**Tvbch_fall**	TCLK to VSB200 fall Hold time	1.143
167	**Tvbcs_rise**	CLK to VSB300 rise Setup time	0.238
168	**Tvbcs_fall**	CLK to VSB300 fall Setup time	0.238
169	**Tvbch_rise**	CLK to VSB300 rise Hold time	1.143
170	**Tvbch_fall**	CLK to VSB300 fall Hold time	1.143
171	**Tvbcs_rise**	TCLK to VSB300 rise Setup time	0.238
172	**Tvbcs_fall**	TCLK to VSB300 fall Setup time	0.238
173	**Tvbch_rise**	TCLK to VSB300 rise Hold time	1.143
174	**Tvbch_fall**	TCLK to VSB300 fall Hold time	1.143
175	**Tvbcs_rise**	CLK to VSB400 rise Setup time	0.238
176	**Tvbcs_fall**	CLK to VSB400 fall Setup time	0.238
177	**Tvbch_rise**	CLK to VSB400 rise Hold time	1.143
178	**Tvbch_fall**	CLK to VSB400 fall Hold time	1.143
179	**Tvbcs_rise**	TCLK to VSB400 rise Setup time	0.238
180	**Tvbcs_fall**	TCLK to VSB400 fall Setup time	0.238
181	**Tvbch_rise**	TCLK to VSB400 rise Hold time	1.143
182	**Tvbch_fall**	TCLK to VSB400 fall Hold time	1.143

Table 9: **AC Timing Parameters**

* This table shows values only for the nominal slews and output loads.

Leakage and Power

#	Parameter	Description	TT_1p00v_25c	FF_1p10v_n40c	FF_1p10v_n55c
1	sl_leak(uW)	Leakage Power::slumber	2309.	5161.	3891.
2	sz_leak(uW)	Leakage Power::snooze	2340.	4549.	3187.
3	hn_leak(uW)	Leakage Power::hibernate	1990.	4268.	3080.
4	sd_leak(uW)	Leakage Power::shutdown	1829.	4007.	2918.
5	static_leak(uW)	Leakage Power::standby	2728.	5448.	4048.
6	Power_WE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1921	0.1110	0.1110
7	Power_WE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1975	0.1126	0.1126
8	Power_TWE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1921	0.1110	0.1110
9	Power_TWE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1975	0.1126	0.1126
10	Power_A_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1921	0.1110	0.1110
11	Power_A_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1921	0.1110	0.1110
12	Power_TA_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1921	0.1110	0.1110
13	Power_TA_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1921	0.1110	0.1110
14	Power_WE_r::chip_en(uW/MHZ)	Pin Power Rise	3.824	1.923	1.923
15	Power_WE_f::chip_en(uW/MHZ)	Pin Power Fall	4.024	1.954	1.954
16	Power_TWE_r::chip_en(uW/MHZ)	Pin Power Rise	3.824	1.923	1.923
17	Power_TWE_f::chip_en(uW/MHZ)	Pin Power Fall	4.024	1.954	1.954
18	Power_A_r::chip_en(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
19	Power_A_f::chip_en(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
20	Power_TA_r::chip_en(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
21	Power_TA_f::chip_en(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
22	Pread(uW/MHZ)	Read Power Rise	8.473	10.01	10.01
23	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
24	Pwrite(uW/MHZ)	Write Power Rise	10.91	10.16	10.16
25	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
26	Power_CLK_r(uW/MHZ)	Pin Power Rise	2.880	1.531	1.531
27	Power_CLK_f(uW/MHZ)	Pin Power Fall	2.809	1.541	1.541
28	Pread(uW/MHZ)	Read Power Rise	8.473	10.01	10.01
29	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
30	Pwrite(uW/MHZ)	Write Power Rise	10.91	10.16	10.16
31	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
32	Power_TCLK_r(uW/MHZ)	Pin Power Rise	2.880	1.531	1.531
33	Power_TCLK_f(uW/MHZ)	Pin Power Fall	2.809	1.541	1.541
34	Power_SZ_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
35	Power_SZ_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
36	Power_SL_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
37	Power_SL_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
38	Power_HN_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
39	Power_HN_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
40	Power_SD_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
41	Power_SD_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
42	Power_VSB100_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
43	Power_VSB100_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
44	Power_VSB200_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
45	Power_VSB200_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
46	Power_VSB300_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
47	Power_VSB300_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
48	Power_VSB400_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
49	Power_VSB400_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938

Table 10: **Leakage & Dynamic Power**

* Read/Write power is due to the rising edge of the clock only.
* Read/Write power is for the alternate active cycles
* Read/Write power is measured with 50% data and address bus toggling.
* Address/Data power is for each individual bit of the bus

Table 11: **Leakage & Dynamic Power**

#	Parameter	Description	FF_1p10v_125c	SS_0p90v_n40c	SS_0p90v_n55c
1	sl_leak(uW)	Leakage Power::slumber	4.530e+04	515.0	562.9
2	sz_leak(uW)	Leakage Power::snooze	5.063e+04	241.3	221.8
3	hn_leak(uW)	Leakage Power::hibernate	4.157e+04	413.6	459.9
4	sd_leak(uW)	Leakage Power::shutdown	3.863e+04	375.1	426.2
5	static_leak(uW)	Leakage Power::standby	5.597e+04	335.9	317.1
6	Power_WE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1110	0.01046	0.01046
7	Power_WE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1126	0.01165	0.01165
8	Power_TWE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1110	0.01046	0.01046
9	Power_TWE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1126	0.01165	0.01165
10	Power_A_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1110	0.01046	0.01046
11	Power_A_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1110	0.01046	0.01046
12	Power_TA_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1110	0.01046	0.01046
13	Power_TA_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1110	0.01046	0.01046
14	Power_WE_r::chip_en(uW/MHZ)	Pin Power Rise	1.923	0.4144	0.4144
15	Power_WE_f::chip_en(uW/MHZ)	Pin Power Fall	1.954	0.3998	0.3998
16	Power_TWE_r::chip_en(uW/MHZ)	Pin Power Rise	1.923	0.4144	0.4144
17	Power_TWE_f::chip_en(uW/MHZ)	Pin Power Fall	1.954	0.3998	0.3998
18	Power_A_r::chip_en(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
19	Power_A_f::chip_en(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
20	Power_TA_r::chip_en(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
21	Power_TA_f::chip_en(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
22	Pread(uW/MHZ)	Read Power Rise	10.01	3.200	3.200
23	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
24	Pwrite(uW/MHZ)	Write Power Rise	10.16	4.007	4.007
25	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
26	Power_CLK_r(uW/MHZ)	Pin Power Rise	1.531	0.1297	0.1297
27	Power_CLK_f(uW/MHZ)	Pin Power Fall	1.541	0.1383	0.1383
28	Pread(uW/MHZ)	Read Power Rise	10.01	3.200	3.200
29	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
30	Pwrite(uW/MHZ)	Write Power Rise	10.16	4.007	4.007
31	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
32	Power_TCLK_r(uW/MHZ)	Pin Power Rise	1.531	0.1297	0.1297
33	Power_TCLK_f(uW/MHZ)	Pin Power Fall	1.541	0.1383	0.1383
34	Power_SZ_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
35	Power_SZ_f(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
36	Power_SL_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
37	Power_SL_f(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
38	Power_HN_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
39	Power_HN_f(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
40	Power_SD_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
41	Power_SD_f(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
42	Power_VSB100_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
43	Power_VSB100_f(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
44	Power_VSB200_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
45	Power_VSB200_f(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
46	Power_VSB300_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
47	Power_VSB300_f(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
48	Power_VSB400_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
49	Power_VSB400_f(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322

Table 11: **Leakage & Dynamic Power**

* Read/Write power is due to the rising edge of the clock only.
* Read/Write power is for the alternate active cycles
* Read/Write power is measured with 50% data and address bus toggling.
* Address/Data power is for each individual bit of the bus

#	Parameter	Description	SS_0p90v_125c
1	sl_leak(uW)	Leakage Power::slumber	2161.
2	sz_leak(uW)	Leakage Power::snooze	2521.
3	hn_leak(uW)	Leakage Power::hibernate	2052.
4	sd_leak(uW)	Leakage Power::shutdown	1969.
5	static_leak(uW)	Leakage Power::standby	2640.

Table 12: **Leakage & Dynamic Power**

6	Power_WE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.01046
7	Power_WE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.01165
8	Power_TWE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.01046
9	Power_TWE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.01165
10	Power_A_r::chip_dis(uW/MHZ)	Pin Power Rise	0.01046
11	Power_A_f::chip_dis(uW/MHZ)	Pin Power Fall	0.01046
12	Power_TA_r::chip_dis(uW/MHZ)	Pin Power Rise	0.01046
13	Power_TA_f::chip_dis(uW/MHZ)	Pin Power Fall	0.01046
14	Power_WE_r::chip_en(uW/MHZ)	Pin Power Rise	0.4144
15	Power_WE_f::chip_en(uW/MHZ)	Pin Power Fall	0.3998
16	Power_TWE_r::chip_en(uW/MHZ)	Pin Power Rise	0.4144
17	Power_TWE_f::chip_en(uW/MHZ)	Pin Power Fall	0.3998
18	Power_A_r::chip_en(uW/MHZ)	Pin Power Rise	0.08451
19	Power_A_f::chip_en(uW/MHZ)	Pin Power Fall	4.322
20	Power_TA_r::chip_en(uW/MHZ)	Pin Power Rise	0.08451
21	Power_TA_f::chip_en(uW/MHZ)	Pin Power Fall	4.322
22	Pread(uW/MHZ)	Read Power Rise	3.200
23	Pread(uW/MHZ)	Read Power Fall	0.000
24	Pwrite(uW/MHZ)	Write Power Rise	4.007
25	Pwrite(uW/MHZ)	Write Power Fall	0.000
26	Power_CLK_r(uW/MHZ)	Pin Power Rise	0.1297
27	Power_CLK_f(uW/MHZ)	Pin Power Fall	0.1383
28	Pread(uW/MHZ)	Read Power Rise	3.200
29	Pread(uW/MHZ)	Read Power Fall	0.000
30	Pwrite(uW/MHZ)	Write Power Rise	4.007
31	Pwrite(uW/MHZ)	Write Power Fall	0.000
32	Power_TCLK_r(uW/MHZ)	Pin Power Rise	0.1297
33	Power_TCLK_f(uW/MHZ)	Pin Power Fall	0.1383
34	Power_SZ_r(uW/MHZ)	Pin Power Rise	0.08451
35	Power_SZ_f(uW/MHZ)	Pin Power Fall	4.322
36	Power_SL_r(uW/MHZ)	Pin Power Rise	0.08451
37	Power_SL_f(uW/MHZ)	Pin Power Fall	4.322
38	Power_HN_r(uW/MHZ)	Pin Power Rise	0.08451
39	Power_HN_f(uW/MHZ)	Pin Power Fall	4.322
40	Power_SD_r(uW/MHZ)	Pin Power Rise	0.08451
41	Power_SD_f(uW/MHZ)	Pin Power Fall	4.322
42	Power_VSB100_r(uW/MHZ)	Pin Power Rise	0.08451
43	Power_VSB100_f(uW/MHZ)	Pin Power Fall	4.322
44	Power_VSB200_r(uW/MHZ)	Pin Power Rise	0.08451
45	Power_VSB200_f(uW/MHZ)	Pin Power Fall	4.322
46	Power_VSB300_r(uW/MHZ)	Pin Power Rise	0.08451
47	Power_VSB300_f(uW/MHZ)	Pin Power Fall	4.322
48	Power_VSB400_r(uW/MHZ)	Pin Power Rise	0.08451
49	Power_VSB400_f(uW/MHZ)	Pin Power Fall	4.322

Table 12: **Leakage & Dynamic Power**

* Read/Write power is due to the rising edge of the clock only.
* Read/Write power is for the alternate active cycles
* Read/Write power is measured with 50% data and address bus toggling.
* Address/Data power is for each individual bit of the bus

Input Pin Capacitance

#	PIN	Description(unit:pF)	TT_1p00v_25c	FF_1p10v_n40c	FF_1p10v_n55c
1	BISTE	Pin Capacitance	0.002	0.002	0.002
2	AWT	Pin Capacitance	0.002	0.002	0.002
3	CLK	Pin Capacitance	0.008	0.007	0.007
4	TCLK	Pin Capacitance	0.008	0.007	0.007
5	CE	Pin Capacitance	0.002	0.002	0.002
6	TCE	Pin Capacitance	0.002	0.002	0.002
7	WE	Pin Capacitance	0.002	0.002	0.002
8	TWE	Pin Capacitance	0.002	0.002	0.002
9	BWM	Pin Capacitance	0.002	0.002	0.002
10	TBWM	Pin Capacitance	0.002	0.002	0.002
11	A	Pin Capacitance	0.002	0.002	0.002
12	TA	Pin Capacitance	0.002	0.002	0.002
13	D	Pin Capacitance	0.002	0.002	0.002
14	TD	Pin Capacitance	0.002	0.002	0.002
15	RM	Pin Capacitance	0.002	0.002	0.002
16	WM	Pin Capacitance	0.002	0.002	0.002
17	RA	Pin Capacitance	0.002	0.002	0.002
18	LVTEST	Pin Capacitance	0.002	0.002	0.002
19	SZ	Pin Capacitance	0.005	0.005	0.005
20	SL	Pin Capacitance	0.005	0.005	0.005
21	BADIO	Pin Capacitance	–	–	–
22	HN	Pin Capacitance	0.011	0.011	0.011
23	SD	Pin Capacitance	0.006	0.006	0.006
24	VSB100	Pin Capacitance	0.002	0.002	0.002
25	VSB200	Pin Capacitance	0.002	0.002	0.002
26	VSB300	Pin Capacitance	0.002	0.002	0.002
27	VSB400	Pin Capacitance	0.002	0.002	0.002
28	VDD	Pin Capacitance	–	–	–

Table 13: **Capacitance**

#	PIN	Description(unit:pF)	FF_1p10v_125c	SS_0p90v_n40c	SS_0p90v_n55c
1	BISTE	Pin Capacitance	0.002	0.002	0.002
2	AWT	Pin Capacitance	0.002	0.002	0.002
3	CLK	Pin Capacitance	0.007	0.009	0.009
4	TCLK	Pin Capacitance	0.007	0.009	0.009
5	CE	Pin Capacitance	0.002	0.002	0.002
6	TCE	Pin Capacitance	0.002	0.002	0.002
7	WE	Pin Capacitance	0.002	0.002	0.002
8	TWE	Pin Capacitance	0.002	0.002	0.002
9	BWM	Pin Capacitance	0.002	0.002	0.002
10	TBWM	Pin Capacitance	0.002	0.002	0.002
11	A	Pin Capacitance	0.002	0.002	0.002
12	TA	Pin Capacitance	0.002	0.002	0.002
13	D	Pin Capacitance	0.002	0.002	0.002
14	TD	Pin Capacitance	0.002	0.002	0.002
15	RM	Pin Capacitance	0.002	0.002	0.002
16	WM	Pin Capacitance	0.002	0.002	0.002
17	RA	Pin Capacitance	0.002	0.002	0.002
18	LVTEST	Pin Capacitance	0.002	0.002	0.002
19	SZ	Pin Capacitance	0.005	0.005	0.005
20	SL	Pin Capacitance	0.005	0.005	0.005
21	BADIO	Pin Capacitance	–	–	–
22	HN	Pin Capacitance	0.011	0.011	0.011
23	SD	Pin Capacitance	0.006	0.005	0.005
24	VSB100	Pin Capacitance	0.002	0.002	0.002
25	VSB200	Pin Capacitance	0.002	0.002	0.002
26	VSB300	Pin Capacitance	0.002	0.002	0.002
27	VSB400	Pin Capacitance	0.002	0.002	0.002
28	VDD	Pin Capacitance	–	–	–

Table 14: **Capacitance**

#	PIN	Description(unit:pF)	SS_0p90v_125c
1	BISTE	Pin Capacitance	0.002
2	AWT	Pin Capacitance	0.002
3	CLK	Pin Capacitance	0.009
4	TCLK	Pin Capacitance	0.009
5	CE	Pin Capacitance	0.002
6	TCE	Pin Capacitance	0.002
7	WE	Pin Capacitance	0.002
8	TWE	Pin Capacitance	0.002
9	BWM	Pin Capacitance	0.002
10	TBWM	Pin Capacitance	0.002
11	A	Pin Capacitance	0.002
12	TA	Pin Capacitance	0.002
13	D	Pin Capacitance	0.002
14	TD	Pin Capacitance	0.002
15	RM	Pin Capacitance	0.002
16	WM	Pin Capacitance	0.002
17	RA	Pin Capacitance	0.002
18	LVTEST	Pin Capacitance	0.002
19	SZ	Pin Capacitance	0.005
20	SL	Pin Capacitance	0.005
21	BADIO	Pin Capacitance	–
22	HN	Pin Capacitance	0.011
23	SD	Pin Capacitance	0.005
24	VSB100	Pin Capacitance	0.002
25	VSB200	Pin Capacitance	0.002
26	VSB300	Pin Capacitance	0.002
27	VSB400	Pin Capacitance	0.002
28	VDD	Pin Capacitance	–

Table 15: **Capacitance**

Corruption Table

#	Parameter	Related Pin	CEM	CCL
1	Tcc(Violation)	CLK	YES	NO
2	Tcl(Violation)	CLK	YES	NO
3	Tch(Violation)	CLK	YES	NO
4	Tacs_rise(Violation)	A	YES	NO
5	Tach_rise(Violation)	A	YES	NO
6	Trwcs_rise(Violation)	WE	NO	YES
7	Trwch_rise(Violation)	WE	NO	YES
8	Tbyms_rise(Violation)	BWM	NO	YES
9	Tbymh_rise(Violation)	BWM	NO	YES
10	Tces_rise(Violation)	CE	YES	NO
11	Tceh_rise(Violation)	CE	YES	NO
12	Tdcs_rise(Violation)	D	NO	YES
13	Tdch_rise(Violation)	D	NO	YES
14	Tsnzrc(Violation)	SZ	YES	NO
15	Tsnzrm(Violation)	SZ	YES	NO
16	Tslprc(Violation)	SL	YES	NO
17	Tslprm(Violation)	SL	YES	NO
18	Thbrntrc(Violation)	HN	YES	NO
19	Thbrntprm(Violation)	HN	YES	NO
20	Tdslprc(Violation)	SD	YES	NO
21	Tdslprm(Violation)	SD	YES	NO

Table 16: **Violation in case of Write Mode**

* CEM : Corrupt Entire Memory

* CCL : Corrupt Current Location (Selected Word)

#	Parameter	Related Pin	CEM	CCL
1	Tcc(Violation)	CLK	YES	NO
2	Tcl(Violation)	CLK	YES	NO
3	Tch(Violation)	CLK	YES	NO
4	Tacs_rise(Violation)	A	YES	NO
5	Tach_rise(Violation)	A	YES	NO
6	Trwcs_rise(Violation)	WE	NO	YES
7	Trwch_rise(Violation)	WE	NO	YES
8	Tces_rise(Violation)	CE	YES	NO
9	Tceh_rise(Violation)	CE	YES	NO
10	Tsnzrc(Violation)	SZ	YES	NO
11	Tsnzrm(Violation)	SZ	YES	NO
12	Tslprc(Violation)	SL	YES	NO
13	Tslprm(Violation)	SL	YES	NO
14	Thbrntrc(Violation)	HN	YES	NO
15	Thbrntprm(Violation)	HN	YES	NO
16	Tdslprc(Violation)	SD	YES	NO
17	Tdslprm(Violation)	SD	YES	NO

Table 17: **Violation in case of Read Mode**

* CEM : Corrupt Entire Memory

* CCL : Corrupt Current Location (Selected Word)

Timing Diagrams

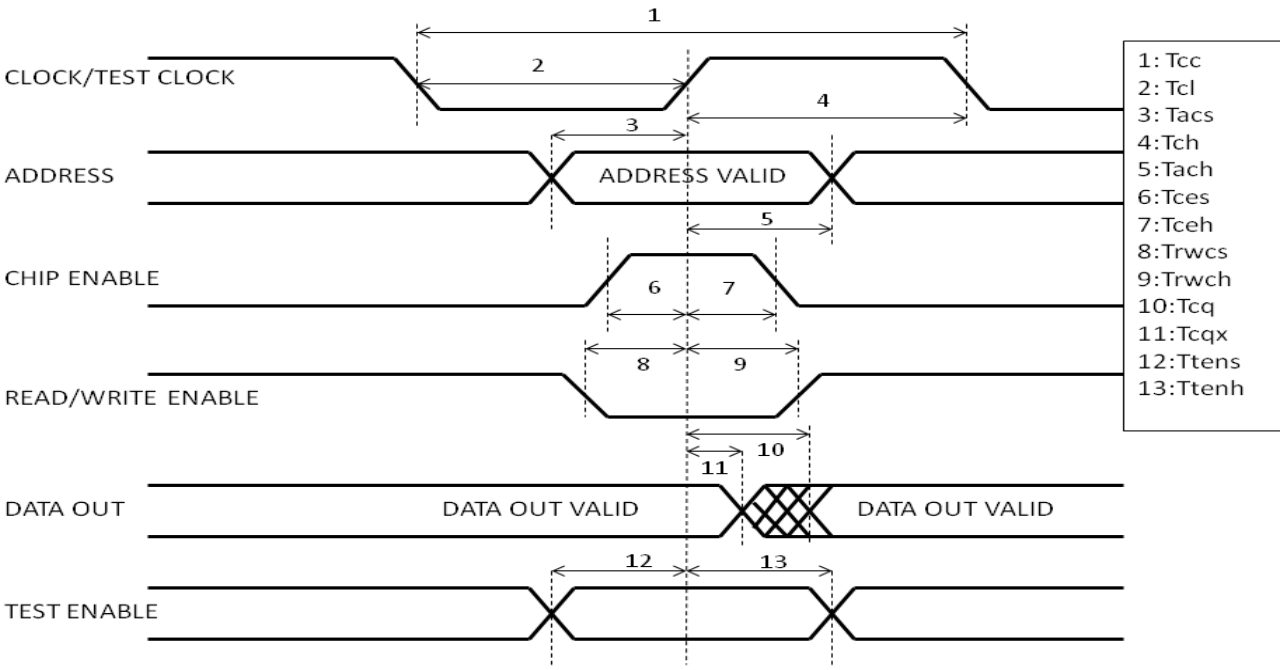


Figure 1: **Read Timing**

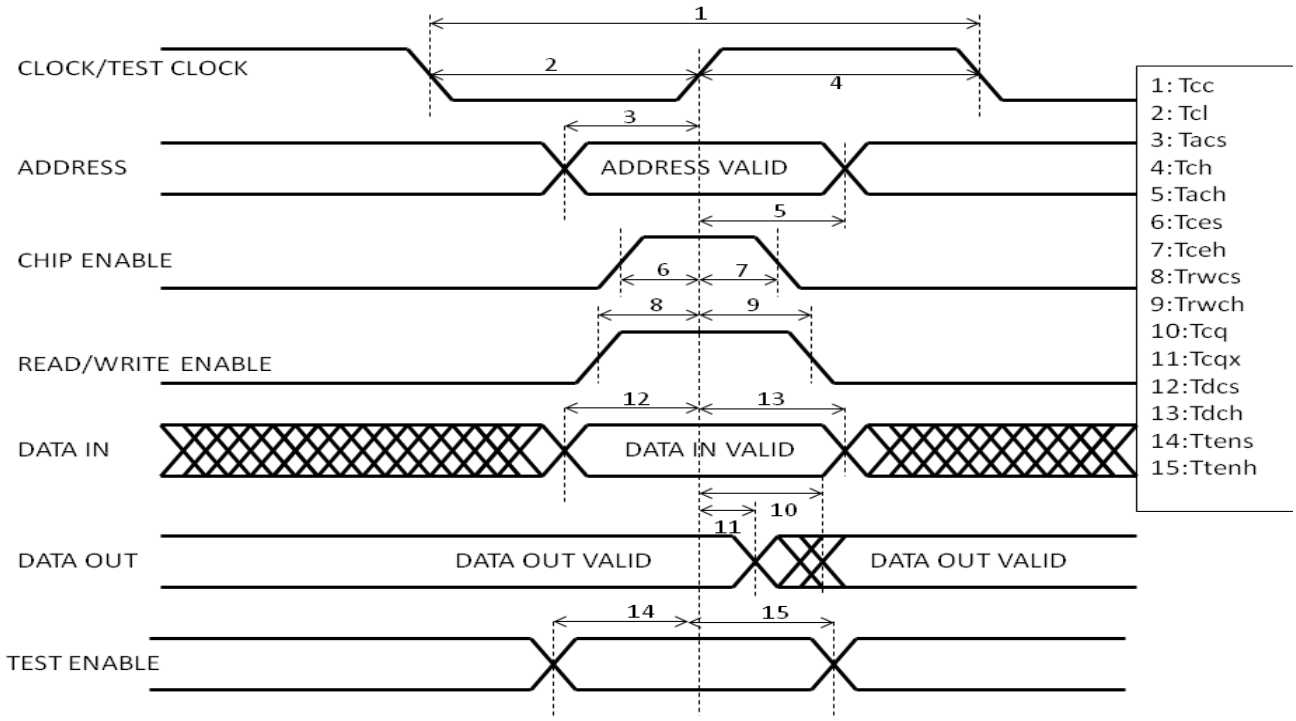


Figure 2: **Write Timing**

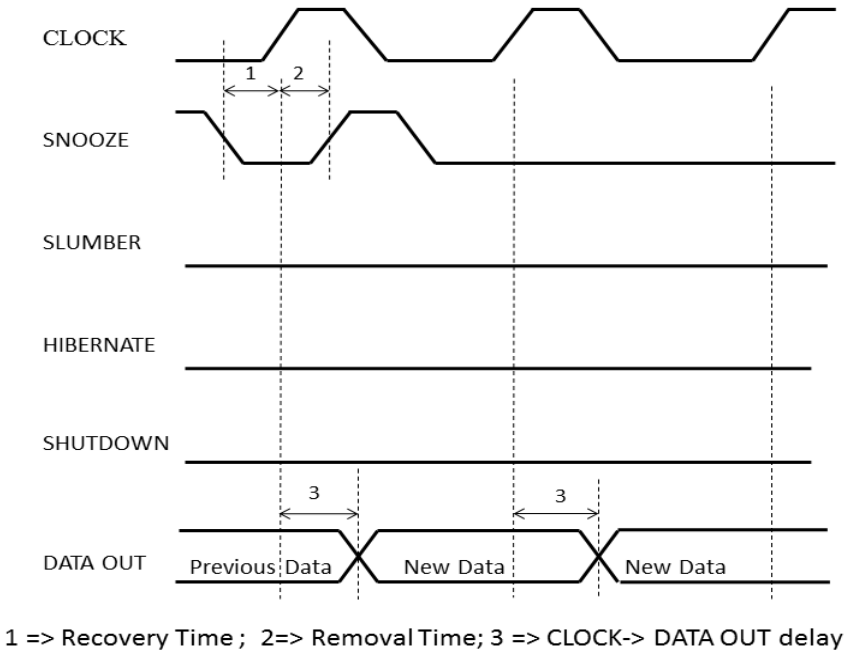
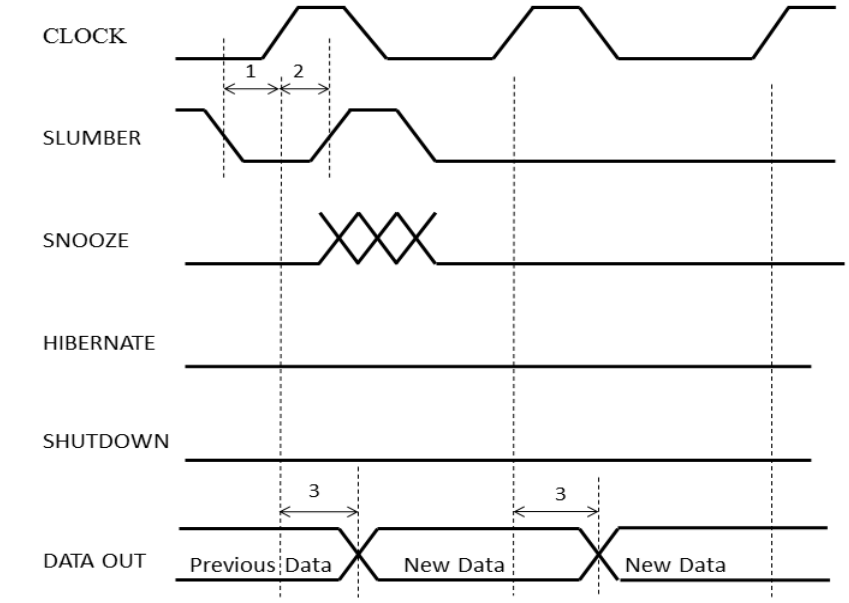
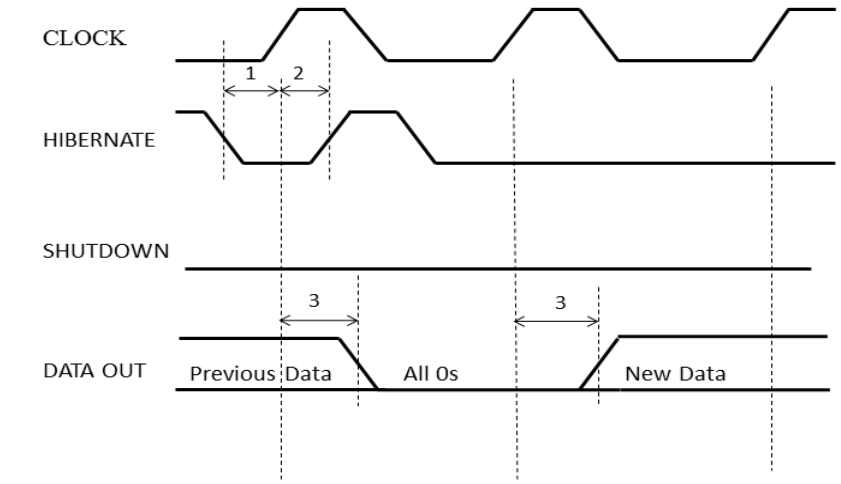


Figure 3: **Snooze Timing**



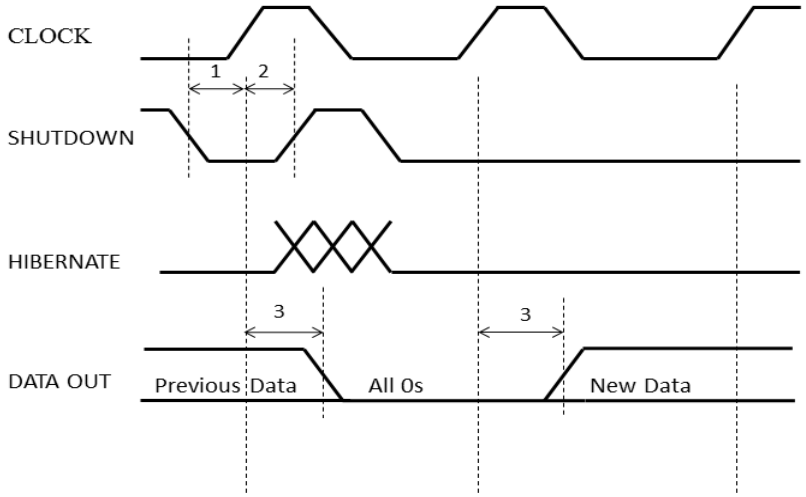
1 => Recovery Time ; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

Figure 4: **Slumber Timing**



1 => Recovery Time ; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

Figure 5: **Hibernate Timing**



1 => Recovery Time ; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

Figure 6: **Shutdown Timing**

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