GF-45RFSOI Single-Port Static RAM

(spram_4096x16m16b1pm2re1)

Datasheet

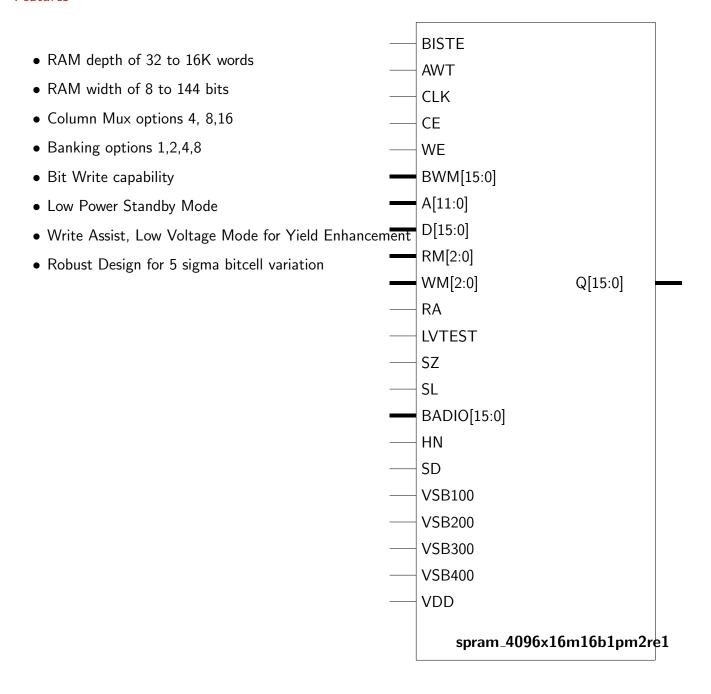
Version: 1.71



Introduction

The SpectralRAM IP Random Access Memory (RAM) core is a fully verified memory unit that uses state of the art power saving techniques to reduce standby power in deep sub-micron process nodes. The width, depth, memory type, and other optional features of the RAM core can be customized based on specifications.

Features





Software	MemoryTime 2.2.1
Compiler Name	Single-Port
Platform	Linux-CentOS
Date of Generation	06/14/19
Technology	GF-45RFSOI
Description	High Density Low Power RAM

Table 1: Compiler Information

Number of Words	4096
Number of Bits	16
Column-Mux	16
Width(um)	138.414
Height(um)	339.788
Area(square um)	47031.4
Frequency(MHz)	874.81
Top Metal Layer	Metal 4

Table 2: Instance Information



Pin Information

Signal Name	In/Out	Description
BISTE	input	Test Enable: When High Memory operates in test mode else
		if low Memory operates in Normal Mode
AWT	input	
CLK	clock	Clock: All normal read/write operations are synchronous to
		the rising edge of the clock
TCLK	clock	Test Clock: All test read/write operations are synchronous to
		the rising edge of the clock
CE	input	Control signal used to select the macro. When the macro is
		deselected, primary inputs like address data are inhibited from
		accessing the memory array. If the power savings mode is
		selected, this pin will have no impact on the leakage savings
		operations
TCE	input	Test Control signal used to select the macro. When the macro
		is deselected, primary inputs like address data are inhibited
		from accessing the memory array. If the power savings mode
		is selected, this pin will have no impact on the leakage savings
		operations
WE	input	Read/Write Enable(Active High): Control signal used to se-
		lect between read and write operation
TWE	input	Test-Read/Write Enable(Active High): Control signal used to
		select between read and write operation
BWM[15:0]	input	Write Mask(Active High): Bitwise control signal to mask se-
		lected write locations of a word during the write operation.
		The selected word would retain the previous data for all the
		masked bits. The output latches for the masked bits would
		also retain the data read from the prior read operation. This
		bus is a don't care during the read operation
TBWM[15:0]	input	Test Write Mask(Active High): Bitwise control signal to mask
		selected write locations of a word during the write operation.
		The selected word would retain the previous data for all the
		masked bits. The output latches for the masked bits would
		also retain the data read from the prior read operation. This
2544.03		bus is a don't care during the read operation
A[11:0]	input	Address: Address bus Specifies read and write Locations
TA[11:0]	input	Test Address: Address bus Specifies read and write Locations
D[15:0]	input	Data In: Data bus specifies the contents that get written into
		the Memory for an address specified
TD[15:0]	input	Test Data In: Data bus specifies the contents that get written
		into the Memory for an address specified
Q[15:0]	output	Data out: Data bus used to read contents of the Memory
RM[2:0]	input	Read Margin: this pin is used to control internal timer
WM[2:0]	input	Write Margin: this pin is used to control internal write boost

Table 3: Pin Information



RA	input	Read Assist: Please refer to the Compiler User Guide for the		
		details		
LVTEST	input	Low Voltage Mode for Yield: WL follows Clock High. Please		
		refer to the Compiler User Guide for the details		
SZ	input	SNOOZE: Array Source Bias (Data Retained)		
SL	input	SLUMBER: Periphery Shutdown (Data Retained)		
BADIO[15:0]	input	BADIO: Repair Shifting Signal		
HN	input	HIBERNATE: Array Source Bias + Periphery Shutdown (Data		
		Retained)		
SD	input	SHUTDOWN: Array $+$ Periphery Shutdown (Data Lost)		
VSB100	input	Source Bias (Lowest Level). Please refer to the Compiler User		
		Guide for the details		
VSB200	input	Source Bias (Med-Low Level). Please refer to the Compiler		
		User Guide for the details		
VSB300	input	Source Bias (Med-High Level). Please refer to the Compiler		
		User Guide for the details		
VSB400	input	Source Bias (Highest Level). Please refer to the Compiler		
		User Guide for the details		
VDD	input	Array Power Supply		

Table 3: Pin Information



Truth Table

	WRITE	READ	STANDBY	SNOOZE	SLUMBER	HIBERNATE	SHUTDOWN	TEST
A/TA [11:0]	ADDRESS	ADDRESS	X	X	X	X	X	TADDRESS
D/TD[15:0]	DATA	X	X	X	X	X	X	TDATA
BWM/TBWM[15:0]	MASK	X	X	X	X	X	X	TMASK
CLK/TCLK	^CLOCK	^CLOCK	X	X	X	X	X	^TCLOCK
WE/TWE	1	0	X	X	X	X	X	TREAD/TWRIT
CE/TCE	1	1	0	X	X	X	X	TCHIPENABLE
SZ	0	0	0	1	X	X	X	0
SL	0	0	0	0	1	X	X	0
HN	0	0	0	0	0	1	X	0
SD	0	0	0	0	0	0	1	0
Q[15:0]	DATA	DATA	Prev DATA	Prev DATA	Prev DATA	Prev DATA	0	TDATA
BISTE	0	0	X	X	X	X	X	1
MemoryCore	Retained	Retained	Retained	Retained	Retained	Retained	Not Retained	Retained

Table 4: Logic Truth Table

- * ^CLOCK/^TCLOCK: Positive Edge of Clock
- * MemoryCore : State of the stored Memory Contents
- * Each subsequent power down state reduces leakage more than the previous state

 SNOOZE Leakage > SLUMBER Leakage > HIBERNATE Leakage > SHUTDOWN Leakage
- * Each subsequent power down state consumes higher wake-up power than the previous state SNOOZE Power < SLUMBER Power < HIBERNATE Power < SHUTDOWN Power
- * Each subsequent power down state has a higher recovery time than the previous state

 SNOOZE Rec Time < SLUMBER Rec Time < HIBERNATE Rec Time < SHUTDOWN Rec Time



Look Up Table

Index	1	2	3	4	5	6	7
Input Slope(ns)	0.0021	0.0142	0.08	0.1359	0.2311	0.3467	0.52
Input Clock Slope(ns)	0.0021	0.0142	0.08	0.1359	0.2311	0.3467	0.52
Output Load(pF)	0.004	0.009	0.018	0.035	0.075	0.15	0.3

Table 5: Input slope & Output Load

Table shows the Input slews and Output loads that were used to characterize the memory

Operating Conditions

#	PVT Corner	Process	Voltage(V)	Temperature(C)
1	TT_1p00v_25c	TT	1	25
2	FF_1p10v_n40c	FF	1.1	-40
3	FF_1p10v_n55c		1.1	-55
4	FF_1p10v_125c	FF	1.1	125
5	SS_0p90v_n40c	SS	0.9	-40
6	SS_0p90v_n55c		0.9	-55
7	SS_0p90v_125c	SS	0.9	125

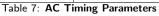
Table 6: **PVT Corners**

Table Depicts different process, voltage and temperature corners that were characterized for this memory.



AC Timing Parameters

#	Parameter(ns)	Description	TT_1p00v_25c	FF_1p10v_n40c	FF_1p10v_n55c				
1	Ttens_rise	CLK to BISTE rise Setup time	0.163	0.123	0.123				
2	Ttens_fall	CLK to BISTE fall Setup time	0.163	0.123	0.123				
3	Ttenh_rise	CLK to BISTE rise Hold time	0.723	0.415	0.415				
4	Ttens_fall	CLK to BISTE fall Hold time	0.723	0.415	0.415				
5	Ttens_rise	TCLK to BISTE rise Setup time	0.163	0.123	0.123				
6	Ttens_fall	TCLK to BISTE fall Setup time	0.163	0.123	0.123				
7	Ttenh_rise	TCLK to BISTE rise Hold time	0.723	0.415	0.415				
8	Ttens_fall	TCLK to BISTE fall Hold time	0.723	0.415	0.415				
9	Tbms	CLK to AWT rise Setup time	0.081	0.062	0.061				
10	Tbmx	CLK to AWT fall Setup time	0.081	0.062	0.061				
11	Thms	CLK to AWT rise Hold time	0.022	0.020	0.020				
12	Tbms	CLK to AWT fall Hold time TCLK to AWT rise	0.022	0.020	0.020				
13	Tbms	TCLK to AWT rise Setup time TCLK to AWT fall	0.081	0.062	0.061				
15	Tbms	Setup time TCLK to AWT rise Hold	0.022	0.020	0.001				
		time							
16	Tbmx	TCLK to AWT fall Hold time	0.022	0.020	0.020				
17	Тсс	CLK Cycle Time	0.723	0.415	0.415				
18	Tch	CLK Pulse Width High	0.160	0.153	0.152				
19	Tcl	CLK Pulse Width Low	0.158	0.108	0.107				
20	Тсс	TCLK Cycle Time	0.723	0.415	0.415				
21	Tch	TCLK Pulse Width High	0.160	0.153	0.152				
22	Tcl	TCLK Pulse Width Low	0.158	0.108	0.107				
23	Tces_rise	CLK to CE rise Setup	0.158	0.108	0.107				
24	Tces_fall	CLK to CE fall Setup time	0.158	0.108	0.107				
25	Tceh_rise	CLK to CE rise Hold time	0.015	0.013	0.013				
26	Tceh_fall	CLK to CE fall Hold time	0.015	0.013	0.013				
27	Tces_rise Tces_fall	TCLK to TCE rise Setup time TCLK to TCE fall Setup	0.158	0.108	0.107				
28	Tceh_rise	time TCLK to TCE fall Setup time TCLK to TCE rise Hold	0.015	0.108	0.107				
30	Tceh_fall	time TCLK to TCE rise Hold TCLK to TCE fall Hold	0.015	0.013	0.013				
31	Trwcs_rise	time CLK to WE rise Setup	0.015	0.013	0.013				
32	Trwcs_fall	time CLK to WE rise Setup time CLK to WE fall Setup	0.102	0.066	0.065				
33	Trwcs_fall Trwch_rise	time CLK to WE rise Hold	0.102	0.006	0.005				
34	Trwch_fall	time CLK to WE fall Hold	0.019	0.021	0.021				
35	Trwcs_rise	time TCLK to TWE rise	0.102	0.021	0.021				
33	i i wcs_rise	Setup time			0.000				
	Table 7: AC Timing Parameters								





36	Trwcs_fall	TCLK to TWE fall Setup time	0.102	0.066	0.065			
37	Trwch_rise	TCLK to TWE rise Hold	0.019	0.021	0.021			
38	Trwch_fall	TCLK to TWE fall Hold time	0.019	0.021	0.021			
39	Tbyms_rise	CLK to BWM rise Setup	0.020	0.011	0.011			
40	Tbyms_fall	CLK to BWM fall Setup	0.020	0.011	0.011			
41	Tbymh_rise	CLK to BWM rise Hold time	0.047	0.042	0.041			
42	Tbymh₋fall	CLK to BWM fall Hold time	0.047	0.042	0.041			
43	Tbyms_rise	TCLK to TBWM rise Setup time	0.020	0.011	0.011			
44	Tbyms_fall	TCLK to TBWM fall Setup time	0.020	0.011	0.011			
45	Tbymh_rise	TCLK to TBWM rise Hold time	0.047	0.042	0.041			
46	Tbymh_fall	TCLK to TBWM fall Hold time	0.047	0.042	0.041			
47	Tacs_rise	CLK to A rise Setup	0.081	0.062	0.061			
48	Tacs_fall	CLK to A fall Setup time	0.081	0.062	0.061			
49	Tach_rise	CLK to A rise Hold time	0.022	0.020	0.020			
50	Tach_fall	CLK to A fall Hold time	0.022	0.020	0.020			
51	Tacs_rise	TCLK to TA rise Setup time	0.081	0.062	0.061			
52	Tacs_fall	TCLK to TA fall Setup time	0.081	0.062	0.061			
53	Tach_rise	TCLK to TA rise Hold time	0.022	0.020	0.020			
54	Tach_fall	TCLK to TA fall Hold time	0.022	0.020	0.020			
55 56	Tdcs_rise Tdcs_fall	CLK to D rise Setup time CLK to D fall Setup	0.001	0.001	0.001			
57	Tdcs_rail Tdch_rise	time CLK to D rise Hold time	0.001	0.001	0.001			
	Tdch_fall		0.047	0.042	0.041			
58 59	Tdcs_rise	CLK to D fall Hold time TCLK to TD rise Setup	0.047	0.042	0.041			
60	Tdcs_fall	time TCLK to TD fall Setup	0.001	0.001	0.001			
61	Tdch rise	time TCLK to TD rise Hold	0.047	0.042	0.041			
62	Tdch_fall	time TCLK to TD fall Hold	0.047	0.042	0.041			
63	Tcqh	time CLK to Q rise Delay	0.654	0.374	0.371			
64	Tcql	CLK to Q fise Delay	0.684	0.392	0.392			
65	Tcqxh	CLK to Q rise Retain	0.548	0.313	0.311			
66	TcqxI	CLK to Q fall Retain	0.548	0.313	0.311			
67	Tcqh	D to Q rise Delay	0.654	0.374	0.371			
68	Tcql	D to Q fall Delay	0.684	0.392	0.392			
69	Tcqxh	D to Q rise Retain	0.548	0.313	0.311			
70	Tcqxl	D to Q fall Retain	0.548	0.313	0.311			
71	Tcqh	TD to Q rise Delay	0.654	0.374	0.371			
72	Tcql	TD to Q fall Delay	0.684	0.392	0.392			
73	Tcqxh	TD to Q rise Retain	0.548	0.313	0.311			
74	Tcqxl	TD to Q fall Retain	0.548	0.313	0.311			
75	Tcqh	TCLK to Q rise Delay	0.654	0.374	0.371			
76	Tcql	TCLK to Q fall Delay	0.684	0.392	0.392			
77	Tcqxh	TCLK to Q rise Retain	0.548	0.313	0.311			
78	Tcqxl	TCLK to Q fall Retain	0.548	0.313	0.311			
79	Trmcs_rise	CLK to RM rise Setup time	0.163	0.123	0.123			
80	Trmcs_fall	CLK to RM fall Setup time	0.163	0.123	0.123			
	Table 7: AC Timing Parameters							

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81	Trmch_rise	CLK to RM rise Hold	0.723	0.415	0.415
01	TTTTCT_TISC	time	0.725	0.415	0.415
82	Trmch_fall	CLK to RM fall Hold time	0.723	0.415	0.415
83	Trmcs_rise	TCLK to RM rise Setup time	0.163	0.123	0.123
84	Trmcs_fall	TCLK to RM fall Setup	0.163	0.123	0.123
85	Trmch_rise	TCLK to RM rise Hold	0.723	0.415	0.415
86	Trmch_fall	TCLK to RM fall Hold time	0.723	0.415	0.415
87	Twmcs_rise	CLK to WM rise Setup	0.163	0.123	0.123
88	Twmcs_fall	CLK to WM fall Setup	0.163	0.123	0.123
89	Twmch_rise	CLK to WM rise Hold time	0.723	0.415	0.415
90	Twmch_fall	CLK to WM fall Hold	0.723	0.415	0.415
91	Twmcs_rise	TCLK to WM rise Setup	0.163	0.123	0.123
92	Twmcs_fall	TCLK to WM fall Setup	0.163	0.123	0.123
93	Twmch₋rise	TCLK to WM rise Hold	0.723	0.415	0.415
94	Twmch_fall	time TCLK to WM fall Hold	0.723	0.415	0.415
95	Tracs_rise	time CLK to RA rise Setup	0.163	0.123	0.123
96	Tracs_fall	time CLK to RA fall Setup	0.163	0.123	0.123
97	Trach_rise	time CLK to RA rise Hold	0.723	0.415	0.415
98	Trach_fall	time CLK to RA fall Hold	0.723	0.415	0.415
99	Tracs_rise	TCLK to RA rise Setup	0.163	0.123	0.123
100	Tracs_fall	time TCLK to RA fall Setup time	0.163	0.123	0.123
101	Trach_rise	TCLK to RA rise Hold time	0.723	0.415	0.415
102	Trach_fall	TCLK to RA fall Hold time	0.723	0.415	0.415
103	Tlvcs₋rise	CLK to LVTEST rise	0.163	0.123	0.123
104	Tlvcs_fall	Setup time CLK to LVTEST fall Setup time	0.163	0.123	0.123
105	Tlvch₋rise	CLK to LVTEST rise Hold time	0.723	0.415	0.415
106	Tlvch_fall	CLK to LVTEST fall Hold time	0.723	0.415	0.415
107	Tlvcs_rise	TCLK to LVTEST rise Setup time	0.163	0.123	0.123
108	Tlvcs_fall	TCLK to LVTEST fall Setup time	0.163	0.123	0.123
109	Tlvch_rise	TCLK to LVTEST rise Hold time	0.723	0.415	0.415
110	Tlvch₋fall	TCLK to LVTEST fall Hold time	0.723	0.415	0.415
111	Tszrch	CLK to SZ rise Setup	0.325	0.247	0.245
112	Tszrcl	CLK to SZ fall Setup	0.325	0.247	0.245
113	Tszrmh	CLK to SZ rise Hold	0.723	0.415	0.415
114	Tszrml	time CLK to SZ fall Hold	9.309	7.450	7.430
115	Tszrch	TCLK to SZ rise Setup	0.325	0.247	0.245
		Table 7: AC T	 iming Parameters		

Table 7: AC Timing Parameters



116	Tszrcl	TCLK to SZ fall Setup	0.325	0.247	0.245
		time			
117	Tszrmh	TCLK to SZ rise Hold time	0.723	0.415	0.415
118	Tszrml	TCLK to SZ fall Hold time	9.309	7.450	7.430
119	Tslrch	CLK to SL rise Setup	0.325	0.247	0.245
120	Tslrcl	CLK to SL fall Setup time	0.325	0.247	0.245
121	Tslrmh	CLK to SL rise Hold time	0.723	0.415	0.415
122	Tslrml	CLK to SL fall Hold time	9.309	7.450	7.430
123	Tslrch	TCLK to SL rise Setup time	0.325	0.247	0.245
124	Tslrcl	TCLK to SL fall Setup time	0.325	0.247	0.245
125	Tslrmh	TCLK to SL rise Hold time	0.723	0.415	0.415
126	Tslrml	TCLK to SL fall Hold time	9.309	7.450	7.430
127	Tbiosh	CLK to BADIO rise Setup time	1.343	1.024	1.018
128	Tbiosl	CLK to BADIO fall Setup time	1.343	1.024	1.018
129	Tbiohh	CLK to BADIO rise Hold time	1.343	1.024	1.018
130	Tbiohl	CLK to BADIO fall Hold time	1.343	1.024	1.018
131	Tbiosh	TCLK to BADIO rise Setup time	1.343	1.024	1.018
132	Tbiosl	TCLK to BADIO fall Setup time	1.343	1.024	1.018
133	Tbiohh	TCLK to BADIO rise Hold time	1.343	1.024	1.018
134	Tbiohl	TCLK to BADIO fall Hold time	1.343	1.024	1.018
135	Thnrch	CLK to HN rise Setup time	0.325	0.247	0.245
136	Thnrcl	CLK to HN fall Setup time	0.325	0.247	0.245
137	Thnrmh	CLK to HN rise Hold time	0.723	0.415	0.415
138	Thnrml	CLK to HN fall Hold time	9.309	7.450	7.430
139	Thnrch	TCLK to HN rise Setup time	0.325	0.247	0.245
140	Thnrcl	TCLK to HN fall Setup time	0.325	0.247	0.245
141	Thnrmh	TCLK to HN rise Hold time	0.723	0.415	0.415
142	Thnrml	TCLK to HN fall Hold time	9.309	7.450	7.430
143	Tsdrch	CLK to SD rise Setup time	0.325	0.247	0.245
144	Tsdrcl	CLK to SD fall Setup time	0.325	0.247	0.245
145	Tsdrmh	CLK to SD rise Hold time	0.723	0.415	0.415
146	Tsdrml	CLK to SD fall Hold time	9.309	7.450	7.430
147	Tsdrch	TCLK to SD rise Setup time	0.325	0.247	0.245
148	Tsdrcl	TCLK to SD fall Setup	0.325	0.247	0.245
149	Tsdrmh	TCLK to SD rise Hold time	0.723	0.415	0.415
150	Tsdrml	TCLK to SD fall Hold time	9.309	7.450	7.430
	<u> </u>		iming Parameters	1	1

Table 7: AC Timing Parameters



151	Tvbcs_rise	CLK to VSB100 rise Setup time	0.163	0.123	0.123
152	Tvbcs_fall	CLK to VSB100 fall	0.163	0.123	0.123
		Setup time			
153	Tvbch_rise	CLK to VSB100 rise	0.723	0.415	0.415
154	T. L. L. C. II	Hold time	0.702	0.415	0.415
154	Tvbch_fall	CLK to VSB100 fall Hold time	0.723	0.415	0.415
155	Tvbcs_rise	TCLK to VSB100 rise	0.163	0.123	0.123
100	T T D C D _ I I D C	Setup time	0.100	0.125	0.120
156	Tvbcs_fall	TCLK to VSB100 fall	0.163	0.123	0.123
		Setup time			
157	Tvbch_rise	TCLK to VSB100 rise	0.723	0.415	0.415
158	Tvbch_fall	Hold time TCLK to VSB100 fall	0.723	0.415	0.415
130	I VDCII_Iaii	Hold time	0.723	0.415	0.415
159	Tvbcs_rise	CLK to VSB200 rise	0.163	0.123	0.123
		Setup time			
160	Tvbcs_fall	CLK to VSB200 fall	0.163	0.123	0.123
		Setup time			
161	Tvbch_rise	CLK to VSB200 rise	0.723	0.415	0.415
162	Tvbch_fall	Hold time CLK to VSB200 fall	0.723	0.415	0.415
102	I VDCII_IAII	Hold time	0.725	0.415	0.415
163	Tvbcs_rise	TCLK to VSB200 rise	0.163	0.123	0.123
		Setup time			
164	Tvbcs_fall	TCLK to VSB200 fall	0.163	0.123	0.123
		Setup time			
165	Tvbch_rise	TCLK to VSB200 rise	0.723	0.415	0.415
166	Tvbch_fall	Hold time TCLK to VSB200 fall	0.723	0.415	0.415
100	I VDCII_Iaii	Hold time	0.723	0.413	0.413
167	Tvbcs_rise	CLK to VSB300 rise	0.163	0.123	0.123
		Setup time			
168	Tvbcs_fall	CLK to VSB300 fall	0.163	0.123	0.123
160	Tvbch_rise	Setup time	0.723	0.415	0.415
169	i vocii_rise	CLK to VSB300 rise Hold time	0.725	0.415	0.415
170	Tvbch_fall	CLK to VSB300 fall	0.723	0.415	0.415
		Hold time			
171	Tvbcs_rise	TCLK to VSB300 rise	0.163	0.123	0.123
1=-	T 1	Setup time	0.166	0.100	0.100
172	Tvbcs_fall	TCLK to VSB300 fall Setup time	0.163	0.123	0.123
173	Tvbch_rise	TCLK to VSB300 rise	0.723	0.415	0.415
113	I VIJCII_IISC	Hold time	0.120	0.713	0.713
174	Tvbch_fall	TCLK to VSB300 fall	0.723	0.415	0.415
		Hold time			
175	Tvbcs_rise	CLK to VSB400 rise	0.163	0.123	0.123
176	Tubes fell	Setup time CLK to VSB400 fall	0.162	0.102	0.102
176	Tvbcs_fall	Setup time	0.163	0.123	0.123
177	Tvbch_rise	CLK to VSB400 rise	0.723	0.415	0.415
		Hold time			
178	Tvbch_fall	CLK to VSB400 fall	0.723	0.415	0.415
		Hold time	0.155	0.100	0.100
179	Tvbcs_rise	TCLK to VSB400 rise	0.163	0.123	0.123
180	Tvbcs_fall	Setup time TCLK to VSB400 fall	0.163	0.123	0.123
100	I ANC2-IQII	Setup time	0.103	0.123	0.123
181	Tvbch_rise	TCLK to VSB400 rise	0.723	0.415	0.415
		Hold time			
182	Tvbch_fall	TCLK to VSB400 fall	0.723	0.415	0.415
		Hold time	ming Paramotors		

Table 7: AC Timing Parameters

^{*} This table shows values only for the nominal slews and output loads.



#	Parameter(ns)	Description	FF_1p10v_125c	SS_0p90v_n40c	SS_0p90v_n55c
1	Ttens_rise	CLK to BISTE rise	0.134	0.226	0.304
2	Ttens_fall	Setup time CLK to BISTE fall Setup time	0.134	0.226	0.304
3	Ttenh_rise	CLK to BISTE rise Hold time	0.678	1.083	1.095
4	Ttens_fall	CLK to BISTE fall Hold	0.678	1.083	1.095
5	Ttens_rise	TCLK to BISTE rise Setup time	0.134	0.226	0.304
6	Ttens_fall	TCLK to BISTE fall Setup time	0.134	0.226	0.304
7	Ttenh_rise	TCLK to BISTE rise Hold time	0.678	1.083	1.095
8	Ttens_fall	TCLK to BISTE fall Hold time	0.678	1.083	1.095
9	Tbms	CLK to AWT rise Setup time	0.067	0.113	0.152
10	Tbmx	CLK to AWT fall Setup time	0.067	0.113	0.152
11	Tbms	CLK to AWT rise Hold time	0.024	0.026	0.026
12	Tbmx	CLK to AWT fall Hold time	0.024	0.026	0.026
13	Tbms	TCLK to AWT rise Setup time	0.067	0.113	0.152
14	Tbmx	TCLK to AWT fall Setup time	0.067	0.113	0.152
15	Tbms	TCLK to AWT rise Hold time	0.024	0.026	0.026
16	Tbmx	TCLK to AWT fall Hold time	0.024	0.026	0.026
17	Tcc	CLK Cycle Time	0.678	1.083	1.095
18	Tch	CLK Pulse Width High	0.155	0.179	0.177
19	Tcl	CLK Pulse Width Low	0.126	0.228	0.236
20	Тсс	TCLK Cycle Time	0.678	1.083	1.095
21	Tch	TCLK Pulse Width High	0.155	0.179	0.177
22	Tcl	TCLK Pulse Width Low	0.126	0.228	0.236
23	Tces_rise Tces_fall	CLK to CE rise Setup time CLK to CE fall Setup	0.126	0.228	0.236
		time CLK to CE fall Setup time			0.236
25 26	Tceh_rise Tceh_fall	time CLK to CE rise Hold time CLK to CE fall Hold	0.020	0.021	0.017
		time TCLK to CE fall Hold time			
27	Tces_rise Tces_fall	time TCLK to TCE rise Setup TCLK to TCE fall Setup	0.126 0.126	0.228	0.236
29	Tceh_rise	time TCLK to TCE rail Setup TCLK to TCE rise Hold	0.020	0.228	0.230
30	Tceh_fall	time TCLK to TCE rise Hold TCLK to TCE fall Hold	0.020	0.021	0.017
31	Trwcs_rise	time CLK to WE rise Setup	0.020	0.021	0.017
32	Trwcs_fall	time CLK to WE fall Setup	0.081	0.145	0.138
33	Trwcs_ran Trwch_rise	time CLK to WE rise Hold	0.001	0.024	0.026
34	Trwch_fall	time CLK to WE fall Hold	0.024	0.024	0.026
35	Trwcs_rise	time TCLK to TWE rise	0.024	0.024	0.020
36	Trwcs_fall	Setup time TCLK to TWE fall	0.081	0.145	0.138
37	Trwch_rise	Setup time TCLK to TWE rise Hold	0.024	0.024	0.026
		time	iming Parameters	3.021	3.020

Table 8: AC Timing Parameters



38	Trwch_fall	TCLK to TWE fall Hold	0.024	0.024	0.026
39	Tbyms_rise	CLK to BWM rise Setup	0.010	0.027	0.030
40	Tbyms_fall	time CLK to BWM fall Setup	0.010	0.027	0.030
70	i byilis_lali	time	0.010	0.021	0.030
41	Tbymh_rise	CLK to BWM rise Hold	0.048	0.065	0.055
42	Tbymh_fall	CLK to BWM fall Hold time	0.048	0.065	0.055
43	Tbyms_rise	TCLK to TBWM rise	0.010	0.027	0.030
		Setup time			
44	Tbyms_fall	TCLK to TBWM fall Setup time	0.010	0.027	0.030
45	Tbymh_rise	TCLK to TBWM rise Hold time	0.048	0.065	0.055
46	Tbymh_fall	TCLK to TBWM fall Hold time	0.048	0.065	0.055
47	Tacs_rise	CLK to A rise Setup time	0.067	0.113	0.152
48	Tacs_fall	CLK to A fall Setup time	0.067	0.113	0.152
49	Tach_rise	CLK to A rise Hold time	0.024	0.026	0.026
50	Tach_fall	CLK to A fall Hold time	0.024	0.026	0.026
51	Tacs_rise	TCLK to TA rise Setup	0.067	0.113	0.152
52	Tacs_fall	TCLK to TA fall Setup	0.067	0.113	0.152
53	Tach_rise	time TCLK to TA rise Hold	0.024	0.026	0.026
		time			
54	Tach ₋ fall	TCLK to TA fall Hold time	0.024	0.026	0.026
55	Tdcs_rise	CLK to D rise Setup time	0.001	0.001	0.006
56	Tdcs_fall	CLK to D fall Setup time	0.001	0.001	0.006
57	Tdch_rise	CLK to D rise Hold time	0.048	0.065	0.055
58	Tdch_fall	CLK to D fall Hold time	0.048	0.065	0.055
59	Tdcs_rise	TCLK to TD rise Setup time	0.001	0.001	0.006
60	Tdcs_fall	TCLK to TD fall Setup time	0.001	0.001	0.006
61	Tdch₋rise	TCLK to TD rise Hold time	0.048	0.065	0.055
62	Tdch₋fall	TCLK to TD fall Hold time	0.048	0.065	0.055
63	Tcqh	CLK to Q rise Delay	0.527	0.966	0.974
64	Tcql	CLK to Q fall Delay	0.549	1.024	1.035
65	Tcqxh	CLK to Q rise Retain	0.442	0.010	0.816
66				0.810	
	Tcqxl	CLK to Q fall Retain	0.442	0.810	0.816
67	Tcqh	CLK to Q fall Retain D to Q rise Delay	0.442 0.527	0.810 0.966	0.816 0.974
67 68	Tcqh Tcql	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay	0.442 0.527 0.549	0.810 0.966 1.024	0.816 0.974 1.035
67 68 69	Tcqh Tcql Tcqxh	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain	0.442 0.527 0.549 0.442	0.810 0.966 1.024 0.810	0.816 0.974 1.035 0.816
67 68 69 70	Tcqh Tcql Tcqxh Tcqxl	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain	0.442 0.527 0.549 0.442 0.442	0.810 0.966 1.024 0.810 0.810	0.816 0.974 1.035 0.816 0.816
67 68 69 70 71	Tcqh Tcql Tcqxh Tcqxl Tcqh	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain TD to Q rise Delay	0.442 0.527 0.549 0.442 0.442 0.527	0.810 0.966 1.024 0.810 0.810 0.966	0.816 0.974 1.035 0.816 0.816 0.974
67 68 69 70 71 72	Tcqh Tcql Tcqxh Tcqxl Tcqh Tcql	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay	0.442 0.527 0.549 0.442 0.442 0.527 0.549	0.810 0.966 1.024 0.810 0.810 0.966 1.024	0.816 0.974 1.035 0.816 0.816 0.974 1.035
67 68 69 70 71 72 73	Tcqh Tcql Tcqxh Tcqxl Tcqh Tcql Tcqxh	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q rise Retain	0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442	0.810 0.966 1.024 0.810 0.810 0.966 1.024 0.810	0.816 0.974 1.035 0.816 0.816 0.974 1.035 0.816
67 68 69 70 71 72 73 74	Tcqh Tcql Tcqxh Tcqxl Tcqh Tcql Tcqxh	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q rise Retain TD to Q fall Retain	0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442 0.442	0.810 0.966 1.024 0.810 0.810 0.966 1.024 0.810 0.810	0.816 0.974 1.035 0.816 0.816 0.974 1.035 0.816 0.816
67 68 69 70 71 72 73 74 75	Tcqh Tcql Tcqxh Tcqxl Tcqh Tcql Tcqxh Tcqch Tcqch	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Delay TD to Q rise Retain TD to Q rise Retain TD to Q rise Retain TC to Q fall Retain	0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442 0.442 0.527	0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.810 0.810 0.810 0.966	0.816 0.974 1.035 0.816 0.816 0.974 1.035 0.816 0.816 0.816
67 68 69 70 71 72 73 74 75	Tcqh Tcql Tcqxh Tcqxl Tcqh Tcql Tcqxh Tcqch Tcqxh Tcqxl Tcqxl	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Retain TD to Q fall Retain TD to Q rise Retain TD to Q rise Retain TC to Q fall Retain TCLK to Q rise Delay TCLK to Q fall Delay	0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442 0.442 0.527 0.549	0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.810 0.810 0.966 1.024	0.816 0.974 1.035 0.816 0.816 0.974 1.035 0.816 0.816 0.974 1.035
67 68 69 70 71 72 73 74 75 76	Tcqh Tcql Tcqxh Tcqxl Tcqh Tcql Tcqxh Tcqxh Tcqxl Tcqxl Tcqxl Tcqh Tcqh	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q fall Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Retain TD to Q fall Retain TD to Q rise Retain TD to Q rise Retain TCLK to Q rise Delay TCLK to Q fall Delay TCLK to Q fall Delay	0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442	0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.810 0.810 0.810 0.966	0.816 0.974 1.035 0.816 0.816 0.974 1.035 0.816 0.816 0.816
67 68 69 70 71 72 73 74 75	Tcqh Tcql Tcqxh Tcqxl Tcqh Tcql Tcqxh Tcqch Tcqxh Tcqxl Tcqxl	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Retain TD to Q fall Retain TD to Q rise Retain TD to Q rise Retain TC to Q fall Retain TCLK to Q rise Delay TCLK to Q fall Delay	0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442 0.442 0.527 0.549	0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.810 0.810 0.966 1.024 0.966 1.024 0.966	0.816 0.974 1.035 0.816 0.974 1.035 0.816 0.974 1.035 0.816 0.974 1.035 0.816
67 68 69 70 71 72 73 74 75 76 77	Tcqh Tcql Tcqxh Tcqh Tcqh Tcqxh Tcqch Tcqxh Tcqxl Tcqch Tcqh Tcqh Tcql	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q fall Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Retain TD to Q fall Retain TD to Q rise Retain TD to Q rise Retain TCLK to Q rise Delay TCLK to Q fall Delay TCLK to Q fall Delay TCLK to Q rise Retain TCLK to Q rise Retain	0.442 0.527 0.549 0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442 0.527 0.549 0.442	0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.810 0.966 1.024 0.810 0.966 1.024 0.810	0.816 0.974 1.035 0.816 0.974 1.035 0.816 0.974 1.035 0.816 0.974 1.035 0.816 0.974 1.035
67 68 69 70 71 72 73 74 75 76 77 78	Tcqh Tcql Tcqxh Tcqh Tcqh Tcqxh Tcqxh Tcqxl Tcqh Tcqt Tcqt Tcqt Trqxh Trqt Trqxh Trqxh Trqxl Trqxh	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Retain TD to Q fall Retain TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q fall Delay TCLK to Q fall Delay TCLK to Q rise Retain TCLK to R fall Delay TCLK to Q rise Retain TCLK to R fall Retain CLK to R fall Retain CLK to R fall Retain CLK to R fall Setup time	0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442 0.527 0.549 0.442 0.442 0.442 0.134	0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.226	0.816 0.974 1.035 0.816 0.816 0.974 1.035 0.816 0.816 0.974 1.035 0.816 0.974 1.035 0.816 0.974
67 68 69 70 71 72 73 74 75 76 77 78 79	Tcqh Tcql Tcqxh Tcqxl Tcqh Tcqt Tcqxh Tcqxh Tcqxl Tcqt Tcqt Tcqxh Tcqt Tcqxh Tcqxh Tcqxh Tcqxh Tcqxh Tcqxh Tcqxh Tcqxh	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Delay TD to Q fall Retain TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q fall Delay TCLK to Q fall Retain TCLK to RM rise Setup time CLK to RM fall Setup time CLK to RM rise Hold time	0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442 0.42 0.527 0.549 0.442 0.442 0.442 0.442 0.442 0.442 0.442 0.442 0.442 0.443 0.4442 0.1344 0.1344 0.6778	0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.810 0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.226 0.226	0.816 0.974 1.035 0.816 0.816 0.974 1.035 0.816 0.816 0.816 0.974 1.035 0.816 0.974 1.035 0.816 0.974 1.035 0.816
67 68 69 70 71 72 73 74 75 76 77 78 79	Tcqh Tcql Tcqxh Tcqh Tcqh Tcqxh Tcqxh Tcqxl Tcqh Tcqt Tcqt Tcqt Trqxh Trqt Trqxh Trqxh Trqxl Trqxh	CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q fall Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Delay TD to Q fall Retain TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q fall Delay TCLK to Q fall Retain TCLK to RM rise Setup time CLK to RM fall Setup time CLK to RM rise Hold time CLK to RM fall Hold time	0.442 0.527 0.549 0.442 0.442 0.527 0.549 0.442 0.527 0.549 0.442 0.442 0.442 0.134	0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.810 0.966 1.024 0.810 0.966 1.024 0.810 0.226	0.816 0.974 1.035 0.816 0.816 0.974 1.035 0.816 0.816 0.974 1.035 0.816 0.974 1.035 0.816 0.974

Table 8: AC Timing Parameters



83	Trmcs_rise	TCLK to RM rise Setup	0.134	0.226	0.304
84	Trmcs_fall	TCLK to RM fall Setup	0.134	0.226	0.304
85	Trmch_rise	TCLK to RM rise Hold	0.678	1.083	1.095
86	Trmch_fall	TCLK to RM fall Hold time	0.678	1.083	1.095
87	Twmcs₋rise	CLK to WM rise Setup	0.134	0.226	0.304
88	Twmcs_fall	CLK to WM fall Setup	0.134	0.226	0.304
89	Twmch₋rise	time CLK to WM rise Hold time	0.678	1.083	1.095
90	Twmch_fall	CLK to WM fall Hold	0.678	1.083	1.095
91	Twmcs₋rise	time TCLK to WM rise Setup time	0.134	0.226	0.304
92	Twmcs_fall	TCLK to WM fall Setup	0.134	0.226	0.304
93	Twmch_rise	TCLK to WM rise Hold time	0.678	1.083	1.095
94	Twmch ₋ fall	TCLK to WM fall Hold	0.678	1.083	1.095
95	Tracs_rise	CLK to RA rise Setup	0.134	0.226	0.304
96	Tracs_fall	time CLK to RA fall Setup time	0.134	0.226	0.304
97	Trach_rise	CLK to RA rise Hold time	0.678	1.083	1.095
98	Trach_fall	CLK to RA fall Hold time	0.678	1.083	1.095
99	Tracs_rise	TCLK to RA rise Setup	0.134	0.226	0.304
100	Tracs_fall	TCLK to RA fall Setup	0.134	0.226	0.304
101	Trach_rise	TCLK to RA rise Hold time	0.678	1.083	1.095
102	Trach_fall	TCLK to RA fall Hold time	0.678	1.083	1.095
103	Tlvcs₋rise	CLK to LVTEST rise Setup time	0.134	0.226	0.304
104	Tlvcs_fall	CLK to LVTEST fall Setup time	0.134	0.226	0.304
105	Tlvch_rise	CLK to LVTEST rise Hold time	0.678	1.083	1.095
106	Tlvch_fall	CLK to LVTEST fall Hold time	0.678	1.083	1.095
107	Tlvcs₋rise	TCLK to LVTEST rise Setup time	0.134	0.226	0.304
108	Tlvcs_fall	TCLK to LVTEST fall Setup time	0.134	0.226	0.304
109	Tlvch_rise	TCLK to LVTEST rise Hold time	0.678	1.083	1.095
110	Tlvch_fall	TCLK to LVTEST fall Hold time	0.678	1.083	1.095
111	Tszrch	CLK to SZ rise Setup	0.268	0.451	0.607
112	Tszrcl	CLK to SZ fall Setup	0.268	0.451	0.607
113	Tszrmh	CLK to SZ rise Hold time	0.678	1.083	1.095
114	Tszrml	CLK to SZ fall Hold time	7.635	14.254	14.502
115	Tszrch	TCLK to SZ rise Setup	0.268	0.451	0.607
116	Tszrcl	TCLK to SZ fall Setup	0.268	0.451	0.607
117	Tszrmh	TCLK to SZ rise Hold time	0.678	1.083	1.095
			iming Parameters		

Table 8: AC Timing Parameters



118	Tszrml	TCLK to SZ fall Hold time	7.635	14.254	14.502
119	Tslrch	CLK to SL rise Setup	0.268	0.451	0.607
120	Tslrcl	CLK to SL fall Setup	0.268	0.451	0.607
121	Tslrmh	time CLK to SL rise Hold	0.678	1.083	1.095
122	Tslrml	time CLK to SL fall Hold time	7.635	14.254	14.502
123	Tslrch	TCLK to SL rise Setup	0.268	0.451	0.607
124	Tslrcl	TCLK to SL fall Setup	0.268	0.451	0.607
125	Tslrmh	TCLK to SL rise Hold time	0.678	1.083	1.095
126	Tslrml	TCLK to SL fall Hold	7.635	14.254	14.502
127	Tbiosh	CLK to BADIO rise	1.101	1.871	1.868
128	Tbiosl	Setup time CLK to BADIO fall	1.101	1.871	1.868
129	Tbiohh	Setup time CLK to BADIO rise Hold time	1.101	1.871	1.868
130	Tbiohl	CLK to BADIO fall Hold time	1.101	1.871	1.868
131	Tbiosh	TCLK to BADIO rise Setup time	1.101	1.871	1.868
132	Tbiosl	TCLK to BADIO fall Setup time	1.101	1.871	1.868
133	Tbiohh	TCLK to BADIO rise Hold time	1.101	1.871	1.868
134	Tbiohl	TCLK to BADIO fall Hold time	1.101	1.871	1.868
135	Thnrch	CLK to HN rise Setup	0.268	0.451	0.607
136	Thnrcl	CLK to HN fall Setup	0.268	0.451	0.607
137	Thnrmh	CLK to HN rise Hold	0.678	1.083	1.095
138	Thnrml	CLK to HN fall Hold time	7.635	14.254	14.502
139	Thnrch	TCLK to HN rise Setup	0.268	0.451	0.607
140	Thnrcl	TCLK to HN fall Setup	0.268	0.451	0.607
141	Thnrmh	TCLK to HN rise Hold time	0.678	1.083	1.095
142	Thnrml	TCLK to HN fall Hold time	7.635	14.254	14.502
143	Tsdrch	CLK to SD rise Setup time	0.268	0.451	0.607
144	Tsdrcl	CLK to SD fall Setup time	0.268	0.451	0.607
145	Tsdrmh	CLK to SD rise Hold time	0.678	1.083	1.095
146	Tsdrml	CLK to SD fall Hold time	7.635	14.254	14.502
147	Tsdrch	TCLK to SD rise Setup time	0.268	0.451	0.607
148	Tsdrcl	TCLK to SD fall Setup time	0.268	0.451	0.607
149	Tsdrmh	TCLK to SD rise Hold time	0.678	1.083	1.095
150	Tsdrml	TCLK to SD fall Hold time	7.635	14.254	14.502
151	Tvbcs₋rise	CLK to VSB100 rise Setup time	0.134	0.226	0.304
152	Tvbcs_fall	CLK to VSB100 fall Setup time	0.134	0.226	0.304
		Table O. AC T	iming Parameters		

Table 8: AC Timing Parameters



153	Tvbch_rise	CLK to VSB100 rise	0.678	1.083	1.095
100	T T D C II _ I I D C	Hold time	0.070	1.000	1.030
154	Tvbch_fall	CLK to VSB100 fall	0.678	1.083	1.095
		Hold time			
155	Tvbcs_rise	TCLK to VSB100 rise	0.134	0.226	0.304
156	T. C.	Setup time	0.104	0.006	0.004
156	Tvbcs_fall	TCLK to VSB100 fall Setup time	0.134	0.226	0.304
157	Tvbch_rise	TCLK to VSB100 rise	0.678	1.083	1.095
157	I VIDCII_IISE	Hold time	0.070	1.005	1.095
158	Tvbch_fall	TCLK to VSB100 fall	0.678	1.083	1.095
		Hold time			
159	Tvbcs_rise	CLK to VSB200 rise	0.134	0.226	0.304
1.00		Setup time	0.101	0.006	0.004
160	Tvbcs_fall	CLK to VSB200 fall	0.134	0.226	0.304
161	Tvbch_rise	Setup time CLK to VSB200 rise	0.678	1.083	1.095
101	I VIJCII_IISE	Hold time	0.070	1.005	1.093
162	Tvbch_fall	CLK to VSB200 fall	0.678	1.083	1.095
		Hold time			
163	Tvbcs_rise	TCLK to VSB200 rise	0.134	0.226	0.304
155	T 1 6 "	Setup time	0.104	0.006	0.004
164	Tvbcs_fall	TCLK to VSB200 fall	0.134	0.226	0.304
165	Tvbch_rise	Setup time TCLK to VSB200 rise	0.678	1.083	1.095
103	I VIDCII_IISC	Hold time	0.070	1.005	1.095
166	Tvbch_fall	TCLK to VSB200 fall	0.678	1.083	1.095
		Hold time			
167	Tvbcs_rise	CLK to VSB300 rise	0.134	0.226	0.304
1.50	—	Setup time	0.101	0.006	0.004
168	Tvbcs_fall	CLK to VSB300 fall Setup time	0.134	0.226	0.304
169	Tvbch_rise	CLK to VSB300 rise	0.678	1.083	1.095
100		Hold time	0.070	2.000	1.030
170	Tvbch_fall	CLK to VSB300 fall	0.678	1.083	1.095
		Hold time			
171	Tvbcs_rise	TCLK to VSB300 rise	0.134	0.226	0.304
172	Tvbcs_fall	Setup time TCLK to VSB300 fall	0.134	0.226	0.304
112	I ADC2TI	Setup time	0.134	0.220	0.304
173	Tvbch_rise	TCLK to VSB300 rise	0.678	1.083	1.095
		Hold time			
174	Tvbch_fall	TCLK to VSB300 fall	0.678	1.083	1.095
1	-	Hold time	0.104	0.006	0.004
175	Tvbcs_rise	CLK to VSB400 rise	0.134	0.226	0.304
176	Tvbcs_fall	Setup time CLK to VSB400 fall	0.134	0.226	0.304
		Setup time			
177	Tvbch_rise	CLK to VSB400 rise	0.678	1.083	1.095
		Hold time			
178	Tvbch_fall	CLK to VSB400 fall	0.678	1.083	1.095
179	Tvbcs_rise	Hold time TCLK to VSB400 rise	0.134	0.226	0.304
119	I VDCS_FISE	Setup time	0.134	0.220	0.304
180	Tvbcs_fall	TCLK to VSB400 fall	0.134	0.226	0.304
-55		Setup time			
181	Tvbch_rise	TCLK to VSB400 rise	0.678	1.083	1.095
		Hold time			
182	Tvbch_fall	TCLK to VSB400 fall	0.678	1.083	1.095
		Hold time	iming Parameters		

Table 8: AC Timing Parameters



^{*} This table shows values only for the nominal slews and output loads.

#	Parameter(ns)	Description	SS_0p90v_125c
1	Ttens_rise	CLK to BISTE rise	0.238
		Setup time	
2	Ttens_fall	CLK to BISTE fall Setup time	0.238
3	Ttenh_rise	CLK to BISTE rise Hold time	1.143
4	Ttens_fall	CLK to BISTE fall Hold	1.143
		time	0.000
5	Ttens_rise	TCLK to BISTE rise Setup time	0.238
6	Ttens_fall	TCLK to BISTE fall Setup time	0.238
7	Ttenh_rise	TCLK to BISTE rise	1.143
8	Ttens_fall	Hold time TCLK to BISTE fall	1.143
		Hold time	0.110
9	Tbms	CLK to AWT rise Setup time	0.119
10	Tbmx	CLK to AWT fall Setup	0.119
11	Tbms	CLK to AWT rise Hold	0.032
12	Tbmx	time CLK to AWT fall Hold	0.032
		time	
13	Tbms	TCLK to AWT rise Setup time	0.119
14	Tbmx	TCLK to AWT fall Setup time	0.119
15	Tbms	TCLK to AWT rise Hold	0.032
16	Tbmx	time TCLK to AWT fall Hold	0.032
		time	
17	Тсс	CLK Cycle Time	1.143
18	Tch	CLK Pulse Width High	0.182
19	Tcl	CLK Pulse Width Low	0.235
20	Тсс	TCLK Cycle Time	1.143
21	Tch	TCLK Pulse Width High	0.182
22	Tcl	TCLK Pulse Width Low	0.235
23	Tces₋rise	CLK to CE rise Setup time	0.235
24	Tces_fall	CLK to CE fall Setup	0.235
25	Tceh_rise	CLK to CE rise Hold	0.023
26	Tceh_fall	time CLK to CE fall Hold	0.023
		time	
27	Tces₋rise	TCLK to TCE rise Setup time	0.235
28	Tces_fall	TCLK to TCE fall Setup	0.235
29	Tceh_rise	TCLK to TCE rise Hold	0.023
30	Tceh_fall	time TCLK to TCE fall Hold	0.023
	Trwcs_rise	time CLK to WE rise Setup	0.149
31		time	
32	Trwcs_fall	CLK to WE fall Setup	0.149
33	Trwch_rise	CLK to WE rise Hold	0.028
34	Trwch_fall	time CLK to WE fall Hold	0.028
35	Trwcs_rise	time TCLK to TWE rise	0.149
33	i i wcs_tise	Setup time	0.149
36	Trwcs_fall	TCLK to TWE fall	0.149
37	Trwch_rise	Setup time TCLK to TWE rise Hold	0.028
		time	
	Tabla	9: AC Timing Parameters	

Table 9: AC Timing Parameters



38	Trwch_fall	TCLK to TWE fall Hold	0.028
39	Tbyms_rise	CLK to BWM rise Setup	0.029
		time	
40	Tbyms_fall	CLK to BWM fall Setup	0.029
		time	
41	Tbymh_rise	CLK to BWM rise Hold	0.070
		time	
42	Tbymh ₋ fall	CLK to BWM fall Hold	0.070
43	Tbyms_rise	time TCLK to TBWM rise	0.029
73	I byilis_lise	Setup time	0.029
44	Tbyms_fall	TCLK to TBWM fall	0.029
		Setup time	
45	Tbymh_rise	TCLK to TBWM rise	0.070
46	T	Hold time TCLK to TBWM fall	0.070
46	Tbymh_fall	Hold time	0.070
47	Tacs_rise	CLK to A rise Setup	0.119
		time	· •
48	Tacs_fall	CLK to A fall Setup time	0.119
49	Tach_rise	CLK to A rise Hold time	0.032
50	Tach_fall	CLK to A fall Hold time	0.032
51	Tacs_rise	TCLK to TA rise Setup	0.119
52	Tacs_fall	time TCLK to TA fall Setup	0.119
52	I dC5_IdII	time	0.119
53	Tach_rise	TCLK to TA rise Hold	0.032
		time	
54	Tach ₋ fall	TCLK to TA fall Hold	0.032
		time	
55	Tdcs_rise	CLK to D rise Setup	0.001
-	T	time CLK to D fall Setup	0.001
- hh			
56	Tdcs₋fall	time	0.001
57	Tdch_rise		0.070
		time	
57	Tdch_rise	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup	0.070
57 58 59	Tdch_rise Tdch_fall Tdcs_rise	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time	0.070 0.070 0.001
57 58	Tdch_rise Tdch_fall	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup	0.070 0.070
57 58 59	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time	0.070 0.070 0.001 0.001
57 58 59 60	Tdch_rise Tdch_fall Tdcs_rise	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup	0.070 0.070 0.001
57 58 59 60	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD fall Setup time TCLK to TD rise Hold	0.070 0.070 0.001 0.001
57 58 59 60 61	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time	0.070 0.070 0.001 0.001 0.070
57 58 59 60 61 62	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay	0.070 0.070 0.001 0.001 0.070 0.070
57 58 59 60 61 62 63 64	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080
57 58 59 60 61 62 63 64 65	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865
57 58 59 60 61 62 63 64 65 66	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcql Tcqxh Tcqxl	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Retain	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865
57 58 59 60 61 62 63 64 65 66 67	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcql Tcqxh Tcqxl Tcqh	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q rise Delay CLK to Q fall Retain D to Q rise Delay	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865 1.032
57 58 59 60 61 62 63 64 65 66	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcql Tcqxh Tcqxl	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Retain	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865
57 58 59 60 61 62 63 64 65 66 67 68	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcql Tcqxh Tcqxl Tcqh Tcqt	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q rise Delay D to Q rise Delay	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865 1.032 1.080
57 58 59 60 61 62 63 64 65 66 67 68 69 70	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcql Tcqxh Tcqxl Tcqt Tcqxh Tcqt Tcqxh Tcqt Tcqt	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay D to Q rise Delay D to Q fall Delay D to Q rise Retain D to Q rise Retain D to Q rise Retain	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcql Tcqxh Tcqxl Tcqt Tcqxh Tcql Tcqxh Tcql Tcqch Tcqcl Tcqch Tcqcl Tcqch Tcqcl Tcqcd Tcqcl Tcqcd Tcqcl Tcqxcl Tcqcd Tcqxcl Tcqcd	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Retain D to Q rise Retain TD to Q rise Delay TD to Q fall Retain	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcqxh Tcqxl Tcqh Tcqt Tcqxh Tcqt Tcqt Tcqxh Tcqt Tcqxh Tcqt Tcqxh Tcqt Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Retain D to Q rise Retain D to Q rise Retain D to Q rise Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Delay TD to Q rise Retain	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 1.032 1.080 0.865 0.865 1.032 1.080 0.865 1.032 1.080 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcqxh Tcqxl Tcqxh Tcqt Tcqxh Tcqt Tcqxh Tcqt Tcqxh Tcqt Tcqxh Tcqt Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay D to Q rise Delay D to Q rise Retain D to Q rise Retain D to Q rise Delay TD to Q fall Delay TD to Q fall Delay TD to Q fall Delay	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865 1.032 1.080 0.865 1.032 1.080 0.865 0.865 1.032 1.080 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcqxh Tcqxl Tcqxh Tcqtl Tcqxh Tcqtl Tcqxh Tcqtl Tcqxh Tcqtl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay D to Q fall Delay D to Q rise Retain D to Q rise Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Delay TD to Q fall Retain TD to Q rise Retain TD to Q rise Retain TD to Q rise Retain TD to Q fall Retain TD to Q fall Retain	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865 1.032 1.080 0.865 1.032 1.080 0.865 0.865 1.032 1.080 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqcl Tcqcl Tcqxh Tcqcl Tcqcl Tcqcl Tcqxh	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q rise Retain D to Q rise Retain D to Q rise Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Delay TD to Q fall Retain TD to Q rise Retain	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcqxh Tcqxl	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay D to Q fall Delay D to Q rise Retain D to Q rise Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Retain TD to Q rise Retain TD to Q rise Retain TD to Q rise Retain TD to Q fall Retain TD to Q rise Retain TD to Q fall Retain TD to Q fall Retain TD to Q rise Retain TD to Q fall Retain TD to Q fall Retain TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q rise Retain	0.070 0.070 0.001 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqcl Tcqcl Tcqxh Tcqcl Tcqcl Tcqcl Tcqxh	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay CLK to Q fall Retain D to Q rise Delay D to Q fall Retain TD to Q rise Delay TD to Q fall Retain TCLK to Q rise Retain TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q rise Retain TCLK to Q rise Retain TCLK to Q rise Retain	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqtl Tcqxh Tcqtl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay D to Q fall Delay D to Q rise Retain D to Q rise Retain TD to Q rise Delay TD to Q fall Delay TD to Q fall Retain TD to Q rise Retain TD to Q rise Retain TD to Q rise Retain TD to Q fall Retain TD to Q rise Retain TD to Q fall Retain TD to Q fall Retain TD to Q rise Retain TD to Q fall Retain TD to Q fall Retain TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q rise Delay TCLK to Q rise Retain	0.070 0.070 0.001 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqh Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqtl Tcqxh Tcqtl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqcl Tcqxh Tcqxl Tcqxh Tcqxl Tcqxh Tcqxl	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Delay D to Q fall Delay D to Q fall Retain D to Q rise Delay TD to Q fall Retain TD to Q rise Retain TD to Q fall Delay TD to Q fall Delay TD to Q fall Delay TD to Q fall Retain TD to Q fall Retain TCLK to Q rise Retain TCLK to Q fall Retain TCLK to Q fall Retain	0.070 0.070 0.001 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q rise Retain CLK to Q fall Retain D to Q rise Retain D to Q rise Retain D to Q rise Retain TD to Q rise Delay TD to Q fall Retain TD to Q rise Retain TCLK to Q rise Retain CLK to RM rise Setup time CLK to RM fall Setup time	0.070 0.070 0.001 0.001 0.001 0.070 0.070 0.070 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 0.865 1.032 1.080 0.865 0.865 0.865 1.032 1.080 0.865 0.865 0.865 0.865 0.865 0.865 0.865 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcqt Tcqxh Tcqxh Tcqxl	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q fall Delay TD to Q rise Retain TD to Q rise Delay TD to Q rise Delay TD to Q rise Retain TCLK to RM rise Setup time CLK to RM rise Setup time CLK to RM fall Setup time CLK to RM rise Hold	0.070 0.070 0.001 0.001 0.001 0.070 0.070 1.032 1.080 0.865 0.865 1.032 1.080 0.865 0.865 1.032 1.080 0.865 0.865 1.032 1.080 0.865 0.865 0.865 0.865 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcql Tcqxh Tcql Tcqxh Tcql Tcqxh Tcql Tcqxh Trql Trqxl Trmcs_rise	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q fall Delay TD to Q rise Retain TD to Q rise Delay TD to Q fall Retain TD to Q rise Retain TD to Q rise Retain TD to Q rise Retain TCLK to RM rise Setup time CLK to RM rise Hold time	0.070 0.070 0.001 0.001 0.070 0.070 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 0.865 1.032 1.080 0.865 0.865 0.865 0.865 1.032 1.080 0.865 0.865 0.865 0.865 0.865
57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79	Tdch_rise Tdch_fall Tdcs_rise Tdcs_fall Tdcs_fall Tdch_rise Tdch_fall Tcqh Tcql Tcqxh Tcqxl	time CLK to D rise Hold time CLK to D fall Hold time TCLK to TD rise Setup time TCLK to TD fall Setup time TCLK to TD rise Hold time TCLK to TD fall Hold time CLK to Q rise Delay CLK to Q fall Delay CLK to Q fall Retain D to Q rise Delay D to Q fall Delay D to Q fall Delay TD to Q rise Retain TD to Q rise Delay TD to Q rise Delay TD to Q rise Retain TCLK to RM rise Setup time CLK to RM rise Setup time CLK to RM fall Setup time CLK to RM rise Hold	0.070 0.070 0.001 0.001 0.001 0.070 0.070 0.070 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 1.032 1.080 0.865 0.865 1.032 1.080 0.865 0.865 0.865 1.032 1.080 0.865 0.865 0.865 0.865 0.865 0.865 0.865 0.865

Table 9: AC Timing Parameters



83	Trmcs_rise	TCLK to RM rise Setup	0.238
84	Trmcs_fall	TCLK to RM fall Setup	0.238
85	Trmch_rise	TCLK to RM rise Hold time	1.143
86	Trmch_fall	TCLK to RM fall Hold time	1.143
87	Twmcs₋rise	CLK to WM rise Setup	0.238
88	Twmcs_fall	CLK to WM fall Setup	0.238
89	Twmch₋rise	CLK to WM rise Hold	1.143
90	Twmch_fall	CLK to WM fall Hold time	1.143
91	Twmcs_rise	TCLK to WM rise Setup	0.238
92	Twmcs_fall	TCLK to WM fall Setup	0.238
93	Twmch₋rise	TCLK to WM rise Hold	1.143
94	Twmch_fall	TCLK to WM fall Hold time	1.143
95	Tracs_rise	CLK to RA rise Setup	0.238
96	Tracs_fall	CLK to RA fall Setup	0.238
97	Trach_rise	CLK to RA rise Hold time	1.143
98	Trach_fall	CLK to RA fall Hold time	1.143
99	Tracs_rise	TCLK to RA rise Setup	0.238
100	Tracs_fall	TCLK to RA fall Setup	0.238
101	Trach_rise	TCLK to RA rise Hold time	1.143
102	Trach_fall	TCLK to RA fall Hold time	1.143
103	Tlvcs₋rise	CLK to LVTEST rise Setup time	0.238
104	Tlvcs_fall	CLK to LVTEST fall Setup time	0.238
105	Tlvch₋rise	CLK to LVTEST rise Hold time	1.143
106	Tlvch_fall	CLK to LVTEST fall Hold time	1.143
107	Tlvcs₋rise	TCLK to LVTEST rise Setup time	0.238
108	Tlvcs_fall	TCLK to LVTEST fall Setup time	0.238
109	Tlvch₋rise	TCLK to LVTEST rise Hold time	1.143
110	Tlvch₋fall	TCLK to LVTEST fall Hold time	1.143
111	Tszrch	CLK to SZ rise Setup time	0.476
112	Tszrcl	CLK to SZ fall Setup time	0.476
113	Tszrmh	CLK to SZ rise Hold time	1.143
114	Tszrml	CLK to SZ fall Hold time	14.427
115	Tszrch	TCLK to SZ rise Setup time	0.476
116	Tszrcl	TCLK to SZ fall Setup time	0.476
117	Tszrmh	TCLK to SZ rise Hold time 9: AC Timing Parameters	1.143

Table 9: AC Timing Parameters



118	Tszrml	TCLK to SZ fall Hold time	14.427
119	Tslrch	CLK to SL rise Setup	0.476
		time	
120	Tslrcl	CLK to SL fall Setup	0.476
121	Tslrmh	CLK to SL rise Hold	1.143
		time	
122	Tslrml	CLK to SL fall Hold time	14.427
123	Tslrch	TCLK to SL rise Setup time	0.476
124	Tslrcl	TCLK to SL fall Setup	0.476
		time	
125	Tslrmh	TCLK to SL rise Hold time	1.143
126	Tslrml	TCLK to SL fall Hold	14.427
107		time	2.010
127	Tbiosh	CLK to BADIO rise Setup time	2.013
128	Tbiosl	CLK to BADIO fall	2.013
	 -	Setup time	
129	Tbiohh	CLK to BADIO rise	2.013
		Hold time	
130	Tbiohl	CLK to BADIO fall Hold	2.013
		time	
131	Tbiosh	TCLK to BADIO rise Setup time	2.013
132	Tbiosl	TCLK to BADIO fall	2.013
132	1 5.031	Setup time	010
133	Tbiohh	TCLK to BADIO rise	2.013
		Hold time	
134	Tbiohl	TCLK to BADIO fall	2.013
		Hold time	
135	Thnrch	CLK to HN rise Setup	0.476
		time	
136	Thnrcl	CLK to HN fall Setup	0.476
	-	time	
137	Thnrmh	CLK to HN rise Hold	1.143
		time	
138	Thnrml	CLK to HN fall Hold	14.427
		time	
139	Thnrch	TCLK to HN rise Setup	0.476
		time	
140	Thnrcl	TCLK to HN fall Setup	0.476
		time	
141	Thnrmh	TCLK to HN rise Hold	1.143
		time	
142	Thnrml	TCLK to HN fall Hold time	14.427
143	Tsdrch	CLK to SD rise Setup	0.476
143	i surcii	time	0.470
144	Tsdrcl	CLK to SD fall Setup	0.476
144	i Surci	time	0.470
145	Tsdrmh	CLK to SD rise Hold	1.143
1.5		time	
146	Tsdrml	CLK to SD fall Hold	14.427
		time	
147	Tsdrch	TCLK to SD rise Setup	0.476
		time	
148	Tsdrcl	TCLK to SD fall Setup	0.476
140	Tada. I	time	1 142
149	Tsdrmh	TCLK to SD rise Hold	1.143
150	Tsdrml	time TCLK to SD fall Hold	14.427
130	i surmi		14.421
161	Tubes :::e-	time	0.220
151	Tvbcs_rise	CLK to VSB100 rise Setup time	0.238
152	Tvbcs_fall	CLK to VSB100 fall	0.238
		Setup time	
	T-1-1-	9: AC Timing Parameters	<u> </u>

Table 9: AC Timing Parameters



153	Tvbch_rise	CLK to VSB100 rise Hold time	1.143
154	Tvbch_fall	CLK to VSB100 fall Hold time	1.143
155	Tvbcs_rise	TCLK to VSB100 rise	0.238
156	Tvbcs_fall	Setup time TCLK to VSB100 fall	0.238
157	Tvbch_rise	Setup time TCLK to VSB100 rise	1.143
158	Tvbch_fall	Hold time TCLK to VSB100 fall Hold time	1.143
159	Tvbcs₋rise	CLK to VSB200 rise	0.238
160	Tvbcs_fall	Setup time CLK to VSB200 fall Setup time	0.238
161	Tvbch_rise	CLK to VSB200 rise Hold time	1.143
162	Tvbch_fall	CLK to VSB200 fall Hold time	1.143
163	Tvbcs_rise	TCLK to VSB200 rise Setup time	0.238
164	Tvbcs_fall	TCLK to VSB200 fall Setup time	0.238
165	Tvbch_rise	TCLK to VSB200 rise Hold time	1.143
166	Tvbch_fall	TCLK to VSB200 fall Hold time	1.143
167	Tvbcs_rise	CLK to VSB300 rise Setup time	0.238
168	Tvbcs_fall	CLK to VSB300 fall Setup time	0.238
169	Tvbch_rise	CLK to VSB300 rise Hold time	1.143
170	Tvbch_fall	CLK to VSB300 fall Hold time	1.143
171	Tvbcs_rise	TCLK to VSB300 rise Setup time	0.238
172	Tvbcs_fall	TCLK to VSB300 fall Setup time	0.238
173	Tvbch_rise	TCLK to VSB300 rise Hold time	1.143
174	Tvbch_fall	TCLK to VSB300 fall Hold time	1.143
175	Tvbcs₋rise	CLK to VSB400 rise Setup time	0.238
176	Tvbcs_fall	CLK to VSB400 fall Setup time	0.238
177	Tvbch_rise	CLK to VSB400 rise Hold time	1.143
178	Tvbch_fall	CLK to VSB400 fall Hold time	1.143
179	Tvbcs_rise	TCLK to VSB400 rise Setup time	0.238
180	Tvbcs_fall	TCLK to VSB400 fall Setup time	0.238
181	Tvbch_rise	TCLK to VSB400 rise Hold time	1.143
182	Tvbch_fall	TCLK to VSB400 fall Hold time 9: AC Timing Parameters	1.143

Table 9: AC Timing Parameters



^{*} This table shows values only for the nominal slews and output loads.

Leakage and Power

#	Parameter	Description	TT_1p00v_25c	FF_1p10v_n40c	FF_1p10v_n55c
1	sl_leak(uW)	Leakage Power::slumber	2309.	5161.	3891.
2	sz_leak(uW)	Leakage Power::snooze	2340.	4549.	3187.
3	hn_leak(uW)	Leakage Power::hibernate	1990.	4268.	3080.
4	sd_leak(uW)	Leakage Power::shutdown	1829.	4007.	2918.
5	static_leak(uW)	Leakage Power::standby	2728.	5448.	4048.
6	Power_WE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1921	0.1110	0.1110
7	Power_WE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1975	0.1126	0.1126
8	Power_TWE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1921	0.1110	0.1110
9	Power_TWE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1975	0.1126	0.1126
10	Power_A_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1921	0.1110	0.1110
11	Power_A_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1921	0.1110	0.1110
12	Power_TA_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1921	0.1110	0.1110
13	Power_TA_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1921	0.1110	0.1110
14	Power_WE_r::chip_en(uW/MHZ)	Pin Power Rise	3.824	1.923	1.923
15	Power_WE_f::chip_en(uW/MHZ)	Pin Power Fall	4.024	1.954	1.954
16	Power_TWE_r::chip_en(uW/MHZ)	Pin Power Rise	3.824	1.923	1.923
17	Power_TWE_f::chip_en(uW/MHZ)	Pin Power Fall	4.024	1.954	1.954
18	Power_A_r::chip_en(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
19	Power_A_f::chip_en(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
20	Power_TA_r::chip_en(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
21	Power_TA_f::chip_en(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
22	Pread(uW/MHZ)	Read Power Rise	8.473	10.01	10.01
23	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
24	Pwrite(uW/MHZ)	Write Power Rise	10.91	10.16	10.16
25	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
26	Power_CLK_r(uW/MHZ)	Pin Power Rise	2.880	1.531	1.531
27	Power_CLK_f(uW/MHZ)	Pin Power Fall	2.809	1.541	1.541
28	Pread(uW/MHZ)	Read Power Rise	8.473	10.01	10.01
29	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
30	Pwrite(uW/MHZ)	Write Power Rise	10.91	10.16	10.16
31	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
32	Power_TCLK_r(uW/MHZ)	Pin Power Rise	2.880	1.531	1.531
33	Power_TCLK_f(uW/MHZ)	Pin Power Fall	2.809	1.541	1.541
34	$Power_SZ_r(uW/MHZ)$	Pin Power Rise	0.5552	0.3129	0.3129
35	Power_SZ_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
36	Power_SL_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
37	Power_SL_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
38	Power_HN_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
39	Power_HN_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
40	Power_SD_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
41	Power_SD_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
42	Power_VSB100_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
43	Power_VSB100_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
44	Power_VSB200_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
45	Power_VSB200_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
46	Power_VSB300_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
47	Power_VSB300_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938
48	Power_VSB400_r(uW/MHZ)	Pin Power Rise	0.5552	0.3129	0.3129
49	Power_VSB400_f(uW/MHZ)	Pin Power Fall	10.89	2.938	2.938

Table 10: Leakage & Dynamic Power

- * Read/Write power is due to the rising edge of the clock only.
- * Read/Write power is for the alternate active cycles
- * Read/Write power is measured with 50% data and address bus toggling.
- * Address/Data power is for each individual bit of the bus



#	Parameter	Description	FF_1p10v_125c	SS_0p90v_n40c	SS_0p90v_n55c
1	sl_leak(uW)	Leakage Power::slumber	4.530e+04	515.0	562.9
2	sz_leak(uW)	Leakage Power::snooze	5.063e+04	241.3	221.8
3	hn_leak(uW)	Leakage Power::hibernate	4.157e+04	413.6	459.9
4	sd_leak(uW)	Leakage Power::shutdown	3.863e+04	375.1	426.2
5	static_leak(uW)	Leakage Power::standby	5.597e+04	335.9	317.1
6	Power_WE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1110	0.01046	0.01046
7	Power_WE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1126	0.01165	0.01165
8	Power_TWE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1110	0.01046	0.01046
9	Power_TWE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1126	0.01165	0.01165
10	Power_A_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1110	0.01046	0.01046
11	Power_A_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1110	0.01046	0.01046
12	Power_TA_r::chip_dis(uW/MHZ)	Pin Power Rise	0.1110	0.01046	0.01046
13	Power_TA_f::chip_dis(uW/MHZ)	Pin Power Fall	0.1110	0.01046	0.01046
14	Power_WE_r::chip_en(uW/MHZ)	Pin Power Rise	1.923	0.4144	0.4144
15	Power_WE_f::chip_en(uW/MHZ)	Pin Power Fall	1.954	0.3998	0.3998
16	Power_TWE_r::chip_en(uW/MHZ)	Pin Power Rise	1.923	0.4144	0.4144
17	Power_TWE_f::chip_en(uW/MHZ)	Pin Power Fall	1.954	0.3998	0.3998
18	Power_A_r::chip_en(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
19	Power_A_f::chip_en(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
20	Power_TA_r::chip_en(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
21	Power_TA_f::chip_en(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
22	Pread(uW/MHZ)	Read Power Rise	10.01	3.200	3.200
23	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
24	Pwrite(uW/MHZ)	Write Power Rise	10.16	4.007	4.007
25	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
26	Power_CLK_r(uW/MHZ)	Pin Power Rise	1.531	0.1297	0.1297
27	Power_CLK_f(uW/MHZ)	Pin Power Fall	1.541	0.1383	0.1383
28	Pread(uW/MHZ)	Read Power Rise	10.01	3.200	3.200
29	Pread(uW/MHZ)	Read Power Fall	0.000	0.000	0.000
30	Pwrite(uW/MHZ)	Write Power Rise	10.16	4.007	4.007
31	Pwrite(uW/MHZ)	Write Power Fall	0.000	0.000	0.000
32	Power_TCLK_r(uW/MHZ)	Pin Power Rise	1.531	0.1297	0.1297
33	Power_TCLK_f(uW/MHZ)	Pin Power Fall	1.541	0.1383	0.1383
34	Power_SZ_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
35	Power_SZ_f(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
36 37	Power_SL_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
38	Power_SL_f(uW/MHZ) Power_HN_r(uW/MHZ)	Pin Power Fall Pin Power Rise	2.938	4.322	4.322
39		Pin Power Rise Pin Power Fall	0.3129 2.938	0.08451 4.322	0.08451 4.322
40	Power_HN_f(uW/MHZ) Power_SD_r(uW/MHZ)	Pin Power Fall Pin Power Rise	0.3129	4.322 0.08451	4.322 0.08451
40		Pin Power Rise Pin Power Fall	2.938	4.322	4.322
41	Power_SD_f(uW/MHZ) Power_VSB100_r(uW/MHZ)	Pin Power Fall Pin Power Rise	0.3129	4.322 0.08451	4.322 0.08451
42	Power_VSB100_r(uW/MHZ) Power_VSB100_f(uW/MHZ)	Pin Power Rise Pin Power Fall	2.938	4.322	4.322
43	Power_VSB100_r(uW/MHZ) Power_VSB200_r(uW/MHZ)	Pin Power Fail Pin Power Rise	0.3129	4.322 0.08451	4.322 0.08451
45	Power_VSB200_r(uW/MHZ) Power_VSB200_f(uW/MHZ)	Pin Power Rise Pin Power Fall	2.938	4.322	4.322
46	Power_VSB300_r(uW/MHZ)	Pin Power Pail Pin Power Rise	0.3129	0.08451	0.08451
47	Power_VSB300_r(uW/MHZ) Power_VSB300_f(uW/MHZ)	Pin Power Rise Pin Power Fall	2.938	4.322	4.322
48	Power_VSB400_r(uW/MHZ)	Pin Power Rise	0.3129	0.08451	0.08451
49	Power_VSB400_r(uW/MHZ)	Pin Power Fall	2.938	4.322	4.322
49	FOWEL_V3D400_I(UVV/IVITL)	Table 11: Leakage & Dynar		4.322	4.322

Table 11: Leakage & Dynamic Power

- * Read/Write power is due to the rising edge of the clock only.
- * Read/Write power is for the alternate active cycles
- * Read/Write power is measured with 50% data and address bus toggling.
- * Address/Data power is for each individual bit of the bus

#	Parameter	Description	SS_0p90v_125c
1	sl_leak(uW)	Leakage Power::slumber	2161.
2	sz_leak(uW)	Leakage Power::snooze	2521.
3	hn_leak(uW)	Leakage Power::hibernate	2052.
4	sd_leak(uW)	Leakage Power::shutdown	1969.
5	static_leak(uW)	Leakage Power::standby	2640.

Table 12: Leakage & Dynamic Power



6	Power_WE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.01046
7	Power_WE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.01165
8	Power_TWE_r::chip_dis(uW/MHZ)	Pin Power Rise	0.01046
9	Power_TWE_f::chip_dis(uW/MHZ)	Pin Power Fall	0.01165
10	Power_A_r::chip_dis(uW/MHZ)	Pin Power Rise	0.01046
11	Power_A_f::chip_dis(uW/MHZ)	Pin Power Fall	0.01046
12	Power_TA_r::chip_dis(uW/MHZ)	Pin Power Rise	0.01046
13	Power_TA_f::chip_dis(uW/MHZ)	Pin Power Fall	0.01046
14	Power_WE_r::chip_en(uW/MHZ)	Pin Power Rise	0.4144
15	Power_WE_f::chip_en(uW/MHZ)	Pin Power Fall	0.3998
16	Power_TWE_r::chip_en(uW/MHZ)	Pin Power Rise	0.4144
17	Power_TWE_f::chip_en(uW/MHZ)	Pin Power Fall	0.3998
18	Power_A_r::chip_en(uW/MHZ)	Pin Power Rise	0.08451
19	Power_A_f::chip_en(uW/MHZ)	Pin Power Fall	4.322
20	Power_TA_r::chip_en(uW/MHZ)	Pin Power Rise	0.08451
21	Power_TA_f::chip_en(uW/MHZ)	Pin Power Fall	4.322
22	Pread(uW/MHZ)	Read Power Rise	3.200
23	Pread(uW/MHZ)	Read Power Fall	0.000
24	Pwrite(uW/MHZ)	Write Power Rise	4.007
25	Pwrite(uW/MHZ)	Write Power Fall	0.000
26	Power_CLK_r(uW/MHZ)	Pin Power Rise	0.1297
27	Power_CLK_f(uW/MHZ)	Pin Power Fall	0.1383
28	Pread(uW/MHZ)	Read Power Rise	3.200
29	Pread(uW/MHZ)	Read Power Fall	0.000
30	Pwrite(uW/MHZ)	Write Power Rise	4.007
31	Pwrite(uW/MHZ)	Write Power Fall	0.000
32	Power_TCLK_r(uW/MHZ)	Pin Power Rise	0.1297
33	Power_TCLK_f(uW/MHZ)	Pin Power Fall	0.1383
34	Power_SZ_r(uW/MHZ)	Pin Power Rise	0.08451
35	Power_SZ_f(uW/MHZ)	Pin Power Fall	4.322
36	Power_SL_r(uW/MHZ)	Pin Power Rise	0.08451
37	Power_SL_f(uW/MHZ)	Pin Power Fall	4.322
38	Power_HN_r(uW/MHZ)	Pin Power Rise	0.08451
39	Power_HN_f(uW/MHZ)	Pin Power Fall	4.322
40	Power_SD_r(uW/MHZ)	Pin Power Rise	0.08451
41	Power_SD_f(uW/MHZ)	Pin Power Fall	4.322
42	Power_VSB100_r(uW/MHZ)	Pin Power Rise	0.08451
43	Power_VSB100_f(uW/MHZ)	Pin Power Fall	4.322
44	Power_VSB200_r(uW/MHZ)	Pin Power Rise	0.08451
45	Power_VSB200_f(uW/MHZ)	Pin Power Fall	4.322
46	Power_VSB300_r(uW/MHZ)	Pin Power Rise	0.08451
47	Power_VSB300_f(uW/MHZ)	Pin Power Fall	4.322
48	Power_VSB400_r(uW/MHZ)	Pin Power Rise	0.08451
49	Power_VSB400_f(uW/MHZ)	Pin Power Fall	4.322

Table 12: Leakage & Dynamic Power

- * Read/Write power is due to the rising edge of the clock only.
- * Read/Write power is for the alternate active cycles
- * Read/Write power is measured with 50% data and address bus toggling.
- * Address/Data power is for each individual bit of the bus



Input Pin Capacitance

#	PIN	Description(unit:pF)	TT_1p00v_25c	FF_1p10v_n40c	FF_1p10v_n55c
1	BISTE	Pin Capacitance	0.002	0.002	0.002
2	AWT	Pin Capacitance	0.002	0.002	0.002
3	CLK	Pin Capacitance	0.008	0.007	0.007
4	TCLK	Pin Capacitance	0.008	0.007	0.007
5	CE	Pin Capacitance	0.002	0.002	0.002
6	TCE	Pin Capacitance	0.002	0.002	0.002
7	WE	Pin Capacitance	0.002	0.002	0.002
8	TWE	Pin Capacitance	0.002	0.002	0.002
9	BWM	Pin Capacitance	0.002	0.002	0.002
10	TBWM	Pin Capacitance	0.002	0.002	0.002
11	Α	Pin Capacitance	0.002	0.002	0.002
12	TA	Pin Capacitance	0.002	0.002	0.002
13	D	Pin Capacitance	0.002	0.002	0.002
14	TD	Pin Capacitance	0.002	0.002	0.002
15	RM	Pin Capacitance	0.002	0.002	0.002
16	WM	Pin Capacitance	0.002	0.002	0.002
17	RA	Pin Capacitance	0.002	0.002	0.002
18	LVTEST	Pin Capacitance	0.002	0.002	0.002
19	SZ	Pin Capacitance	0.005	0.005	0.005
20	SL	Pin Capacitance	0.005	0.005	0.005
21	BADIO	Pin Capacitance	_	_	_
22	HN	Pin Capacitance	0.011	0.011	0.011
23	SD	Pin Capacitance	0.006	0.006	0.006
24	VSB100	Pin Capacitance	0.002	0.002	0.002
25	VSB200	Pin Capacitance	0.002	0.002	0.002
26	VSB300	Pin Capacitance	0.002	0.002	0.002
27	VSB400	Pin Capacitance	0.002	0.002	0.002
28	VDD	Pin Capacitance	-	_	_

Table 13: Capacitance

#	PIN	Description(unit:pF)	FF_1p10v_125c	SS_0p90v_n40c	SS_0p90v_n55c
1	BISTE	Pin Capacitance	0.002	0.002	0.002
2	AWT	Pin Capacitance	0.002	0.002	0.002
3	CLK	Pin Capacitance	0.007	0.009	0.009
4	TCLK	Pin Capacitance	0.007	0.009	0.009
5	CE	Pin Capacitance	0.002	0.002	0.002
6	TCE	Pin Capacitance	0.002	0.002	0.002
7	WE	Pin Capacitance	0.002	0.002	0.002
8	TWE	Pin Capacitance	0.002	0.002	0.002
9	BWM	Pin Capacitance	0.002	0.002	0.002
10	TBWM	Pin Capacitance	0.002	0.002	0.002
11	Α	Pin Capacitance	0.002	0.002	0.002
12	TA	Pin Capacitance	0.002	0.002	0.002
13	D	Pin Capacitance	0.002	0.002	0.002
14	TD	Pin Capacitance	0.002	0.002	0.002
15	RM	Pin Capacitance	0.002	0.002	0.002
16	WM	Pin Capacitance	0.002	0.002	0.002
17	RA	Pin Capacitance	0.002	0.002	0.002
18	LVTEST	Pin Capacitance	0.002	0.002	0.002
19	SZ	Pin Capacitance	0.005	0.005	0.005
20	SL	Pin Capacitance	0.005	0.005	0.005
21	BADIO	Pin Capacitance	_	_	_
22	HN	Pin Capacitance	0.011	0.011	0.011
23	SD	Pin Capacitance	0.006	0.005	0.005
24	VSB100	Pin Capacitance	0.002	0.002	0.002
25	VSB200	Pin Capacitance	0.002	0.002	0.002
26	VSB300	Pin Capacitance	0.002	0.002	0.002
27	VSB400	Pin Capacitance	0.002	0.002	0.002
28	VDD	Pin Capacitance	_	_	_

Table 14: Capacitance



#	PIN	Description(unit:pF)	SS_0p90v_125c
1	BISTE	Pin Capacitance	0.002
2	AWT	Pin Capacitance	0.002
3	CLK	Pin Capacitance	0.009
4	TCLK	Pin Capacitance	0.009
5	CE	Pin Capacitance	0.002
6	TCE	Pin Capacitance	0.002
7	WE	Pin Capacitance	0.002
8	TWE	Pin Capacitance	0.002
9	BWM	Pin Capacitance	0.002
10	TBWM	Pin Capacitance	0.002
11	Α	Pin Capacitance	0.002
12	TA	Pin Capacitance	0.002
13	D	Pin Capacitance	0.002
14	TD	Pin Capacitance	0.002
15	RM	Pin Capacitance	0.002
16	WM	Pin Capacitance	0.002
17	RA	Pin Capacitance	0.002
18	LVTEST	Pin Capacitance	0.002
19	SZ	Pin Capacitance	0.005
20	SL	Pin Capacitance	0.005
21	BADIO	Pin Capacitance	ı
22	HN	Pin Capacitance	0.011
23	SD	Pin Capacitance	0.005
24	VSB100	Pin Capacitance	0.002
25	VSB200	Pin Capacitance	0.002
26	VSB300	Pin Capacitance	0.002
27	VSB400	Pin Capacitance	0.002
28	VDD	Pin Capacitance	_

Table 15: Capacitance



Corruption Table

#	Parameter	Related Pin	CEM	CCL
1	Tcc(Violation)	CLK	YES	NO
2	Tcl(Violation)	CLK	YES	NO
3	Tch(Violation)	CLK	YES	NO
4	Tacs_rise(Violation)	Α	YES	NO
5	Tach_rise(Violation)	A	YES	NO
6	Trwcs_rise(Violation)	WE	NO	YES
7	Trwch_rise(Violation)	WE	NO	YES
8	Tbyms_rise(Violation)	BWM	NO	YES
9	Tbymh_rise(Violation)	BWM	NO	YES
10	Tces_rise(Violation)	CE	YES	NO
11	Tceh_rise(Violation)	CE	YES	NO
12	Tdcs_rise(Violation)	D	NO	YES
13	Tdch_rise(Violation)	D	NO	YES
14	Tsnzrc(Violation)	SZ	YES	NO
15	Tsnzrm(Violation)	SZ	YES	NO
16	Tslprc(Violation)	SL	YES	NO
17	Tslprm(Violation)	SL	YES	NO
18	Thbrntrc(Violation)	HN	YES	NO
19	Thbrntprm(Violation)	HN	YES	NO
20	Tdslprc(Violation)	SD	YES	NO
21	Tdslprm(Violation)	SD	YES	NO
	T 11 40 10 1 1	C 14/ 1:		

Table 16: Violation in case of Write Mode

* CEM : Corrupt Entire Memory

* CCL : Corrupt Current Location (Selected Word)

#	Parameter	Related Pin	CEM	CCL
1	Tcc(Violation)	CLK	YES	NO
2	Tcl(Violation)	CLK	YES	NO
3	Tch(Violation)	CLK	YES	NO
4	Tacs_rise(Violation)	A	YES	NO
5	Tach_rise(Violation)	A	YES	NO
6	Trwcs_rise(Violation)	WE	NO	YES
7	Trwch_rise(Violation)	WE	NO	YES
8	Tces_rise(Violation)	CE	YES	NO
9	Tceh_rise(Violation)	CE	YES	NO
10	Tsnzrc(Violation)	SZ	YES	NO
11	Tsnzrm(Violation)	SZ	YES	NO
12	Tslprc(Violation)	SL	YES	NO
13	Tslprm(Violation)	SL	YES	NO
14	Thbrntrc(Violation)	HN	YES	NO
15	Thbrntprm(Violation)	HN	YES	NO
16	Tdslprc(Violation)	SD	YES	NO
17	Tdslprm(Violation)	SD	YES	NO

Table 17: Violation in case of Read Mode

* CEM : Corrupt Entire Memory

* CCL : Corrupt Current Location (Selected Word)



Timing Diagrams

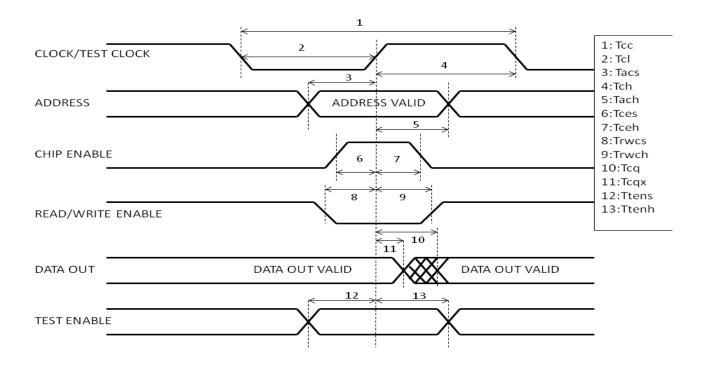


Figure 1: Read Timing



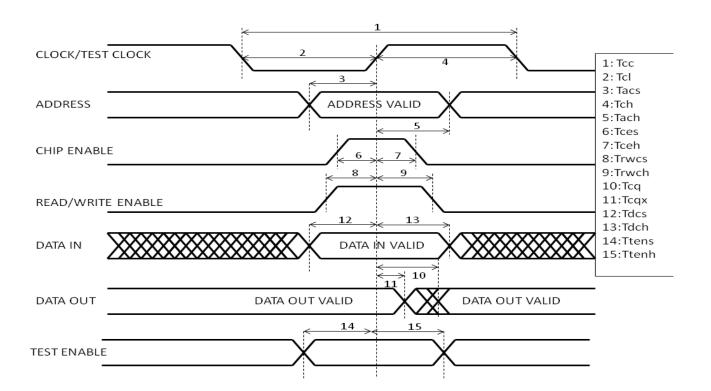
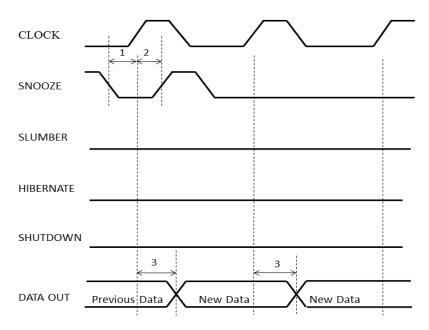


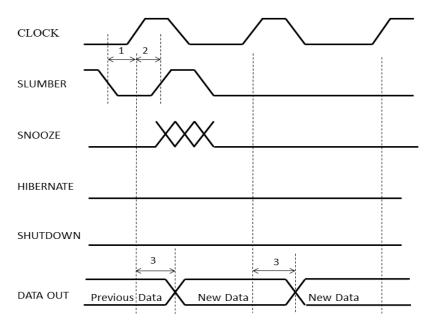
Figure 2: Write Timing



1 => Recovery Time; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

Figure 3: Snooze Timing





1 => Recovery Time; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

CLOCK

HIBERNATE

SHUTDOWN

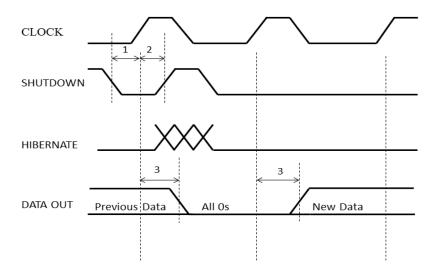
DATA OUT Previous Data All 0s New Data

Figure 4: Slumber Timing

1 => Recovery Time; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

Figure 5: Hibernate Timing





1 => Recovery Time; 2=> Removal Time; 3 => CLOCK-> DATA OUT delay

Figure 6: Shutdown Timing



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