Elizabeth Buitrago, PhD

R&D Project leader BiMOS Chips

PERSONAL INFO

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SKILLS, HONORS & ACTIVITIES

- Bilingual (Spanish, English), basic French and German
- Organization Staff for the International Conference on Micro and Nano Engineering (MNE) 2014, Lausanne-CH.
- Donald F. Othmer Sophomore Academic Excellence Award (AICHE)
- IEEE EPFL student branch member (2010 - present)
- Triton Engineering Council Representative for AICHE (2003 – 2005)

EDUCATION

JUN 2014
PhD Microsystems and Microelectronics
École Polytechnique Fédérale de Lausanne (EPFL)
Switzerland

SEPT 2010
MSc Process Engineering
Eidgenössische Technische Hochschule Zürich (ETHZ)
Switzerland

JUN 2005
BSc Chemical Engineering
University of California San Diego (UCSD)
USA

EXPERIENCE

NOV 2016 - PRESENT: R&D Project leader BiMOS Chips

ABB Switzerland – Lenzburg (Switzerland)

- Development and benchmarking of novel buffer technologies compatible with ultra-thin > 200 mm wafers.
- Process flow assessment and tool set evaluation (laser anneal) for thin wafer backside processing of IGBTs.
- Process integration enabling Tvj(op) = 150 °C capability of 6.5kV, 900A IGBT HiPak Module.
- Project management, process integration of next generation low voltage Trench IGBTs in house and foundry.
- Process and device TCAD simulations, device design, electrical characterization and testing of IGBTs.

JUL 2014 - OCT 2016: Postdoctoral Research Scientist & Nanofabrication Lead

Paul Scherrer Institute (PSI) & ASML, X-Ray Interference Lithography Group (XIL-II) – Villigen (Switzerland)

- Process optimization and characterization of state-state-of the-art chemically amplified (CAR) and inorganic resist and materials for extreme ultraviolet (EUV) lithography at the Swiss Light Synchrotron Source (SLS).
- 10 nm half-pitch resolution achieved with CAR via ASML industrial collaboration.
- Nanofabrication lead in the development of highly efficient diffraction gratings (masks) with novel materials for interference lithography (IL) at the Lab of Micro and Nanotechnology (LMN) in PSI.

OCT 2010 - JUN 2014: Research Engineer (PhD Thesis)

EPFL, Nanoelectronic Devices Laboratory (Nanolab) – Lausanne (Switzerland): Prof. A. M. IonescuLithography Group (XIL-II) – Villigen (Switzerland)

- 3D vertically stacked silicon nanowire (SiNW) field effect transistor (FET) was realized as a proof-of-concept device for its future implementation into low cost biosensors.
- Led a multi-institution collaboration within two European projects (E-BRAINS and SiNAPS) that resulted in the successful microfluidic platform development, electrical characterization and surface functionalization for ultra-low concentration protein sensing.
- Research on high performance SiNW/Fin based FETs for biosensing (junctionless and enhancement mode).
- Careful design and fabrication of CMOS compatible process flow for robust 3D heterogeneous systems integration. 3D TCAD-Sentaurus process and device simulations.
- Teaching and supervision of master students.

SEPT 2007 - OCT 2008: Process Engineer (Wet Etch Process-Cleans)

Micron Technology (300 mm Wafer Fab) – Manassas, VA (USA)

- Direct and sustain process improvements using statistical process control (SPC).
- Strategically identify and analyze process failures.
- Audit process recipes, configure hardware and use procedural methods to perform process enhancements.
- Identifying, understanding, and resolving defect issues, assisting area technicians troubleshooting problems, improving preventative maintenance procedures, and optimizing overall tool performance.
- Proficiency across all wet process modules and toolsets necessary in order to be able to disposition lots efficiently, prevent scrap and continuously improve wet process capabilities.
- Process modules and tool sets: Wet Benches (Tel and DNS Electronics FC-3000, FC-3100), Ash and Descum (Axcelis -Rapid Strip), Single wafer processing, Nanospray and Scrub (SCREEN - DNS, SU-3000, SS-3000), Cu Plating (Semitool - Raider), Dry Bevel Etch (Sosul).
- 50 Series NAND Redundancy Project. Create redundancy for clean process steps across all wet process toolsets in anticipation for wafer processing ramp.

JAN 2006 - JAN 2007: Primary Process Engineer (Metal Deposition)

AMI Semiconductor (ON Semiconductor) – Pocatello, ID (USA)

- Worked directly with production and engineering teams to review existing procedures and identify and implement cost, quality and productivity improvements.
- Statistical analysis, design of experiments (DOE), SPC and process capability studies.
- Responsibilities included sustaining, data analysis, continuous improvement of current procedures, cost savings, new process introduction.
- Tool sets: MRC, Heat Pulse 8108 Rapid Thermal Processor.