

## HW2 b08505039 林楷崴 工海四

The screenshot shows the MobaXterm interface with a terminal window displaying the output of a Verilog compilation process. The terminal output includes the following sections:

```
design_vision> read_verilog HW2.v
Loading db file '/usr/cad/synopsys/synthesis/cur/libraries/syn/gtech.db'
Loading db file '/usr/cad/synopsys/synthesis/cur/libraries/syn/standard.sldb'
Loading link library 'gtech'
Loading verilog file '/home/raid7_2/userb08/b08505039/CA_HW2/HW2.v'
Detecting input file type automatically (-rtl or -netlist).
Reading with Presto HDL Compiler (equivalent to -rtl option).
Running PRESTO HDLC
Warning: Can't read link library file 'your_library.db'. (UID-3)
Compiling source file /home/raid7_2/userb08/b08505039/CA_HW2/HW2.v
Warning: /home/raid7_2/userb08/b08505039/CA_HW2/HW2.v:38: signed to unsigned assignment occurs. (VER-318)
```

Statistics for case statements in always block at line 43 in file '/home/raid7\_2/userb08/b08505039/CA\_HW2/HW2.v':

Line	full/ parallel
45	auto/auto
50	auto/auto

Statistics for case statements in always block at line 103 in file '/home/raid7\_2/userb08/b08505039/CA\_HW2/HW2.v':

Line	full/ parallel
105	auto/auto

Statistics for case statements in always block at line 121 in file '/home/raid7\_2/userb08/b08505039/CA\_HW2/HW2.v':

Line	full/ parallel
123	auto/auto

Statistics for case statements in always block at line 149 in file '/home/raid7\_2/userb08/b08505039/CA\_HW2/HW2.v':

Line	full/ parallel
151	auto/auto

Inferred memory devices in process in routine ALU line 180 in file '/home/raid7\_2/userb08/b08505039/CA\_HW2/HW2.v':

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
shreg_reg	Flip-flop	64	Y	N	Y	N	N	N	N
alu_in_reg	Flip-flop	32	Y	N	Y	N	N	N	N
state_reg	Flip-flop	3	Y	N	Y	N	N	N	N
counter_reg	Flip-flop	5	Y	N	Y	N	N	N	N

Presto compilation completed successfully.  
Current design is now '/home/raid7\_2/userb08/b08505039/CA\_HW2/ALU.db:ALU'.  
Loaded i design.  
Current design is 'ALU'.  
ALU design\_v is ton>