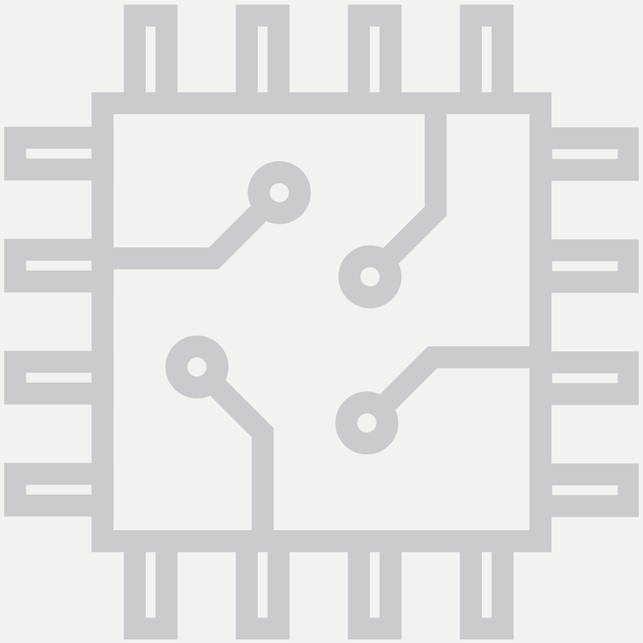
YEAR
2023 Dec

PRESENTER
Evan Lin & Justine Tsai

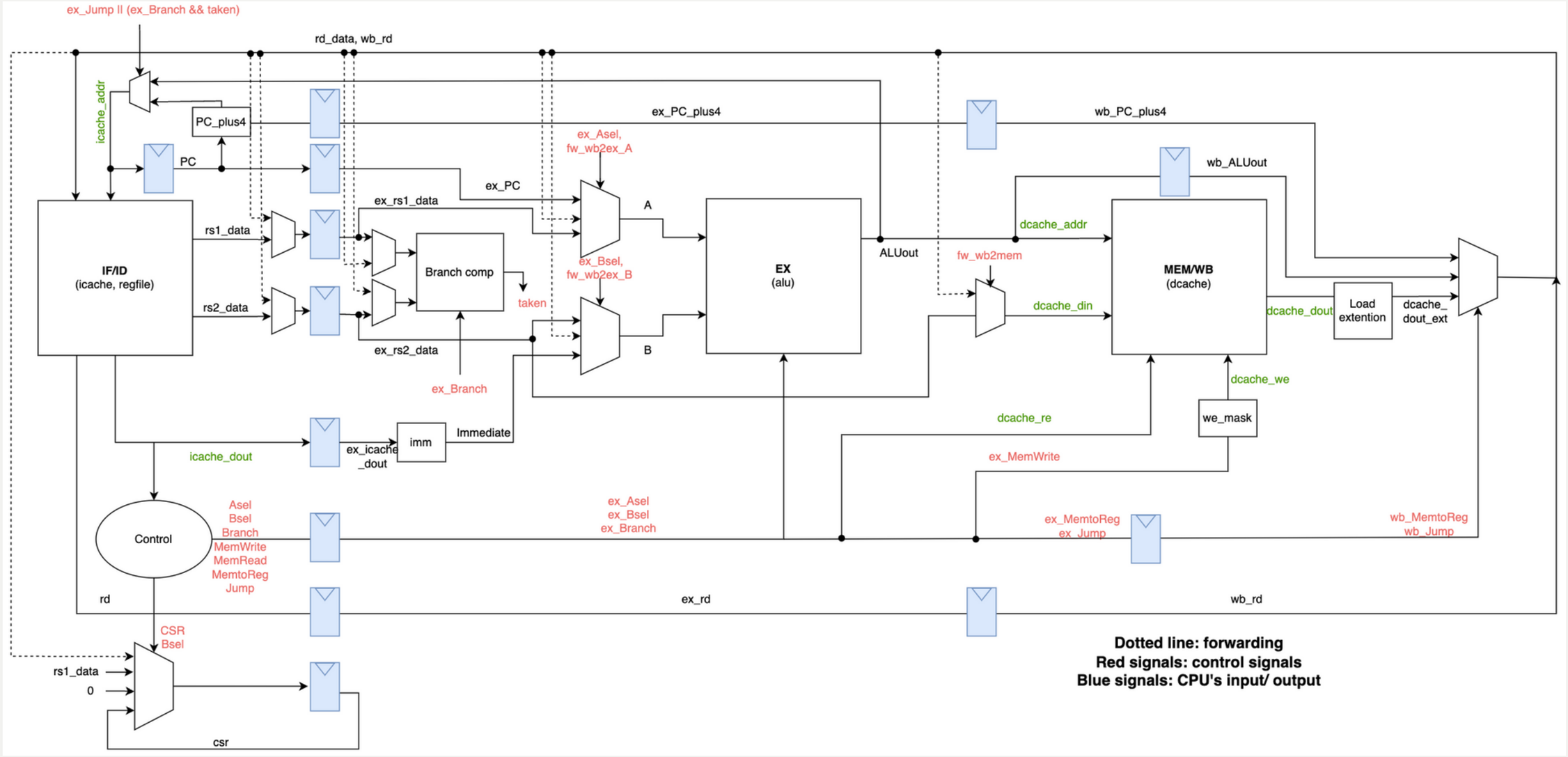
251A
Final Project

3-Stage CPU with Cache



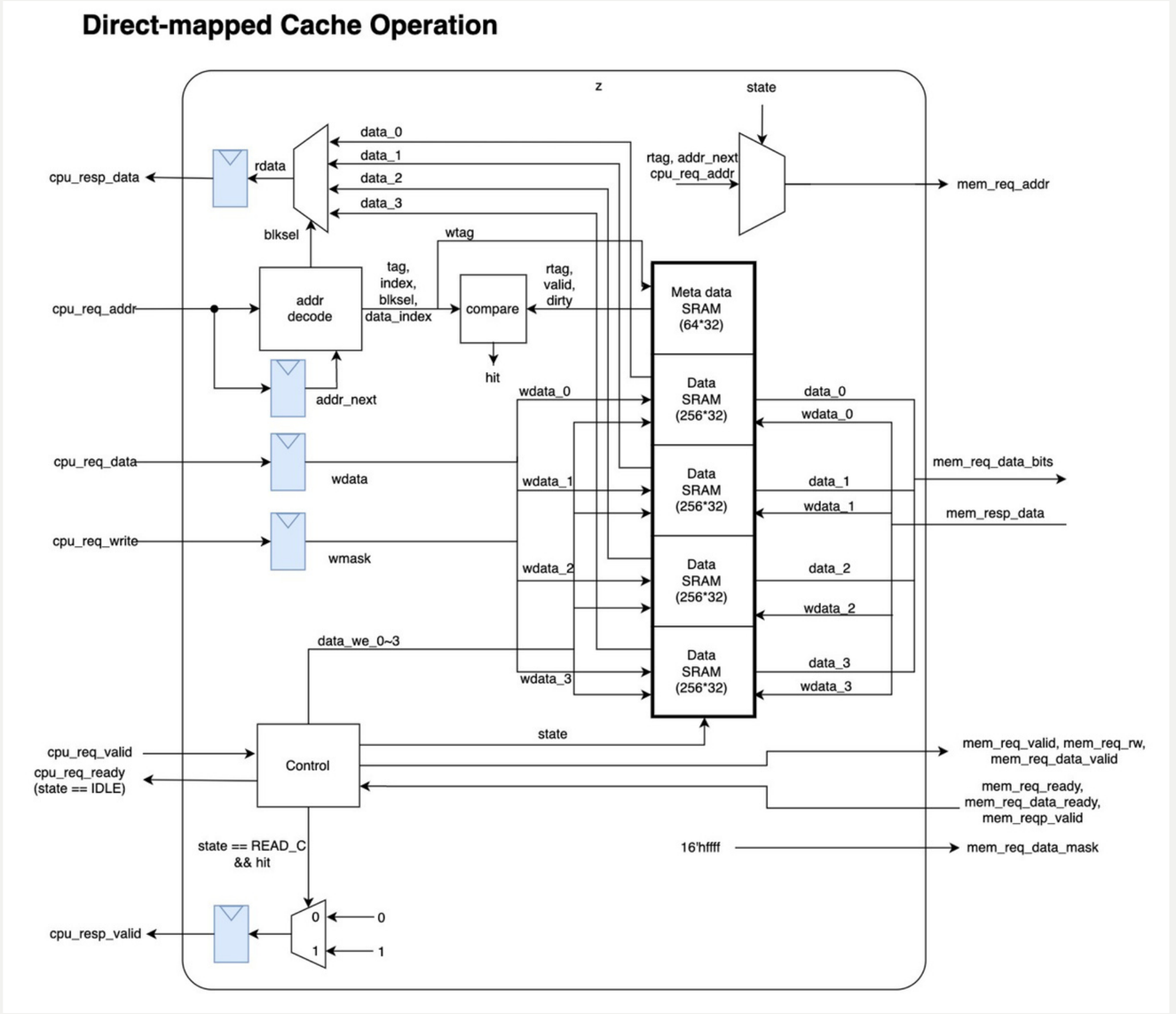
INTRODUCTION TO OUR

CPU Implementation



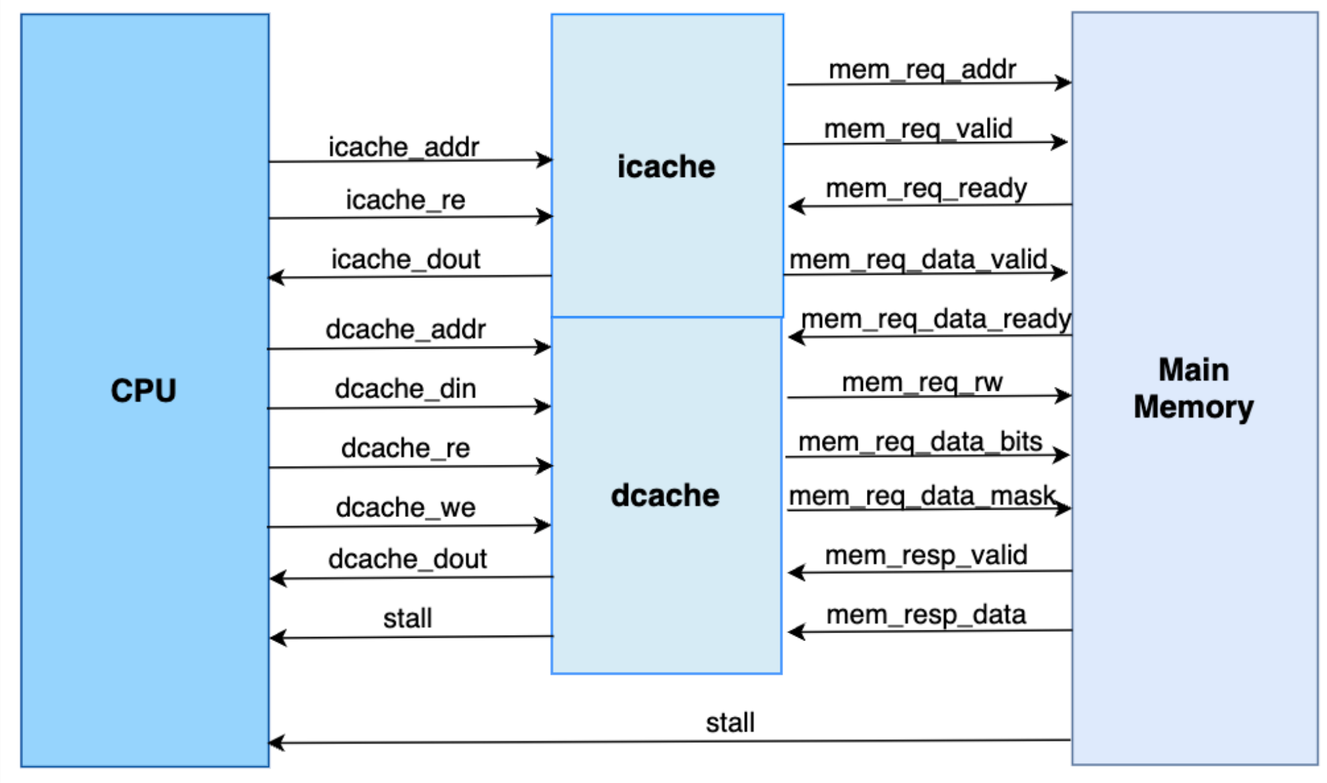
INTRODUCTION TO OUR

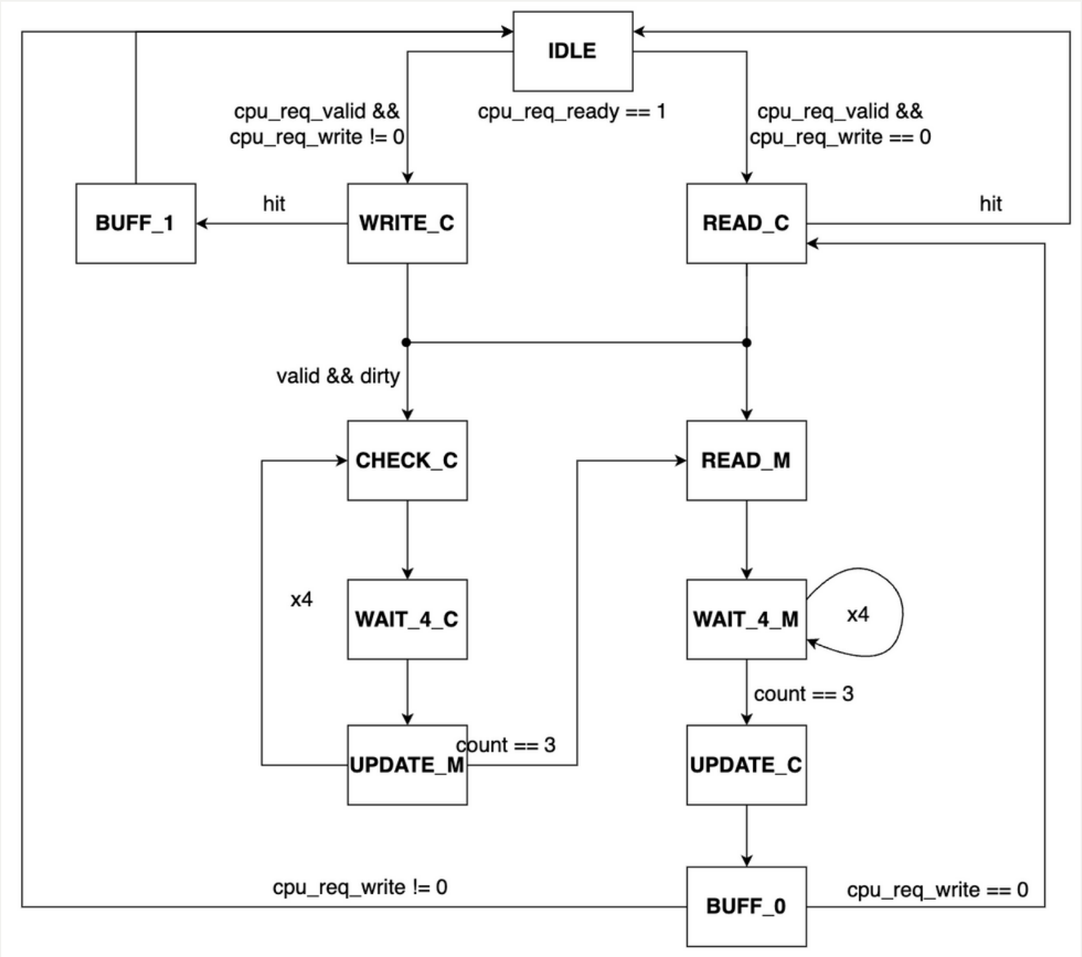
Cache Implementation



INTRODUCTION TO OUR

Cache





Testbech Runing Cycle

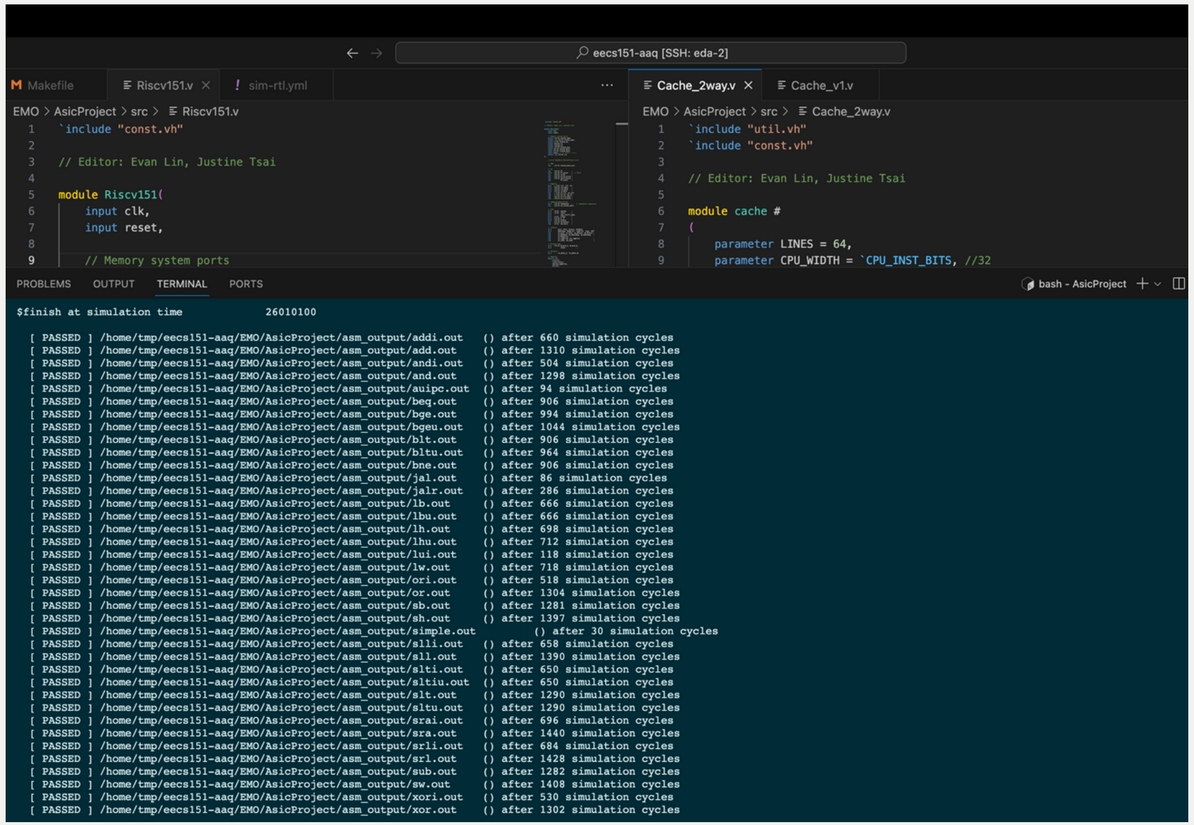
TEST	CYCLES W/O CACHE	CYCLES W DIRECT CACHE	CYCLES W 2-WAY CACHE
cachetest	2424777	5385734	5327428
final	5130	12090	12091
fib	4352	9710	9711
sum	14209599	30966520	31727604
replace	14209629	31155166	31730389

Timing performance

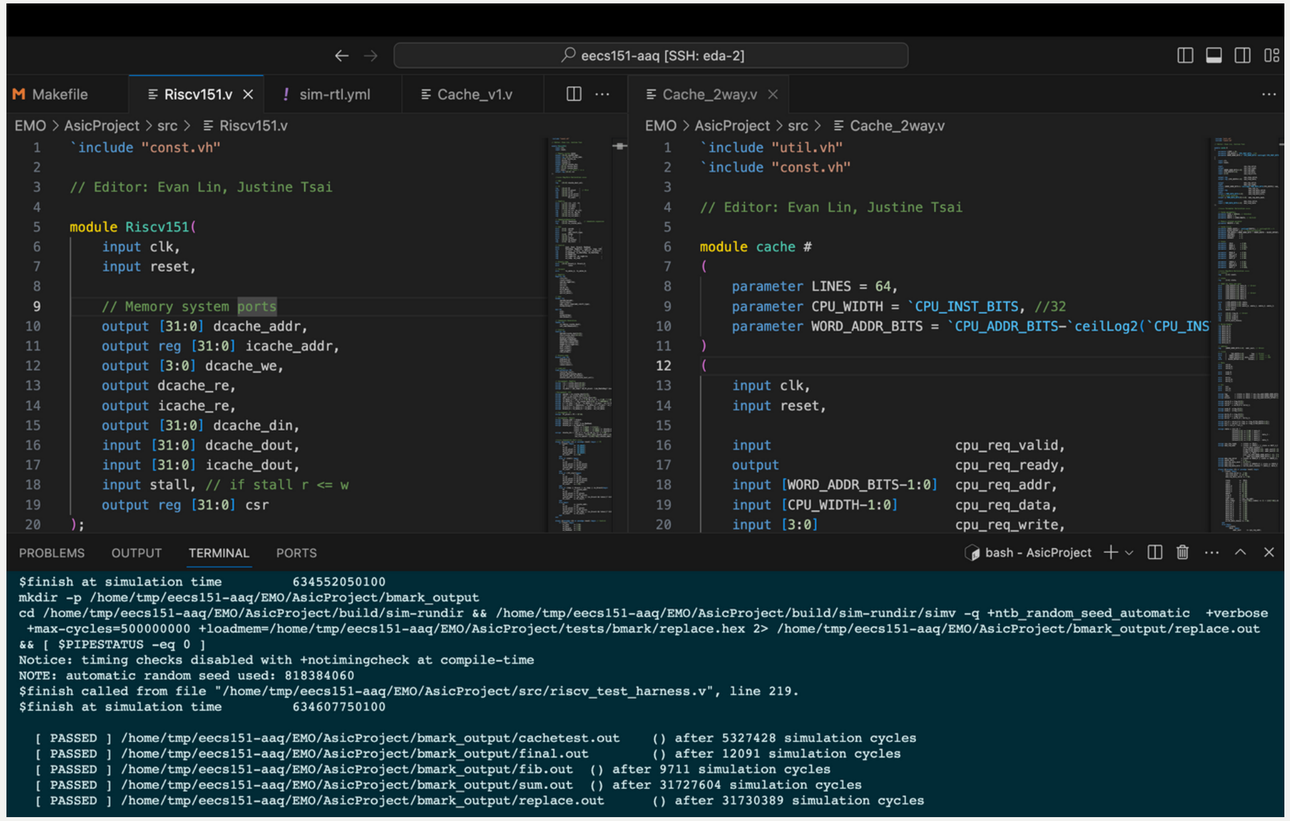
HOLD TIME SLACK	PERIOD
CPU W/ Direct-mapped : 0.011	20ns
CPU W/ 2-way cache : 0.044	20ns

SCREENSHOT OF THE

Passed Testbench (2-way associative cache)



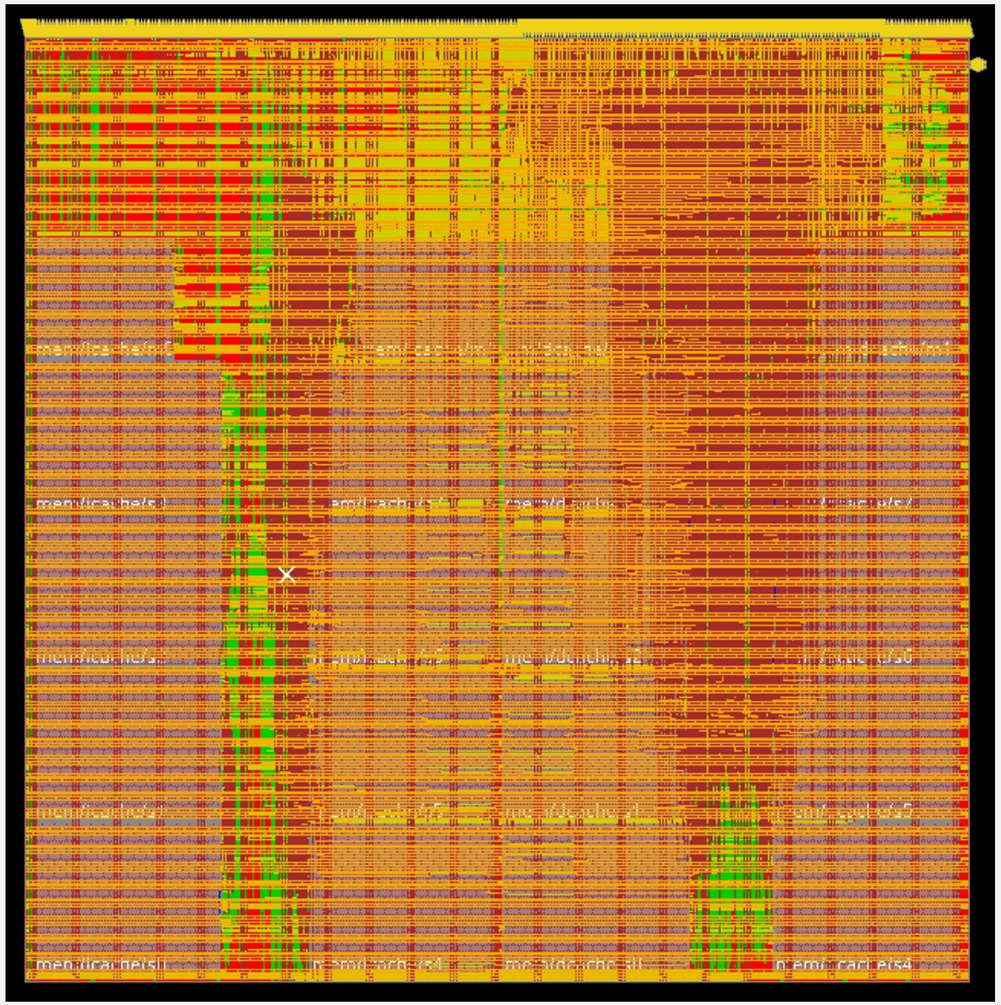
ASM TEST



BENCHMARK TEST

SCREENSHOT OF THE

PnR and Timing(2-way associative cache)



FLOOR PLAN

```
Path 1: MET (0.044 ns) Hold Check with Pin mem/icache/m1/clk->din[14]
              View: ff_n40C_1v95.hold_view
             Group: reg2reg
        Startpoint: (R) mem/icache/wtag_1_reg[14]/CLK
             Clock: (R) clk
          Endpoint: (R) mem/icache/m1/din[14]
             Clock: (R) clk

                     Capture       Launch
       Clock Edge:+    0.000        0.000
      Src Latency:+   -0.729       -0.729
      Net Latency:+    0.789 (P)    0.720 (P)
          Arrival:=    0.060       -0.009

             Hold:+    0.118
      Uncertainty:+    0.100
      Cppr Adjust:-    0.000
    Required Time:=    0.278
     Launch Clock:=   -0.009
        Data Path:+    0.331
            Slack:=    0.044
  Timing Path:
```

TIMING REPORT (POST-PAR)