

YEAR

2023 Dec

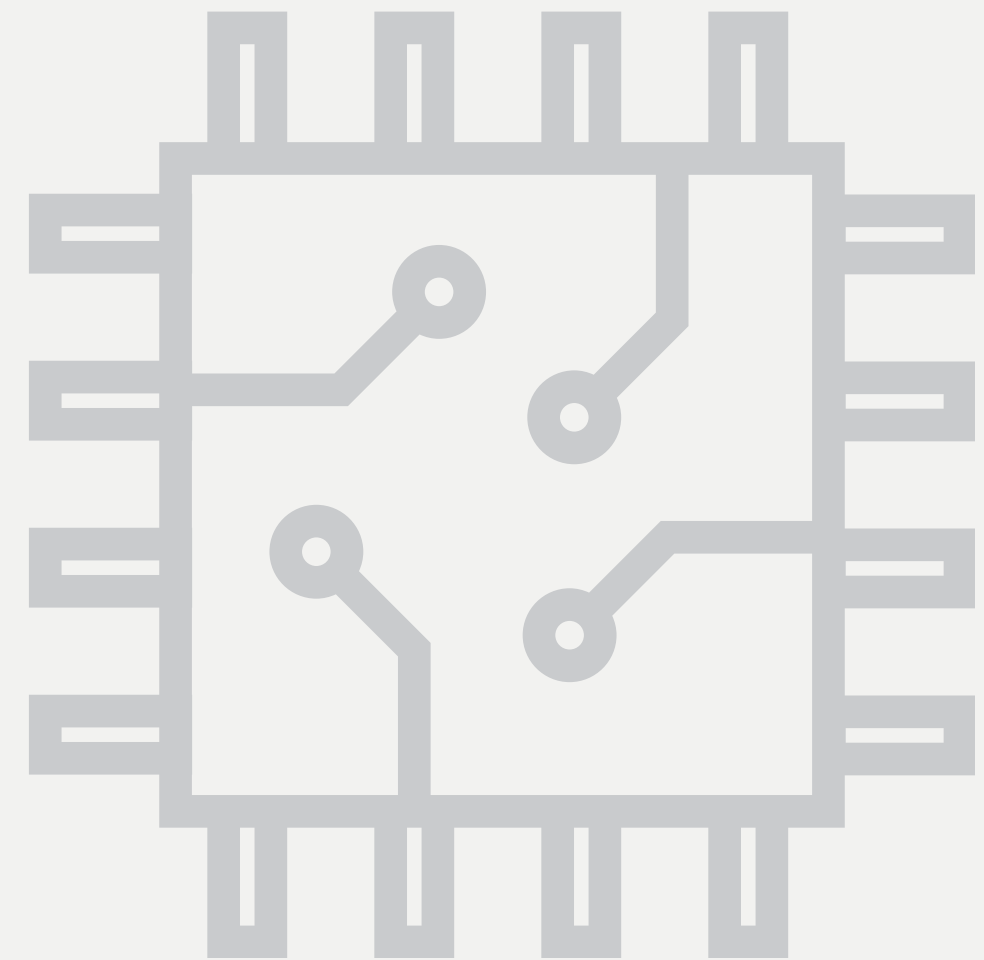
PRESENTER

Evan Lin & Justine Tsai

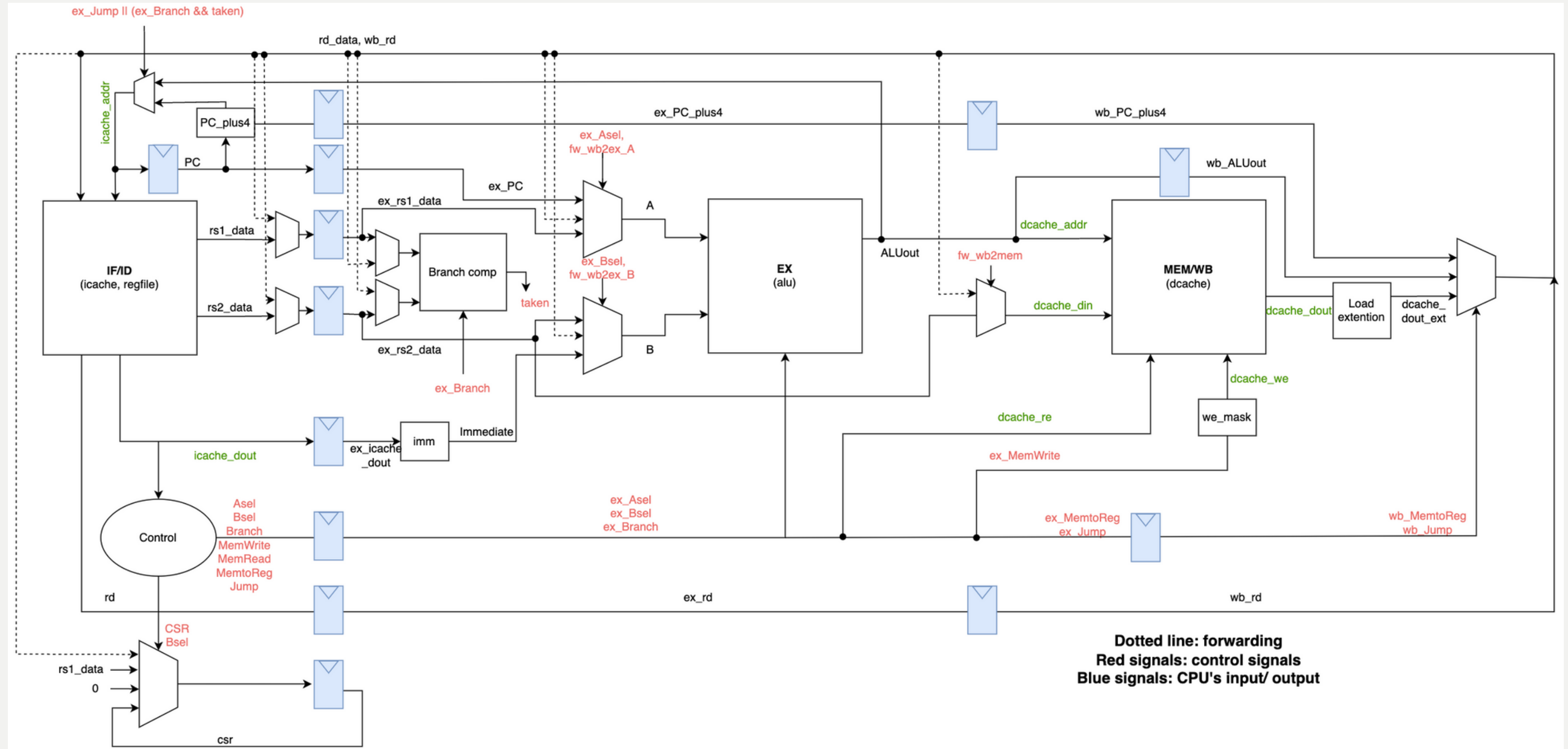
251A

Final Project

3-Stage CPU with Cache

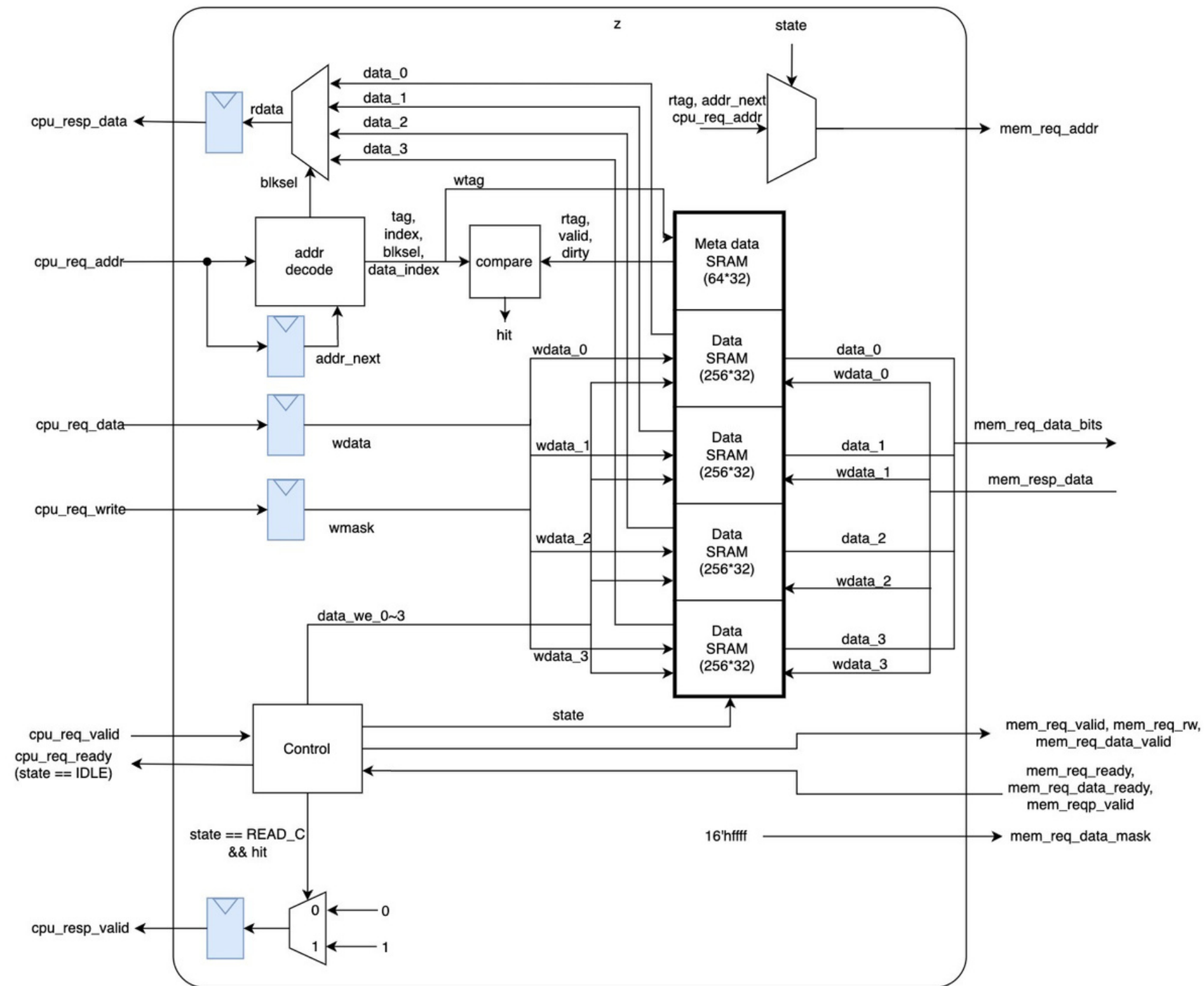


CPU Implementation

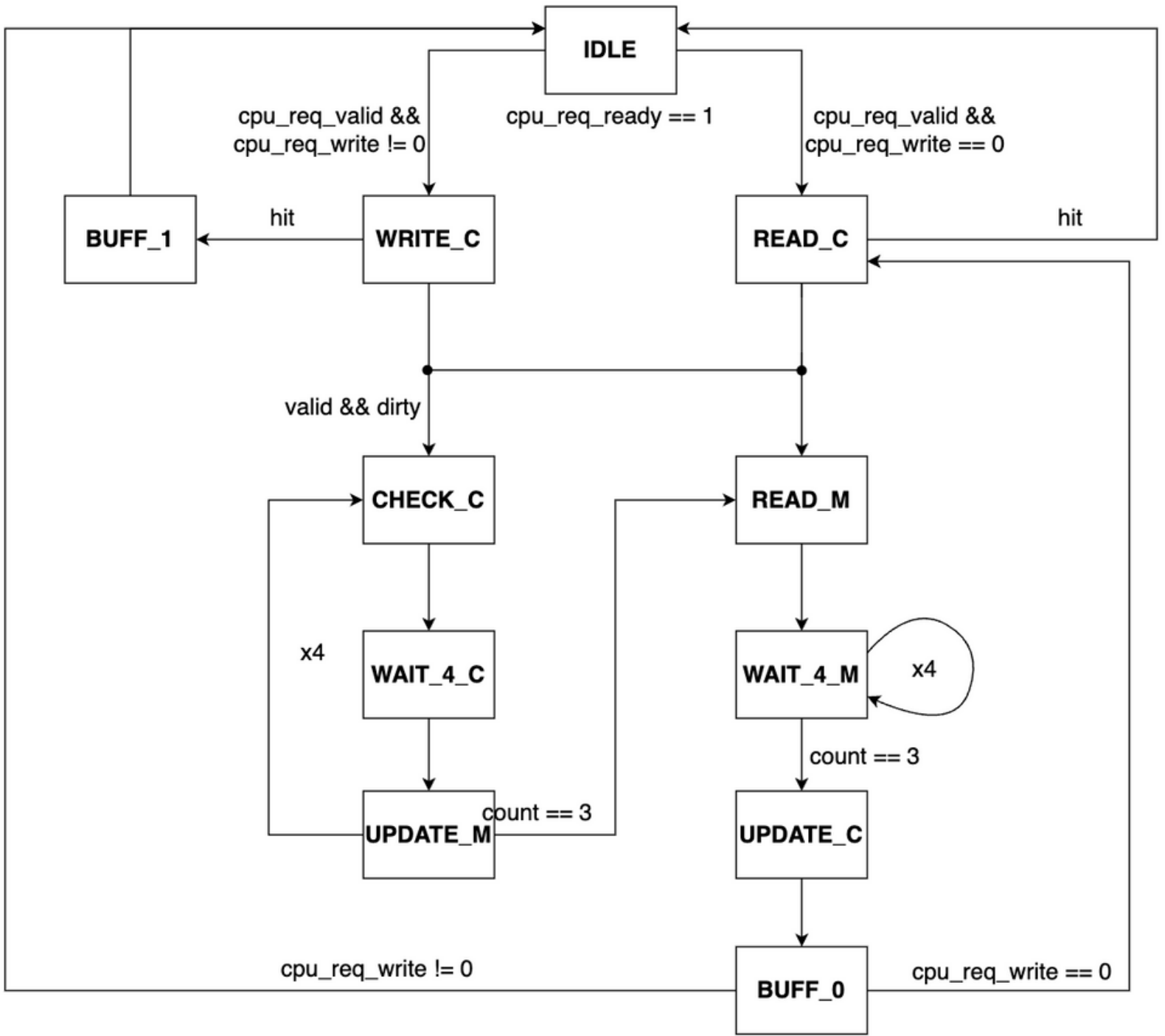
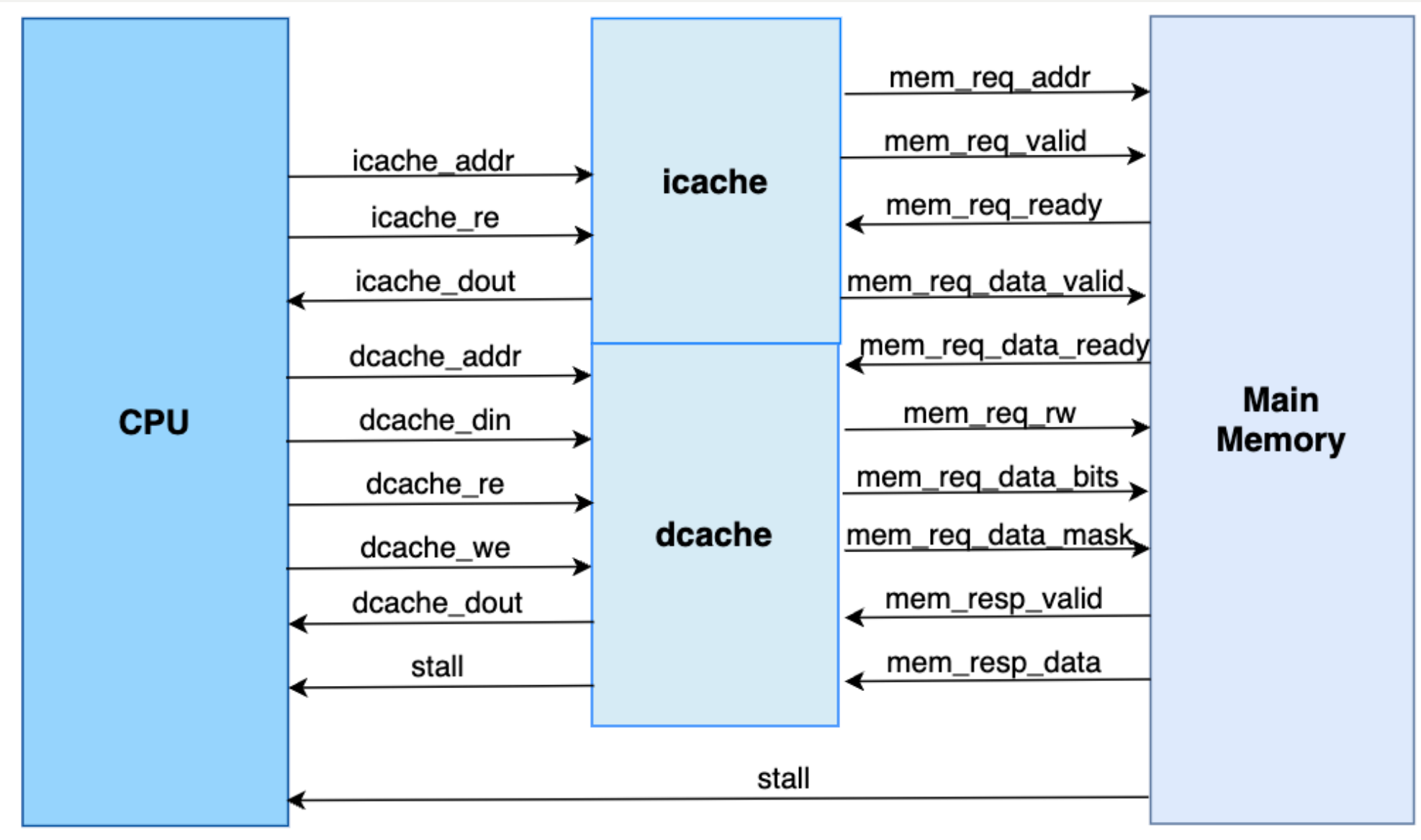


Cache Implementation

Direct-mapped Cache Operation



Cache



Testbech Runing Cycle

TEST	CYCLES W/O CACHE	CYCLES W DIRECT CACHE	CYCLES W 2-WAY CACHE
cachetest	2424777	5385734	5327428
final	5130	12090	12091
fib	4352	9710	9711
sum	14209599	30966520	31727604
replace	14209629	31155166	31730389

Timing performance

HOLD TIME SLACK	PERIOD
CPU W/ Direct-mapped : 0.011	20ns
CPU W/ 2-way cache : 0.044	20ns

SCREENSHOT OF THE

Passed Testbench (2-way associative cache)

←→

eeecs151-aaq [SSH: eda-2]

⌵

Makefile

Riscv151.v

! sim-rtl.yml

Cache_2way.v

Cache_v1.v

EMO > AsicProject > src > Riscv151.v

```
1 `include "const.vh"
2
3 // Editor: Evan Lin, Justine Tsai
4
5 module Riscv151(
6     input clk,
7     input reset,
8
9     // Memory system ports
```

PROBLEMS

OUTPUT

TERMINAL

PORTS

bash - AsicProject

```
$finish at simulation time                26010100

[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/addi.out  () after 660 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/add.out  () after 1310 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/andi.out () after 504 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/and.out  () after 1298 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/auipc.out () after 94 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/beq.out  () after 906 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/bge.out  () after 994 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/bgeu.out () after 1044 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/blt.out  () after 906 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/bltu.out () after 964 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/bne.out  () after 906 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/jal.out  () after 86 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/jalr.out () after 286 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/lb.out  () after 666 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/lbu.out  () after 666 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/lh.out  () after 698 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/lhu.out () after 712 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/lui.out () after 118 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/lw.out  () after 718 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/ori.out  () after 518 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/or.out  () after 1304 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/sb.out  () after 1281 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/sh.out  () after 1397 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/simple.out () after 30 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/slli.out () after 658 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/sll.out  () after 1390 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/slti.out () after 650 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/sltiu.out () after 650 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/slt.out  () after 1290 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/sltu.out () after 1290 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/srai.out () after 696 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/sra.out  () after 1440 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/srli.out () after 684 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/srl.out  () after 1428 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/sub.out  () after 1282 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/sw.out  () after 1408 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/xori.out () after 530 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/asm_output/xor.out  () after 1302 simulation cycles
```

ASM TEST

←→

eeecs151-aaq [SSH: eda-2]

⌵

Makefile

Riscv151.v

! sim-rtl.yml

Cache_v1.v

Cache_2way.v

EMO > AsicProject > src > Riscv151.v

```
1 `include "const.vh"
2
3 // Editor: Evan Lin, Justine Tsai
4
5 module Riscv151(
6     input clk,
7     input reset,
8
9     // Memory system ports
10    output [31:0] dcache_addr,
11    output reg [31:0] icache_addr,
12    output [3:0] dcache_we,
13    output dcache_re,
14    output icache_re,
15    output [31:0] dcache_din,
16    input [31:0] dcache_dout,
17    input [31:0] icache_dout,
18    input stall, // if stall r <= w
19    output reg [31:0] csr
20 );
```

PROBLEMS

OUTPUT

TERMINAL

PORTS

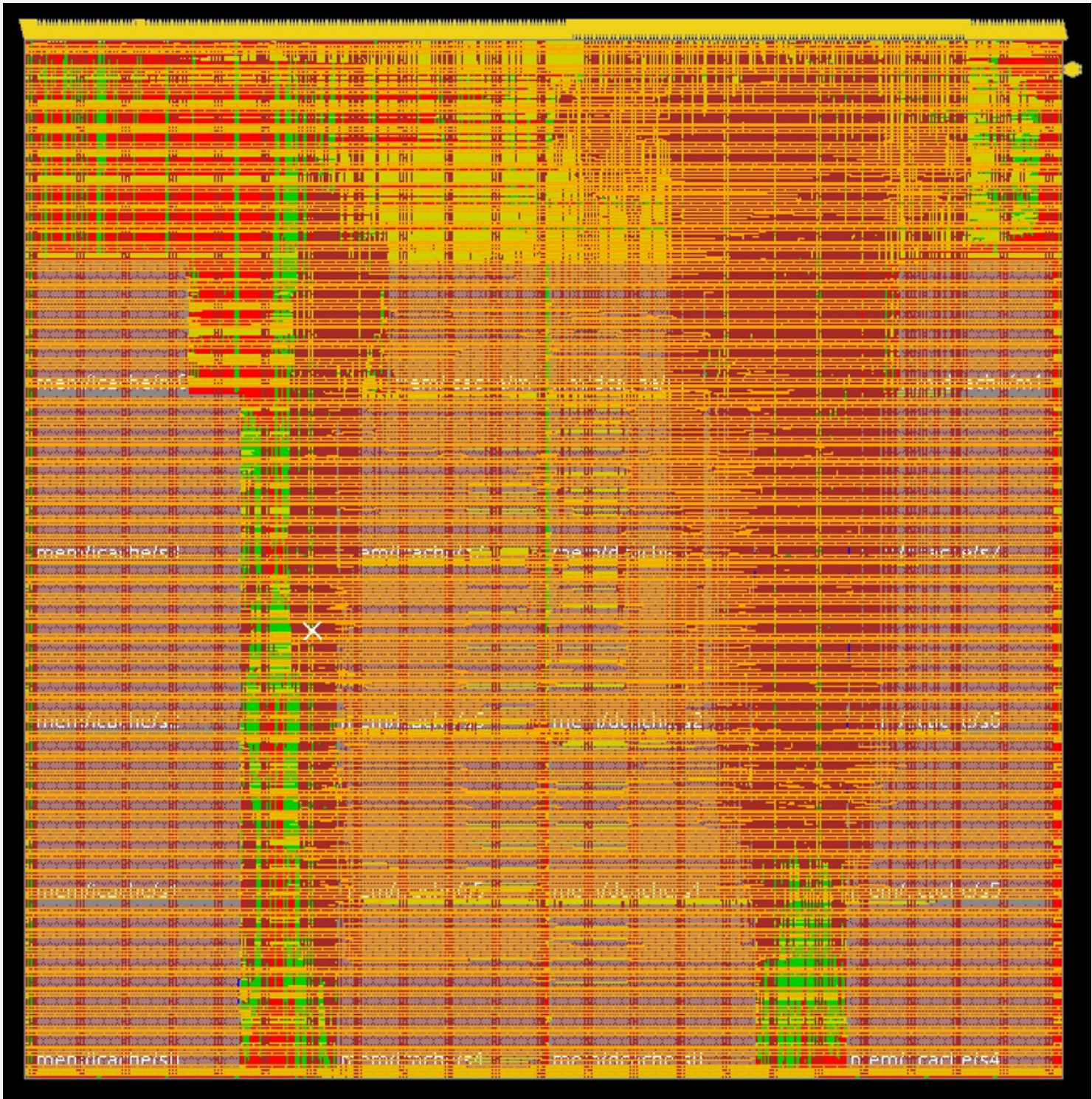
bash - AsicProject

```
$finish at simulation time                634552050100
mkdir -p /home/tmp/eeecs151-aaq/EMO/AsicProject/bmark_output
cd /home/tmp/eeecs151-aaq/EMO/AsicProject/build/sim-rundir && /home/tmp/eeecs151-aaq/EMO/AsicProject/build/sim-rundir/simv -q +ntb_random_seed_automatic +verbose
+max-cycles=500000000 +loadmem=/home/tmp/eeecs151-aaq/EMO/AsicProject/tests/bmark/replace.hex 2> /home/tmp/eeecs151-aaq/EMO/AsicProject/bmark_output/replace.out
&& [ $PIPESTATUS -eq 0 ]
Notice: timing checks disabled with +notimingcheck at compile-time
NOTE: automatic random seed used: 818384060
$finish called from file "/home/tmp/eeecs151-aaq/EMO/AsicProject/src/riscv_test_harness.v", line 219.
$finish at simulation time                634607750100

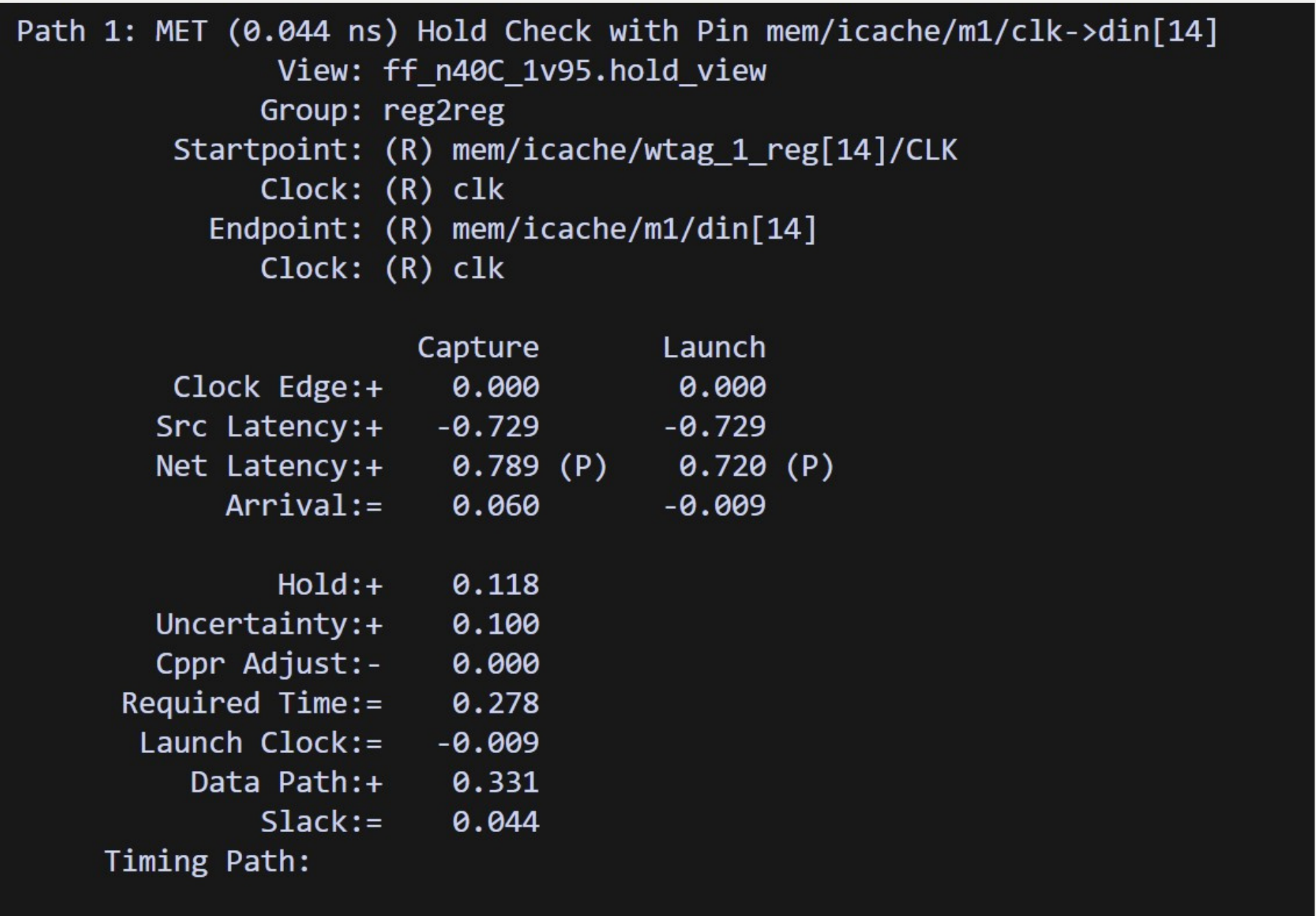
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/bmark_output/cachetest.out  () after 5327428 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/bmark_output/final.out  () after 12091 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/bmark_output/fib.out  () after 9711 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/bmark_output/sum.out  () after 31727604 simulation cycles
[ PASSED ] /home/tmp/eeecs151-aaq/EMO/AsicProject/bmark_output/replace.out  () after 31730389 simulation cycles
```

BENCHMARK TEST

PnR and Timing(2-way associative cache)



FLOOR PLAN



TIMING REPORT (POST-PAR)