VLSI Testing PA3

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1. For *tdfsim.cpp,* I refer to *faultsim.cpp* but modify it to adjust to TDF. First, transition_delay_fault_simulation() is quite same as fault_simulate_vectors(). Second, tdf_sim_vector_one() and tdf_sim_vector_two() are modified from fault_sim_a_vector(). Since we have two patterns to assign and simulate, I divide it into two functions. tdf_sim_vector_one() is a lot easy. Set the input, initialize the circuit and do the sim(), which is in *sim.cpp.* And check fault activation. tdf_sim_vector_two() part 1 is same as tdf_sim_vector_one() but in part 2, we then have to store fault free value and check undetected fault if fault is activated after performing tdf_sim_vector_one(). At last, do the fault simulation and fault dropping. This part is also the same as part of fault_sim_a_vector().

circuit number	number of gates	number of total TDFs	number of detected faults	number of undetected faults	Transition delay fault coverage
C17	6	34	23	11	67.64%
C432	245	1110	3	1107	0.27%
C499	554	2390	1552	838	64.93%
C880	545	2104	792	1312	37.64%
C1355	554	2726	593	2133	21.75%
C2670	1785	6520	4668	1852	71.59%
C3540	2082	7910	1142	6768	14.43%
C6288	4800	17376	16532	844	95.14%
C7552	5679	19456	17421	2035	89.54%

2. For generate_tdfault_list(), I refer to *init_flist.cpp* but modify with no fault collapsing. The reason that we cannot collapse TDFs is that TDFs are not consistent across all gates. We can simply find that through a truth table of a two-input AND gate. All six TDFs about this AND gate are not equivalent(according to midterm exam).