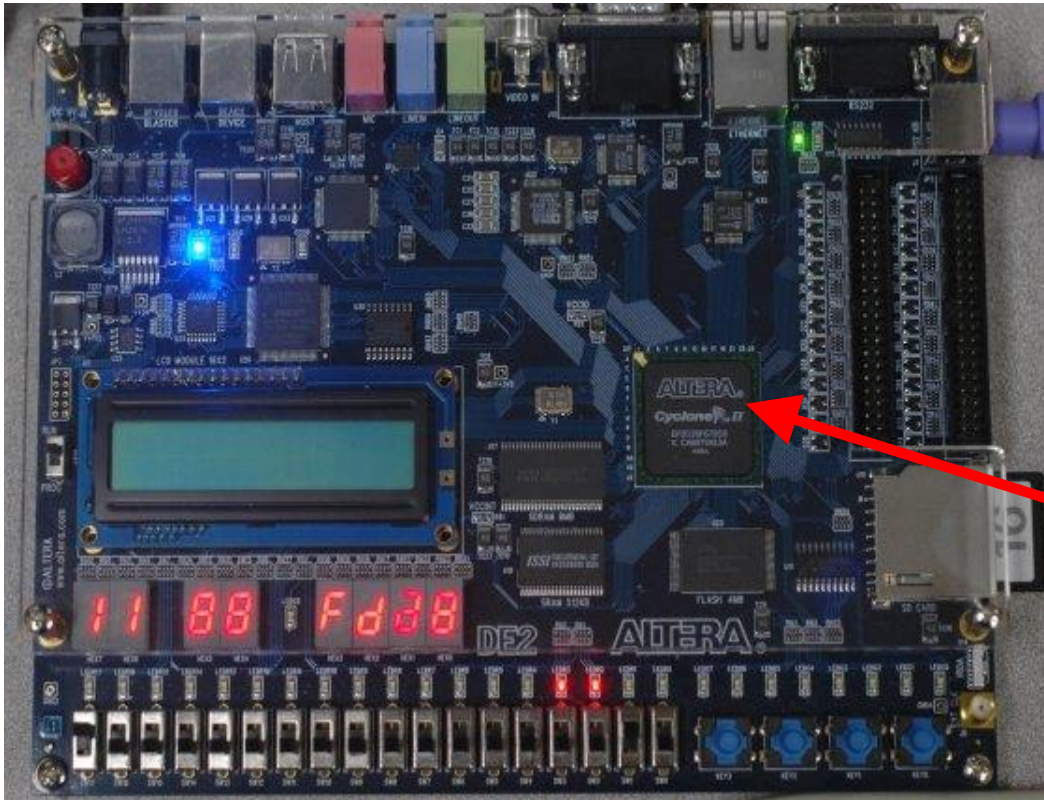


# FPGAs at a glance

The background features a dark blue gradient at the bottom, transitioning into a series of overlapping, wavy, light blue lines that create a sense of depth and movement. The top of the image has a dark blue header bar with a thin white line running across it.

## □ What FPGAs look like?

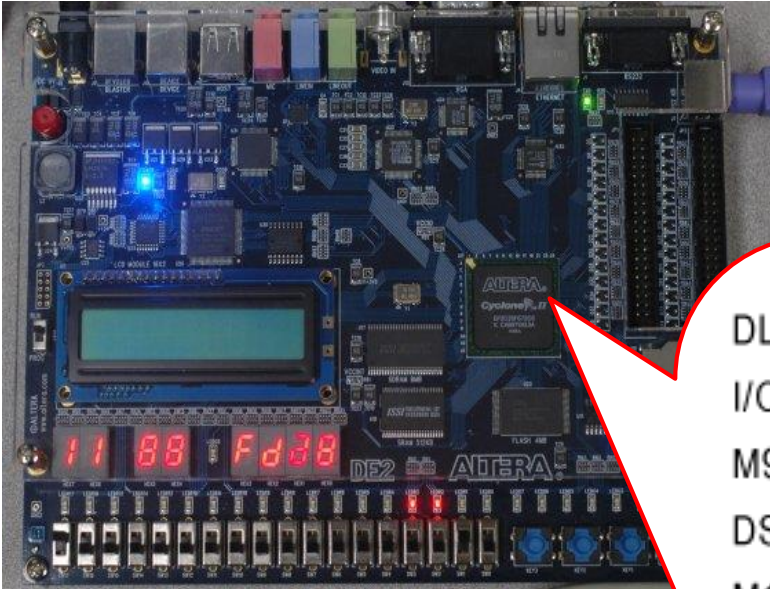
From the outside:



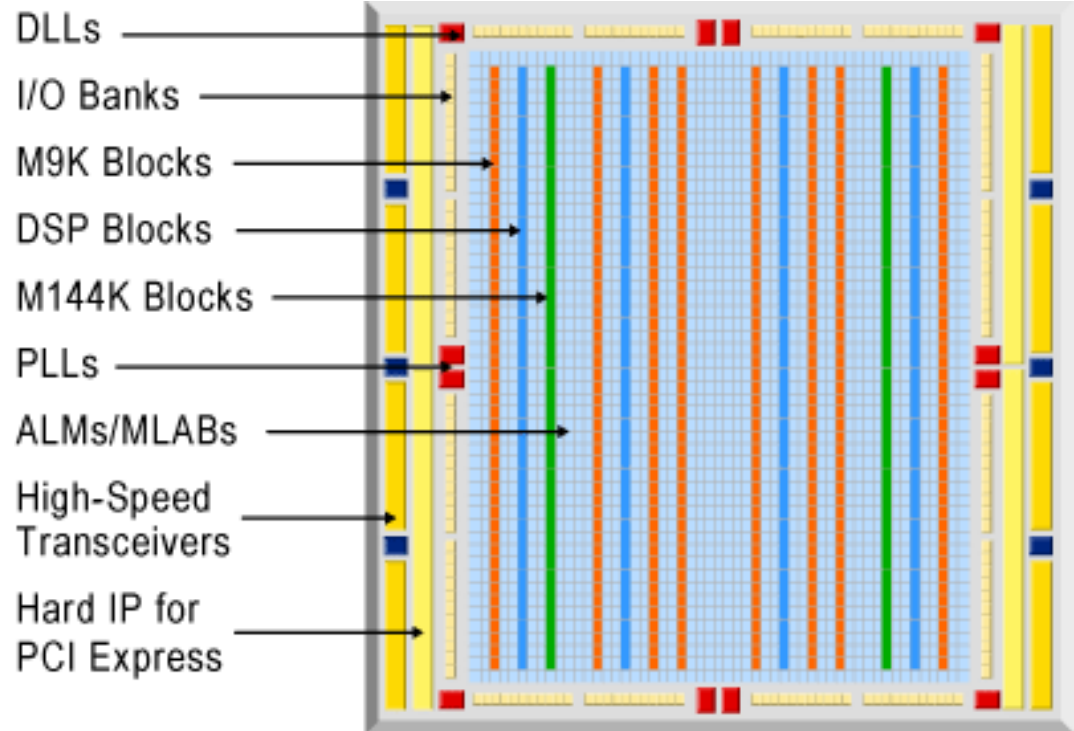
The FPGA !!

## □ What FPGAs look like?

From the outside:

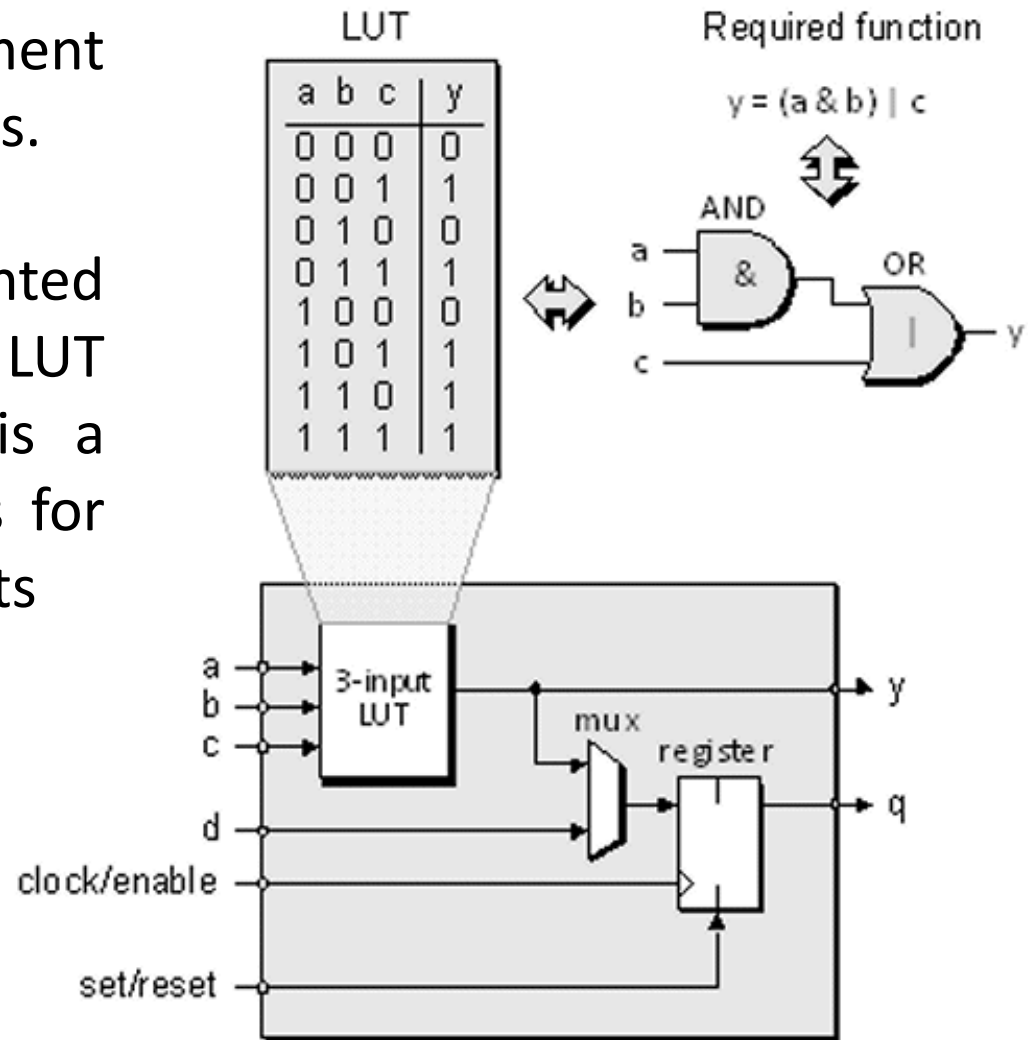


From the inside:



## □ The Look-Up Table (LUT)

- The basic logic unit of an FPGA that is used to implement combination logic instances.
- All functions are implemented as truth tables within a LUT memory. A truth table is a predefined list of outputs for every combination of inputs

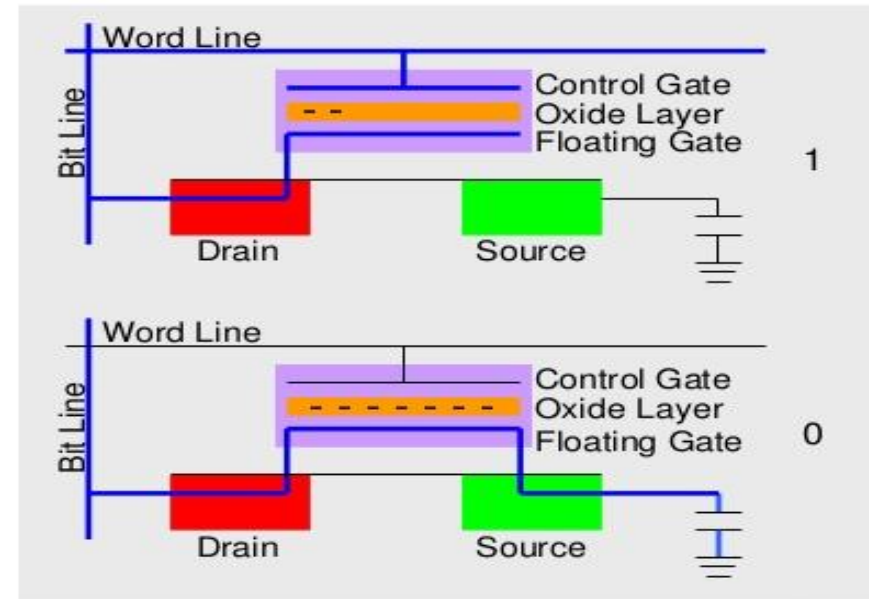
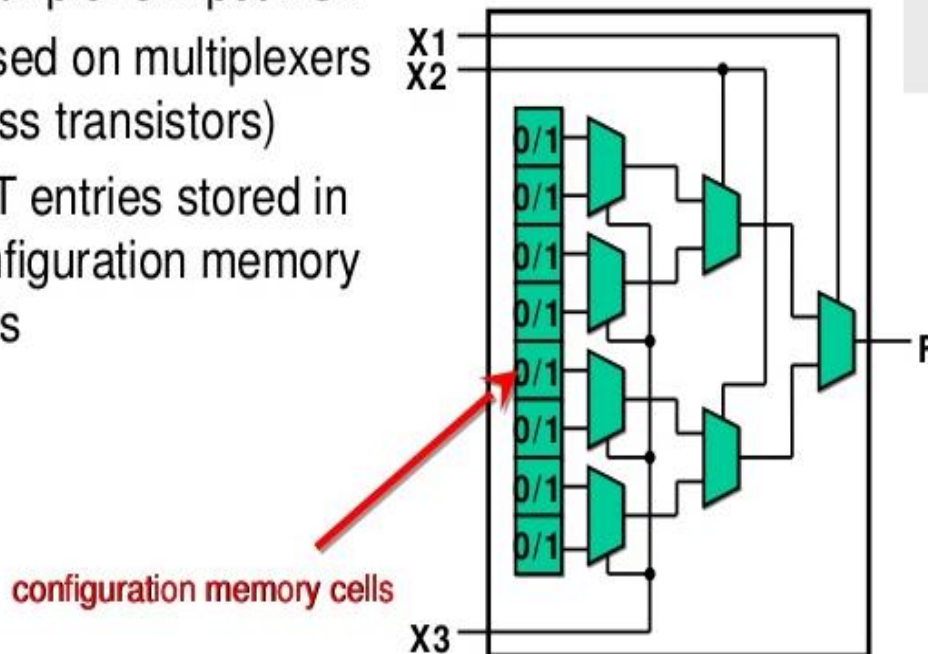




# FPGA architecture

## LUT Implementation

- Example: 3-input LUT
- Based on multiplexers (pass transistors)
- LUT entries stored in configuration memory cells

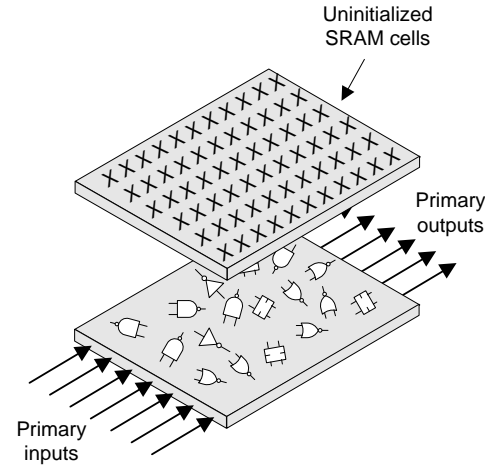
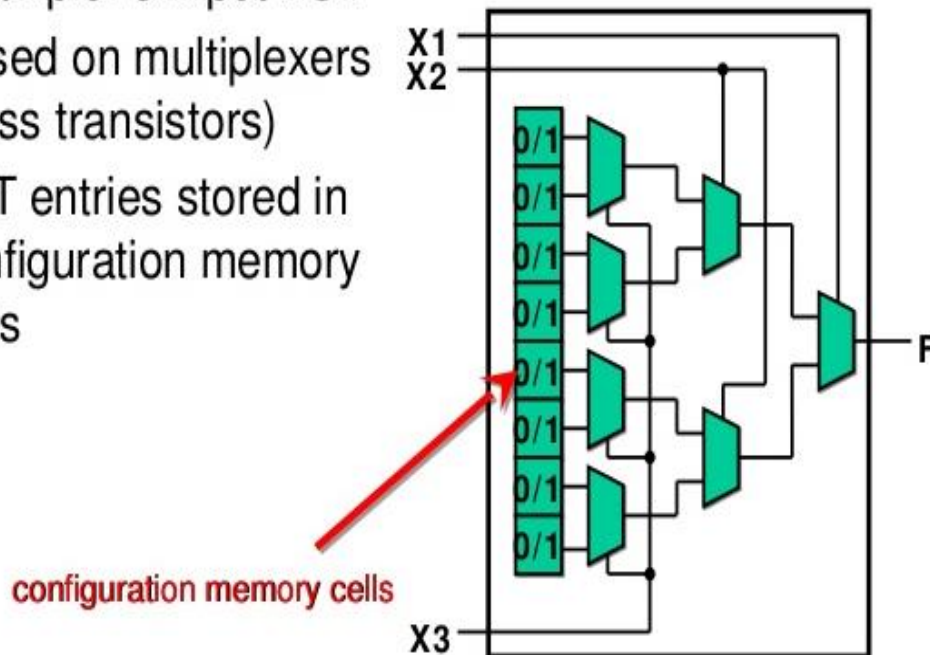




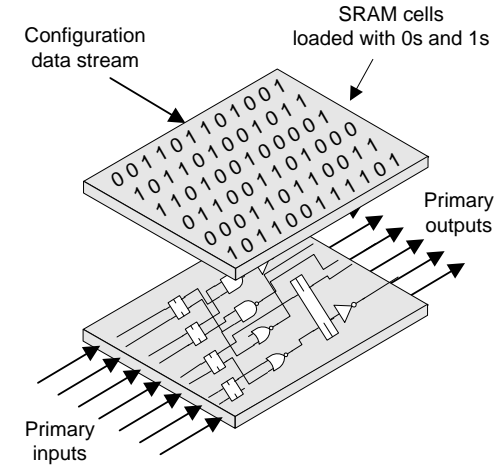
# FPGA architecture

## LUT Implementation

- Example: 3-input LUT
- Based on multiplexers (pass transistors)
- LUT entries stored in configuration memory cells



(a) Unconfigured



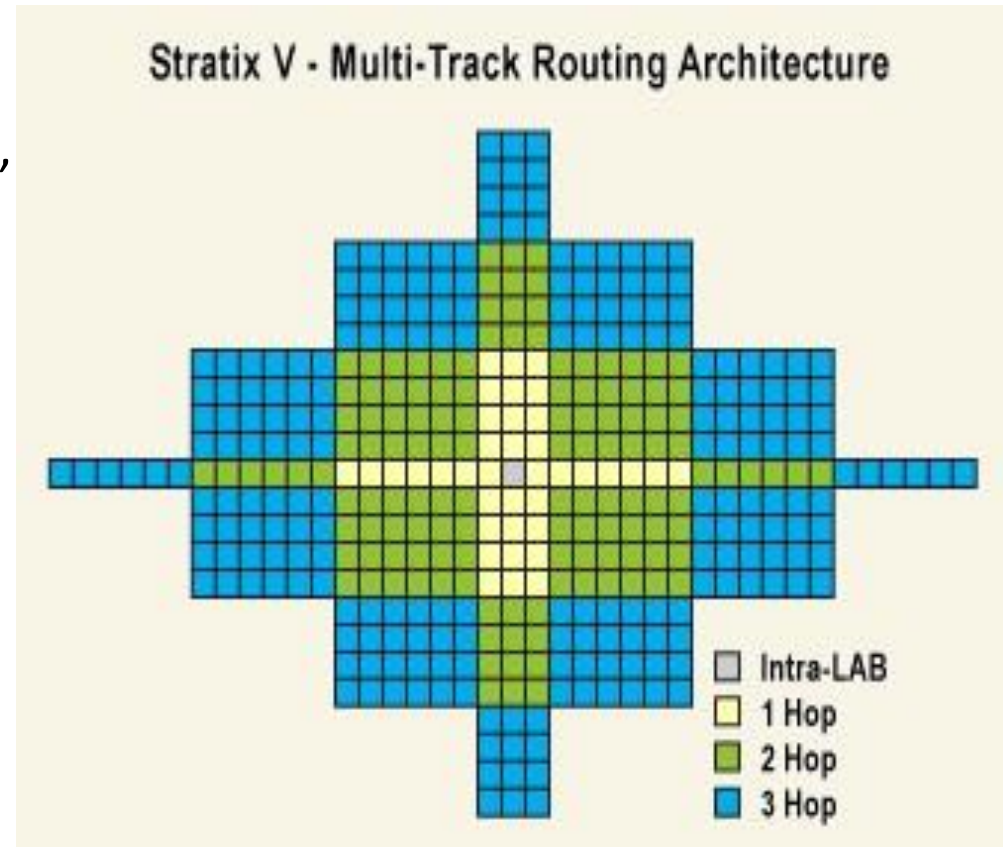
(b) Configured

## MultiTrack Interconnect

The ALMs are routed with the MultiTrack interconnect architecture, enabling FPGAs to implement high-speed logic, arithmetic, and register functions.

### MultiTrack Interconnect:

This technology consists of continuous, performance-optimized routing lines of different lengths used for communication within and between distinct design blocks.

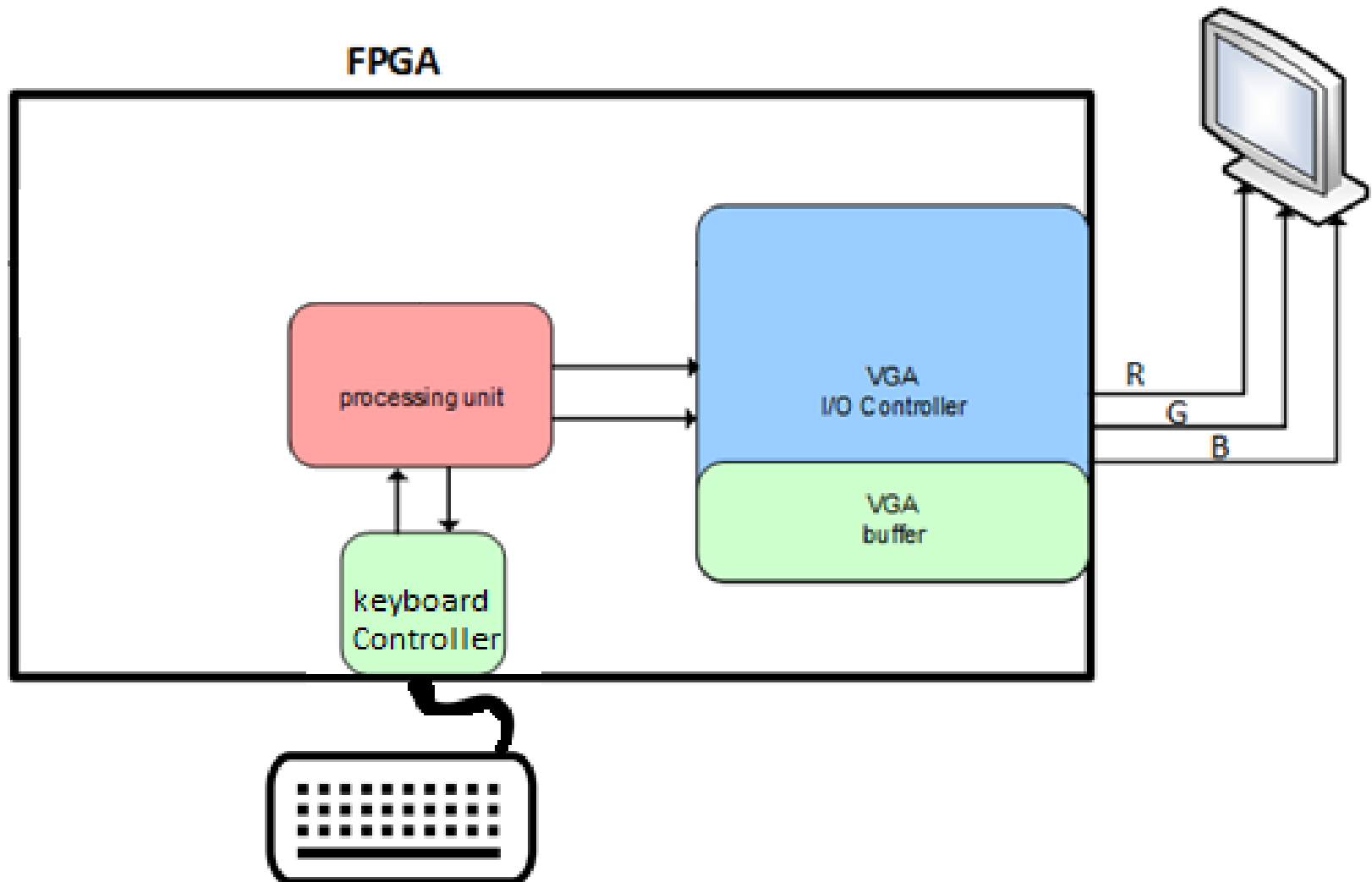


# FPGA Design

The background features a dark blue gradient at the bottom, transitioning into a series of overlapping, wavy, light blue lines that create a sense of depth and movement. The top of the image has a dark blue header bar with a thin white line running across it.

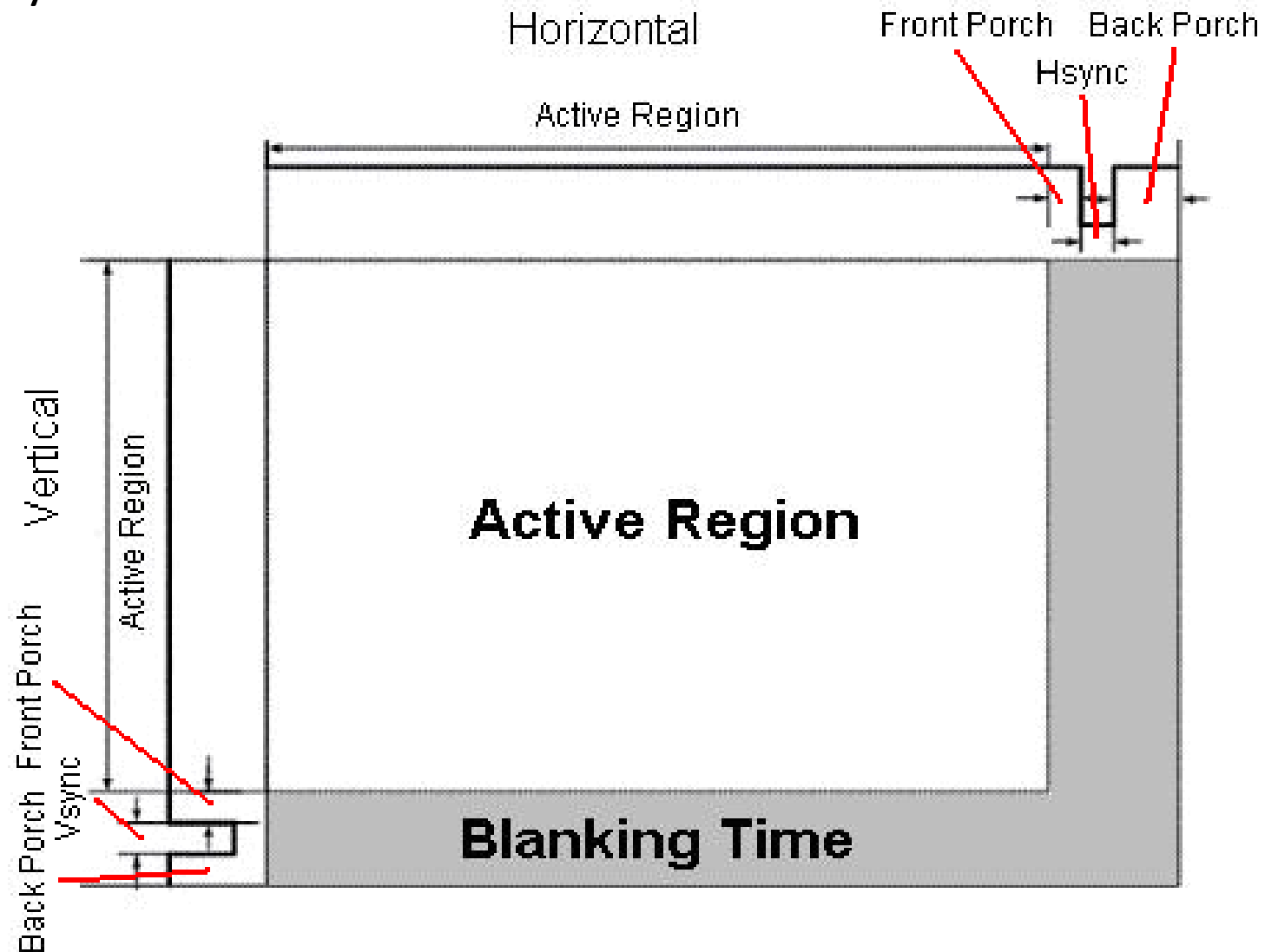


## □ Developing simple examples



## □ VGA controller

### ➤ Synchronization



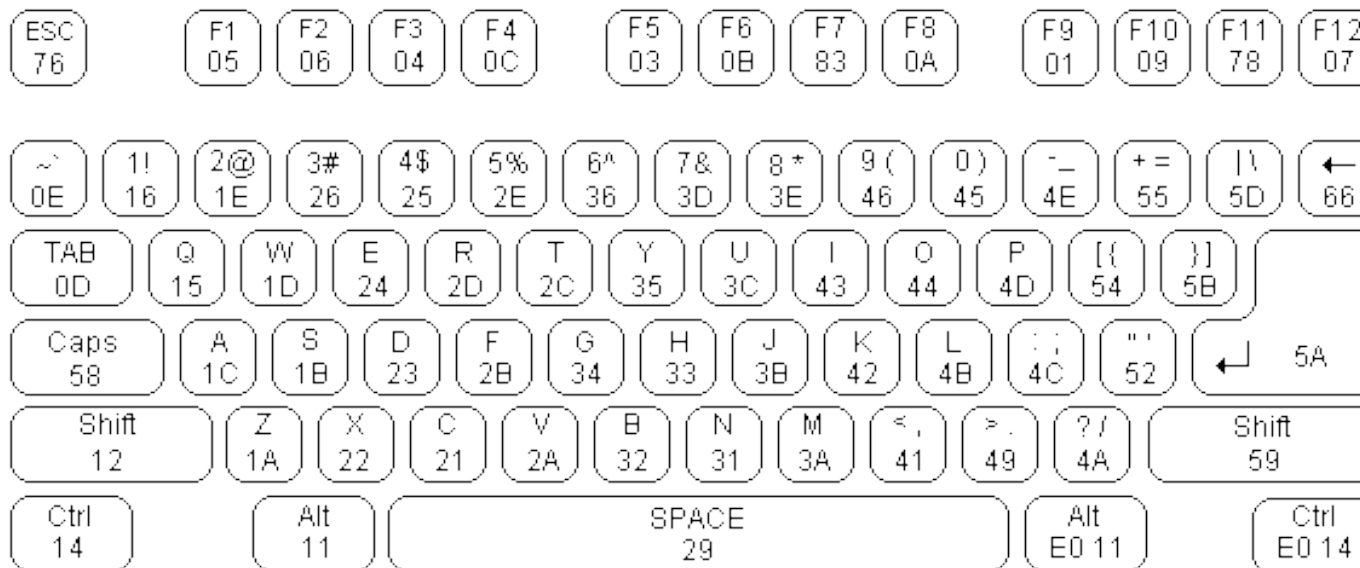
## VGA controller

### ➤ Timings for various resolution:

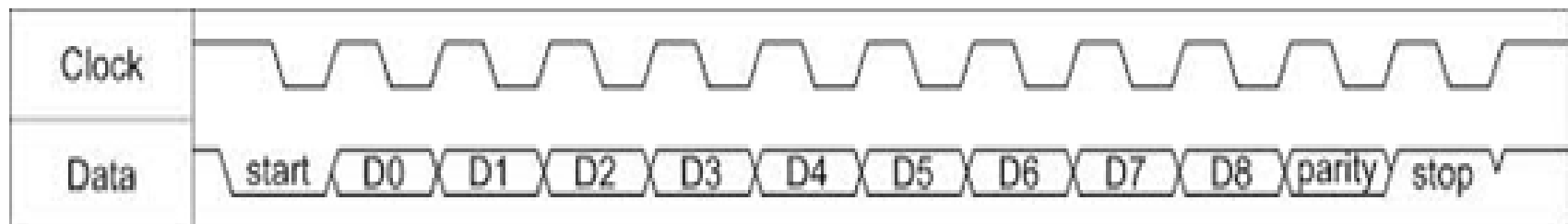
Format	Pixel Clock (MHz)	Horizontal (in Pixels)				Vertical (in Lines)			
		Active Video	Front Porch	Sync Pulse	Back Porch	Active Video	Front Porch	Sync Pulse	Back Porch
640x480, 60Hz	25.175	640	16	96	48	480	11	2	31
640x480, 72Hz	31.500	640	24	40	128	480	9	3	28
640x480, 75Hz	31.500	640	16	96	48	480	11	2	32
640x480, 85Hz	36.000	640	32	48	112	480	1	3	25
800x600, 56Hz	38.100	800	32	128	128	600	1	4	14
800x600, 60Hz	40.000	800	40	128	88	600	1	4	23
800x600, 72Hz	50.000	800	56	120	64	600	37	6	23
800x600, 75Hz	49.500	800	16	80	160	600	1	2	21
800x600, 85Hz	56.250	800	32	64	152	600	1	3	27
1024x768, 60Hz	65.000	1024	24	136	160	768	3	6	29
1024x768, 70Hz	75.000	1024	24	136	144	768	3	6	29
1024x768, 75Hz	78.750	1024	16	96	176	768	1	3	28
1024x768, 85Hz	94.500	1024	48	96	208	768	1	3	36

## Keyboard controller

### ➤ The make scan codes



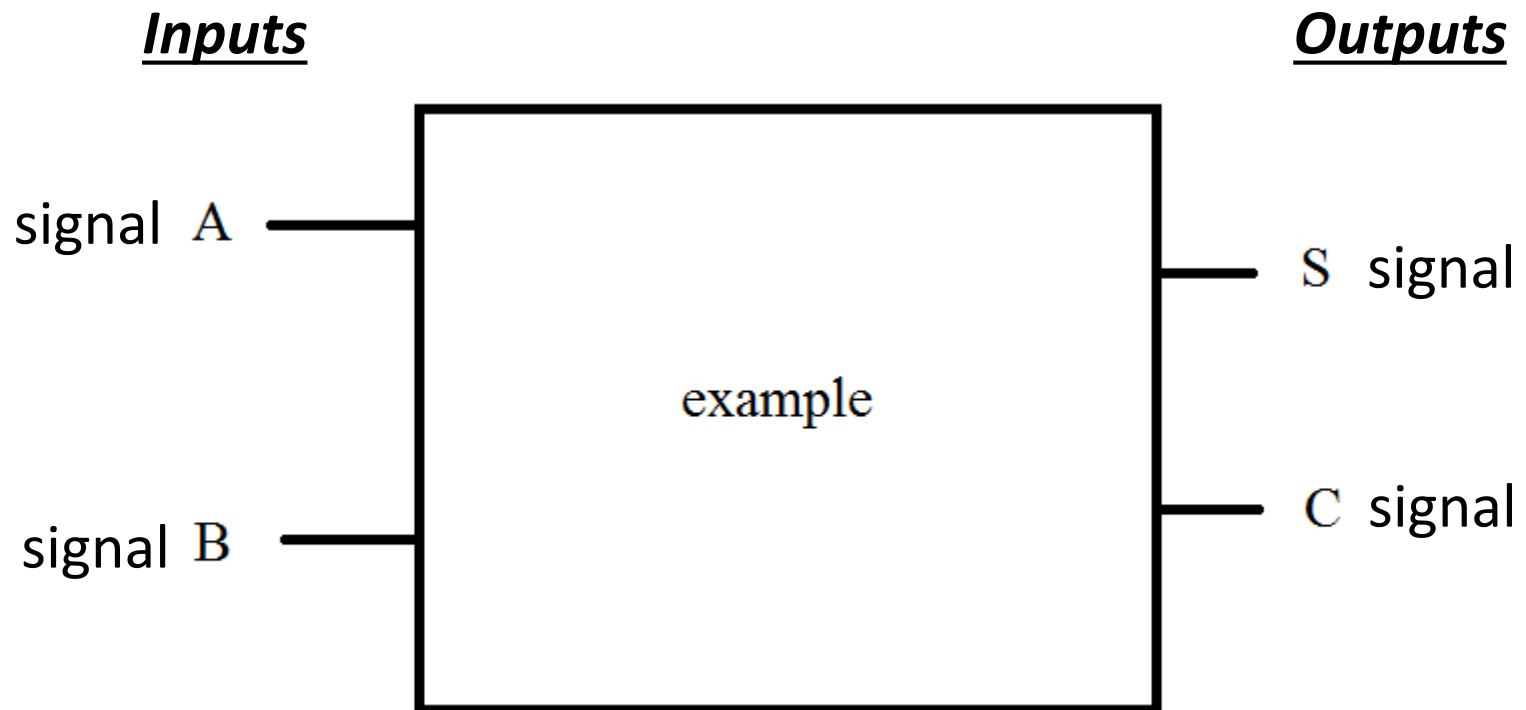
### ➤ How PS/2 works:





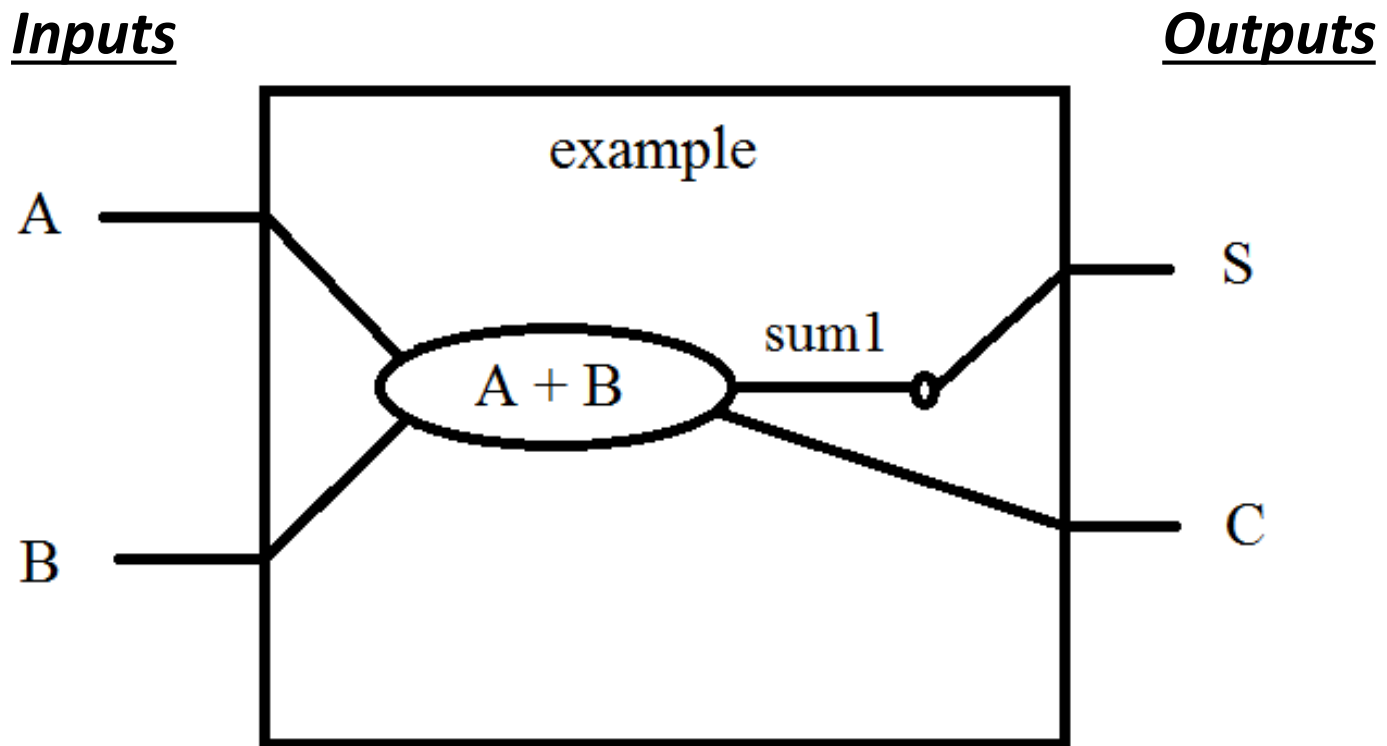
## □ A simple example: Full Adder

➤ The Entity:



## □ A simple example: Full Adder

➤ Internal architecture:

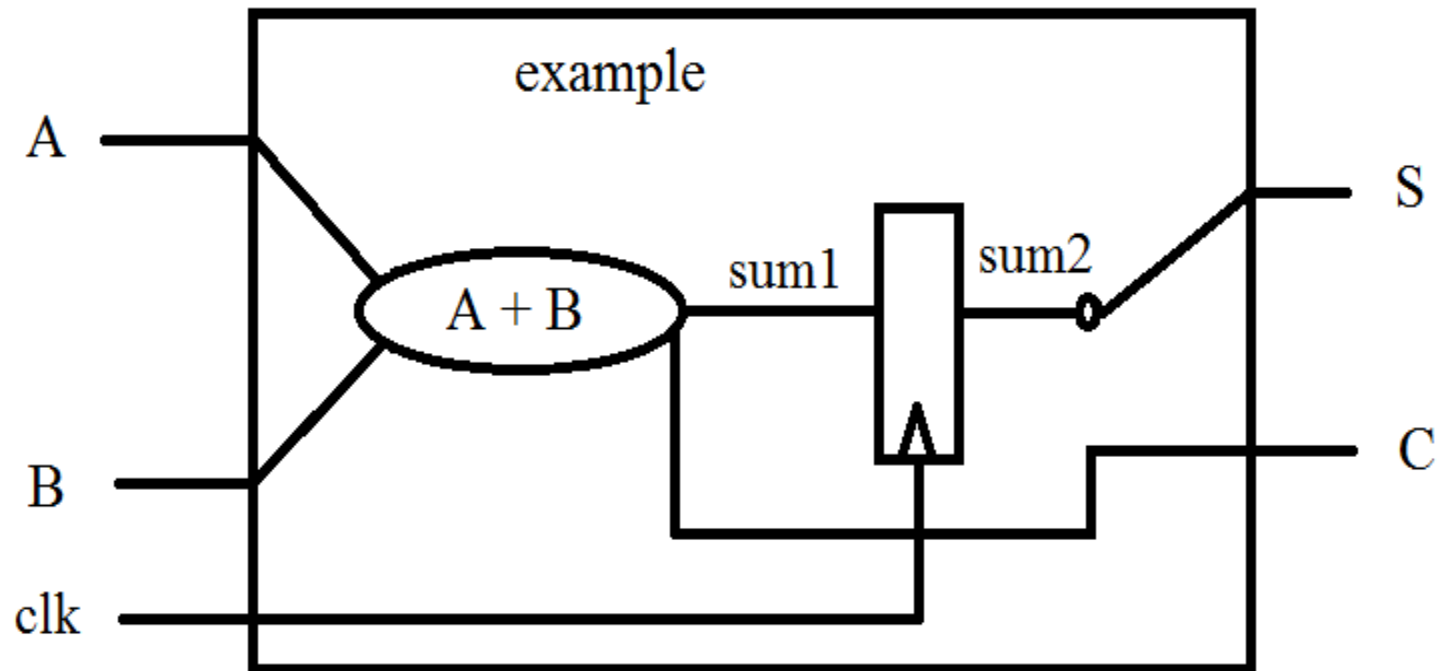


## □ A simple example: Full Adder

➤ Insert timing:

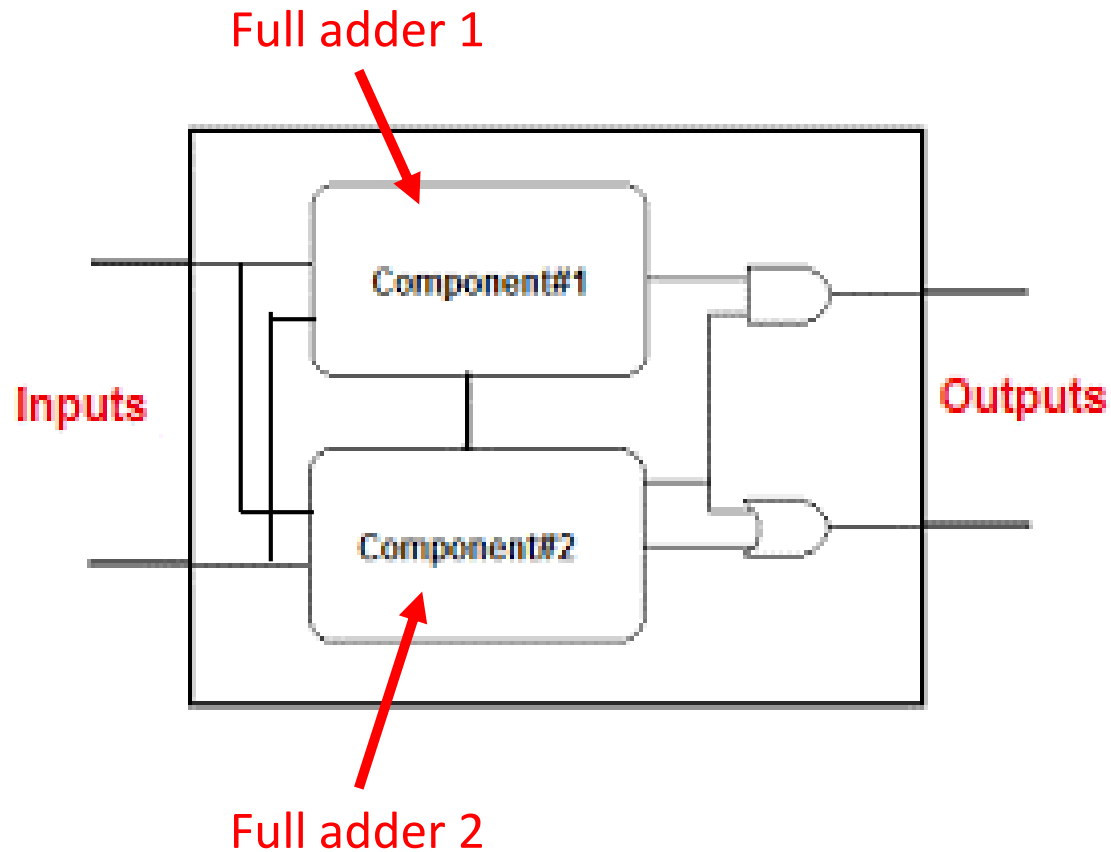
Inputs

Outputs



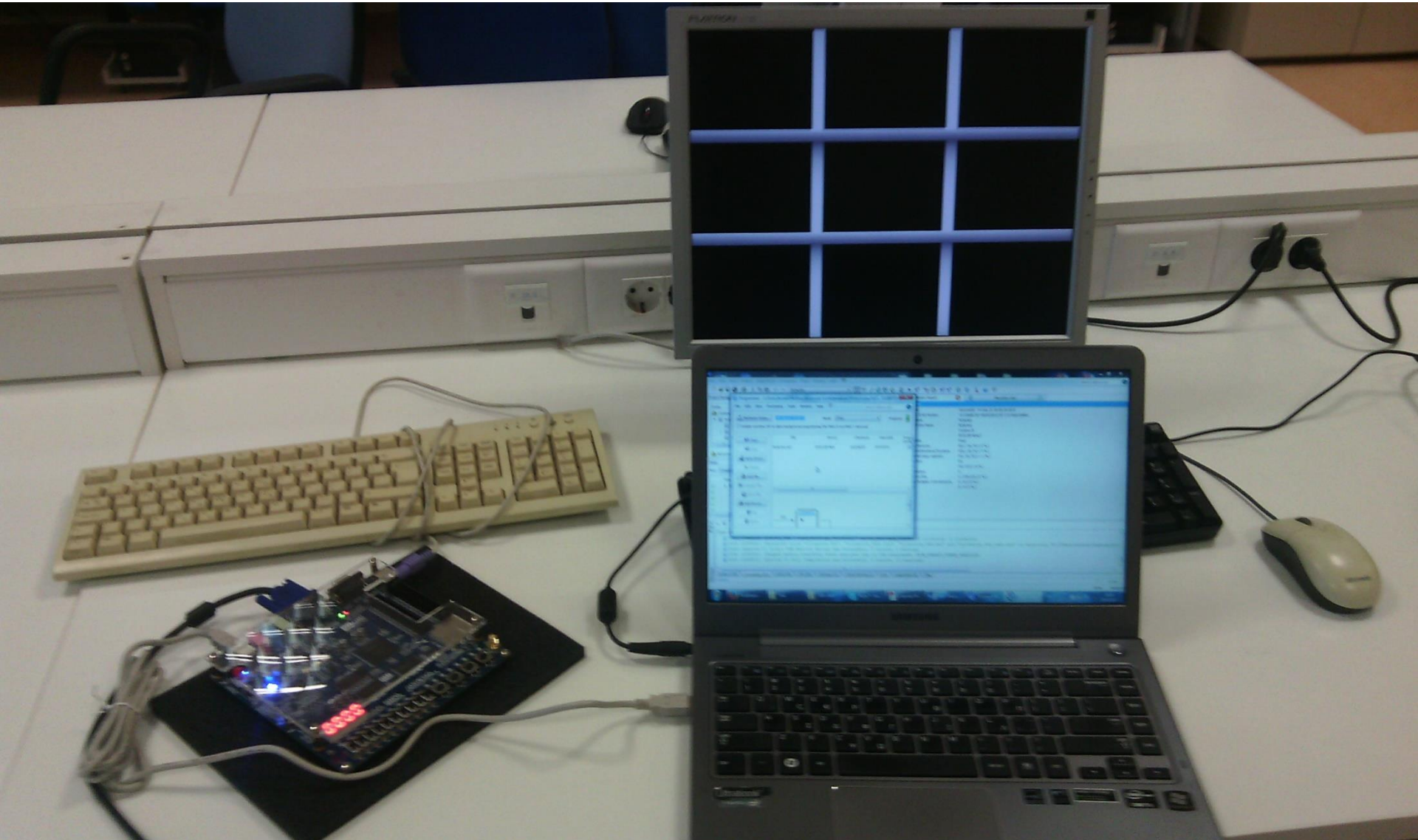
## Combining circuits

- Using 2 full adders:

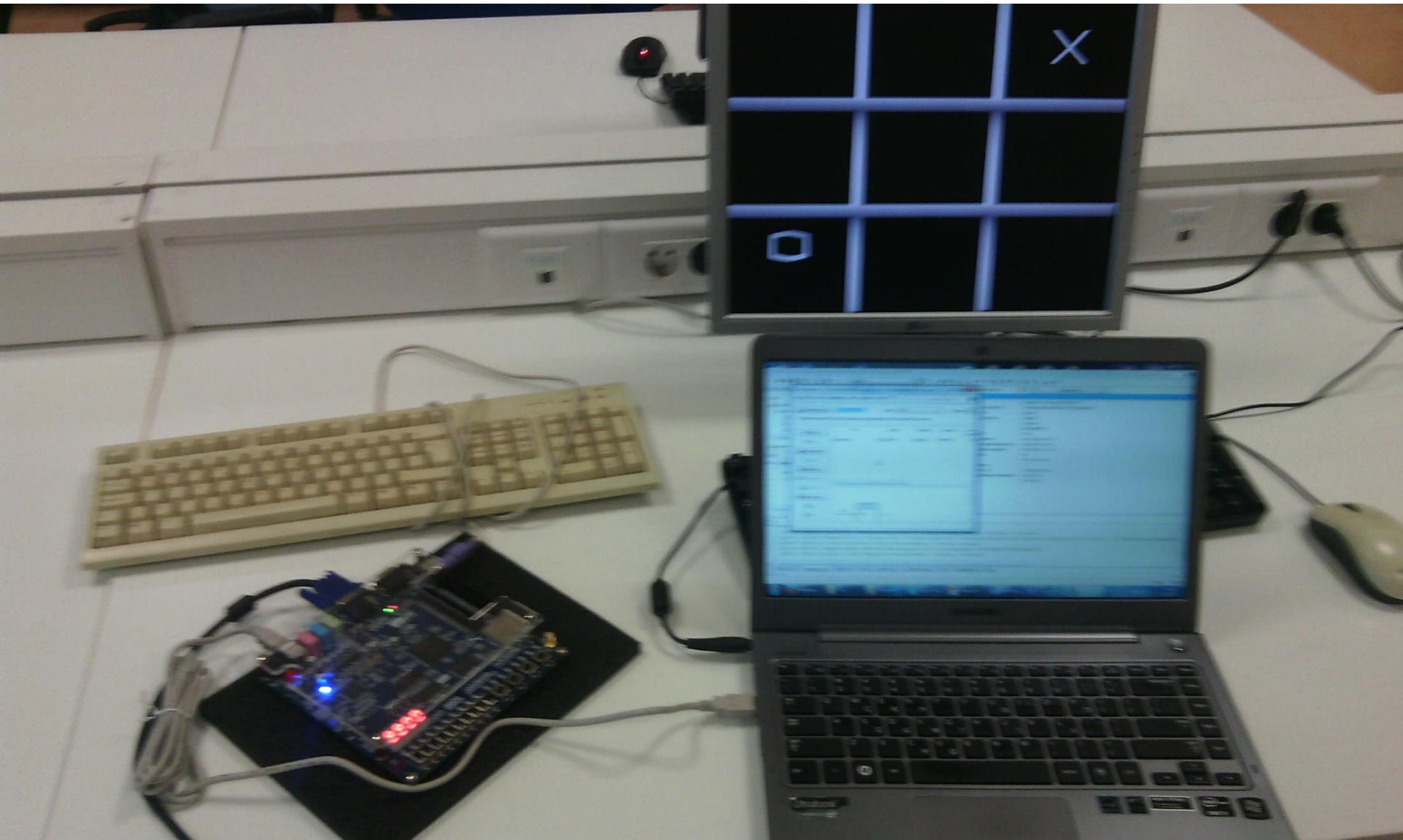




## □ The project examples: Tic Tac Toe

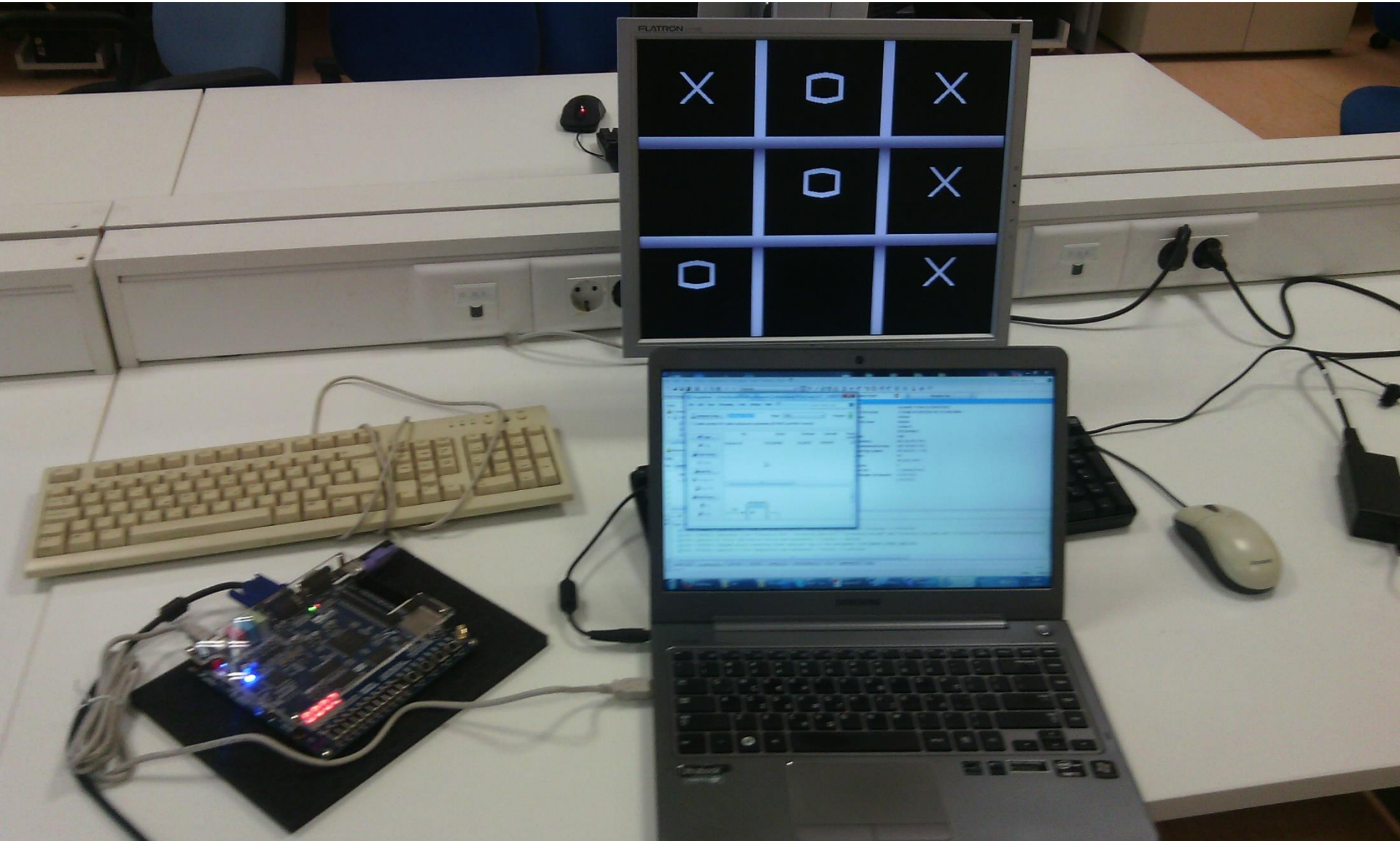


## □ The project examples: Tic Tac Toe

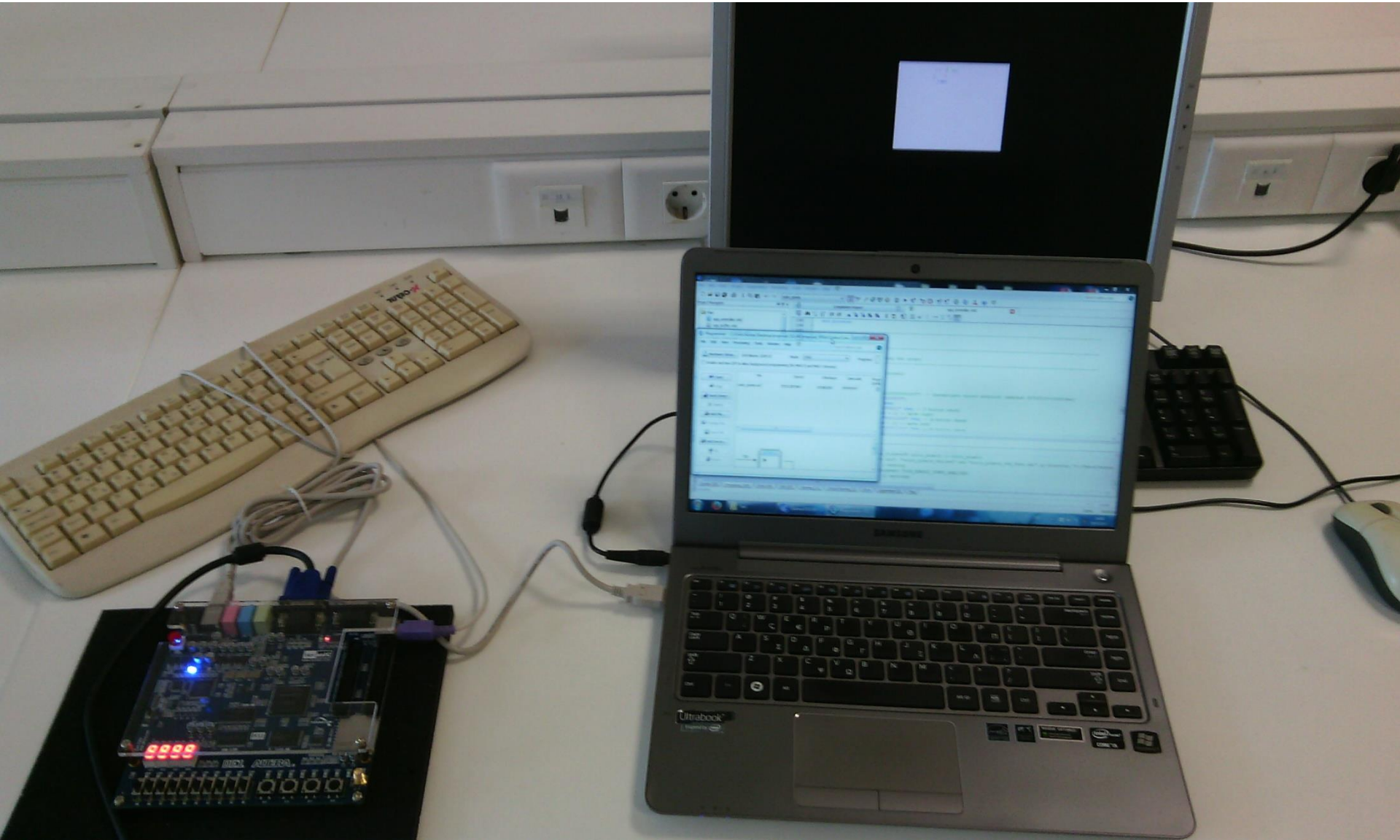




## □ The project examples: Tic Tac Toe

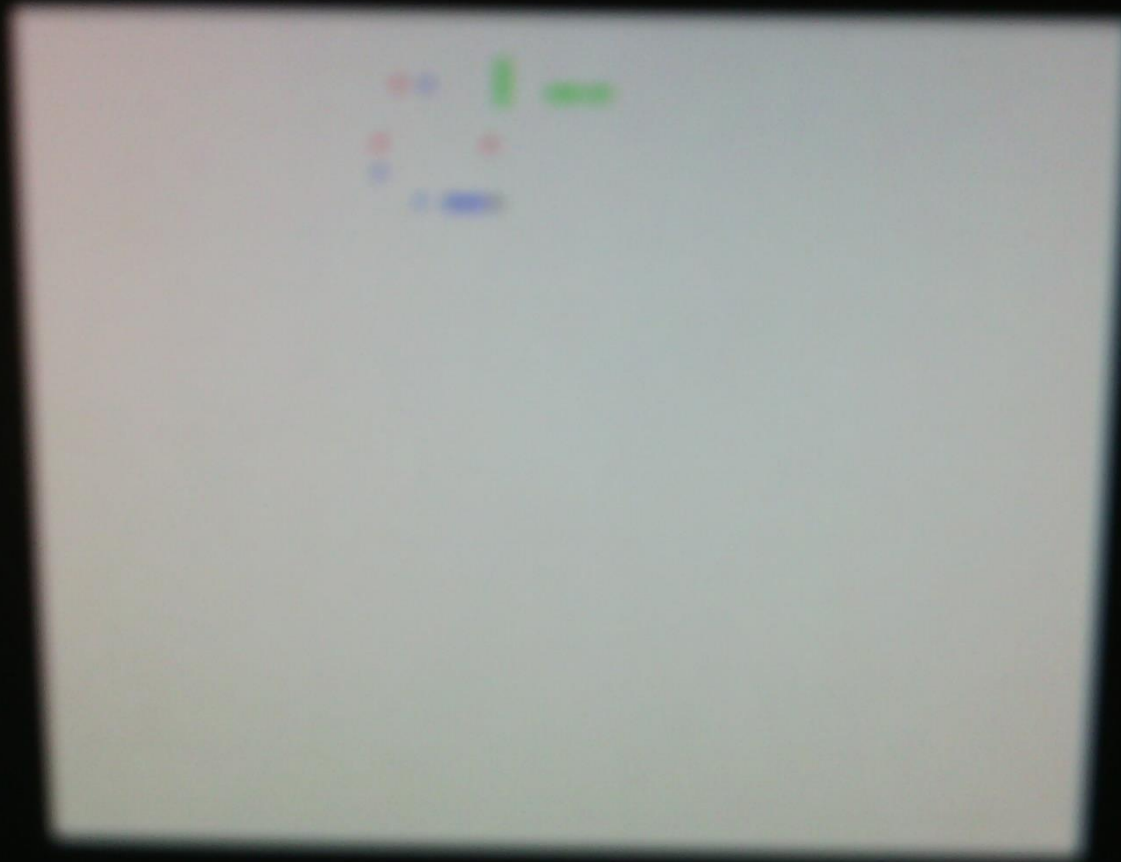


## □ The project examples: Color Pixels





## ❑ The project examples: Color Pixels

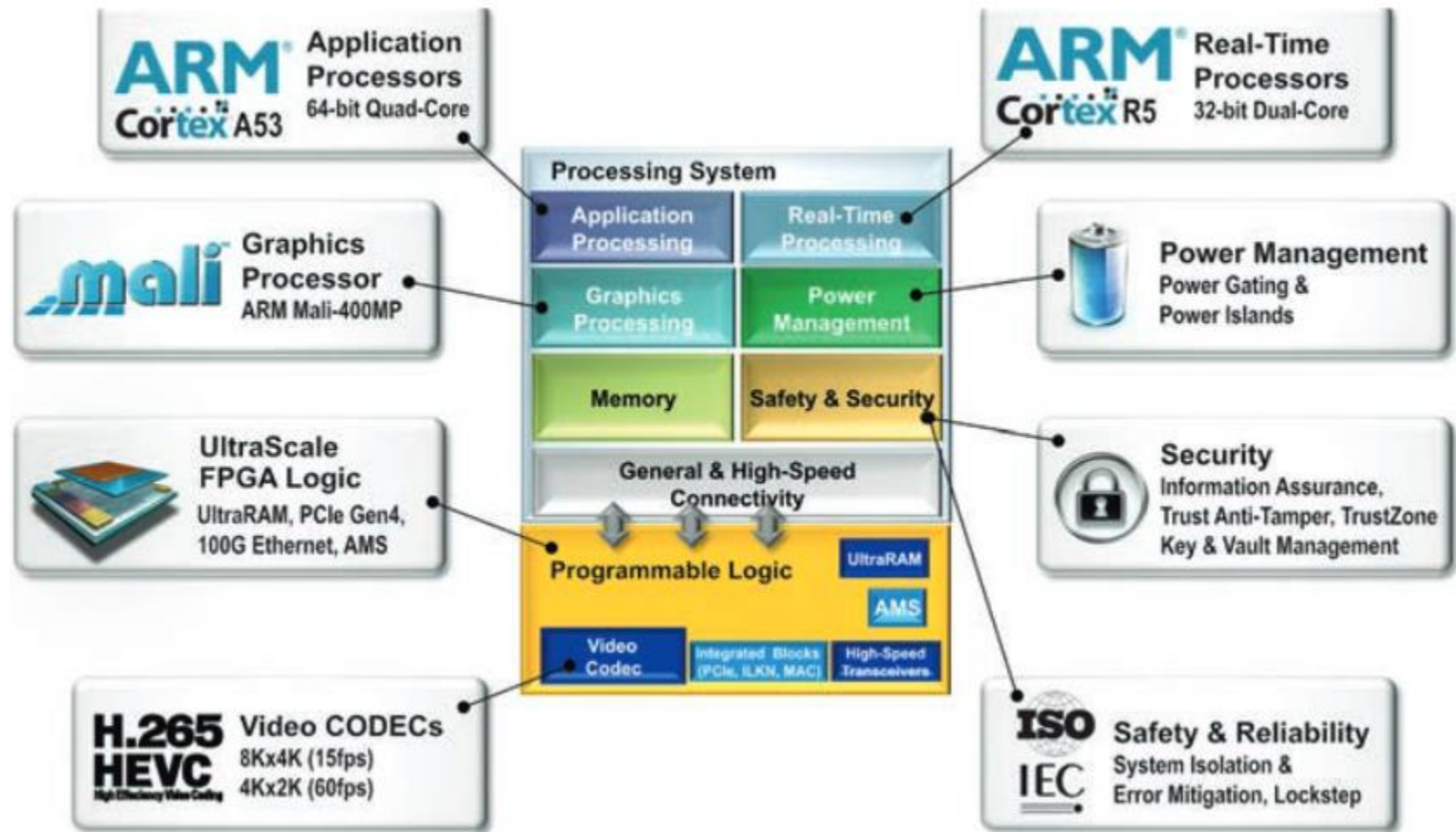




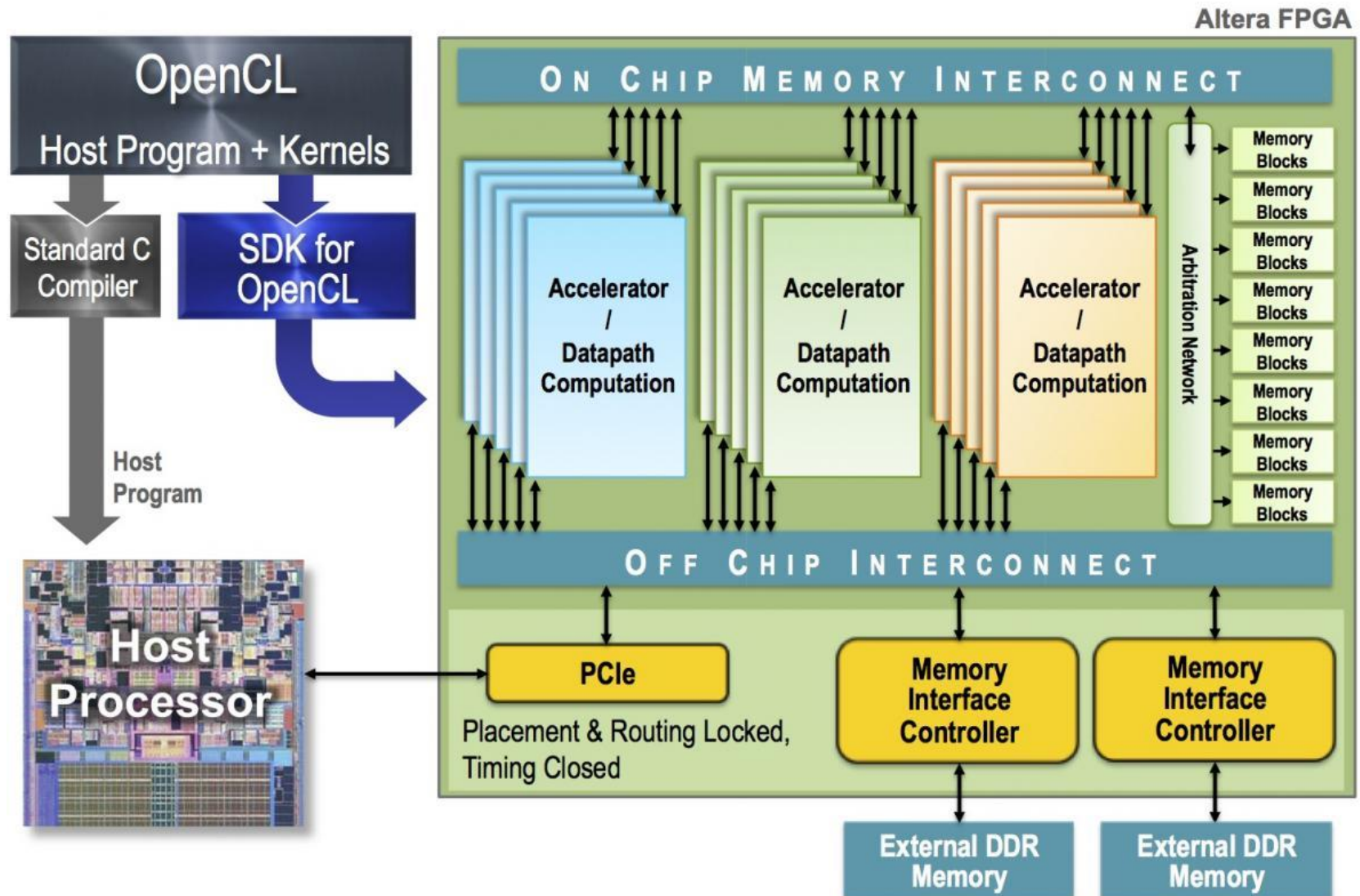
# FPGAs

## The big picture

# Xilinx's Zynq UltraScale+ MPSoC



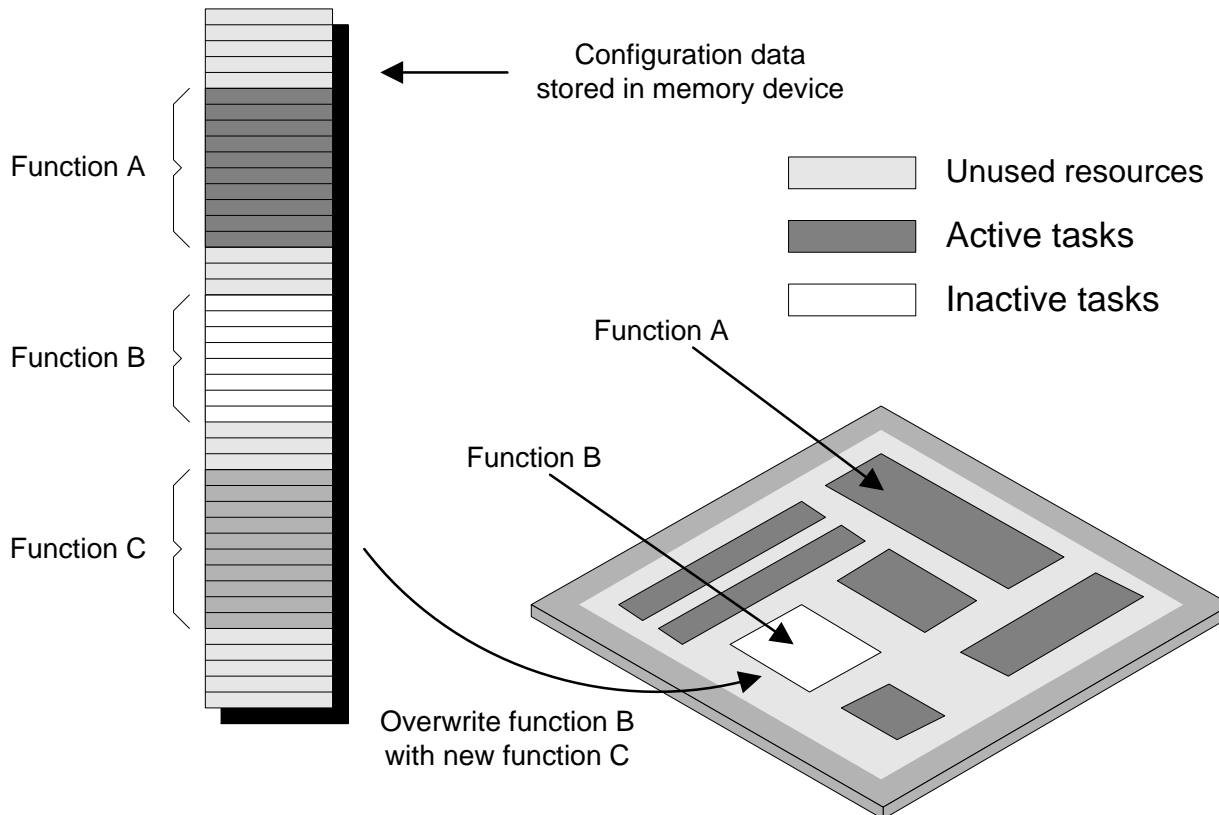
## FPGA acceleration



## FPGA acceleration

### ✓ Intel bought Altera for **\$16,7 Billion**

By acquiring FPGA technology, Intel is thinking outside the CPU, now that the execution of tasks is increasingly off-loaded to graphics processors and other accelerators.

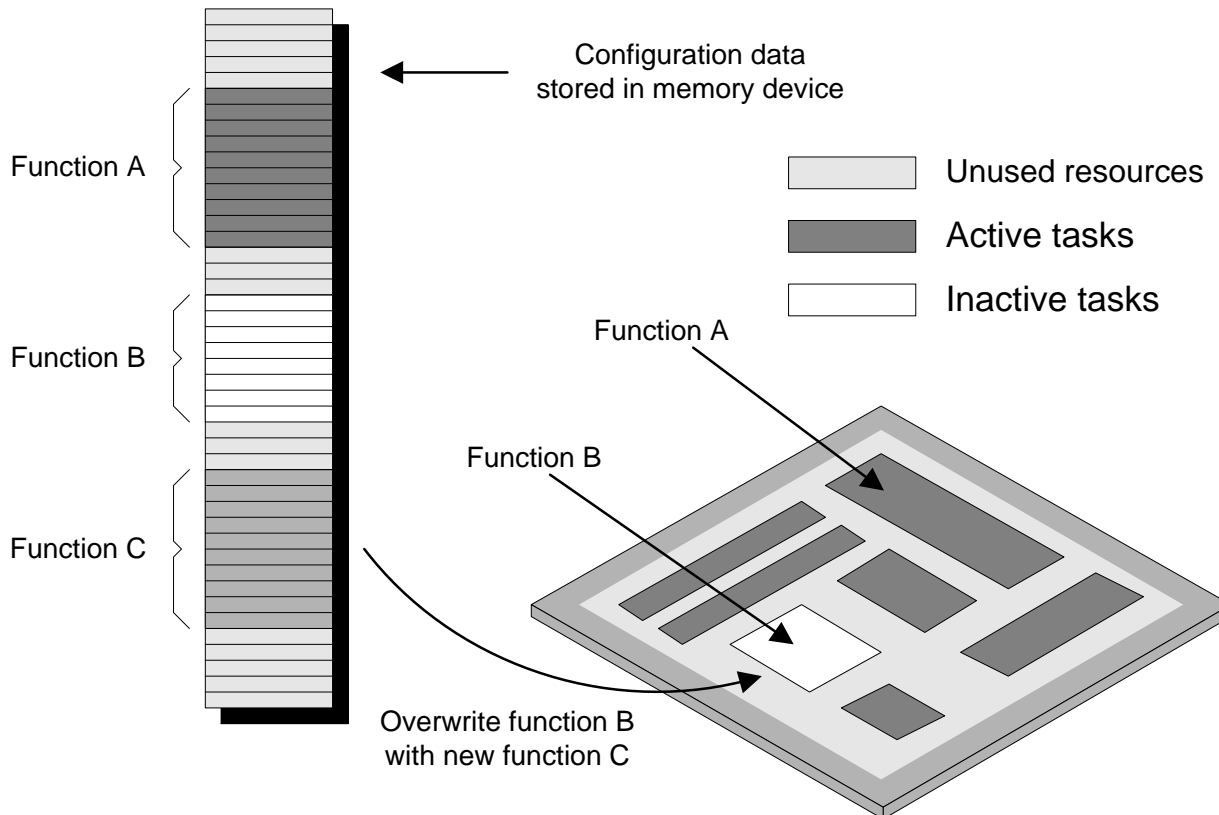




## FPGA acceleration

### ✓ Intel bought Altera for **\$16,7 Billion**

Intel is offering server makers and companies building data centers, the option to package server chips with FPGAs, which are being used for dedicated functions like search, sorting and character matching.



## FPGA acceleration

- High Performance Computing
  - ◆ CRAY XD1 : OPTERON + FPGA

