2017-EE

EE24BTECH11020 - Ellanti Rohith

1) Consider the differential equation

$$\left(t^2 - 81\right)\frac{dy}{dt} + 5t\,y = \sin(t) \quad \text{with } y(1) = 2\pi.$$

There exists a unique solution for this differential equation when t belongs to the interval

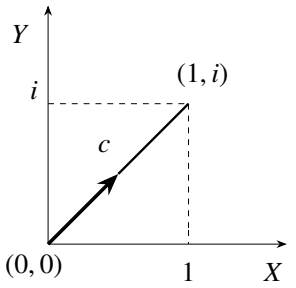
[GATE 2017]

a) $(-2, 2)$
b) $(-10, 10)$
c) $(-10, 2)$
d) $(0, 10)$

2) Consider the line integral

$$I = \int_C \left(x^2 + iy\right) dz,$$

where $z = x + iy$. The line C is shown in the figure below.

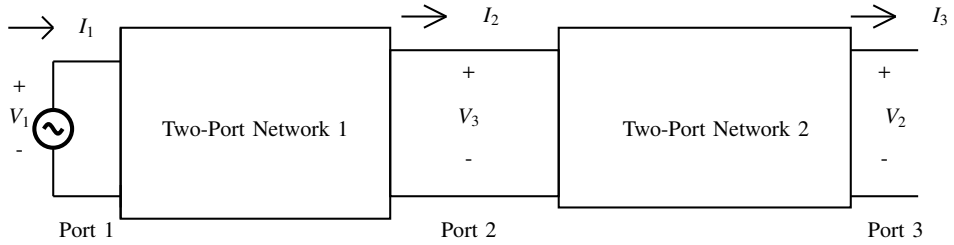


The value of I is

[GATE 2017]

a) $\frac{1}{2}i$
b) $\frac{2}{3}i$
c) $\frac{3}{4}i$
d) $\frac{4}{5}i$

3) Two passive two-port networks are connected in cascade as shown in the figure. A voltage source is connected at port 1.



Given

$$V_1 = A_1 V_2 + B_1 I_2$$
$$I_1 = C_1 V_2 + D_1 I_2$$
$$V_2 = A_2 V_3 + B_2 I_3$$
$$I_2 = C_2 V_3 + D_2 I_3$$

where $A_1, B_1, C_1, D_1, A_2, B_2, C_2$ and D_2 are the generalized circuit constants. If the Thevenin equivalent circuit at port 3 consists of a voltage source V_T and an impedance Z_T, connected in series, then

[GATE 2017]

a) $V_T = \dfrac{V_1}{A_1 + A_2}, \quad Z_T = \dfrac{A_1 B_2 + B_1 D_2}{A_1 A_2}$

b) $V_T = \dfrac{V_1}{A_1 A_2 + B_1 C_2}, \quad Z_T = \dfrac{A_1 B_2 + B_1 D_2}{A_1 A_2 + B_1 C_2}$

c) $V_T = \dfrac{V_1}{A_1 + A_2}, \quad Z_T = \dfrac{A_1 A_2 + B_1 C_2}{A_1 A_2 + B_1 D_2}$

d) $V_T = \dfrac{V_1}{A_1 A_2 + B_1 C_2}, \quad Z_T = \dfrac{A_1 A_2 + B_1 C_2}{A_1 A_2 + B_1 C_2}$

4) Let a causal LTI system be characterized by the following differential equation, with initial rest condition

$$\frac{d^2 y}{dt^2} + 7\frac{dy}{dt} + 10y(t) = 4x(t) + 5\frac{dx(t)}{dt}$$

where $x(t)$ and $y(t)$ are the input and output respectively. The impulse response of the system is $u(t)$ is the unit step function

[GATE 2017]

a) $2e^{-2t}u(t) - 7e^{-5t}u(t)$

b) $-2e^{-2t}u(t) + 7e^{-5t}u(t)$

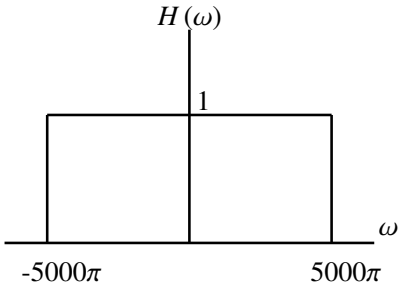
c) $7e^{-2t}u(t) - 2e^{-5t}u(t)$

d) $-7e^{-2t}u(t) + 2e^{-5t}u(t)$

5) Let the signal

$$x(t) = \sum_{k=-\infty}^{+\infty} (-1)^k \delta\left(t - \frac{k}{2000}\right)$$

be passed through an LTI system with frequency response $H(\omega)$, as given in the figure below.



The Fourier series representation of the output is given as

[GATE 2017]

a) $4000 + 4000\cos(2000\pi t) + 4000\cos(4000\pi t)$

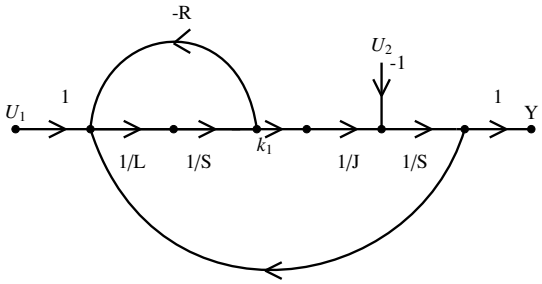
b) $2000 + 2000\cos(2000\pi t) + 2000\cos(4000\pi t)$

c) $2000\cos(2000\pi t)$

d) $4000\cos(2000\pi t)$

6) In the system whose signal flow graph is shown in the figure,$U_1(s)$ and $U_2(s)$ are inputs. The transfer function $\dfrac{Y(s)}{U_1(s)}$ is

[GATE 2017]



a) $\dfrac{k_1}{JLs^2 + JRs + k_1k_2}$

b) $\dfrac{k_1}{JLs^2 - JRs - k_1k_2}$

c) $\dfrac{k_1 - U_2(R + sL)}{JLs^2 + (JR - U_2L)s + k_1k_2 - U_2R}$

d) $\dfrac{k_1 - U_2(sL - R)}{JLs^2 - (JR + U_2L)s - k_1k_2 + U_2R}$

7) The transfer function of the system is given by:

$$x(t) = \begin{pmatrix} 1 & 2 \\ 2 & 0 \end{pmatrix} + \begin{pmatrix} 1 \\ 2 \end{pmatrix} u(t)$$
$$y(t) = \begin{pmatrix} 1 & 0 \end{pmatrix} x(t)$$

The options for the transfer function are: [GATE 2017]

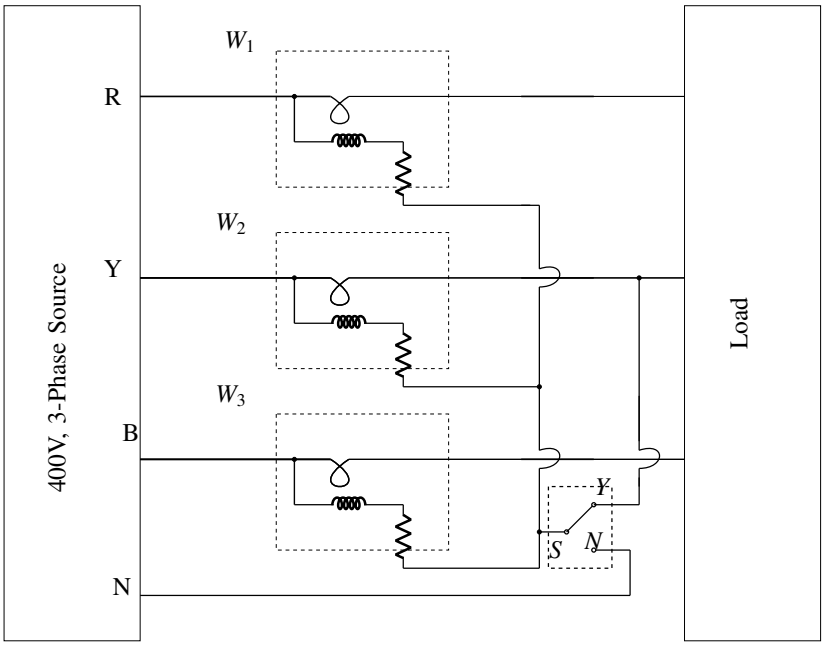
a) $\dfrac{(s+2)}{s^2 - 2s - 2}$

b) $\dfrac{(s-2)}{s^2 + s - 4}$

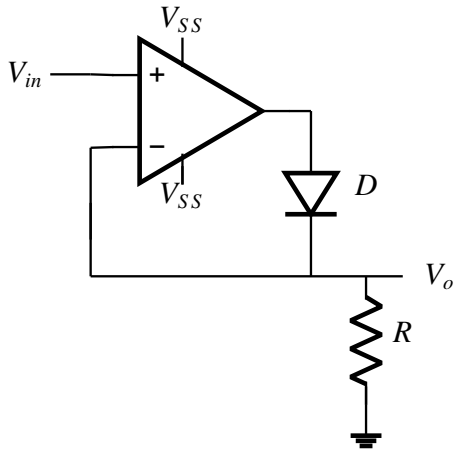
c) $\dfrac{(s+4)}{s^2 + s - 4}$

d) $\dfrac{(s+4)}{s^2 - s - 4}$

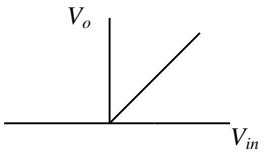
8) The load shown in the figure is supplied by a 400 V (line-to-line), 3-phase source RYB sequence. The load is balanced and inductive, drawing 3464 VA. When the switch S is in position N, the three wattmeters W_1, W_2, and W_3 read 577.35 W each. If the switch is moved to position Y, the readings of the wattmeters in watts will be: [GATE 2017]

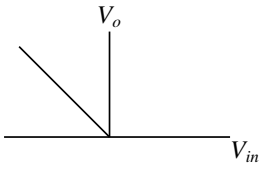


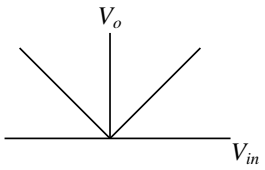
9) The approximate transfer characteristic for the circuit shown below with an ideal operational amplifier and diode is as follows:

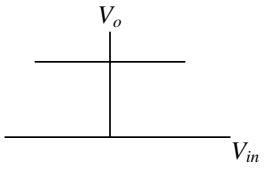


[GATE 2017]

a)


b)


c)


d)


10) The output expression for the Karnaugh map shown below is

$AB\backslash CD$	00	01	11	10
00	0	0	0	0
01	1	0	1	1
11	1	0	1	1
10	0	0	0	0

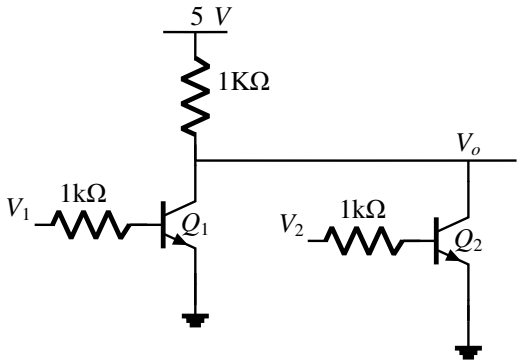
[GATE 2017]

a) $\overline{BD} + BCD$ b) $\overline{B}D + AB$ c) $\overline{B}D + ABC$ d) $B\overline{D} + ABC$

11) A load is supplied by a 230 V, 50 Hz source. The active power P and the reactive power Q consumed by the load are such that 1 kW $\leq P \leq$ 2 kW and 1 kVAR $\leq Q \leq$ 2 kVAR. A capacitor connected across the load for power factor correction generates 1 $kVAR$ reactive power. The worst case power factor after power factor correction is [GATE 2017]

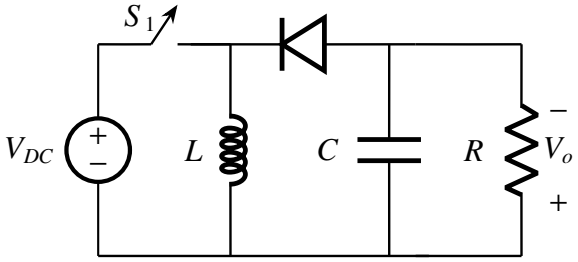
a) 0.447 lag b) 0.707 lag c) 0.894 lag d) 1

12) The logical gate implemented using the circuit shown below where V_1 and V_2 are inputs with (0 V as digital 0 and 5 V as digital 1) and V_{OUT} is the output, is



[GATE 2017]

13) The input voltage V_{DC} of the buck-boost converter shown below varies from 32 V to 72 V. Assume that all components are ideal, inductor current is continuous, and output voltage is ripple-free. The range of duty ratio D of the converter for which the magnitude of the steady-state output voltage remains constant at 48 V is [GATE 2017]



a) $\frac{2}{5} \le D \le \frac{3}{5}$ b) $\frac{2}{3} \le D \le \frac{3}{4}$ c) $0 \le D \le 1$ d) $\frac{1}{3} \le D \le \frac{2}{3}$