Zhezhi (Elliot) He

Assistant Professor
Department of Computer Science and Engineering
Shanghai Jiao Tong University
800 Dongchuan Road, SEIEE-#3 501
Minhang District, Shanghai, 200240, CHN

+86-18921915533
zhezhi.he@sjtu.edu.cn
elliothe.github.io
linkedin.com/in/zhezhi-he
Scholar.google.com
github.com/elliothe

Areas of specialization

- Neuromorphic Computing
- Deep Learning
- Low-power VLSI
- Post-CMOS Device

Education

PH.D., Electrical Engineering
2020 Arizona State University, Tempe, AZ, US
ADVISOR: Deliang Fan

M.ENG., Electrical and Computer Engineering
2015 Oregon State University, Corvallis, OR, US

B.S., Information Engineering
2012 Southeast University, Nanjing, Jiangsu, CHN

Professional experience

2020 Assistant Professor (Tenure track)
Dept. of Computer Science and Engineering, Shanghai Jiao Tong University

2019-2020 Research Assistant
Arizona State University

2019 Research Scientist Intern
Machine Learning System Group, ByteDance AI Lab

2016-2019 Research Assistant
University of Central Florida

Grants, honors & awards

2020 Engineering Graduate Fellowship, Arizona State University
2020 University Graduate Fellowship (UGF), Arizona State University (only recipient of ECEE)
2019 TECHCON travel grant, Semiconductor Research Corporation
2019 ACM SIGDA scholarship for Ph.D. forum, Design Automation Conference
2018 Best Paper Award, IEEE Computer Society Annual Symposium on VLSI [C21] (1/104)
2017 Best Paper Award, IEEE Computer Society Annual Symposium on VLSI [C38] (1/94)
2014 ISAS scholarship, Oregon State University

Publications & Presentations

Statistics as of November 4, 2020 by Google Scholar:
Citations: 586 h-index: 16 i10-index: 24 total-count: 62

= indicates equal contribution among authors.

Research Direction Highlight

- Security and Efficiency in Deep Learning:
  CVPR-2020 [C1, C3], CVPR-2019 [C10, C14], ICCV-2019 [C13], AAAI-2020 [C5], DAC-2020 [C6, C2]
- Brain-inspired In-memory Computing:
  DAC-2019 [C12], DAC-2018 [C22, C18], ICCAD-2018 [C17], DATE-2017 [C34], ICCD-2017 [C31], TCAD [J7], TETC [J11]
- Neural Network Accelerator on FPGA:
  GLSVLSI-2019 [C15], ISLPED-2018 [C25]
- Post-CMOS Device modeling:
  DRC-2019 [C9], MAGL [J10], GLSVLSI-2017 [C33], ISLPED-2016 [C39]

Journal (Total: 11)

[J1] Shaahin Angizi, Zhezhi He, An Chen, and Deliang Fan. "Hybrid Spin-CMOS Polymorphic Logic Gate With Application in In-Memory Computing". In: *IEEE Transactions on Magnetics* 56.2 (2020), pp. 1–15.

[J2] Durjoy Dev, Adithi Krishnaprasad, Mashiyat Shawkat, Zhezhi He, Sonali Das, Hee-Suk Chung, Deliang Fan, Yeonwoong Jung, and Tania Roy. "2D MoS2 Based Threshold Switching Memristor For Artificial Neuron". In: *IEEE Electron Device Letters* (2020).

[J3] Zhezhi He, Li Yang, Shaahin Angizi, Adnan Siraj Rakin, and Deliang Fan. "Sparse BD-Net: A Multiplication-less DNN with Sparse Binarized Depth-wise Separable Convolution". In: *ACM Journal on Emerging Technologies in Computing Systems (JETC)* 16.2 (2020), pp. 1–24.

[J4] Xiaolong Ma, Sheng Lin, Shaokai Ye, Zhezhi He, Linfeng Zhang, Geng Yuan, Sia Huat Tan, Zhengang Li, Deliang Fan, Xuehai Qian, et al. "Non-Structured DNN Weight Pruning–Is It Beneficial in Any Platform?" In: *IEEE Transactions on Neural Networks and Learning Systems (TNNLS)* (2020). (Accepted)

[J5] Shaahin Angizi, Zhezhi He, Amro Awad, and Deliang Fan. "MRIMA: An MRAM-based In-Memory Accelerator". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2019).

[J6] Zhibo Wang, Zhezhi He, Milan Shah, Teng Zhang, Deliang Fan, and Wei Zhang. "Network-based multi-task learning models for biomarker selection and cancer outcome prediction". In: *Oxford academic Bioinformatics* (2019).

[J7] Shaahin Angizi, Zhezhi He, Nader Bagherzadeh, and Deliang Fan. "Design and Evaluation of a Spintronic In-Memory Processing Platform for Nonvolatile Data Encryption". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 37.9 (2018), pp. 1788–1801.

[J8] Zhezhi He, Yang Zhang, Shaahin Angizi, Boqing Gong, and Deliang Fan. "Exploring A SOT-MRAM based In-Memory Computing for Data Processing". In: *IEEE Transactions on Multi-Scale Computing Systems* (2018).

[J9] Farhana Parveen, Shaahin Angizi, Zhezhi He, and Deliang Fan. "IMCS2: Novel Device-to-Architecture Co-Design for Low-Power In-Memory Computing Platform Using Coterminous Spin Switch". In: *IEEE Transactions on Magnetics* 54.7 (2018), pp. 1–14.

[J10] Zhezhi He, Shaahin Angizi, and Deliang Fan. "Current -induced dynamics of multiple skyrmions with domain-wall pair and skyrmion-based majority gate design". In: *IEEE Magnetics Letters* 8 (2017), pp. 1–5.

[J11] Zhezhi He and Deliang Fan. "Energy efficient reconfigurable threshold logic circuit with spintronic devices". In: *IEEE Transactions on Emerging Topics in Computing* 5.2 (2017), pp. 223–237.

Conference (Total: 39)

[C1] Zhezhi He, Adnan Siraj Rakin, Jingtao Li, Chaitali Chakrabarti, and Deliang Fan. "Defending and Harnessing the Bit-Flip based Adversarial Weight Attack". In: *Conference on Computer Vision and Pattern Recognition (CVPR)* (2020).

[C2] Jingtao Li, Adnan Siraj Rakin, Yan Xiong, Liangliang Chang, Zhezhi He, Deliang Fan, and Chaitali Chakrabarti. "Defending Bit-Flip Attack through DNN Weight Reconstruction". In: *57th Design Automation Conference (DAC)* (2020). (Accepted).

[C3] Adnan Siraj Rakin, Zhezhi He, and Deliang Fan. "TBT: Targeted Neural Network Attack with Bit Trojan". In: *Conference on Computer Vision and Pattern Recognition (CVPR)* (2020).

[C4] Adnan Siraj Rakin, Zhezhi He, Yanzhi Wang, Liqiang Wang, and Deliang Fan. "Robust Sparse Regularization: Adversarial Defense with Sparsity and Compactness". In: *ACM Great Lakes Symposium on VLSI (GLSVLSI)* (2020). (Accepted).

[C5] Li Yang, Zhezhi He, and Deliang Fan. "Harmonious Coexistence of Structured Weight Pruning and Ternarization for Deep Neural Networks". In: *Thirty-third AAAI Conference on Artificial Intelligence (AAAI)* (2020). (**Spotlight**)

[C6] Li Yang, Zhezhi He, and Deliang Fan. "Non-uniform DNN Structured Subnets Sampling for Dynamic Inference". In: *57th Design Automation Conference (DAC)* (2020). (Accepted).

[C7] Shaahin Angizi, Zhezhi He, and Deliang Fan. "ParaPIM: a parallel processing-in-memory accelerator for binary-weight deep neural networks". In: *Proceedings of the 24th Asia and South Pacific Design Automation Conference (ASP-DAC)*. ACM. 2019, pp. 127–132.

[C8] Shaahin Angizi, Zhezhi He, Dayane Reis, Sharon Xiaobo Hu, Wilman Tsai, Shy Jay Lin, and Deliang Fan. "Accelerating Deep Neural Networks in Processing-in-Memory Platforms: Analog or Digital Approach?" In: *2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. 2019, pp. 197–202.

[C9] Durjoy Dev, Adithi Krishnaprasad, Zhezhi He, Sonali Das, Mashiyat Sumaiya Shawkat, Madison Manley, Olaleye Aina, Deliang Fan, Yeonwoong Jung, and Tania Roy. "Artificial Neuron using Ag/2D-MoS 2/Au Threshold Switching Memristor". In: *2019 Device Research Conference (DRC)*. IEEE. 2019, pp. 193–194.

[C10] Zhezhi He and Deliang Fan. "Simultaneously Optimizing Weight and Quantizer of Ternary Neural Network using Truncated Gaussian Approximation". In: *Conference on Computer Vision and Pattern Recognition (CVPR)* (2019).

[C11] Zhezhi He, Boqing Gong, and Deliang Fan. "Optimize Deep Convolutional Neural Network with Ternarized Weights and High Accuracy". In: *IEEE Winter Conference on Applications of Computer Vision (WACV)* (2019).

[C12] Zhezhi He, Jie Lin, Rickard Ewetz, Jiann-Shiun Yuan, and Deliang Fan. "Noise Injection Adaption: End-to-End ReRAM Crossbar Non-ideal Effect Adaption for Neural Network Mapping". In: *56-th Design Automation Conference (DAC)* (2019).

[C13] Zhezhi He=, Adnan Siraj Rakin=, and Deliang Fan. "Bit-Flip Attack: Crushing Neural Network with Progressive Bit Search". In: *International Conference on Computer Vision (ICCV)*. 2019.

[C14] Zhezhi He=, Adnan Siraj Rakin=, and Deliang Fan. "Parametric Noise Injection: Trainable Randomness to Improve Deep Neural Network Robustness against Adversarial Attack". In: *Conference on Computer Vision and Pattern (CVPR)* (2019).

[C15] Li Yang, Zhezhi He, and Deliang Fan. "Binarized Depthwise Separable Neural Network for Object Tracking in FPGA". In: *Great Lakes Symposium on VLSI (GLVLSI)* (2019).

[C16] Shaahin Angizi, Zhezhi He, Yu Bai, Jie Han, Mingjie Lin, Ronald F DeMara, and Deliang Fan. "Leveraging Spintronic Devices for Efficient Approximate Logic and Stochastic Neural Networks". In: *Proceedings of the 2018 on Great Lakes Symposium on VLSI*. ACM. 2018, pp. 397–402.

[C17] Shaahin Angizi, Zhezhi He, and Deliang Fan. "DIMA: a depthwise CNN in-memory accelerator". In: *2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*. IEEE. 2018, pp. 1–8.

[C18] Shaahin Angizi, Zhezhi He, and Deliang Fan. "PIMA-logic: a novel processing-in-memory architecture for highly flexible and energy-efficient logic computation". In: *Proceedings of the 55th Annual Design Automation Conference (DAC)*. ACM. 2018, p. 162.

[C19] Shaahin Angizi, Zhezhi He, Farhana Parveen, and Deliang Fan. "Imce: energy-efficient bit-wise in-memory convolution engine for deep neural network". In: *Proceedings of the 23rd Asia and South Pacific Design Automation Conference*. IEEE Press. 2018, pp. 111–116.

[C20] Zhezhi He, Shaahin Angizi, and Deliang Fan. "Accelerating Low Bit-Width Deep Convolution Neural Network in MRAM". In: *2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. IEEE. 2018, pp. 533–538.

[C21] Zhezhi He, Shaahin Angizi, Adnan Siraj Rakin, and Deliang Fan. "BD-NET: A Multiplication-Less DNN with Binarized Depthwise Separable Convolution". In: *2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. IEEE. 2018, pp. 130–135. **Best Paper Award**

[C22] Zhezhi He=, Shaahin Angizi=, Adnan Siraj Rakin, and Deliang Fan. "CMP-PIM: an energy-efficient comparator-based processing-in-memory neural network accelerator". In: *Proceedings of the 55th Annual Design Automation Conference (DAC)*. ACM. 2018, p. 105.

[C23] Farhana Parveen, Zhezhi He, Shaahin Angizi, and Deliang Fan. "HielM: Highly flexible in-memory computing using STT MRAM". In: *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*. IEEE. 2018, pp. 361–366.

[C24] Adnan Siraj Rakin, Shaahin Angizi, Zhezhi He, and Deliang Fan. "PIM-TGAN: A Processing-in-Memory Accelerator for Ternary Generative Adversarial Networks". In: *2018 IEEE 36th International Conference on Computer Design (ICCD)*. IEEE. 2018, pp. 266–273.

[C25] Li Yang, Zhezhi He, and Deliang Fan. "A Fully Onchip Binarized Convolutional Neural Network FPGA Impelmentation with Accurate Inference". In: *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*. ACM. 2018, p. 50.

[C26] Shaahin Angizi, Zhezhi He, Ronald F DeMara, and Deliang Fan. "Composite spintronic accuracy-configurable adder for low power digital signal processing". In: *2017 18th International Symposium on Quality Electronic Design (ISQED)*. IEEE. 2017, pp. 391–396.

[C27] Shaahin Angizi, Zhezhi He, and Deliang Fan. "Energy efficient in-memory computing platform based on 4-terminal spin hall effect-driven domain wall motion devices". In: *Proceedings of the on Great Lakes Symposium on VLSI 2017*. ACM. 2017, pp. 77–82.

[C28] Shaahin Angizi, Zhezhi He, Farhana Parveen, and Deliang Fan. "Rimpa: A new reconfigurable dual-mode in-memory processing architecture with spin hall effect-driven domain wall motion device". In: *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. IEEE. 2017, pp. 45–50.

[C29] Deliang Fan, Shaahin Angizi, and Zhezhi He. "In-memory computing with spintronic devices". In: *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. IEEE. 2017, pp. 683–688.

[C30] Deliang Fan, Zhezhi He, and Shaahin Angizi. "Leveraging spintronic devices for ultra-low power in-memory computing: Logic and neural network". In: *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE. 2017, pp. 1109–1112.

[C31] Zhezhi He, Shaahin Angizi, and Deliang Fan. "Exploring stt-mram based in-memory computing paradigm with application of image edge extraction". In: *2017 IEEE International Conference on Computer Design (ICCD)*. IEEE. 2017, pp. 439–446.

[C32] Zhezhi He, Shaahin Angizi, Farhana Parveen, and Deliang Fan. "High performance and energy-efficient in-memory computing architecture based on sot-mram". In: *2017 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*. IEEE. 2017, pp. 97–102.

[C33] Zhezhi He, Shaahin Angizi, Farhana Parveen, and Deliang Fan. "Leveraging dual-mode magnetic crossbar for ultra-low energy in-memory data encryption". In: *Proceedings of the on Great Lakes Symposium on VLSI 2017*. ACM. 2017, pp. 83–88.

[C34] Zhezhi He and Deliang Fan. "A tunable magnetic skyrmion neuron cluster for energy efficient artificial neural network". In: *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017*. IEEE. 2017, pp. 350–355.

[C35] Zhezhi He and Deliang Fan. "Developing All-Skyrmion Spiking Neural Network". In: *Neuromorphic Computing Symposium (NCS)* (2017).

[C36] Farhana Parveen, Shaahin Angizi, Zhezhi He, and Deliang Fan. "Hybrid polymorphic logic gate using 6 terminal magnetic domain wall motion device". In: *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2017, pp. 1–4.

[C37] Farhana Parveen, Shaahin Angizi, Zhezhi He, and Deliang Fan. "Low power in-memory computing based on dual-mode SOT-MRAM". In: *2017 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*. IEEE. 2017, pp. 1–6.

[C38] Farhana Parveen, Zhezhi He, Shaahin Angizi, and Deliang Fan. "Hybrid polymorphic logic gate with 5-terminal magnetic domain wall motion device". In: *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. IEEE. 2017, pp. 152–157. **Best Paper Award**

[C39] Zhezhi He and Deliang Fan. "A Low Power Current-mode Flash ADC with Spin Hall Effect Based Multi-threshold Comparator". In: *Proceedings of the 2016 International Symposium on Low Power Electronics and Design*. ACM. 2016, pp. 314–319.

Under-review or Archived

[UA1] Wuyang Zhang, Zhezhi He, Luyang Liu, Zhenhua Jia, Yunxin Liu, Marco Gruterser, Dipankar Raychaudhuri, and yanyong zhang. "Elf: Accelerate High-resolution Mobile Deep-Vision with Content-aware Distributed Offloading". In: *18th USENIX Symposium on Networked Systems Design and Implementation (NSDI)* (2021).

[UA2] Adnan Siraj Rakin, Zhezhi He, Boqing Gong, and Deliang Fan. "Robust Pre-Processing: A Robust Defense Method Against Adversary Attack". In: *arXiv preprint arXiv:1802.01549* (2018).

Talk

[T1] *Secure and Efficient AI Computing System: A Software and Hardware Co-design Perspective*. University of Illinois at Chicago. Chicago, Illinois, USA, Mar. 2020.

[T2] *Secure and Efficient AI Computing System: A Software and Hardware Co-design Perspective*. Binghamton University. Binghamton, New York, USA, Mar. 2020.

[T3] *Secure and Efficient AI Computing System: A Software and Hardware Co-design Perspective*. University of Central Florida. Orlando, Florida, USA, Mar. 2020.

[T4] *Secure and Efficient AI Computing System: A Software and Hardware Co-design Perspective*. University of Nevada, Reno. Reno, Nevada, USA, Mar. 2020.

[T5] *Secure and Efficient AI Computing System: A Software and Hardware Co-design Perspective*. Shanghai Jiao Tong University. Shanghai, China, May 2020.

[T6] *Noise Injection Adaption: End-to-End ReRAM Crossbar Non-ideal Effect Adaption for Neural Network Mapping*. 56-th Design Automation Conference (DAC). Las Vegas, NV, USA, June 2019.

[T7] *High Performance and Energy-efficient In-memory Computing Architecture based on SOT-MRAM*. 2017 IEEEACM International Symposium on Nanoscale Architectures. Newport, Rhode Island, USA, July 2017.

Poster

[P1] *Design and Evaluation of in-Memory Processing Unit (MPU) for Data-Centric Computations*. Semiconductor Research Corporation TECHCON. Austin, TX, USA, Sept. 2019.

[P2] *Parametric Noise Injection: Trainable Randomness to Improve Deep Neural Network Robustness against Adversarial Attack*. Conference on Computer Vision and Pattern Recognition (CVPR). Long Beach, CA, USA, June 2019.

[P3] *Simultaneously Optimizing Weight and Quantizer of Ternary Neural Network using Truncated Gaussian Approximation*. Conference on Computer Vision and Pattern Recognition (CVPR). Long Beach, CA, USA, June 2019.

Projects

2017-2020 "Non-Volatile In-Memory Processing Unit: Memory, In-Memory Logic and Deep Neural Network"
Jointly Funded by National Science Foundation (NSF) and Semiconductor Research Corporation (SRC) nCore ($185K).

- Assist the principal investigator with proposal writing.
- Develop in-memory computing system for data-centric applications, and open-source tools.

Teaching

2016-2017 EEL3801 Computer Organization and Design
EGN3373 Introduction to Electrical System I
EEE3342 Digital System: Lab instructor
EEE4309 Electronics II: Lab instructor
EEL4742 Embedded System: Lab instructor

Service to the profession

Technical Program Committee Member

2021 58th edition of the Design Automation Conference (DAC)
2020 30th edition of the ACM Great Lakes Symposium on VLSI (GLSVLSI)

Journal review

2020 Reviewer of IEEE Transactions on Emerging Topics in Computing (TETC)
2020 Reviewer of IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
2020 Reviewer of IEEE Transactions on Parallel and Distributed Systems (TPDS)
2020 Reviewer of IEEE Transactions on Neural Networks and Learning Systems (TNNLS)
2020 Reviewer of IEEE Transactions on Cloud Computing (TCC)
2020 Reviewer of IEEE Design & Test
2020 Reviewer of ElSEVIER Microprocessors and Microsystems
2020 Reviewer of CCF Transactions on High Performance Computing
2019 Reviewer of ELSEVIER Journal of Artificial Intelligence (AI)
2019-2020 Reviewer of IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
2019 Reviewer of IOPscience Applied Physics Express
2019 Reviewer of IEEE Transactions on Electron Devices (TED)
2019 Reviewer of IEEE Access
2018 Reviewer of Microelectronics Journal
2017-2018 Reviewer of IEEE Transactions on Nanotechnology (TNANO)
2017-2020 Reviewer of Integration, the VLSI Journal
2016-2017 Reviewer of IEEE Transactions on Computers (TC)

Conference review

2020 Reviewer of IEEE/ACM International Symposium on Microarchitecture (MICRO)
2020 Reviewer of Neural Information Processing Systems 2020 (NeurIPS)
2020 Reviewer of European Conference on Computer Vision (ECCV)
2020 Sub-reviewer of IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)
2020 Reviewer of Design, Automation and Test in Europe Conference (DATE)
2020 Reviewer of IEEE Conference on Computer Vision and Pattern Recognition (CVPR)
2020 Reviewer of IEEE International Symposium on High-Performance Computer Architecture (HPCA)
2020-2021 Reviewer of IEEE Winter Conference on Application of Computer Vision (WACV)
2018-2020 Expert reviewer of Design Automation Conference (DAC)
2018-2019 Reviewer of International Conference On Computer Aided Design (ICCAD)
2018-2019 Reviewer of ACM Great Lakes Symposium on VLSI (GLSVLSI)
2019 Reviewer of International Symposium on Quality Electronic Design (ISQED)
2018-2019 Reviewer of IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)
2018 Reviewer of IEEE Non-Volatile Memory Systems and Applications Symposium
2017 Reviewer of IEEE Computer Society Annual Symposium on VLSI (ISVLSI)
2017 Reviewer of Asia and South Pacific Design Automation Conference (ASP-DAC)

Courses

- Machine learning
- VLSI system design
- Analog CMOS integrated circuit
- Information theory
- Electric and magnetic fields
- Signals and systems
- Probability and random signals
- Computer architecture
- Linear system
- RF microwave circuit design

Skills

Languages

- English (professional-proficiency)
- Mandarin (native)

Scripting

Machine Learning Framework (Pytorch, Torch, TensorFlow)
Scientific programming (Python, MATLAB, C++/C)
System language (Bash shell, Tcl/Tk)
Hardware language (Verilog/VHDL, SPICE)
Digital typesetting (Latex, Microsoft Word)

EDA tools

- Cadence (IC)
- Mentor Pads (PCB)
- ISE design suit (FPGA)
- ADS (RF)
- Design-Compiler (VLSI)
- OOMMF (Magnetic)

References

- Deliang Fan, Ph.D.
  Assistant Professor
  Arizona State University, Tempe, AZ
  dfan@asu.edu
  +1-480-727-1922
- Yu (Kevin) Cao, Ph.D.
  Professor, IEEE Fellow
  Arizona State University, Tempe, AZ
  Yu.Cao@asu.edu
  +1-480-965-1472
- Yanzhi Wang, Ph.D.
  Assistant Professor
  Northeastern University, Tempe, AZ
  yanz.wang@northeastern.edu
  +1-617-373-8805
- Chaitali Chakrabarti, Ph.D.
  Professor, IEEE Fellow
  Arizona State University, Tempe, AZ
  chaitali@asu.edu
  +1-480-965-9516
- Boqing Gong, Ph.D.
  Research Scientist
  Google
  BoqingGo@outlook.com
  +1-407-801-3470