COMSM0109 Simulator

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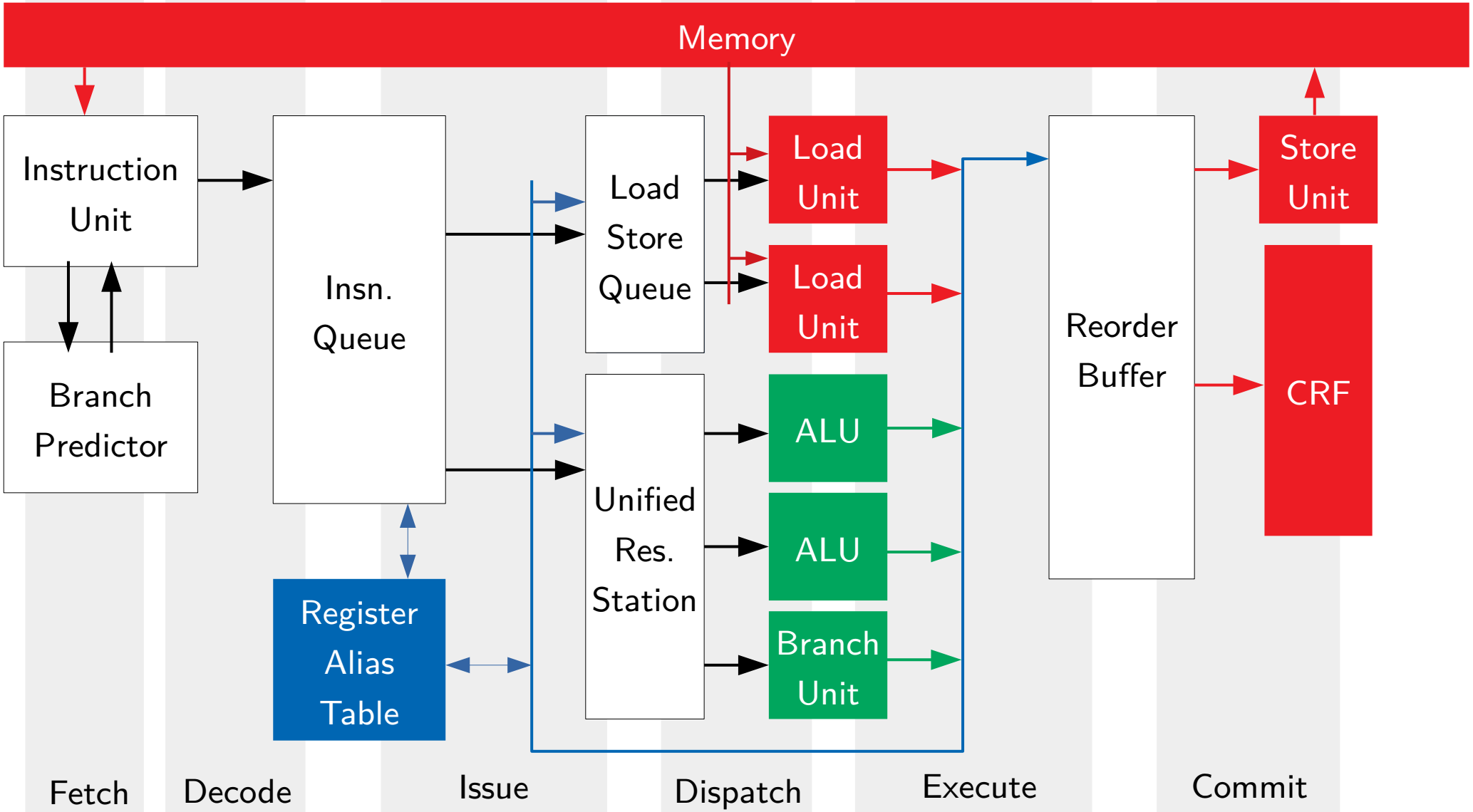
General Description

- 32 bit
- Superscalar out-of-order
  - n-way configurable
- Five Stage Pipeline
  1) Fetch
  2) Decode
  3) Issue
  4) Dispatch/Execute
  5) Commit

- Speculative execution
- Static branch prediction
- Unlimited active branches

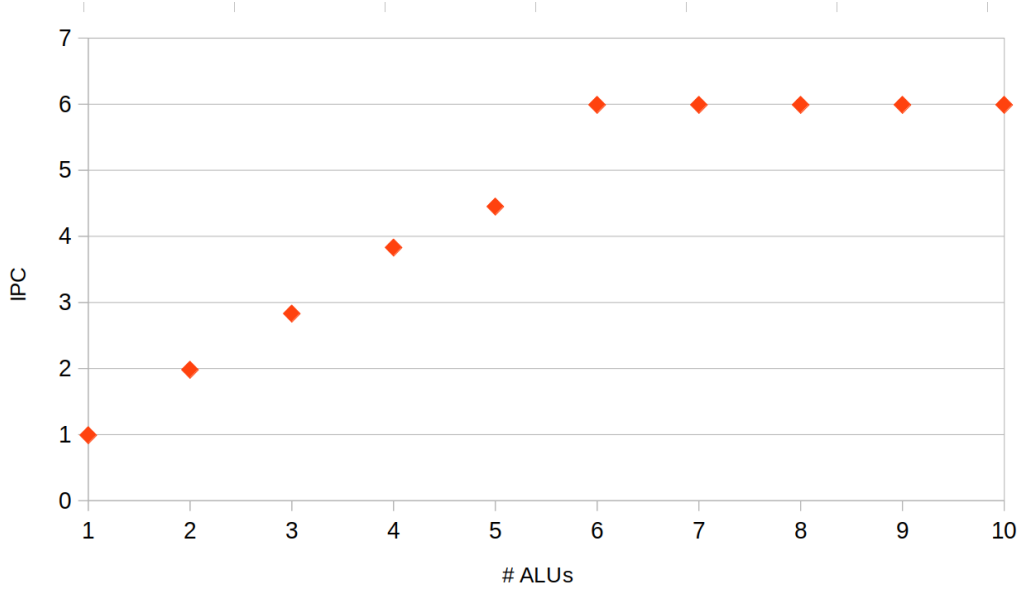
- Configurable execution units. defaulting to:
  - 2 x alu
  - 2 x load unit
  - 1 x store unit

- Unified reservation stations
  - alu instructions
  - branch instructions
- Load/store queue
- Reorder buffer


Memory
Instruction Unit
Branch Predictor
Insn. Queue
Register Alias Table
Load Store Queue
Unified Res. Station
Load Unit
Load Unit
ALU
ALU
Branch Unit
Reorder Buffer
Store Unit
CRF
Fetch
Decode
Issue
Dispatch
Execute
Commit

Experiment #1: Simple ALU

- Tight loop of independent alu instructions
  - Branch hitrate: 99.98% for all
- Should give an IPC approximately equal to the number of alus
- Limited by issue
- Configuration:
  - 6-way ooo, 36 res-stns
  - 40 length rob



Experiment #2: Bubblesort

- Sorting 200 numbers using bubblesort
- Expectation is that by issuing more instructions out-of-order, better performance is achieved
- In reality, diminishing returns beyond 2-way out of order
- Only 75% branch hitrate
- Configuration:
  - 36 res-stns
  - 40 length rob