CEK8903_PIQ_DDR4_ONBOARD

PHYTIUM CONFIDENTIAL

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CECport Firefly Workshop

CEK8903-PIQ

Title: COVER_PAGE

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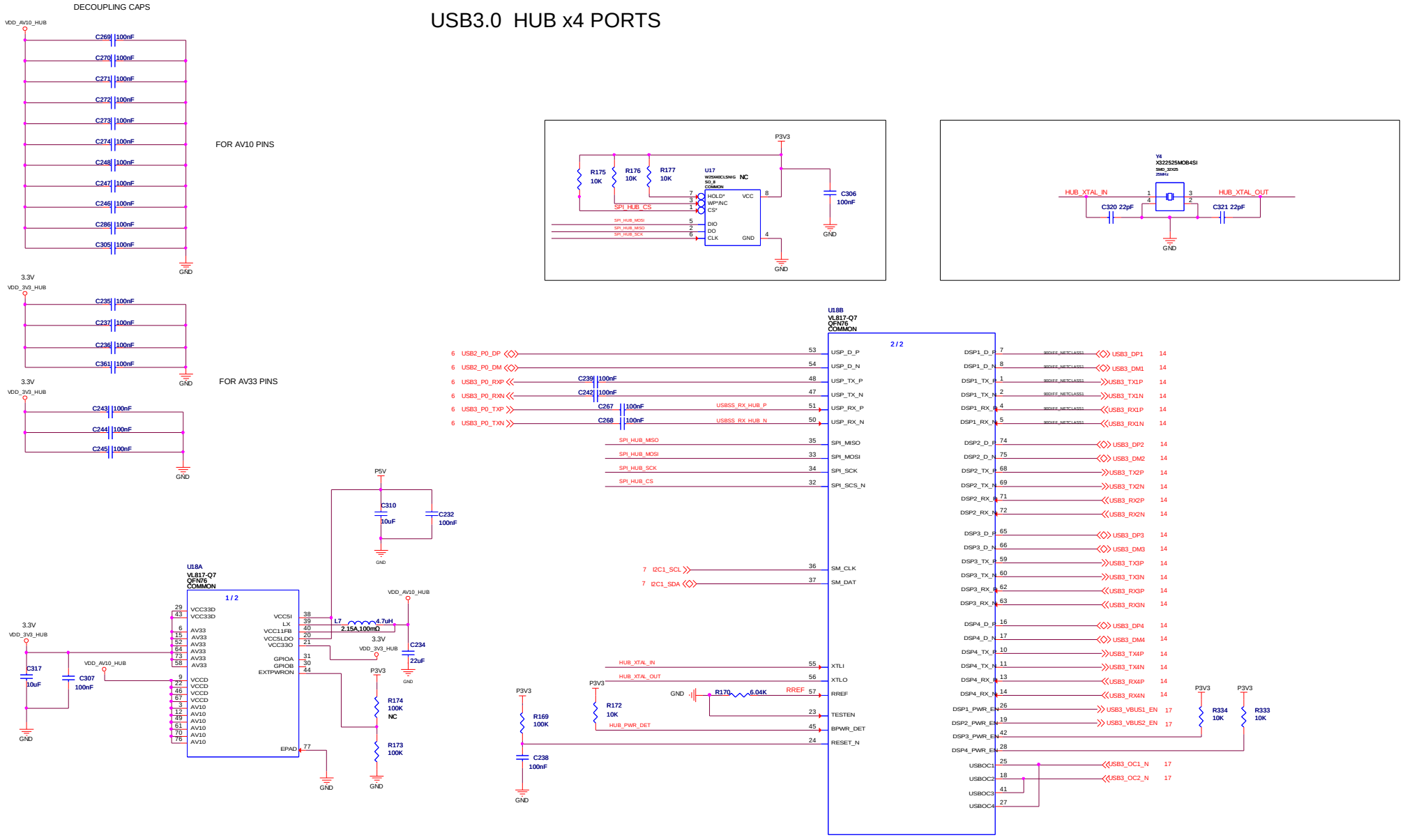
USB3.0 HUB x4 PORTS



	CEK8903-PIQ
Title	USB3.0 HUB
Size: Custom	Document Number: SCH20231129
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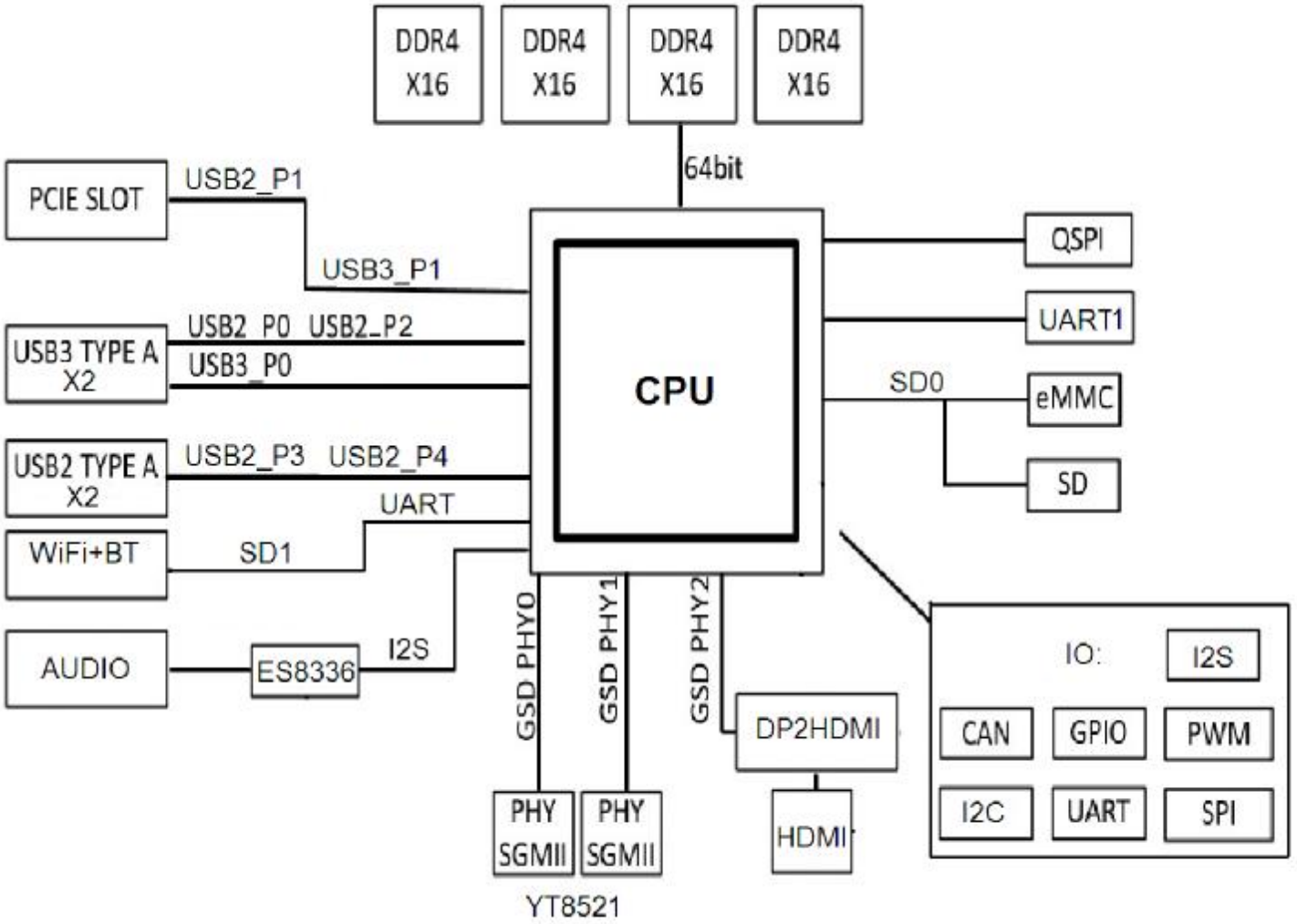

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Title: SYSTEM_BLOCK

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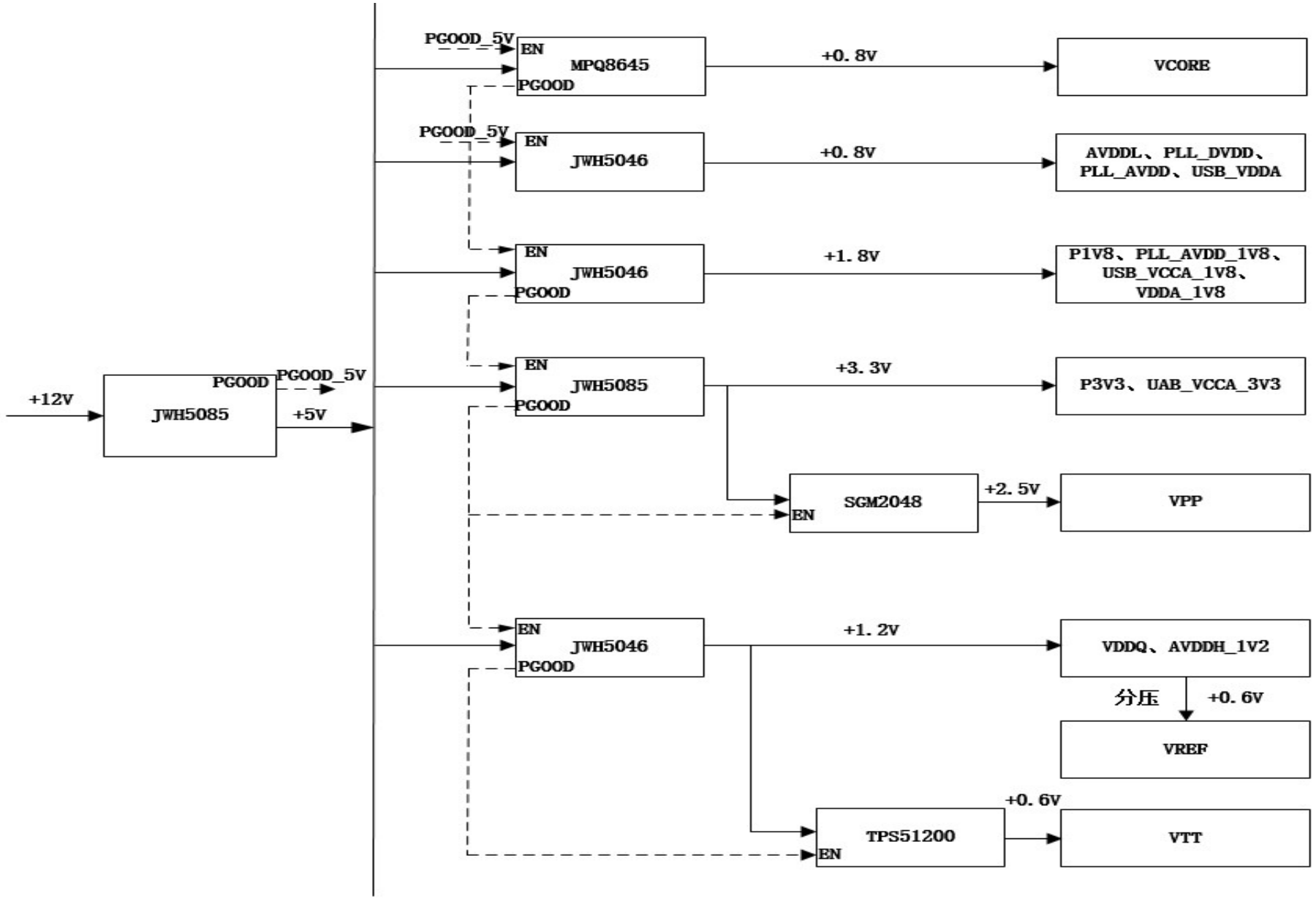

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Title: POWER_BLOCK

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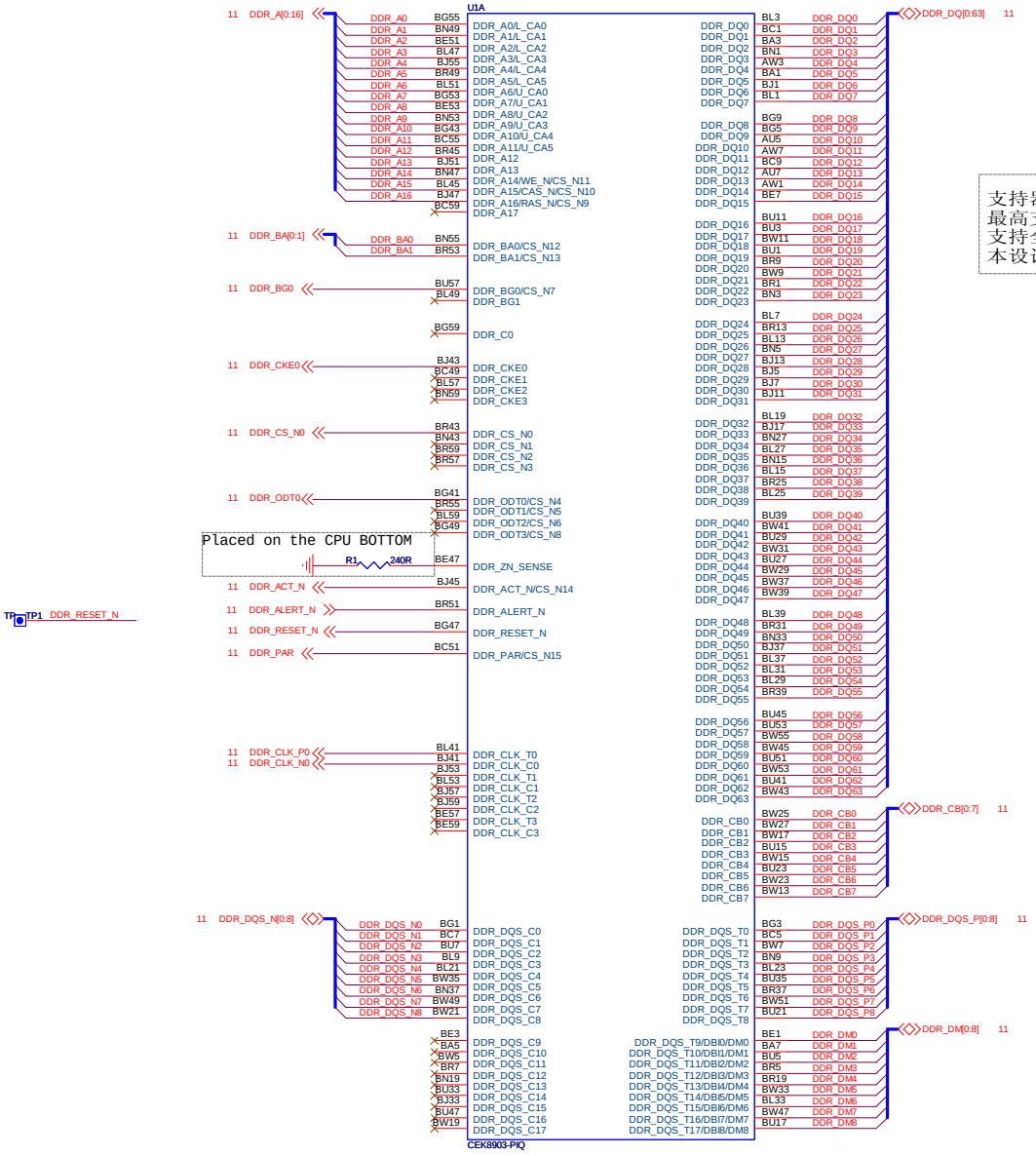

支持器件：DDR4：x4、x8、x16；LPDDR4：x16、x32，
最高支持72个数据位。
支持全位宽模式和半位宽模式（仅支持低32位数据和低4位ECC）
本设计采用DDR4 X16颗粒

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	CEK8903-PIQ
Title	CPU_MCU
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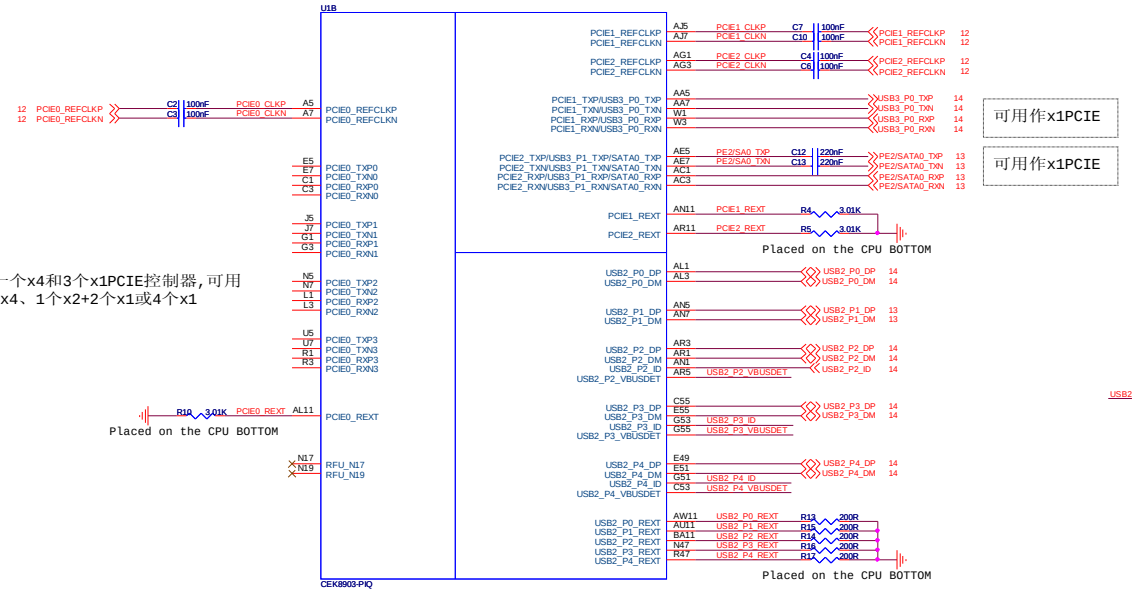
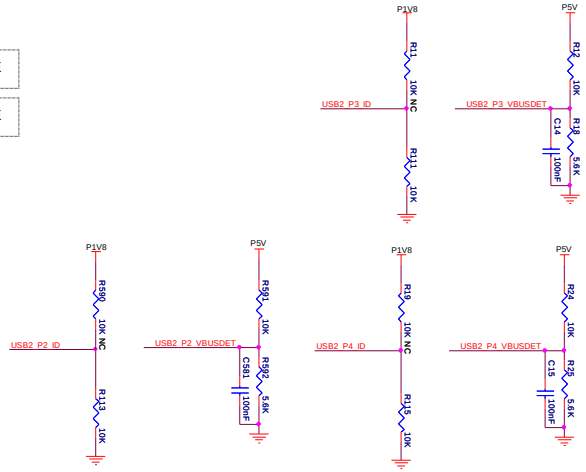
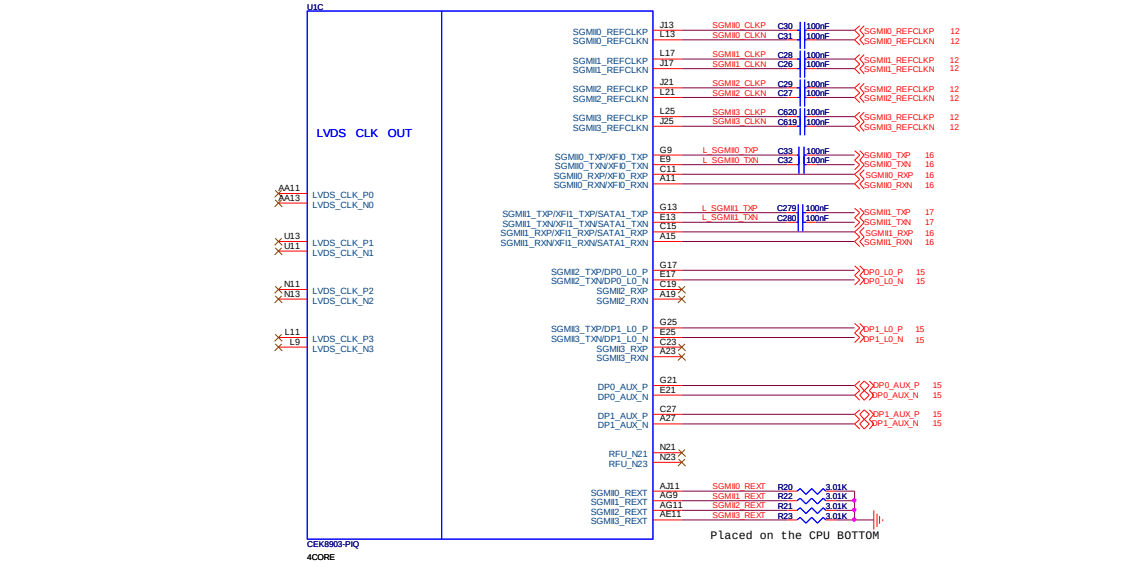


可用作x1PCIE

可用作x1PCIE

包含一个x4和3个x1PCIE控制器,可用作1个x4、1个x2+2个x1或4个x1





CEK8903-PIQ包含了4个MAC控制器MAC0/1支持XFI和SGMII;
MAC2/3支持SGMII和RGMII,且共用MDIO。

MDIO管理接口与MAC端口对应关系

MDIO管理接口	MAC端口类型
MDIO0/MDC0	SGMII0
MDIO1/MDC1	SGMII1
MDIO2/MDC2	SGMII2/RGMII0
MDIO3/MDC3	SGMII3/RGMII1

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CEK8903-PIQ

Title: CPU_SERDES

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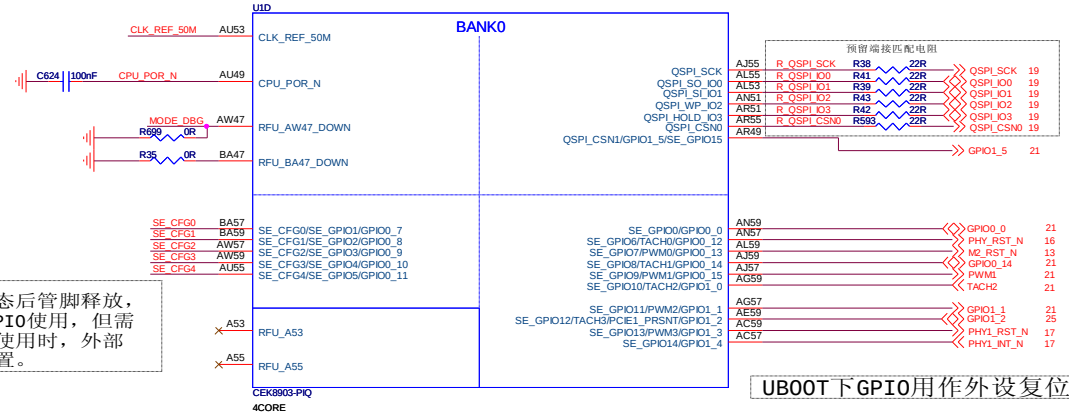
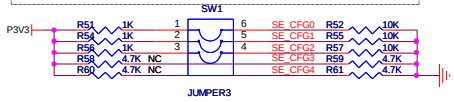


SE_CFG识别到启动设置状态后管脚释放，可以作为通用GPIO与SE_GPIO使用，但需注意这些管脚作为普通IO使用时，外部电气环境不能干扰启动配置。

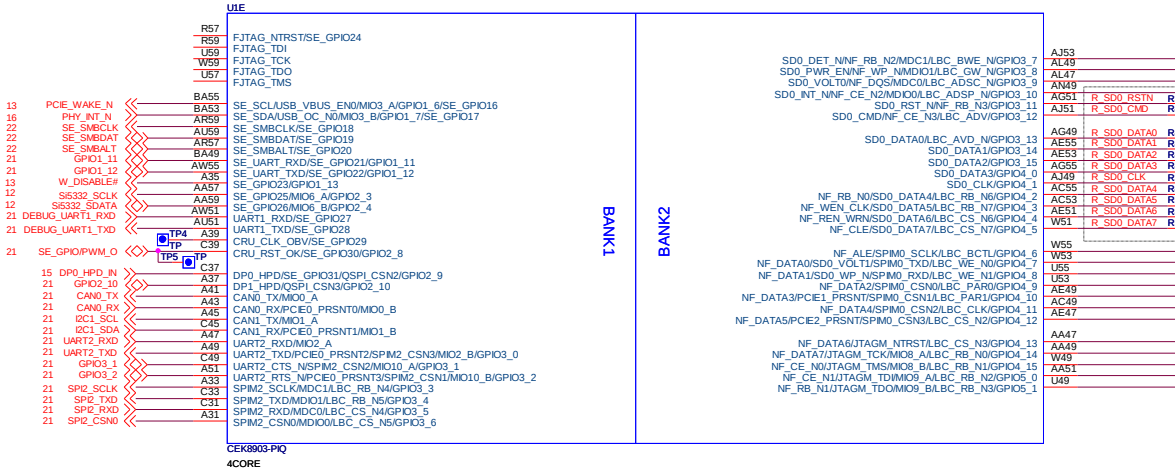
UBOOT下GPIO用作外设复位

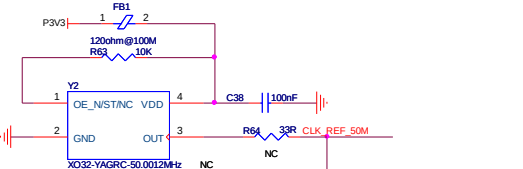
具体应用场景下，建议使用4.7K电阻上下拉确定启动配置信号

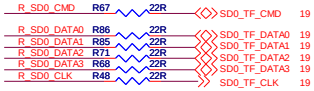


启动配置

SE_CFG[2:0]启动介质:
000:RESERVED
001:QSPI Default
010:LBC
011:NandFlash
100:SD0---SD CARD
101:SD1---SD CARD
110:SD0---eMMC
111:RESERVED
SE_CFG[4:3]启动段位:
00:Default(RECOVER0)
01:RECOVER1
10:RECOVER2
11:RECOVER3







本设计的BANK 电压如下：
bank（0、1、2） ---> 3.3V
bank（3、4、5 ） ---> 1.8V

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	CEK8903-PIQ
Title	CPU_GPIO_1
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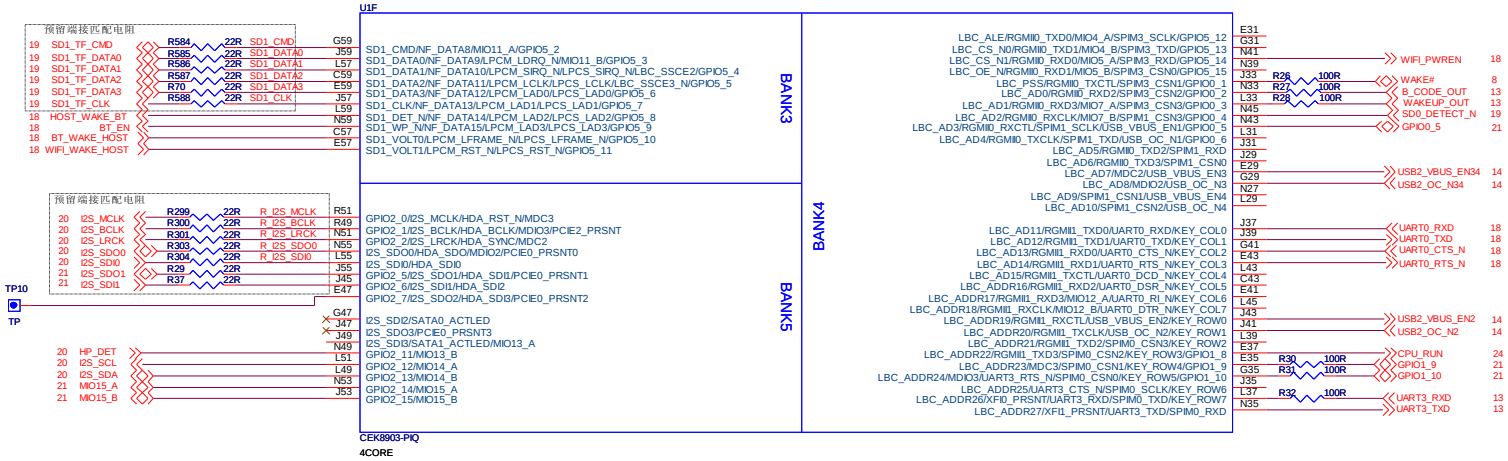

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Title: CPU_GPIO_2

Size	Document Number	Rev
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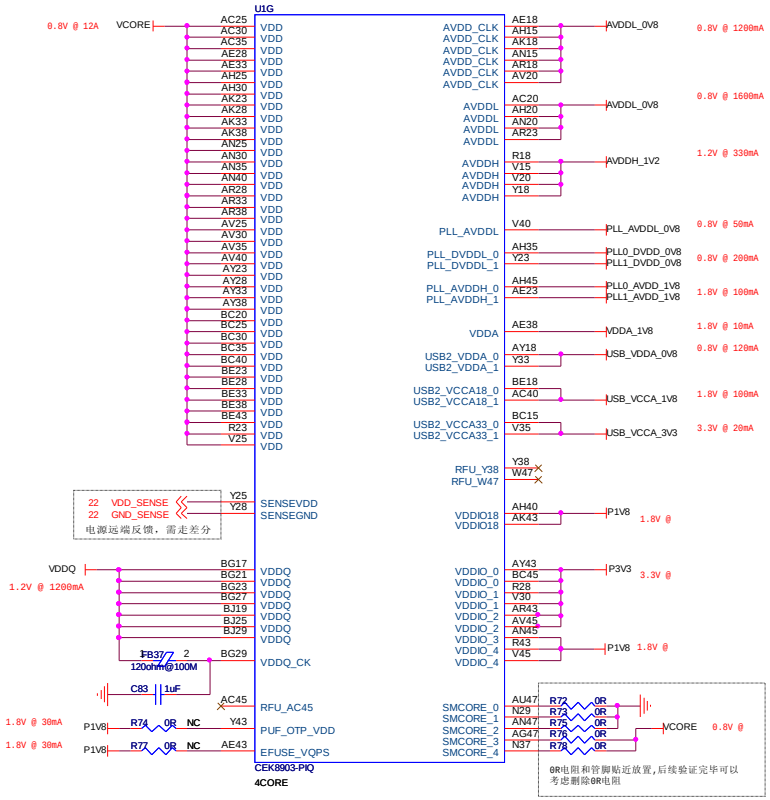

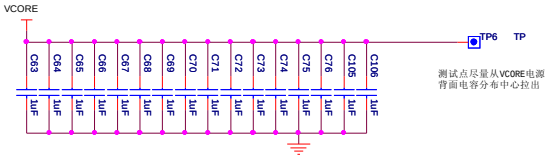

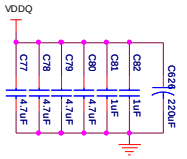

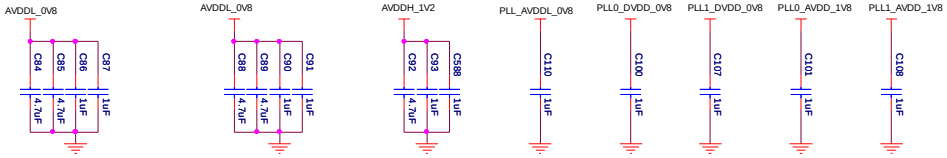

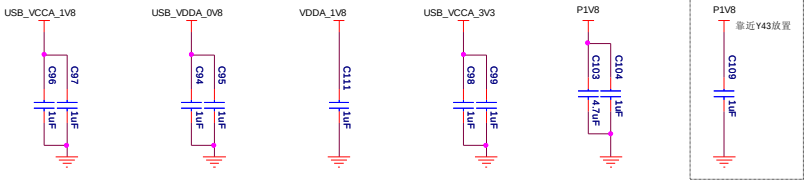

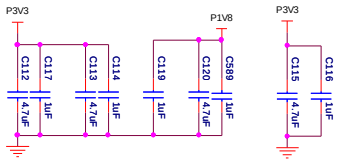

BANK0~BANK4 供电电源为VDDIO_x(0-4),均支持1.8V或3.3V电平;
SMCORE_x(0-4)为各bank电平控制信号，其与VDDIO_x(0-4)对应关系如下表：

SMCORE_x	VDDIO_x
0	3.3V
1	1.8V

1表示SMCORE_x(0-4)接CEK8903-PIQ核心电压VDD
0表示SMCORE_x(0-4)接地

VDDIO18电源为各BANK IO保持电源及BANK5 IO
供电电源，需要保持常供电状态，且固定1.8V。

VDDIO_x接3.3V电源前，SMCORE_x必须接地，上下电过程中须保证
VDDIO_x(3.3V)和VDDIO18的电压压差在1.98V以内,否则有可靠性问题。

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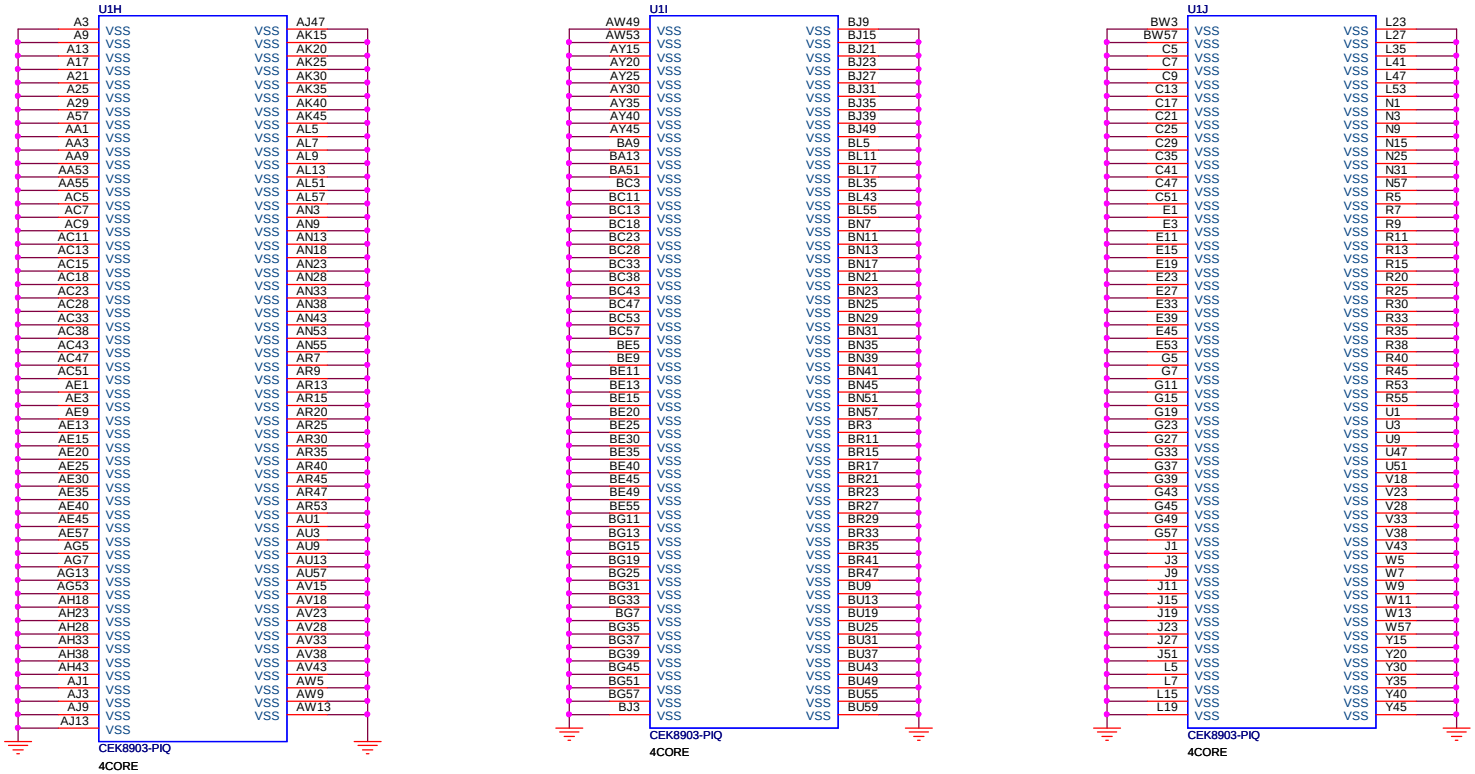

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Title: CPU_VSS

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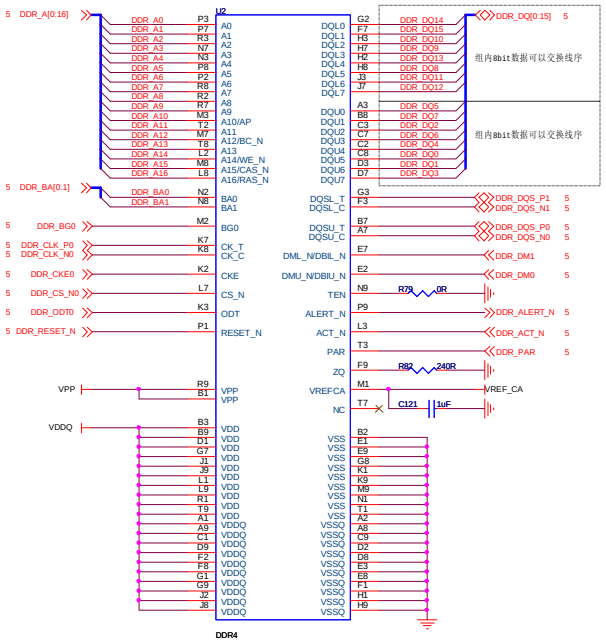
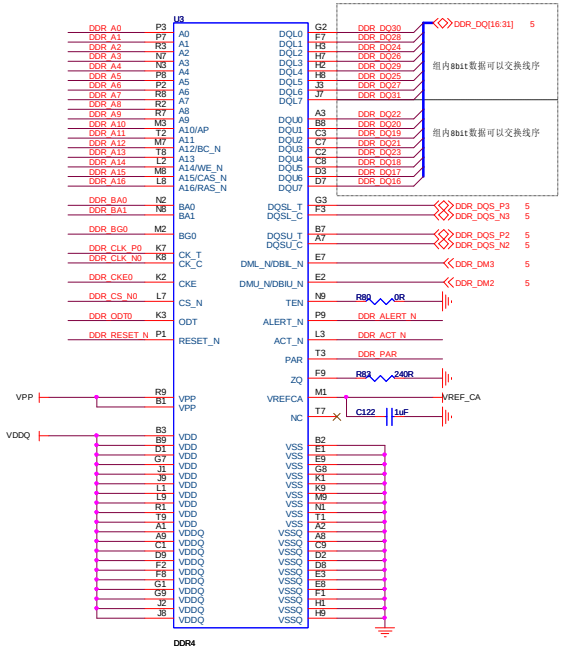
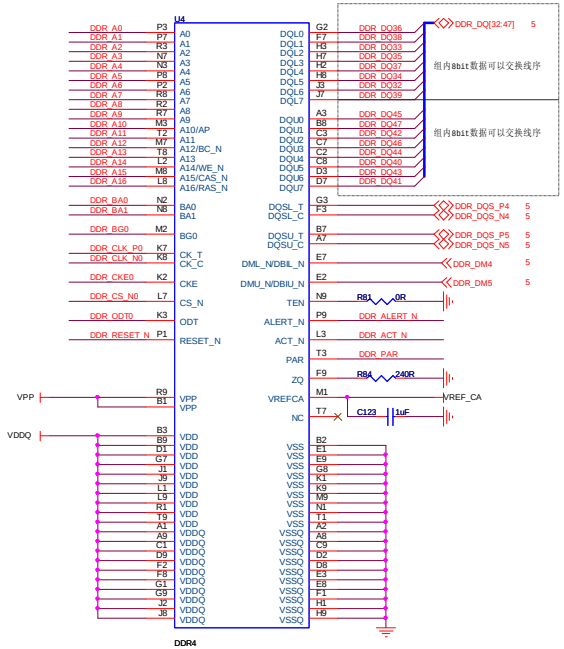
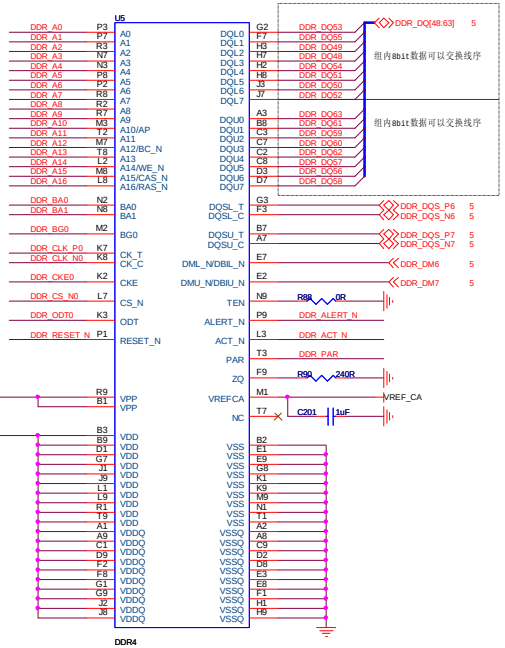
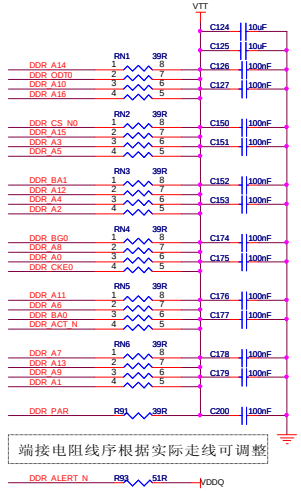




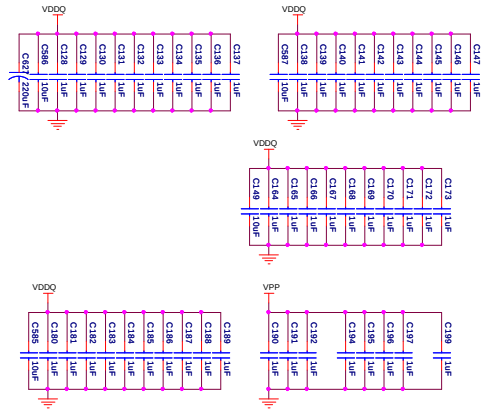


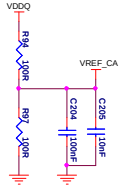
除ECC外，每个slice之间可以交换



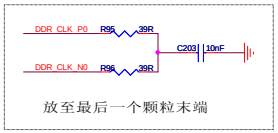


端接电阻线序根据实际走线可调整





对应手册，C203电容由22nF修改为10nF



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Title: DDR4_ONBOARD

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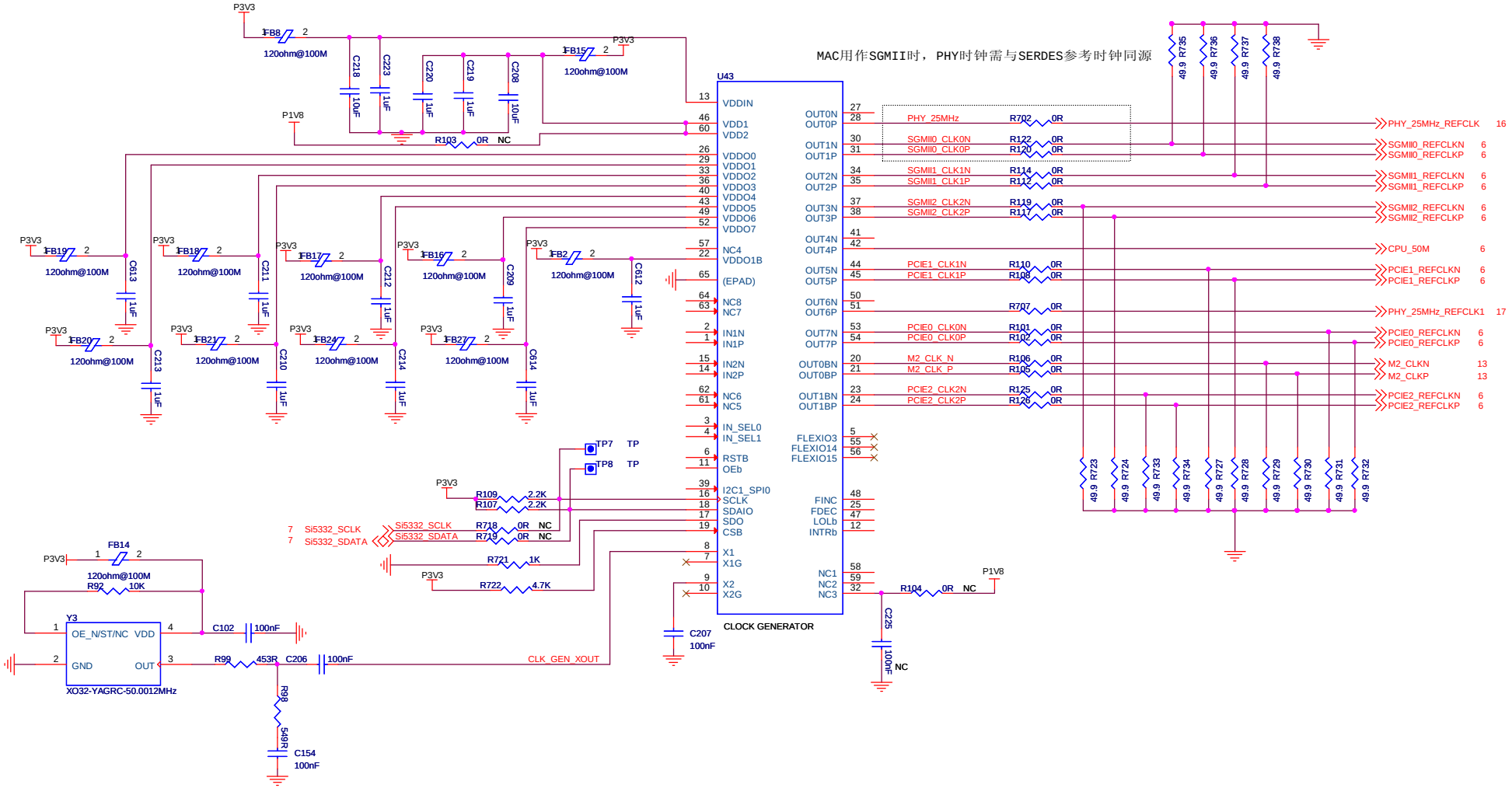

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CEK8903-PIQ			
Title: PCIE_CLKGEN			
Size: A3	Document Number: SCH20221128		Rev: V1
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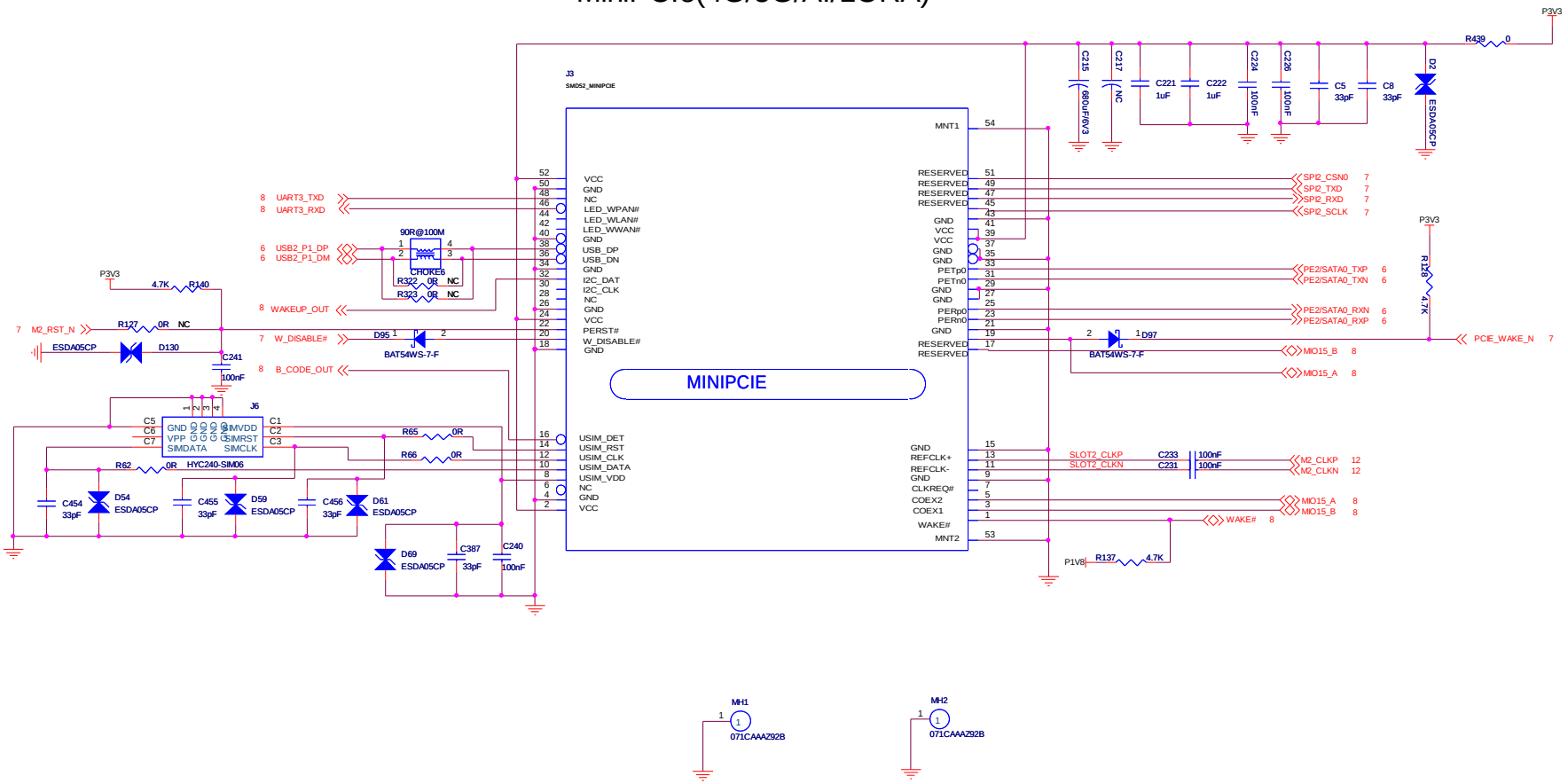
MiniPCIe(4G/5G/AI/LORA)



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Title	MiniPCIe		
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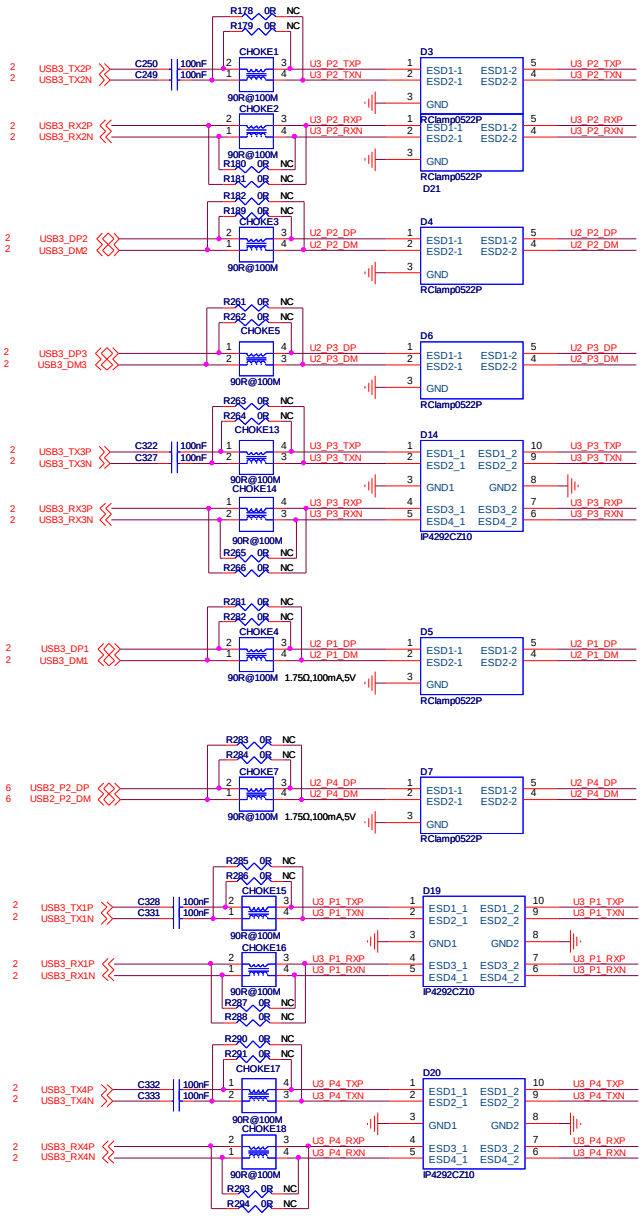
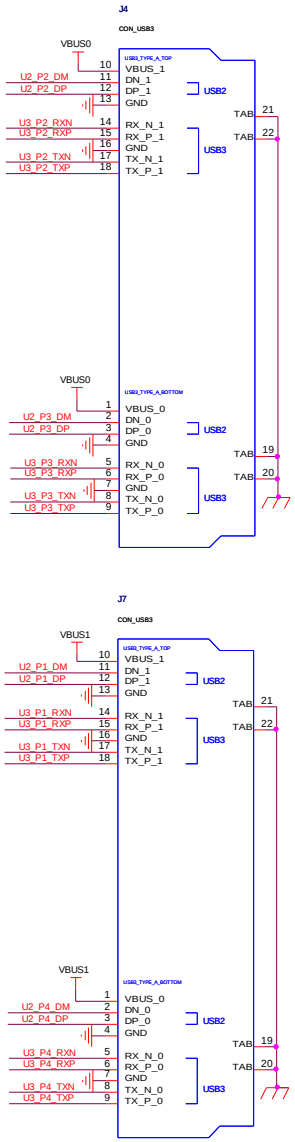
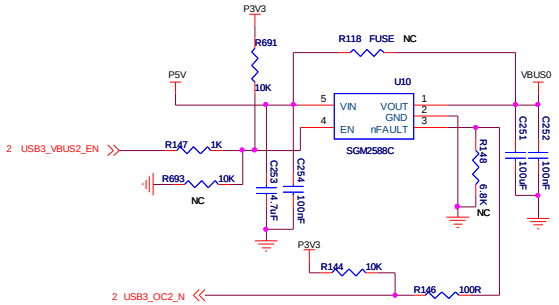
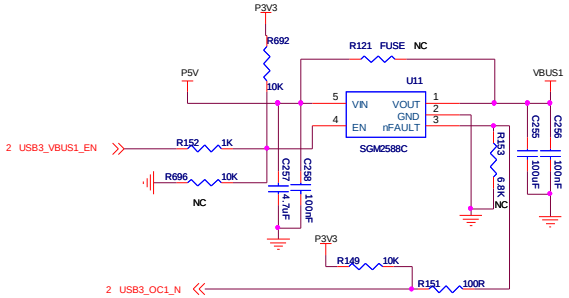




USB3.0和USB2.0做HOST时，VBUS_EN和OC_N可用GPIO代替
用户如需上电直接使能USB，则上拉使能即可（本设计预留）



用户如需上电直接使能USB，则上拉使能即可（本设计预留）



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Title: CONN_USB_A

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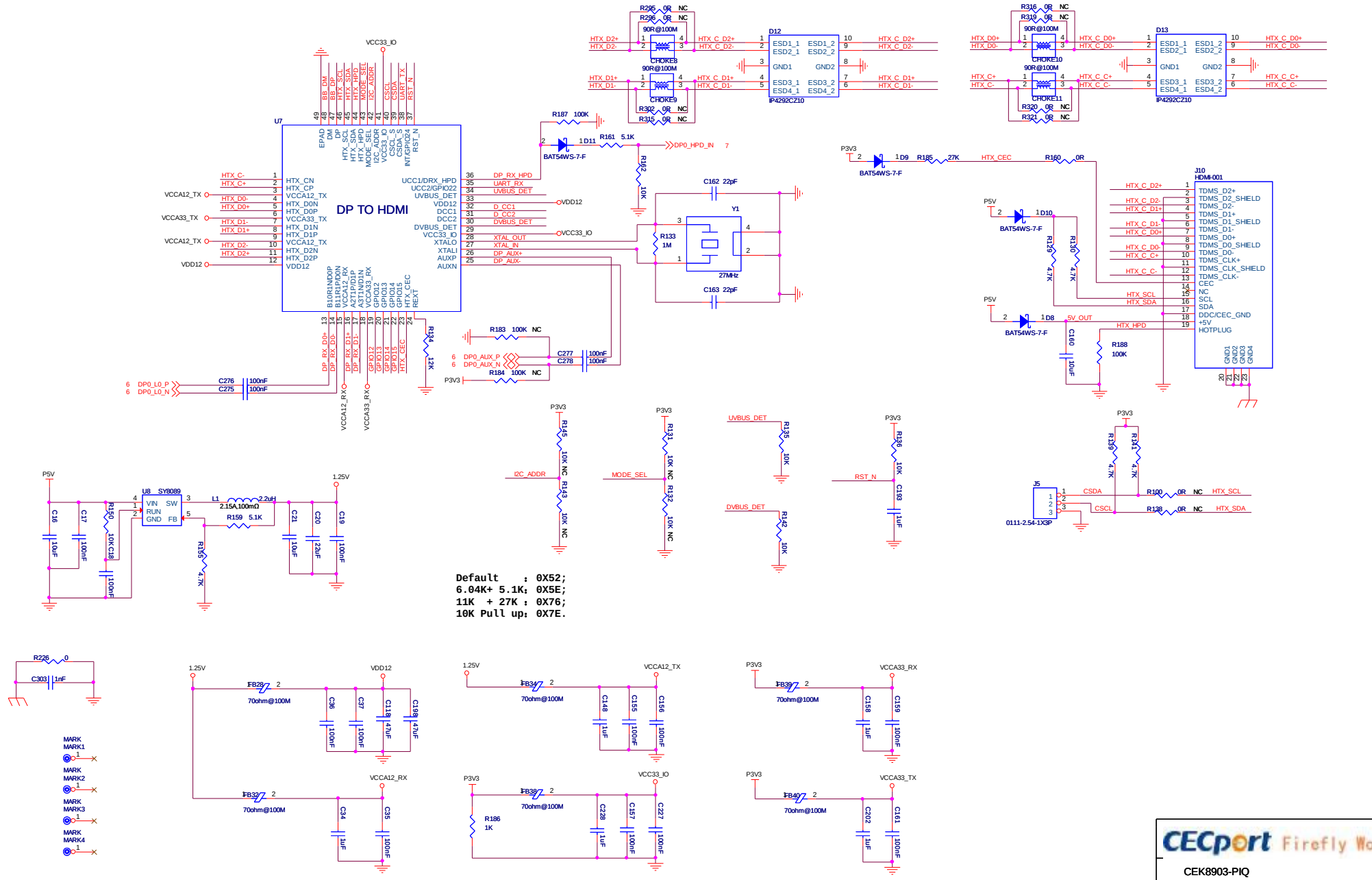
DP TO HDMI
U7
U8 SY8089
J10 HDMI-001
D12 IP4292CZ10
D13 IP4292CZ10
Default : 0X52;
6.04K+ 5.1K: 0X5E;
11K + 27K : 0X76;
10K Pull up: 0X7E.
CEC
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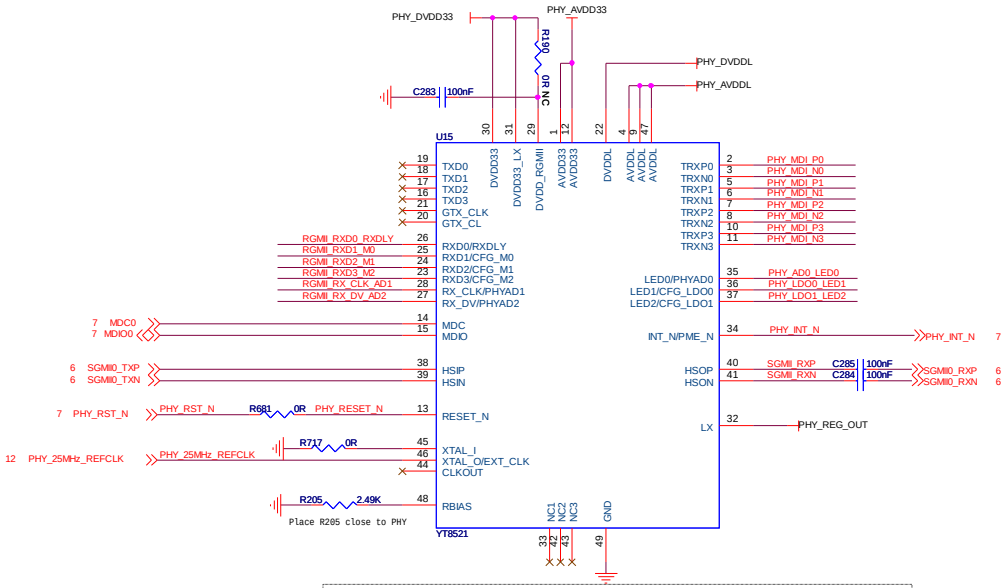
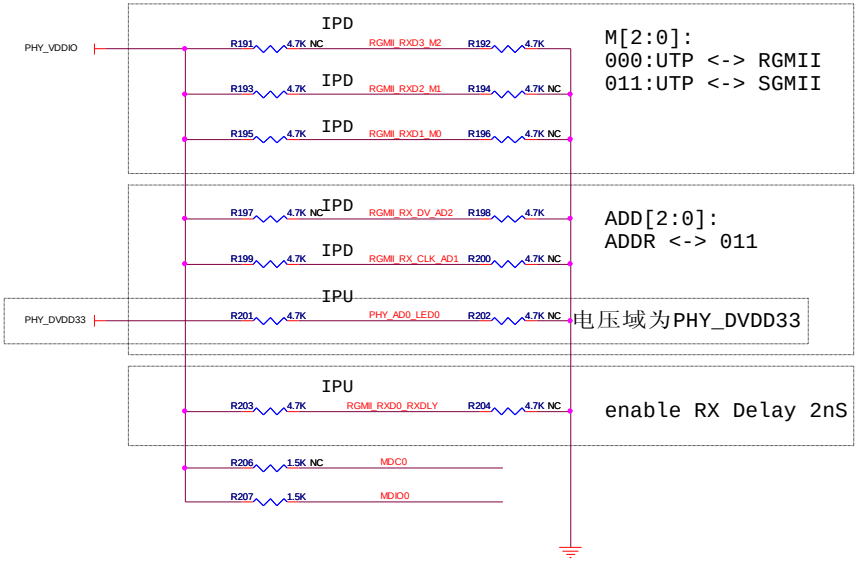
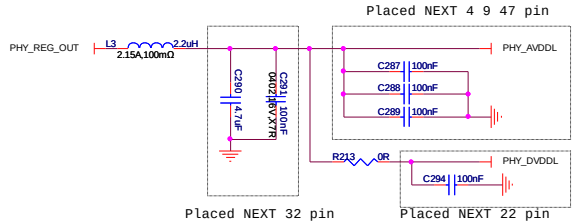
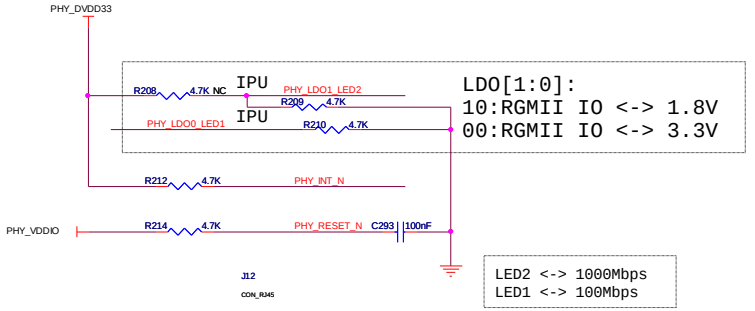
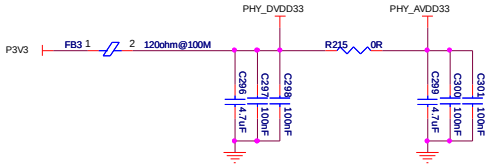


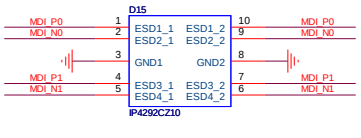
用户可根据实际需求MAC端选择RGMII或者SGMII
本设计使用SGMII



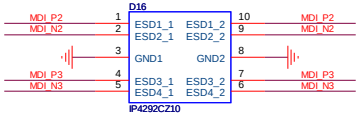




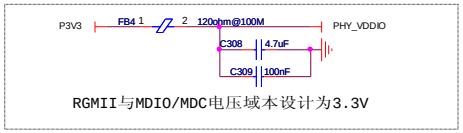


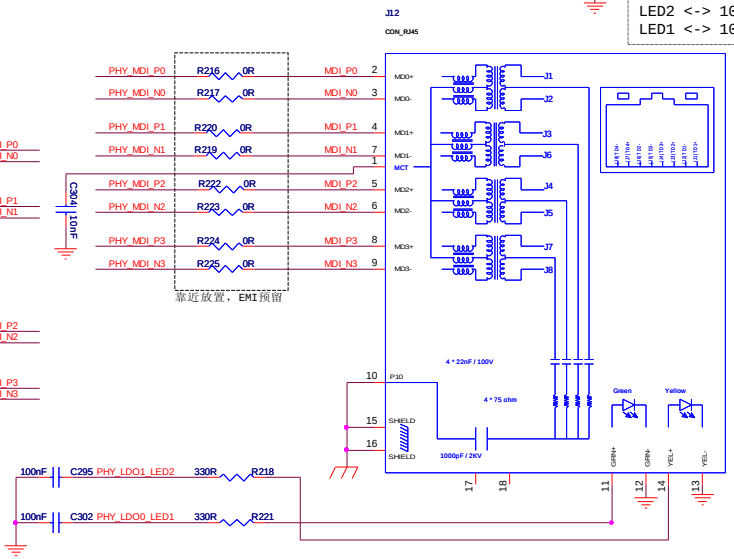


ESD靠近RJ45放置



ESD靠近RJ45放置





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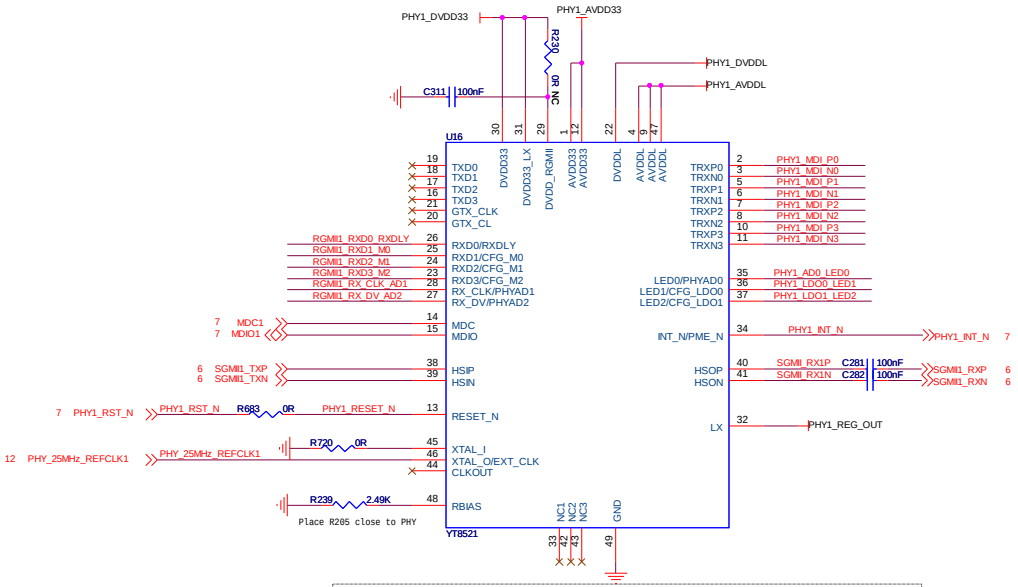
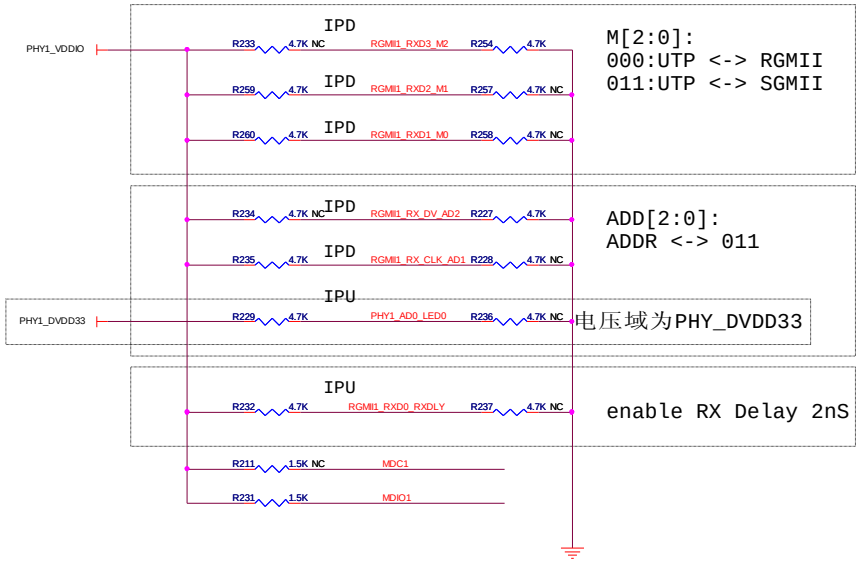
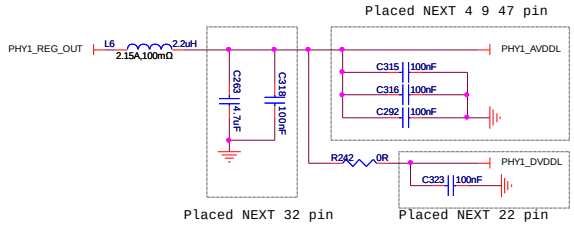
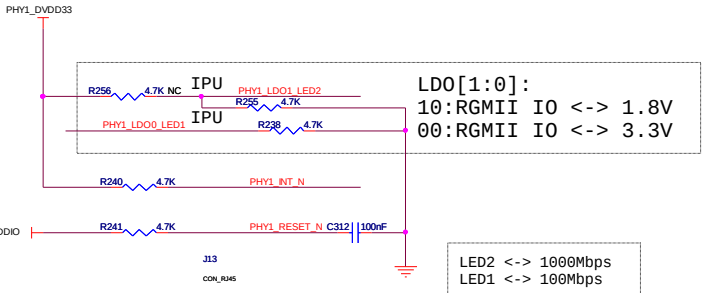
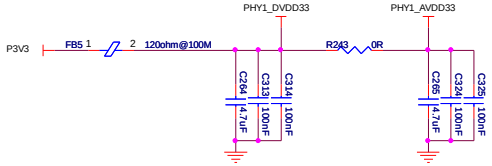


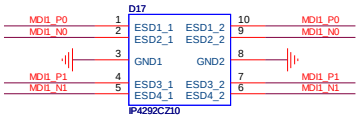


用户可根据实际需求MAC端选择RGMII或者SGMII
本设计使用SGMII

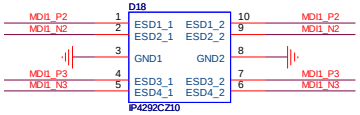




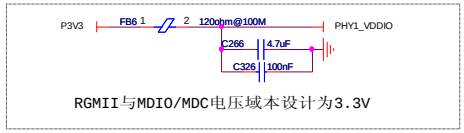




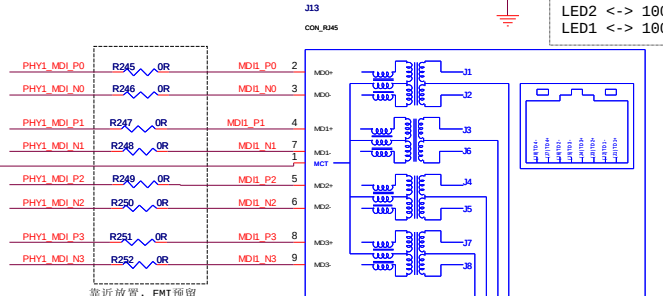
ESD靠近RJ45放置



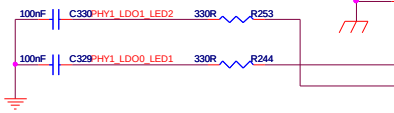
ESD靠近RJ45放置



RGMII与MDIO/MDC电压域本设计为3.3V



LED2 <-> 1000Mbps
LED1 <-> 100Mbps



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Title: SGMII1_ETHERNET

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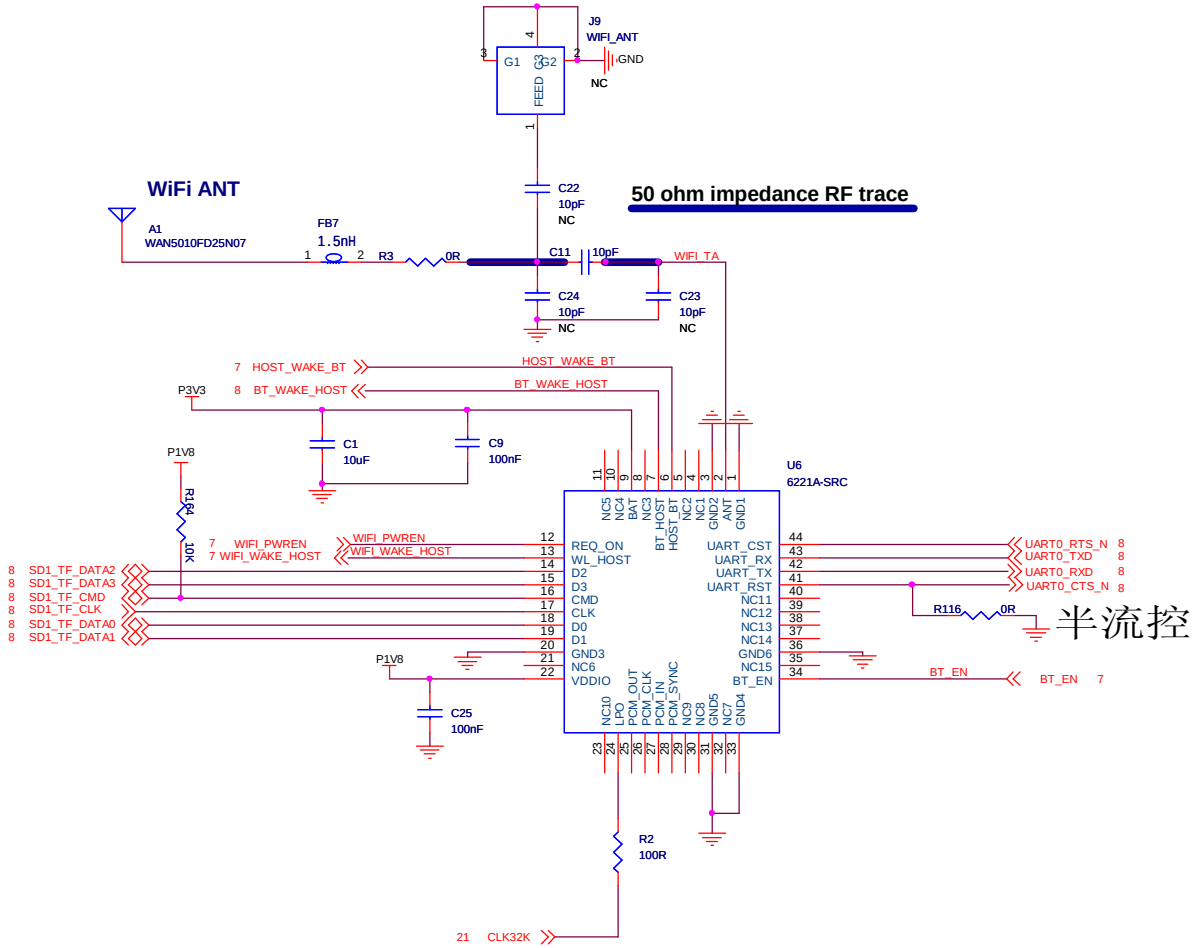

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Title	WIFI&BT	
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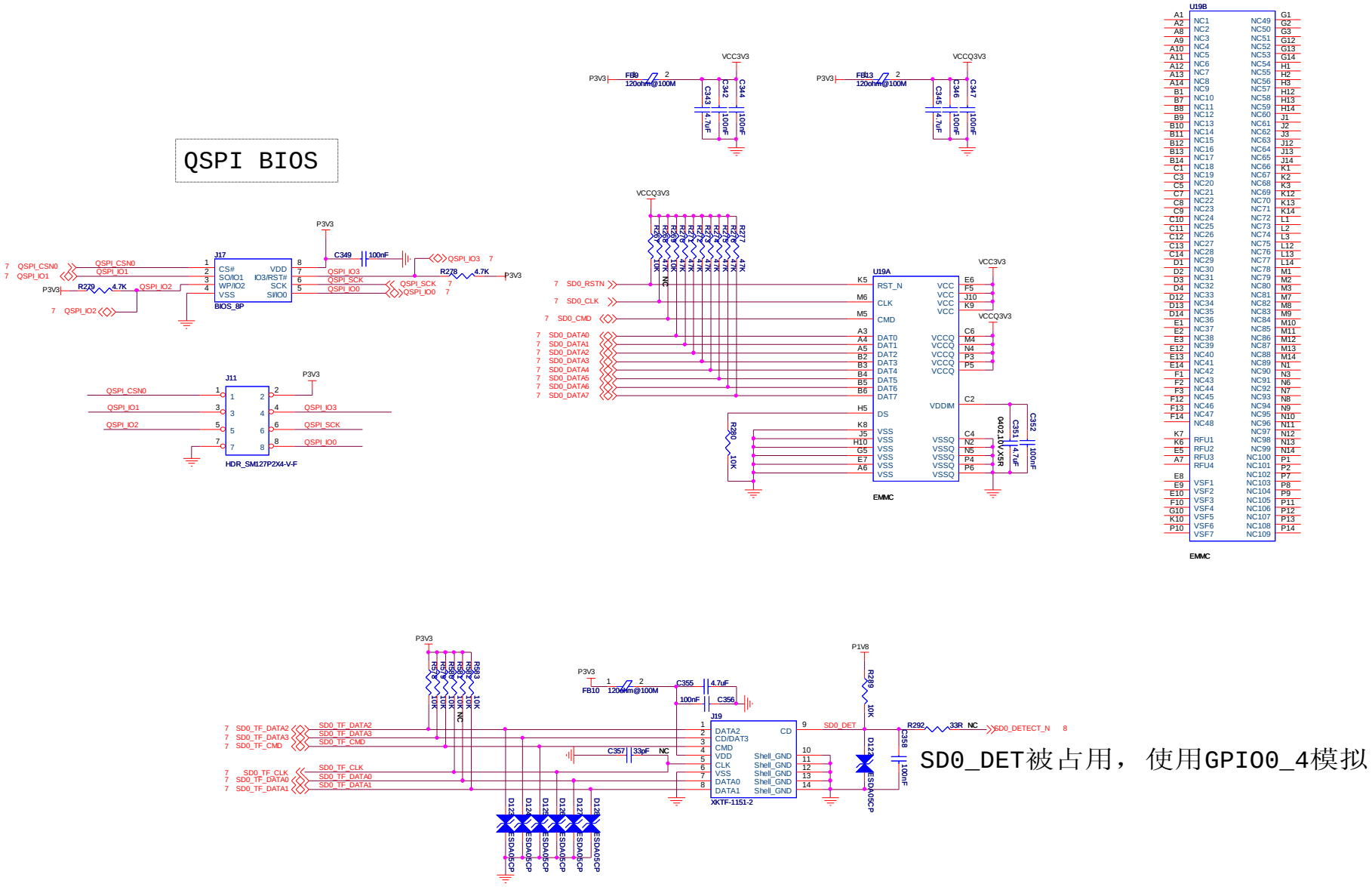

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Title	SD	
Size: Custom	Document Number: SCH20221128	Rev: V1
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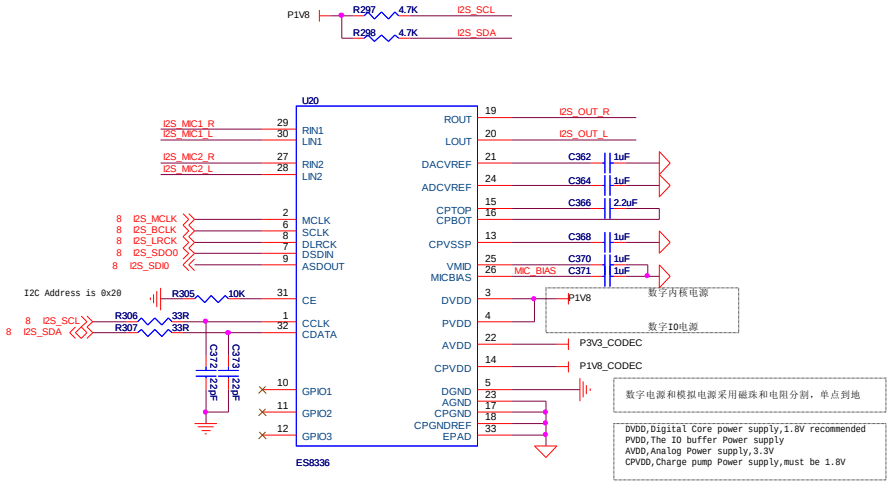

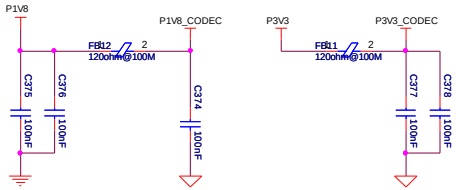

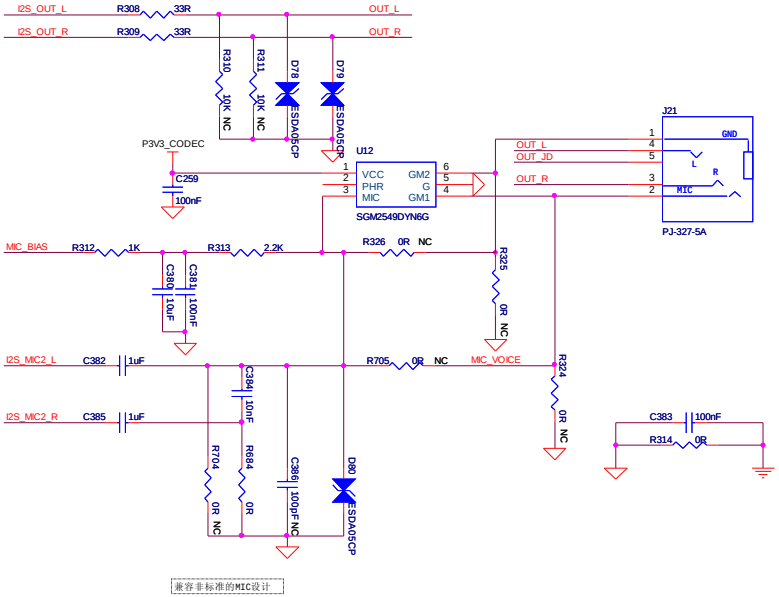

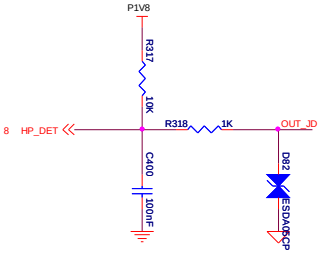

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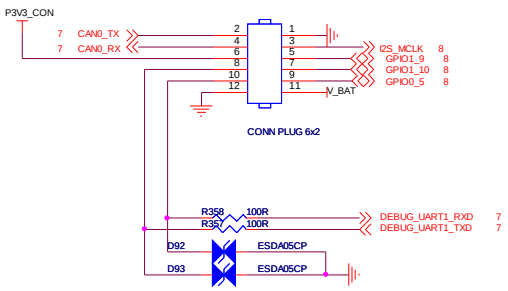
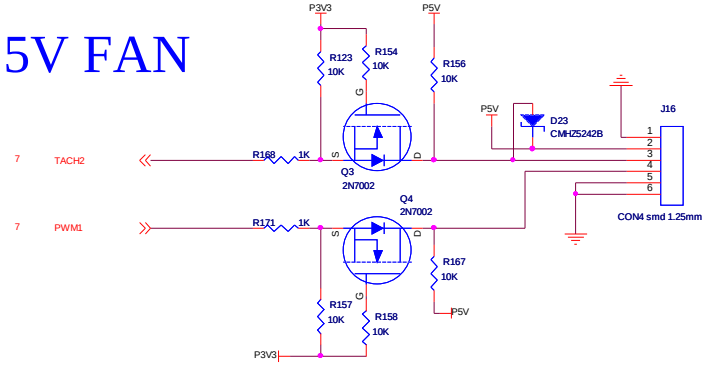
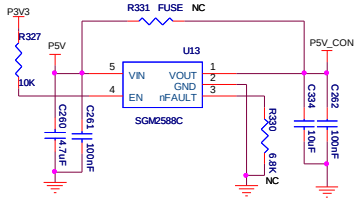
5V FAN

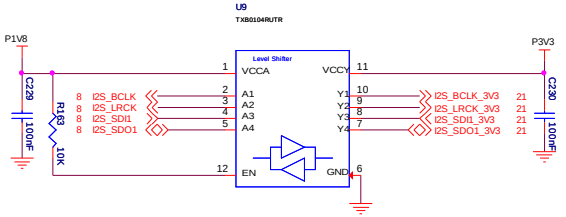
1.8V IO:I2S_MCLK,GPIO0_ 5 ,GPIO1_ 9 10

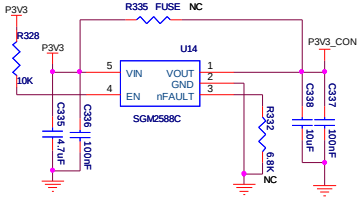


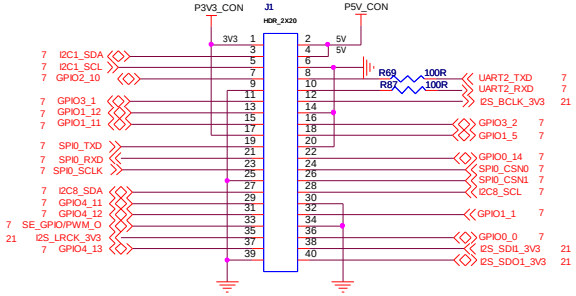
DEBUG UART

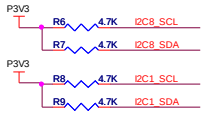


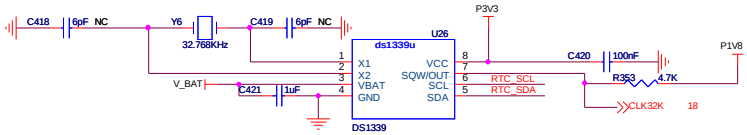


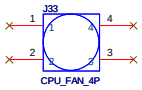


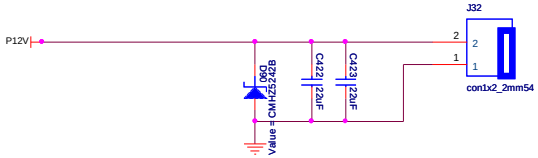












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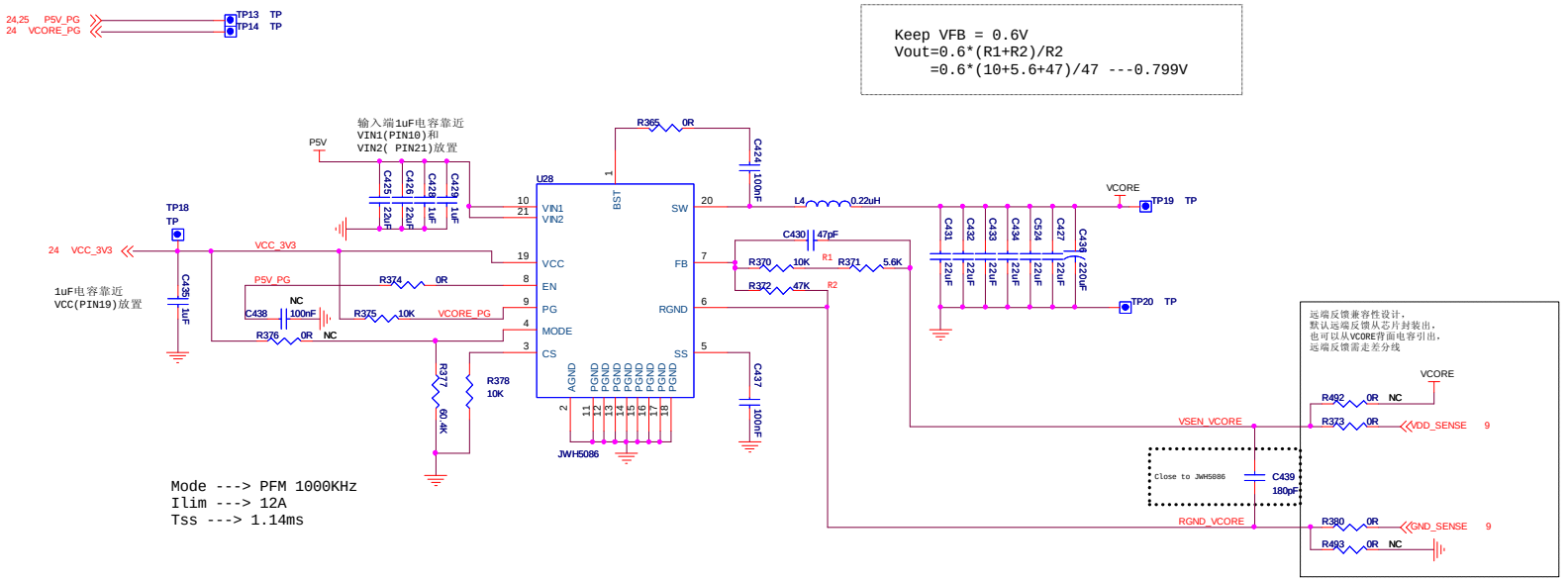

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Title: PWR_VCORE

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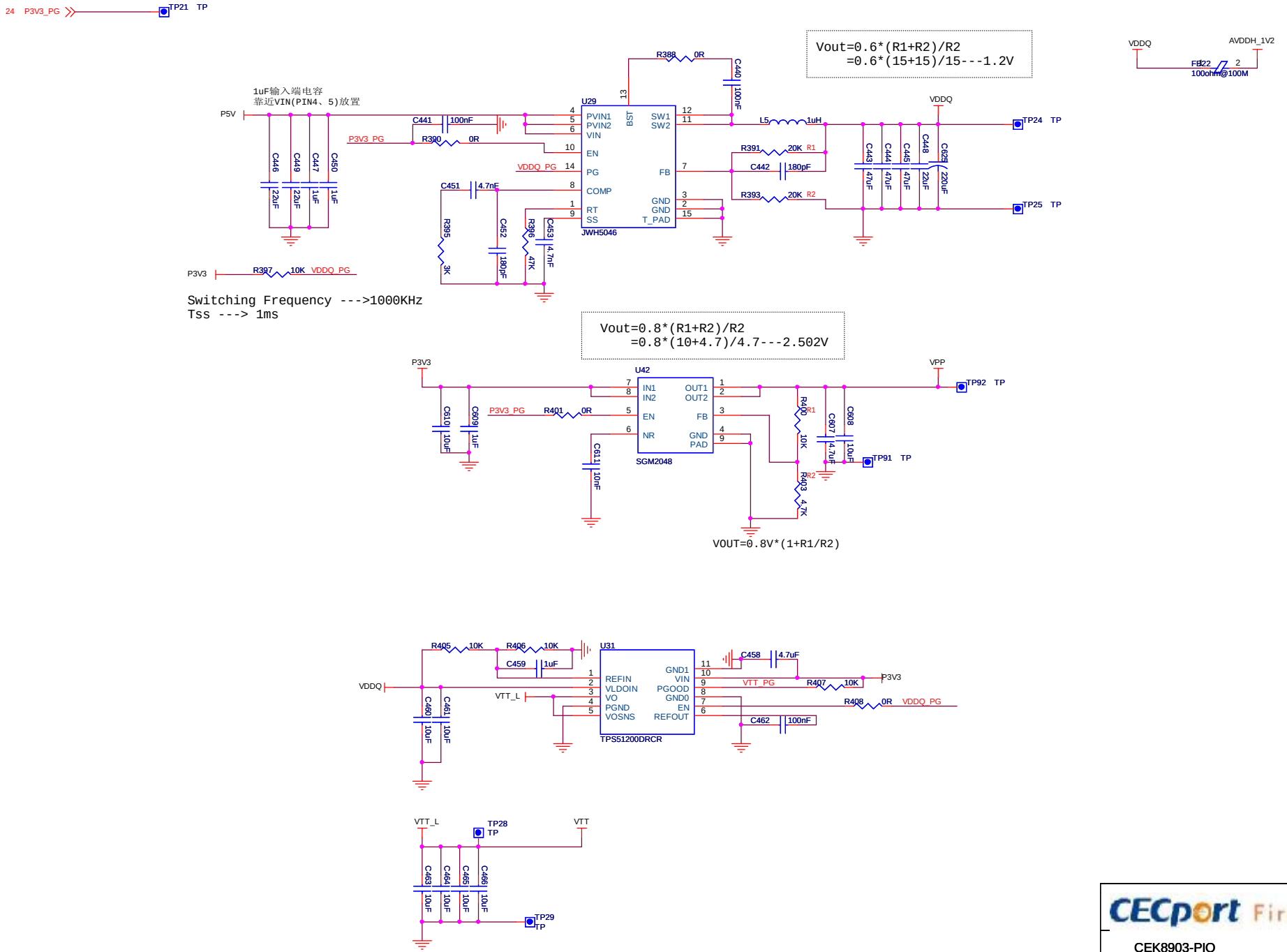
24 P3V3_PG
TP21 TP
Vout=0.6*(R1+R2)/R2
=0.6*(15+15)/15---1.2V
VDDQ
AVDDH_1V2
FB22
100ohm@100M
1uF输入端电容
靠近VIN(PIN4、5)放置
P5V
U29
R388 0R
C440 100nF
C441 100nF
R390 0R
P3V3_PG
VDDQ_PG
C451 4.7nF
C452 180pF
R395 3K
R396 47K
C453 4.7nF
R397 10K VDDQ_PG
P3V3
PVIN1
PVIN2
VIN
EN
PG
COMP
RT
SS
BST
SW1
SW2
FB
GND
GND
T_PAD
JWH5046
L5 1uH
R391 20K R1
C442 180pF
R393 20K R2
C446 22uF
C449 22uF
C447 1uF
C450 1uF
C443 47uF
C444 47uF
C445 47uF
C448 22uF
C629 220uF
TP24 TP
TP25 TP
Switching Frequency --->1000KHz
Tss ---> 1ms
Vout=0.8*(R1+R2)/R2
=0.8*(10+4.7)/4.7---2.502V
U42
P3V3
VPP
TP92 TP
C610 10uF
C609 1uF
P3V3_PG
R401 0R
C611 10nF
IN1
IN2
EN
NR
OUT1
OUT2
FB
GND
PAD
SGM2048
R400 R1
10K
R403 4.7K R2
C607 4.7uF
C608 10uF
TP91 TP
VOUT=0.8V*(1+R1/R2)
R405 10K
R406 10K
C459 1uF
U31
VDDQ
VTT_L
C460 10uF
C461 10uF
REFIN
VLDOIN
VO
PGND
VOSNS
GND1
VIN
PGOOD
GND0
EN
REFOUT
TPS51200DRCR
C458 4.7uF
VTT_PG
R407 10K
P3V3
R408 0R
VDDQ_PG
C462 100nF
VTT_L
TP28 TP
VTT
C463 10uF
C464 10uF
C465 10uF
C466 10uF
TP29 TP
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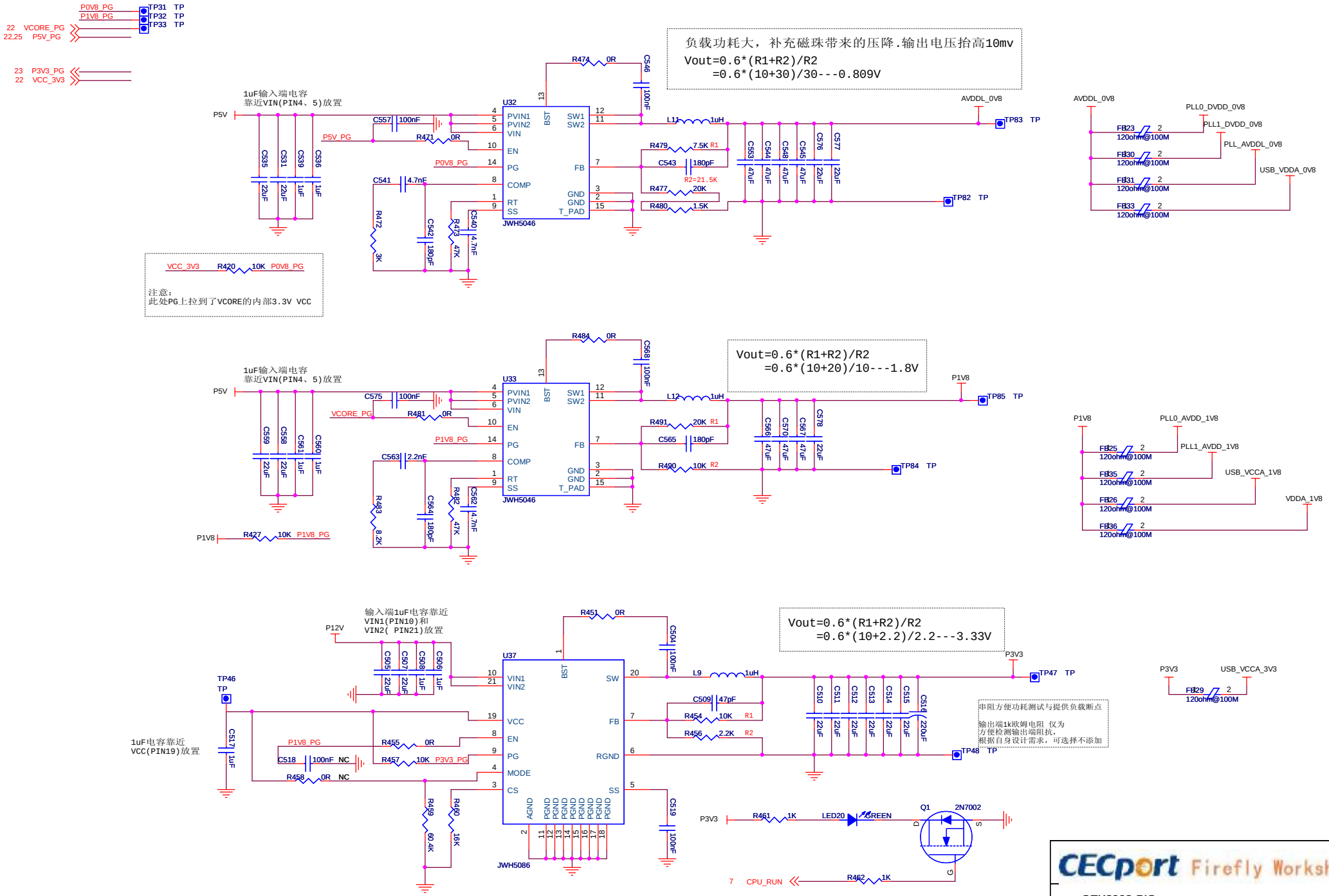
P0V8_PG
P1V8_PG
22 VCORE_PG
22,25 P5V_PG
TP31 TP
TP32 TP
TP33 TP
23 P3V3_PG
22 VCC_3V3
负载功耗大，补充磁珠带来的压降.输出电压抬高10mv
Vout=0.6*(R1+R2)/R2
=0.6*(10+30)/30---0.809V
1uF输入端电容
靠近VIN(PIN4、5)放置
P5V
U32
JWH5046
PVIN1
PVIN2
VIN
EN
PG
COMP
RT
SS
BST
SW1
SW2
FB
GND
T_PAD
R474 0R
C546 100nF
L11 1uH
AVDDL_0V8
TP83 TP
TP82 TP
R479 7.5K R1
C543 180pF
R2=21.5K
R477 20K
R480 1.5K
C557 100nF
R471 0R
C541 4.7nF
R472 3K
C542 180pF
R473 47K
C540 4.7nF
C535 22uF
C531 22uF
C539 1uF
C536 1uF
C553 47uF
C544 47uF
C548 47uF
C545 47uF
C576 22uF
C577 22uF
PLL0_DVDD_0V8
PLL1_DVDD_0V8
PLL_AVDDL_0V8
USB_VDDA_0V8
FB23 120ohm@100M
FB30 120ohm@100M
FB31 120ohm@100M
FB33 120ohm@100M
VCC_3V3 R420 10K P0V8_PG
注意：
此处PG上拉到了VCORE的内部3.3V VCC
Vout=0.6*(R1+R2)/R2
=0.6*(10+20)/10---1.8V
1uF输入端电容
靠近VIN(PIN4、5)放置
P1V8
U33
JWH5046
R484 0R
C568 100nF
L12 1uH
TP85 TP
TP84 TP
R491 20K R1
C565 180pF
R490 10K R2
C575 100nF
R481 0R
C563 2.2nF
R483 8.2K
C564 180pF
R482 47K
C562 4.7nF
C559 22uF
C558 22uF
C561 1uF
C560 1uF
C566 47uF
C570 47uF
C567 47uF
C578 22uF
PLL0_AVDD_1V8
PLL1_AVDD_1V8
USB_VCCA_1V8
VDDA_1V8
FB25 120ohm@100M
FB35 120ohm@100M
FB26 120ohm@100M
FB36 120ohm@100M
P1V8 R427 10K P1V8_PG
输入端1uF电容靠近
VIN1(PIN10)和
VIN2(PIN21)放置
P12V
U37
JWH5086
VIN1
VIN2
VCC
EN
PG
MODE
CS
BST
SW
FB
RGND
SS
AGND
PGND
R451 0R
C504 100nF
L9 1uH
P3V3
TP47 TP
TP48 TP
C509 47pF
R454 10K R1
R456 2.2K R2
C510 22uF
C511 22uF
C512 22uF
C513 22uF
C514 22uF
C515 22uF
C516 220uF
串阻方便功耗测试与提供负载断点
输出端1k欧姆电阻 仅为
方便检测输出端阻抗，
根据自身设计需求，可选择不添加
C505 22uF
C507 22uF
C508 1uF
C506 1uF
TP46
TP
C517 1uF
1uF电容靠近
VCC(PIN19)放置
P1V8_PG
R455 0R
C518 100nF NC
R457 10K P3V3_PG
R458 0R NC
R459 60.4K
R460 16K
C519 100nF
P3V3
USB_VCCA_3V3
FB29 120ohm@100M
R461 1K
LED20
GREEN
Q1
2N7002
R462 1K
7 CPU_RUN
Mode ---> PFM 1000KHz
Ilim ---> 9.5A
Tss ---> 1.14ms
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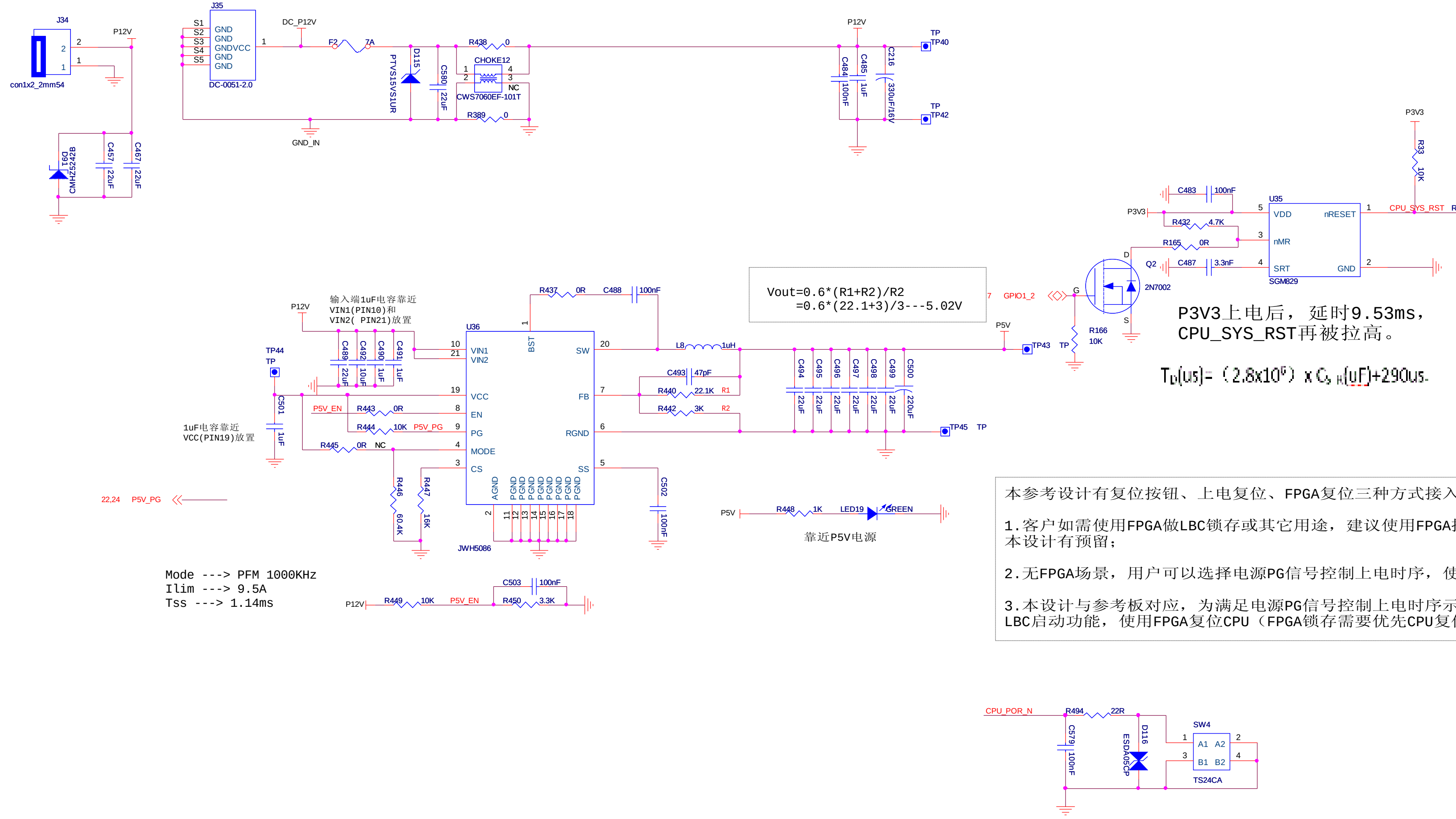

Vout=0.6*(R1+R2)/R2
=0.6*(22.1+3)/3---5.02V

P3V3上电后，延时9.53ms，
CPU_SYS_RST再被拉高。

$T_D(us) = (2.8\times10^5)\times C_{SRT}(uF) + 290us$

Mode ---> PFM 1000KHz
Ilim ---> 9.5A
Tss ---> 1.14ms

本参考设计有复位按钮、上电复位、FPGA复位三种方式接入了CPU的POR_RST：

1.客户如需使用FPGA做LBC锁存或其它用途，建议使用FPGA控制上电复位，
本设计有预留；

2.无FPGA场景，用户可以选择电源PG信号控制上电时序，使用复位芯片上电复位；

3.本设计与参考板对应，为满足电源PG信号控制上电时序示例的同时，验证
LBC启动功能，使用FPGA复位CPU（FPGA锁存需要优先CPU复位）。

CECport Firefly Workshop

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