1. Description

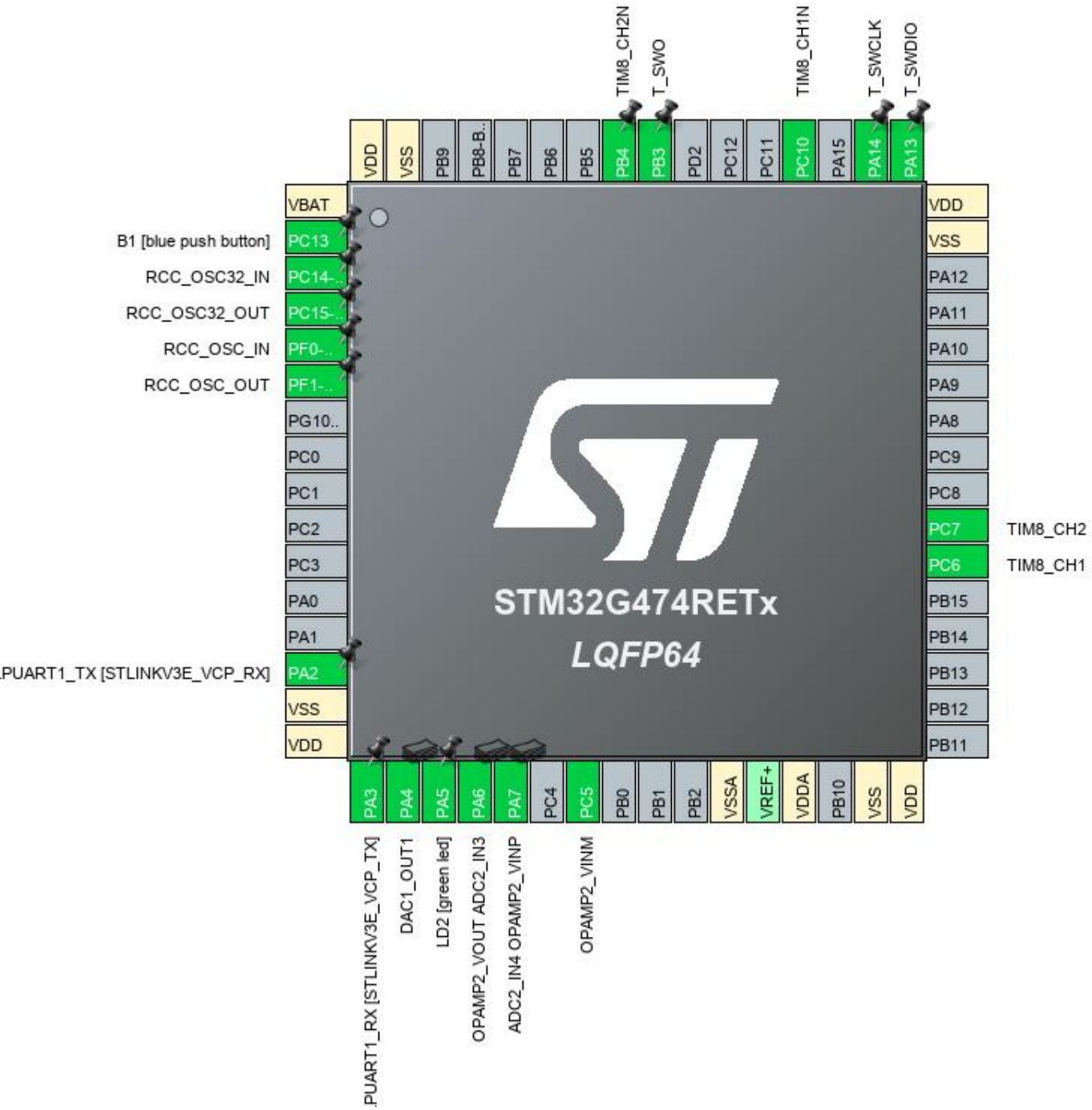
1.1. Project

Project Name	g4-usonic-wind1
Board Name	NUCLEO-G474RE
Generated with:	STM32CubeMX 5.5.0
Date	01/08/2020

1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x4
MCU name	STM32G474RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration

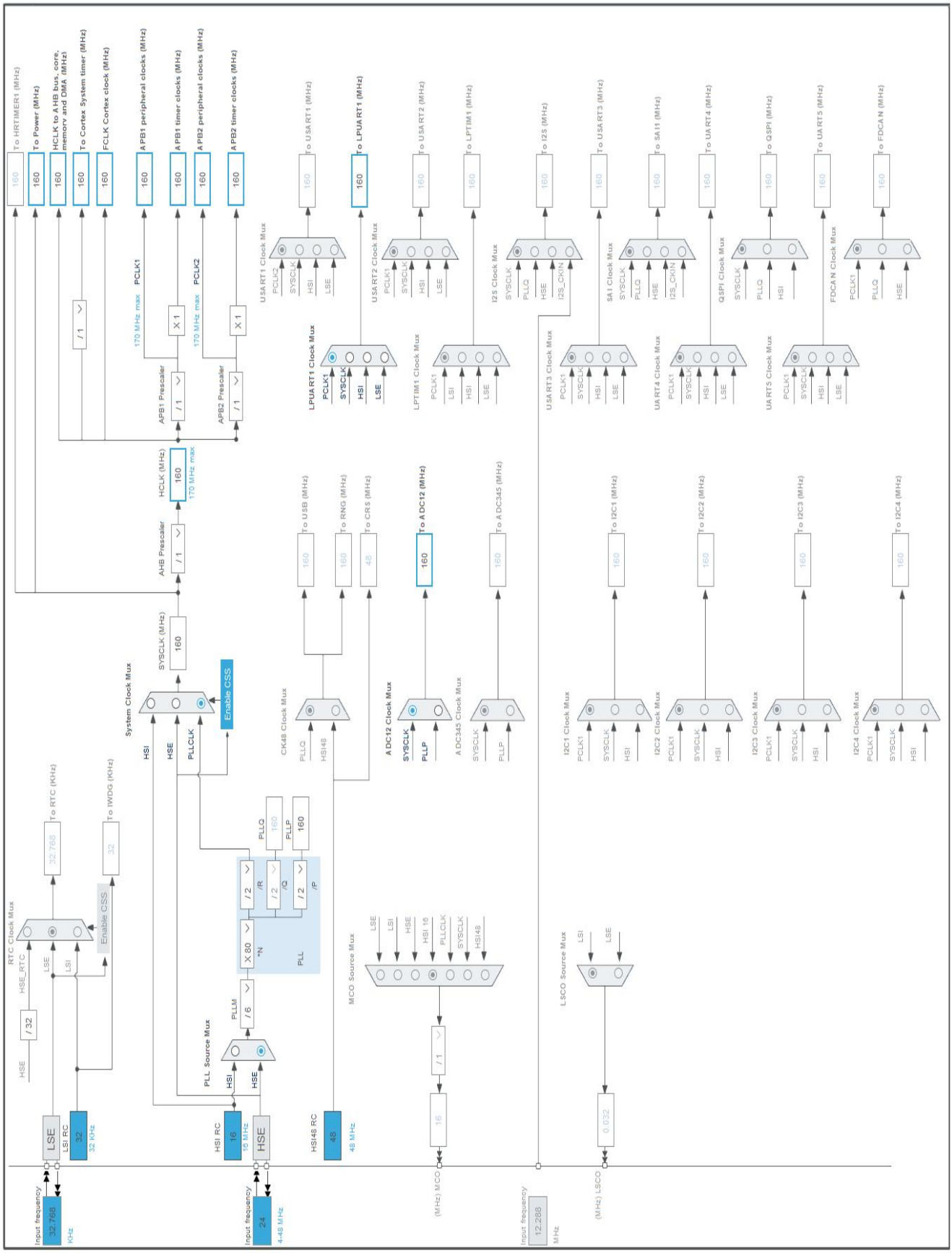


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [blue push button]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
14	PA2	I/O	LPUART1_TX	LPUART1_TX [STLINKV3E_VCP_RX]
15	VSS	Power		
16	VDD	Power		
17	PA3	I/O	LPUART1_RX	LPUART1_RX [STLINKV3E_VCP_TX]
18	PA4	I/O	DAC1_OUT1	
19	PA5 *	I/O	GPIO_Output	LD2 [green led]
20	PA6	I/O	OPAMP2_VOUT, ADC2_IN3	
21	PA7	I/O	ADC2_IN4, OPAMP2_VINP	
23	PC5	I/O	OPAMP2_VINM	
27	VSSA	Power		
29	VDDA	Power		
31	VSS	Power		
32	VDD	Power		
38	PC6	I/O	TIM8_CH1	
39	PC7	I/O	TIM8_CH2	
47	VSS	Power		
48	VDD	Power		
49	PA13	I/O	SYS_JTMS-SWDIO	T_SWDIO
50	PA14	I/O	SYS_JTCK-SWCLK	T_SWCLK
52	PC10	I/O	TIM8_CH1N	
56	PB3	I/O	SYS_JTDO-SWO	T_SWO
57	PB4	I/O	TIM8_CH2N	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	g4-usonic-wind1
Project Folder	D:\projects\g4-usonic-wind1
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.1.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x4
MCU	STM32G474RETx
Datasheet	DS12288_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. ADC2

IN3: IN3 Differential

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Low Power Auto Wait	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
Overrun behaviour	Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. CORDIC

mode: Activated

7.3. DAC1

OUT1 mode: Connected to external pin only

7.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
DAC High Frequency	Mode Automatic
DMA Double Data	Disable
Signed Format	Disable
Trigger	None
Trigger2	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.4. GPIO

7.5. LPUART1

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.6. OPAMP2

Mode: Standalone

7.6.1. Parameter Settings:

Basic Parameters:

Power Mode	Normal
User Trimming	Disable

7.7. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.7.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	7WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1 boost

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.8. SYS

Debug: Trace Asynchronous Sw

VREFBUF Mode: External voltage reference

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.9. TIM8

Channel1: Output Compare CH1 CH1N

Channel2: Output Compare CH2 CH2N

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**1999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Output Compare (OC4REF) ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable

BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
DeadTime Preload	Disable
Dead Time	0
Asymmetrical DeadTime	Disable
Falling Dead Time	0

Clear Input:

Clear Input Source	Disable

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

Output Compare Channel 1 and 1N:

Mode	**Toggle on match ***
Pulse (16 bits value)	**300 ***
Output compare preload	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 2 and 2N:

Mode	**Toggle on match ***
Pulse (16 bits value)	**600 ***
Output compare preload	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC2	PA6	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC2_IN4	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
LPUART1	PA2	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LPUART1_TX [STLINKV3E_VCP_RX]
	PA3	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LPUART1_RX [STLINKV3E_VCP_TX]
OPAMP2	PA6	OPAMP2_VOUT	Analog mode	No pull-up and no pull-down	n/a	
	PA7	OPAMP2_VINP	Analog mode	No pull-up and no pull-down	n/a	
	PC5	OPAMP2_VINM	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	T_SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	T_SWCLK
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	T_SWO
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC10	TIM8_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4	TIM8_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B1 [blue push button]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green led]

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC2	DMA1_Channel1	Peripheral To Memory	Low

ADC2: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupt	unused		
TIM8 break interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger and commutation interrupts	unused		
TIM8 capture compare interrupt	unused		
TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts	unused		
FPU global interrupt	unused		
LPUART1 global interrupt	unused		
CORDIC interrupt	unused		

*** User modified value**

9. Software Pack Report