



## 1. Description

### 1.1. Project

Project Name	mech_mast_module
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	04/27/2021

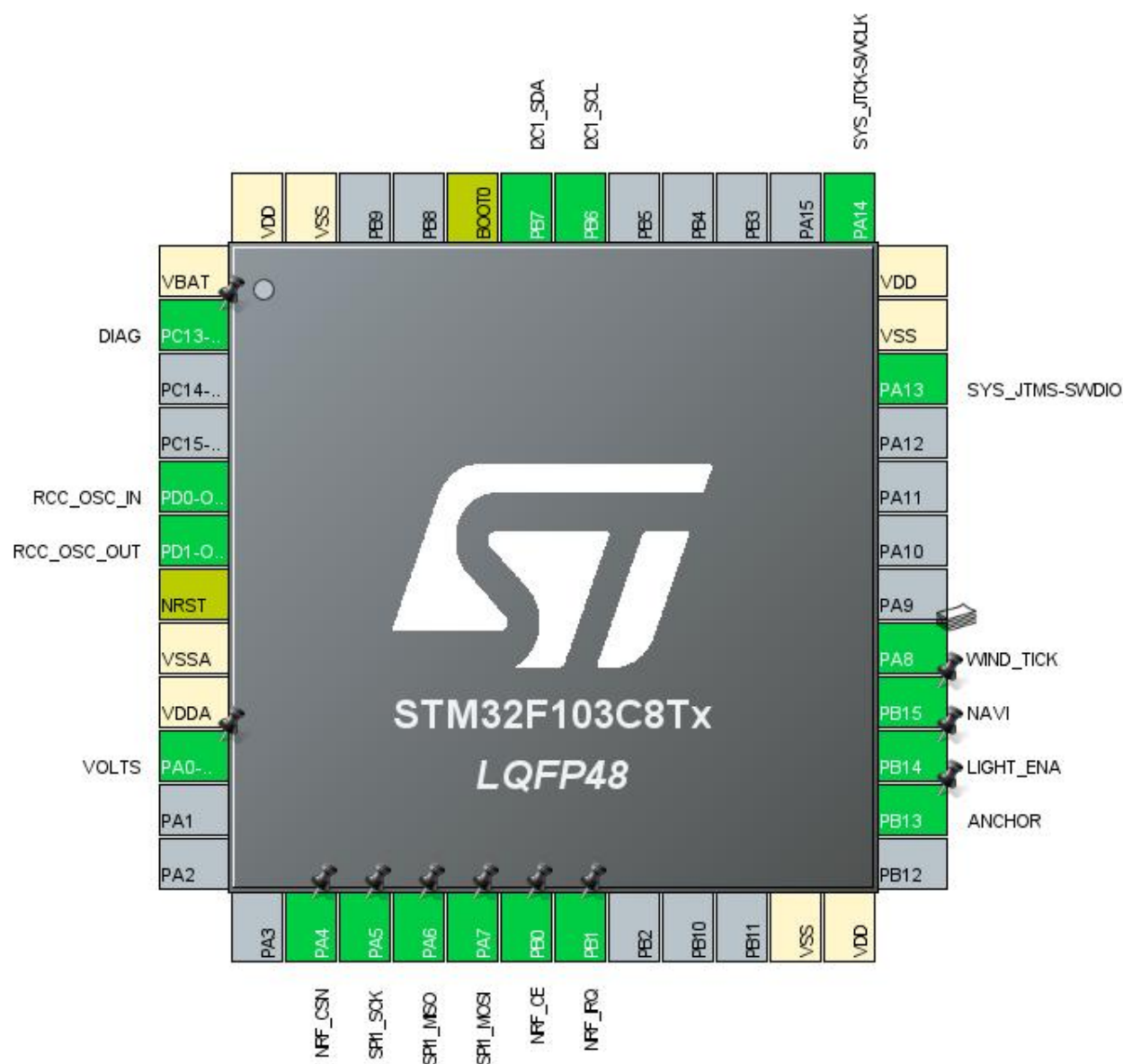
### 1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

### 1.3. Core(s) information

Core(s)	Arm Cortex-M3
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## 2. Pinout Configuration

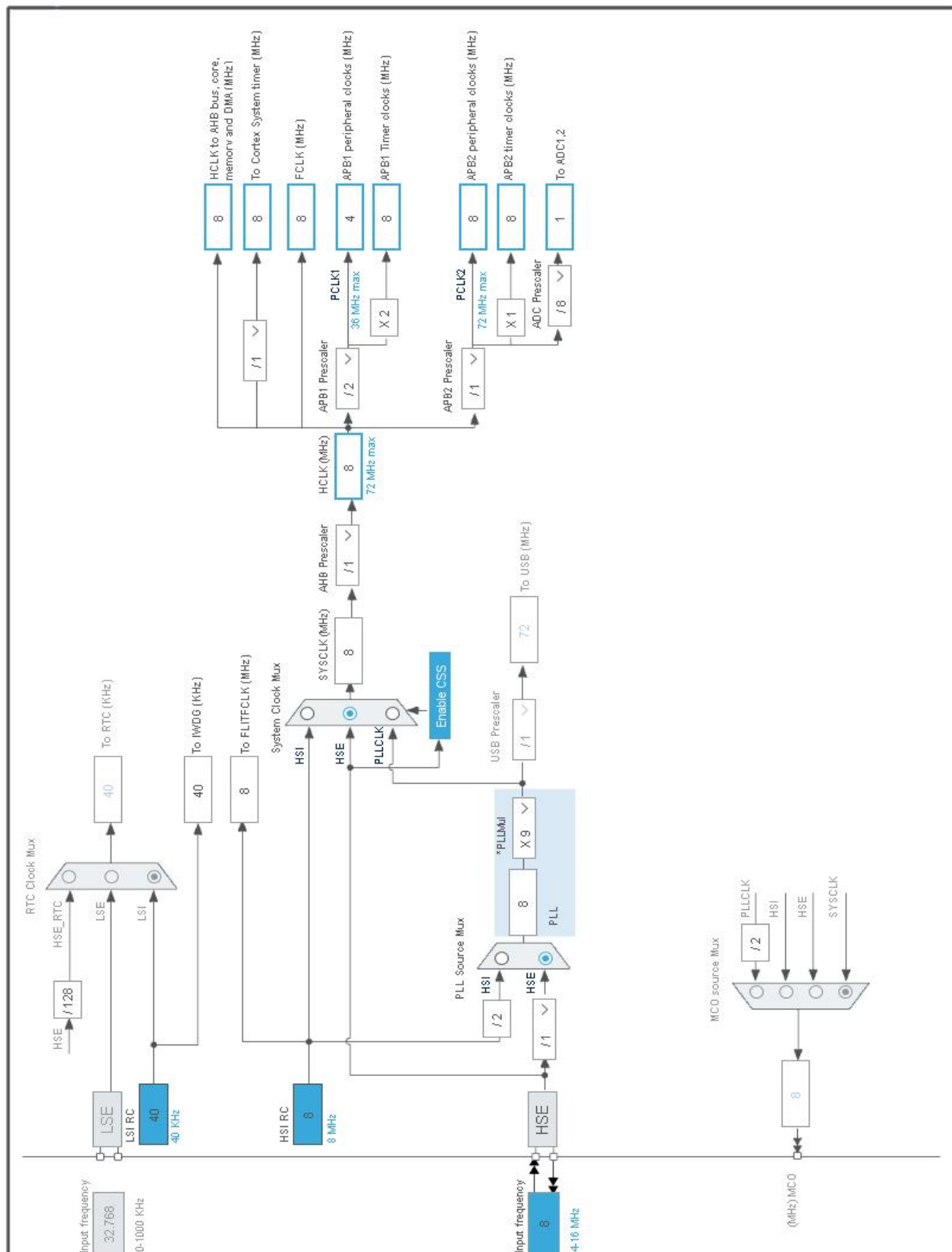


### 3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Output	DIAG
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	ADC1_IN0	VOLTS
14	PA4 *	I/O	GPIO_Output	NRF_CSN
15	PA5	I/O	SPI1_SCK	
16	PA6	I/O	SPI1_MISO	
17	PA7	I/O	SPI1_MOSI	
18	PB0 *	I/O	GPIO_Output	NRF_CE
19	PB1	I/O	GPIO_EXTI1	NRF_IRQ
23	VSS	Power		
24	VDD	Power		
26	PB13 *	I/O	GPIO_Output	ANCHOR
27	PB14 *	I/O	GPIO_Output	LIGHT_ENA
28	PB15 *	I/O	GPIO_Output	NAVI
29	PA8	I/O	TIM1_CH1	WIND_TICK
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
42	PB6	I/O	I2C1_SCL	
43	PB7	I/O	I2C1_SDA	
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	mech_mast_module
Project Folder	D:\projects\windsensor\mech_mast_module
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.3
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	Yes

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_I2C1_Init	I2C1
4	MX_SPI1_Init	SPI1
5	MX_ADC1_Init	ADC1
6	MX_TIM1_Init	TIM1
7	MX_IWDG_Init	IWDG
8	MX_TIM2_Init	TIM2

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	DS5319_Rev17

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

#### 6.4. Sequence

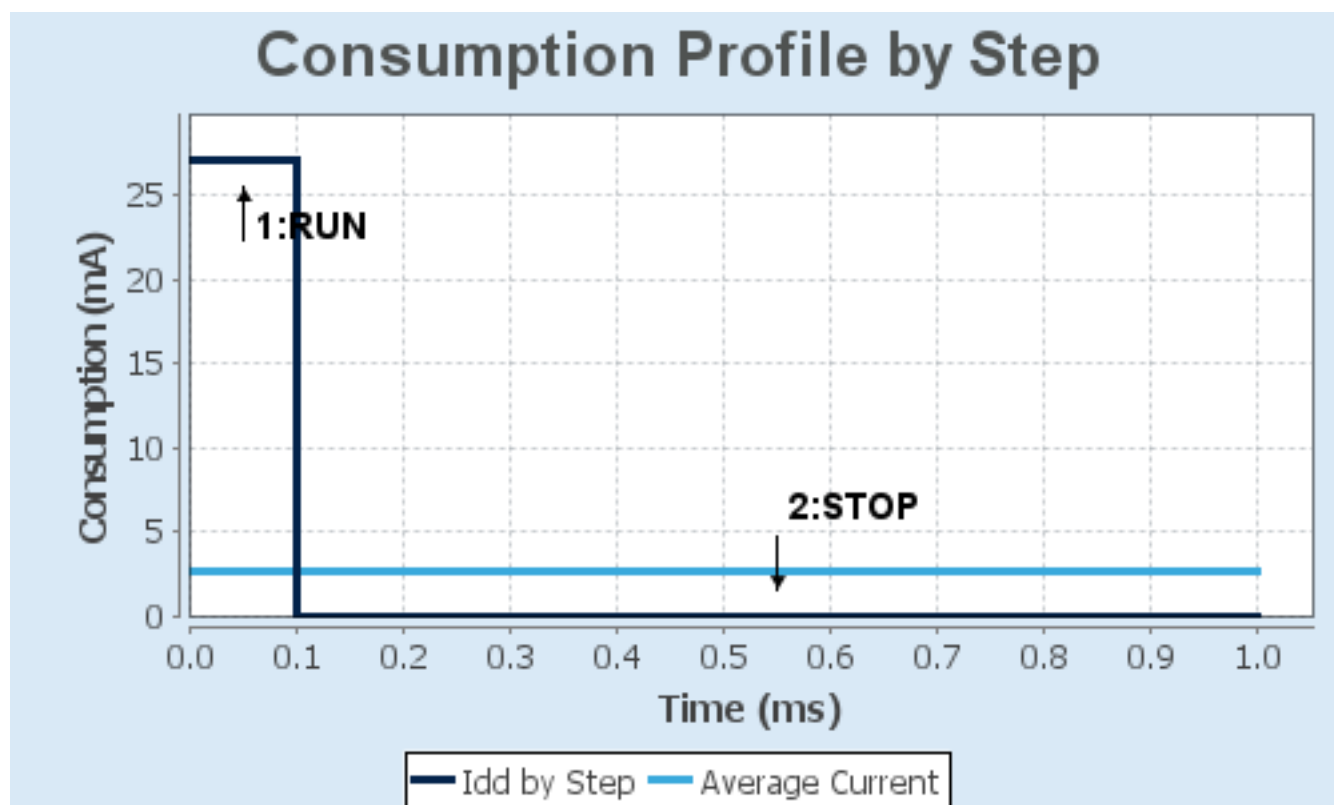
<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	No Scale	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	72 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP
<b>Clock Source Frequency</b>	8 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	27 mA	14 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	90.0	0.0
<b>Ta Max</b>	100.1	105
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days, 17 hours	Average DMIPS	61.0 DMIPS

#### 6.6. Chart





## 7. Peripherals and Middlewares Configuration

### 7.1. ADC1

mode: IN0

mode: Vrefint Channel

#### 7.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Data Alignment Right alignment

Scan Conversion Mode Enabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions **Disable \***

##### ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

External Trigger Source Injected Conversion launched by software

##### WatchDog:

Enable Analog WatchDog Mode false

### 7.2. I2C1

I2C: I2C

#### 7.2.1. Parameter Settings:

##### Master Features:

I2C Speed Mode Standard Mode

I2C Clock Speed (Hz) **30000 \***

##### Slave Features:

Clock No Stretch Mode Disabled

Primary Address Length selection 7-bit

Dual Address Acknowledged Disabled

Primary slave address 0

General Call address detection Disabled

### 7.3. IWDG

**mode: Activated**

#### 7.3.1. Parameter Settings:

**Clocking:**

IWDG counter clock prescaler	4
IWDG down-counter reload value	4095

### 7.4. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

#### 7.4.1. Parameter Settings:

**System Parameters:**

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

**RCC Parameters:**

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

### 7.5. SPI1

**Mode: Full-Duplex Master**

#### 7.5.1. Parameter Settings:

**Basic Parameters:**

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

**Clock Parameters:**

Prescaler (for Baud Rate)	<b>16 *</b>
Baud Rate	<b>500.0 KBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
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NSS Signal Type

Software

## 7.6. SYS

**Debug: Serial Wire**

**Timebase Source: SysTick**

## 7.7. TIM1

**Clock Source : Internal Clock**

**Combined Channels: PWM Input on CH1**

### 7.7.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>799 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	<b>Compare Pulse (OC1) *</b>

#### **PWM Input CH1 :**

Input Trigger	TI1FP1
Slave Mode Controller	Reset Mode
____ Parameters for Channel 1 ____	
Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	<b>8 *</b>

____ Parameters for Channel 2 ____	
Polarity Selection (opposite CH1)	Falling Edge
IC Selection	Indirect
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

## 7.8. TIM2

## Clock Source : Internal Clock

### 7.8.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>7999 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>99 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

\* User modified value

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	VOLTS
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	n/a	High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	n/a	High *	
RCC	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	n/a	High *	
	PA6	SPI1_MISO	Input mode	No pull-up and no pull-down	n/a	
	PA7	SPI1_MOSI	Alternate Function Push Pull	n/a	High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Input mode	Pull-up *	n/a	WIND_TICK
GPIO	PC13-TAMPER-RTC	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIAG
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NRF_CSN
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	NRF_CE
	PB1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	NRF_IRQ
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ANCHOR
	PB14	GPIO_Output	Output Open Drain *	No pull-up and no pull-down	Low	LIGHT_ENA
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NAVI

### 8.2. DMA configuration

nothing configured in DMA service

### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line1 interrupt	true	0	0
TIM1 capture compare interrupt	true	0	0
TIM2 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		

#### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line1 interrupt	false	true	true
TIM1 capture compare interrupt	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
TIM2 global interrupt	false	true	false

\* User modified value



## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

Middleware

System Core	Analog	Timers	Connectivity	Computing
DMA	ADC1	TIM1	I2C1	
GPIO		TIM2	SPI1	
IWDG				
NVIC				
RCC				
SYS				

## 10. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/CD00161566.pdf">http://www.st.com/resource/en/datasheet/CD00161566.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/CD00171190.pdf">http://www.st.com/resource/en/reference_manual/CD00171190.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/CD00228163.pdf">http://www.st.com/resource/en/programming_manual/CD00228163.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/CD00283419.pdf">http://www.st.com/resource/en/programming_manual/CD00283419.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/CD00190234.pdf">http://www.st.com/resource/en/errata_sheet/CD00190234.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00160362.pdf">http://www.st.com/resource/en/application_note/CD00160362.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00164185.pdf">http://www.st.com/resource/en/application_note/CD00164185.pdf</a>
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Application note	<a href="http://www.st.com/resource/en/application_note/CD00249778.pdf">http://www.st.com/resource/en/application_note/CD00249778.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00259245.pdf">http://www.st.com/resource/en/application_note/CD00259245.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264321.pdf">http://www.st.com/resource/en/application_note/CD00264321.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264342.pdf">http://www.st.com/resource/en/application_note/CD00264342.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264379.pdf">http://www.st.com/resource/en/application_note/CD00264379.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00024853.pdf">http://www.st.com/resource/en/application_note/DM00024853.pdf</a>
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