
STM32
CubeMX

1. Description

1.1. Project

Project Name	mech_deck_module
Board Name	NUCLEO-L476RG
Generated with:	STM32CubeMX 6.2.1
Date	06/07/2021

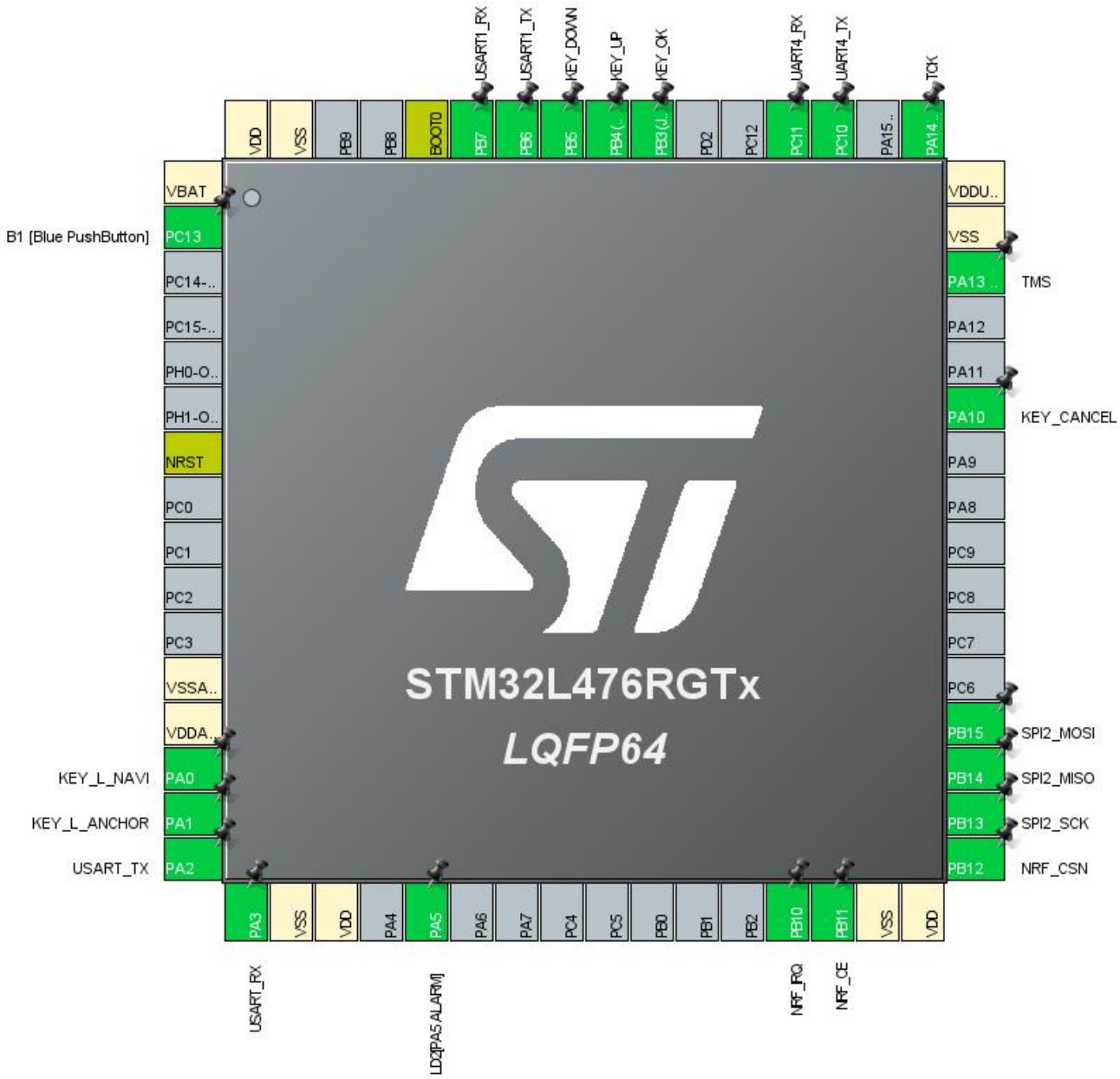
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

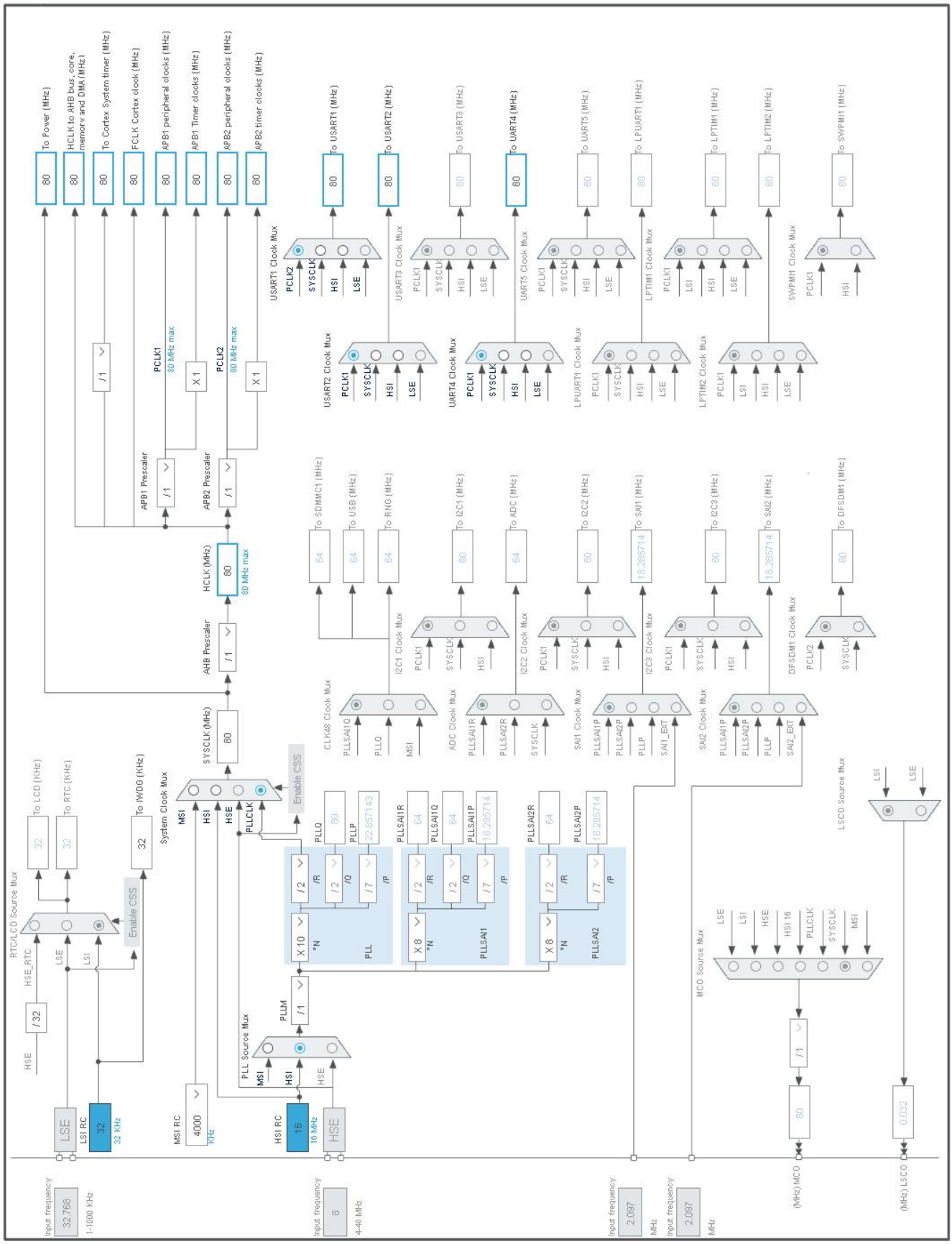


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
7	NRST	Reset		
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0 *	I/O	GPIO_Input	KEY_L_NAVI
15	PA1 *	I/O	GPIO_Input	KEY_L_ANCHOR
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5	I/O	TIM2_CH1	LD2[PA5 ALARM]
29	PB10	I/O	GPIO_EXTI10	NRF_IRQ
30	PB11 *	I/O	GPIO_Output	NRF_CE
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	NRF_CSN
34	PB13	I/O	SPI2_SCK	
35	PB14	I/O	SPI2_MISO	
36	PB15	I/O	SPI2_MOSI	
43	PA10 *	I/O	GPIO_Input	KEY_CANCEL
46	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDDUSB	Power		
49	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
51	PC10	I/O	UART4_TX	
52	PC11	I/O	UART4_RX	
55	PB3 (JTDO-TRACESWO) *	I/O	GPIO_Input	KEY_OK
56	PB4 (NJTRST) *	I/O	GPIO_Input	KEY_UP
57	PB5 *	I/O	GPIO_Input	KEY_DOWN
58	PB6	I/O	USART1_TX	
59	PB7	I/O	USART1_RX	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	mech_deck_module
Project Folder	D:\projects\windsensor\mech_deck_module
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x1200
Minimum Stack Size	0x1400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_UART4_Init	UART4
4	MX_USART2_UART_Init	USART2
5	MX_SPI2_Init	SPI2
6	MX_USART1_UART_Init	USART1
7	MX_IWDG_Init	IWDG
8	MX_TIM2_Init	TIM2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476RGTx
Datasheet	DS10198_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

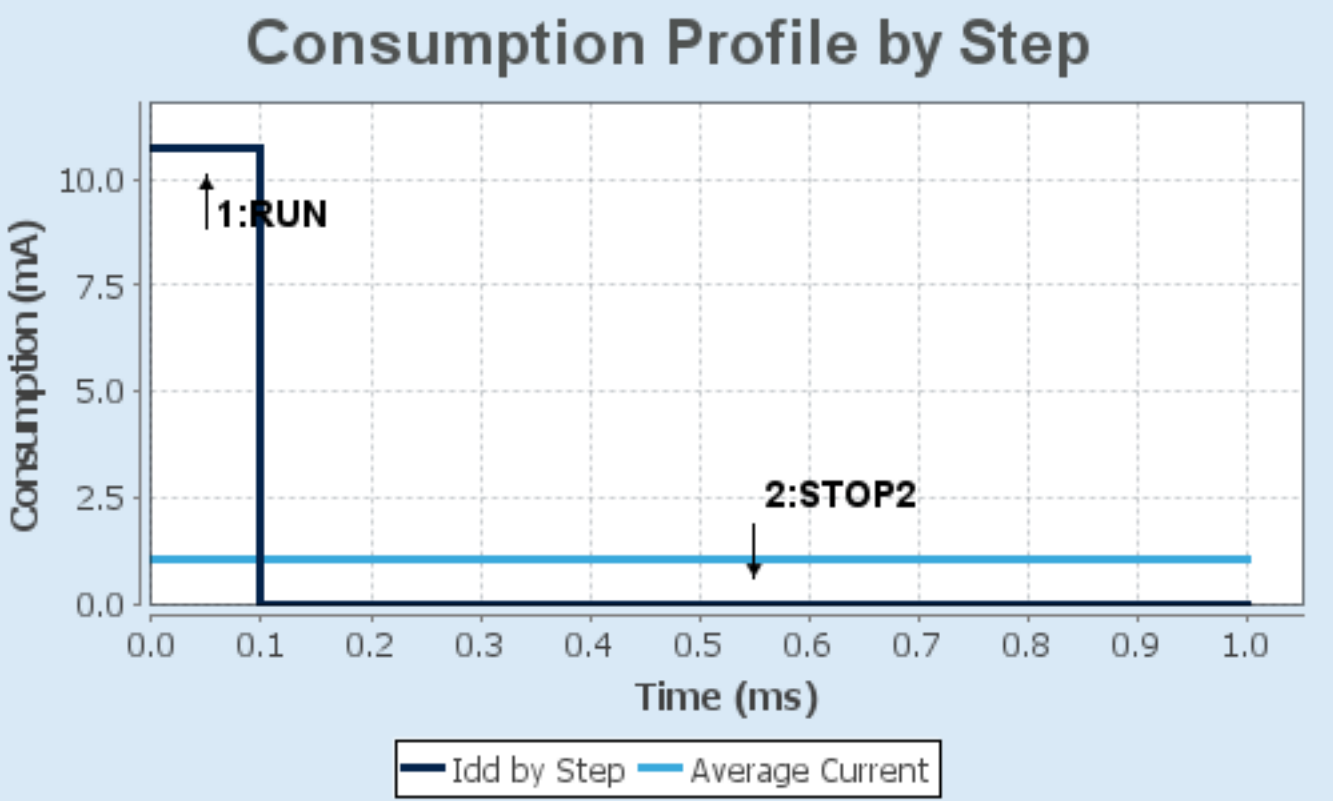
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10.7 mA	1.18 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.56	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10 days, 3 hours	Average DMIPS	100.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP2
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. IWDG

mode: Activated

7.1.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	**64 ***
IWDG window value	4095
IWDG down-counter reload value	4095

7.2. RCC

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.3. SPI2

Mode: Full-Duplex Master

7.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**2.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**9999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	**999 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.6. UART4

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	**625000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	**Transmit Only ***
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.7. USART1

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.8. USART2

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LD2[PA5 ALARM]
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART1	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USART_RX
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA0	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY_L_NAVI
	PA1	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY_L_ANCHOR
	PB10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	NRF_IRQ
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	NRF_CE
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High**	NRF_CSN

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PA10	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY_CANCEL
	PB3 (JTDO-TRACESWO)	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY_OK
	PB4 (NJTRST)	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY_UP
	PB5	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY_DOWN

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM2 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
UART4 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

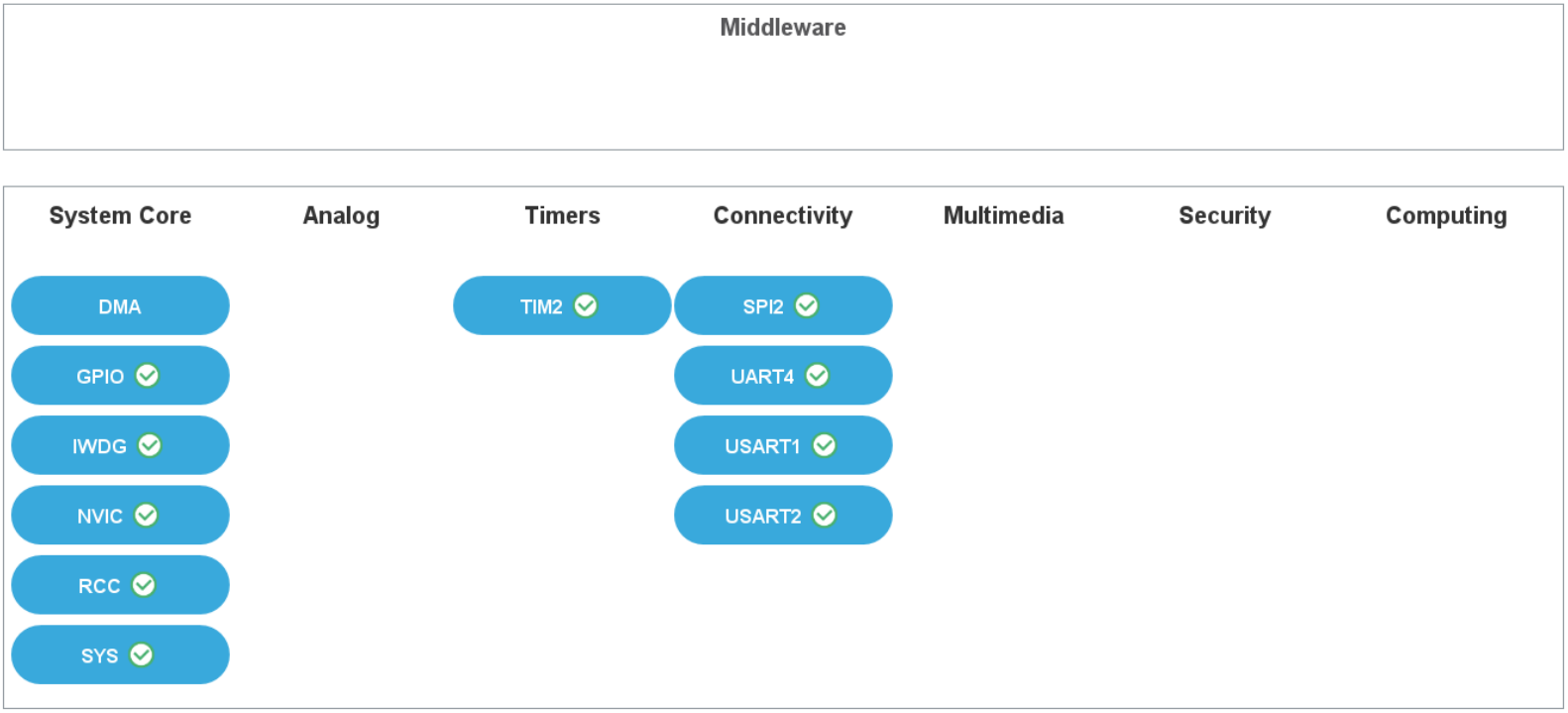
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00108832.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00083560.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00111498.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00125306.pdf
Application note	http://www.st.com/resource/en/application_note/DM00141025.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00148033.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209768.pdf
Application note	http://www.st.com/resource/en/application_note/DM00216518.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00269143.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00223574.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
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