MP5475

Fully Integrated, 12V, 6A, Quad-Buck PMIC with I²C, Telemetry, and Flexible System Configurations

DESCRIPTION

The MP5475 is a complete power management IC (PMIC) that integrates four high efficiency step-down DC/DC converters and a flexible logic interface.

The integrated DC/DC converters provide constant-on-time (COT) control to achieve fast transient response. In addition, the 1MHz switching frequency (f_{SW}) minimizes the external inductor and capacitor size. Full protection features include under-voltage lockout (UVLO), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The output voltage (V_{OUTx}) (where x = A, B, C, or D) can be adjusted via the I²C bus, or it can be preset by the multiple-time programmable (MTP) memory function. The power on/off sequence can also be configured by the MTP, or it can be controlled online via the I²C.

The first two rails or the last two rails can work in either independent mode or parallel mode, which can be configured via the MTP. The current-sharing function is implemented in parallel mode.

The MP5475 requires a minimal number of external components, and it is available in a space-saving QFN-35 (5mmx5mm) package.

FEATURES

- Wide 3V to 16V Input Voltage (V_{INx}) (where x = A, B, C, or D) Range
- Adaptive Constant-On-Time (COT) Control for Ultra-Fast Transient Response
- Four High-Efficiency Step-Down Converters:
  - Buck A: 6A, 15mΩ/5mΩ DC/DC Converter
  - Buck B: 6A, 15mΩ/5mΩ DC/DC Converter
  - Buck C: 6A, 15mΩ/5mΩ DC/DC Converter
  - Buck D: 6A, 15mΩ/5mΩ DC/DC Converter

FEATURES *(continued)*

- Buck A/B and Buck C/D Support Up to 12A of Continuous Current in Dual-Phase Mode
- 2 x 50mA Low-Dropout (LDO) Regulators
- Differential Output Voltage (V_{OUTx}) (where x = A, B, C, or D) Remote Sense
- I²C Slave Address Configurable via the Multiple-Time Programmable (MTP) Memory
- I²C-Configurable, 0.3V to 2.048V Reference Voltage (V_{REF}) in 2mV Steps with Slew Rate Control
- Configurable 500kHz to 2MHz Switching Frequency (f_{SW})
- Open-Drain Power Good (PG) Indication and General Status Interrupt
- MTP-Configurable Soft-Start (SS)/Soft Shutdown and Delay
- Selectable Pulse-Frequency Modulation (PFM)/Pulse-Width Modulation (PWM) Mode, Adjustable Frequency, and Current Limit via the I²C
- Pre-Biased Start-Up
- Over-Current Protection (OCP), Under-Voltage Lockout (UVLO), Under-Voltage Protection (UVP), Over-Voltage Protection (OVP), and Thermal Shutdown Protection
- Available in a QFN-35 (5mmx5mm) Package

MPL Optimized Performance with MPS Inductor MPL4020 Series

APPLICATIONS

- Storage and Networking
- Enterprise Solid-State Drives (SSDs)
- General Enterprise Applications

TYPICAL APPLICATIONS

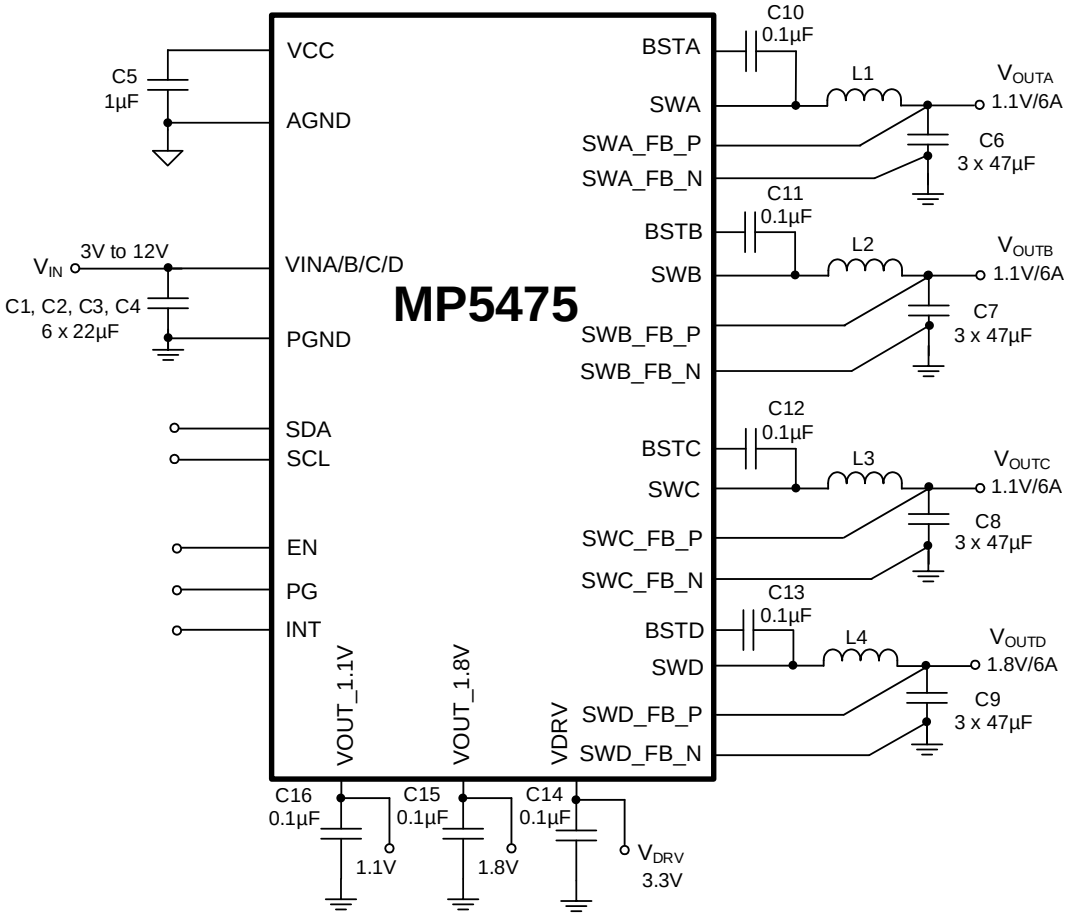


Figure 1: Typical Application (Buck A and Buck B in Single-Phase Regulator Mode)

TYPICAL APPLICATIONS *(continued)*

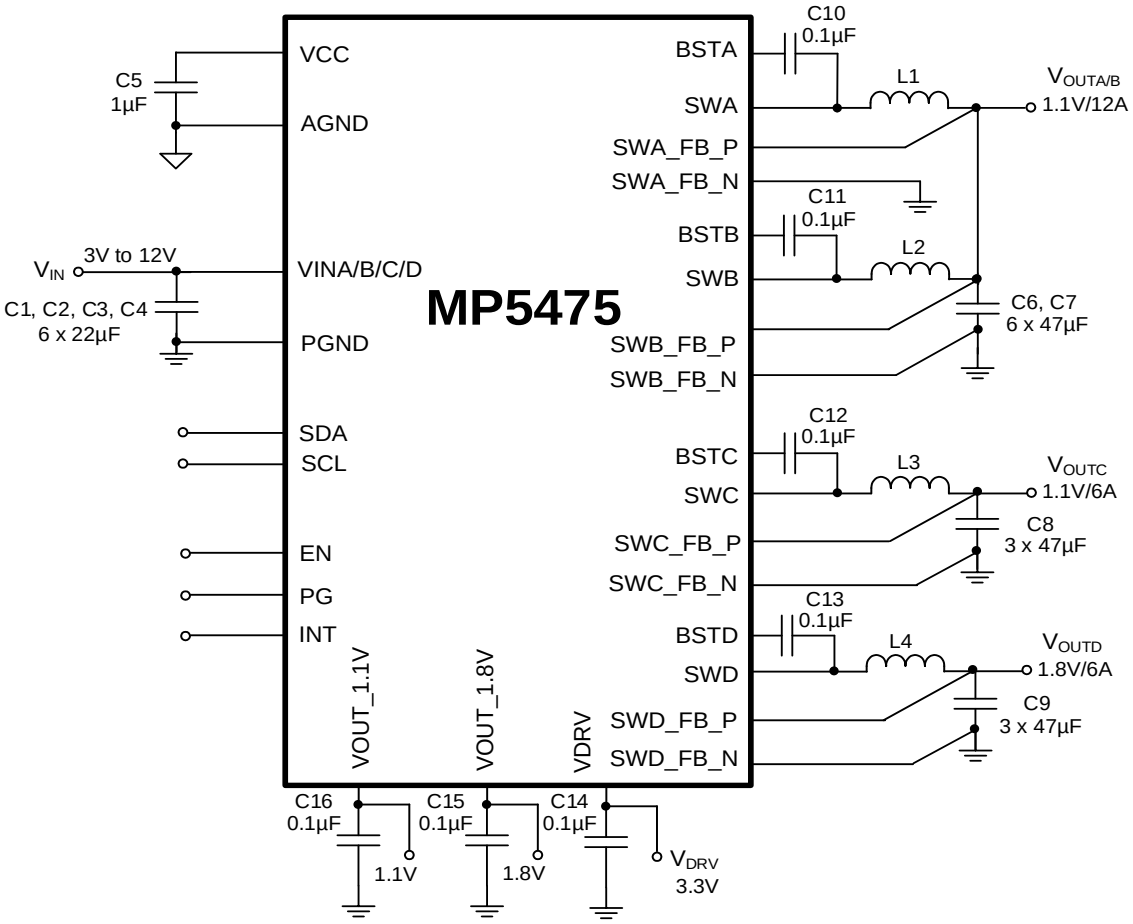
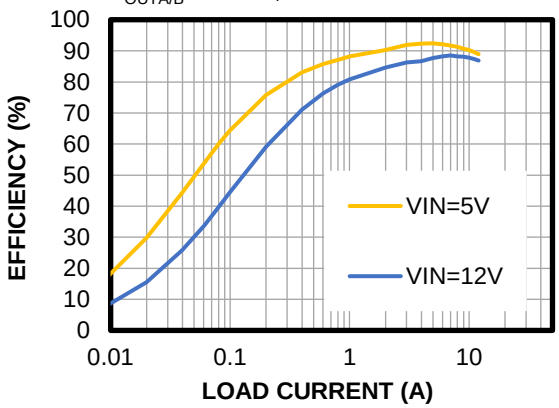


Figure 2: Typical Application (Buck A and Buck B in Dual-Phase Regulator Mode)

TYPICAL APPLICATIONS *(continued)*

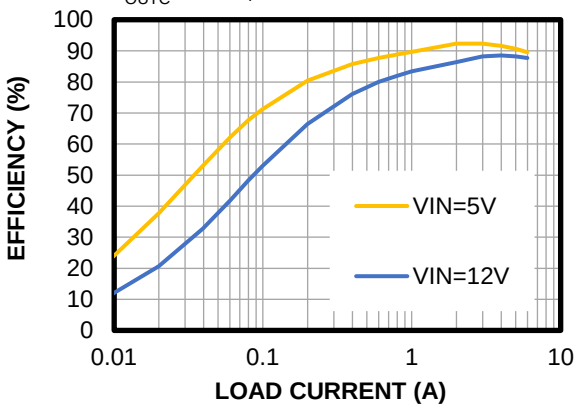
Efficiency vs. Load Current

$V_{OUTA/B}$ = 0.86V, PFM mode



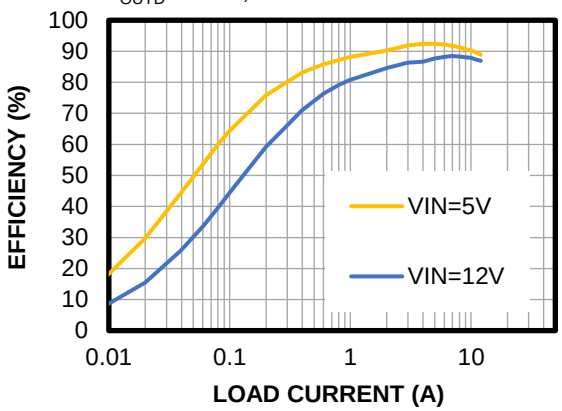
Efficiency vs. Load Current

V_{OUTC} = 0.9V, PFM mode



Efficiency vs. Load Current

V_{OUTD} = 0.9V, PFM mode



DEFAULT MULTIPLE-TIME PROGRAMMABLE (MTP) SELECTION

OTP Items	Buck A	Buck B	Buck C	Buck D
Output voltage (V_{OUT})	1.1V	1.1V	1.1V	1.8V
Initial on/off	On	On	On	On
Mode	Forced PWM	Forced PWM	Forced PWM	Forced PWM
Start-up delay/time slot number	15ms/3	10ms/2	5ms/1	0ms/0
Switching frequency (f_{SW})	750kHz	750kHz	750kHz	750kHz
Low-power mode (LPM)	Disabled	Disabled	Disabled	Disabled
Active voltage positioning (AVP) mode	Disabled		Disabled	
Buck parallel mode	Unparalleled		Unparalleled	
Software initial I²C slave address	0x60			
V_{IN} under-voltage lockout (UVLO) rising threshold	2.85V			
Multiple-time programmable (MTP) configuration code	0000			

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5475GU-xxxx**	QFN-35 (5mmx5mm)	*See Below*	1
MP5475GU-0000			

* For Tape & Reel, add suffix -Z (e.g. MP5475GU-xxxx-Z).

** "xxxx" is the configuration code identifier for the register setting stored in the multiple-time programmable (MTP) memory. The default code is "0000". Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the "0000" code. The MP5475GU-0000 is the default version.

TOP MARKING

MPSYYWW
MP5475
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP5475: part number
LLLLLLL: Lot number

EVALUATION KIT (EVKT-5475)

EVKT-5475 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVL5475-U-00B	MP5475 evaluation board	1
2	EVKT-USBI2C-02	Includes one USB-to-I²C communication interface device, one USB cable, and one ribbon cable	1
3	MP5475GU-0018	MP5475 IC (can be used for MTP configuration)	2
4	Online resources	Includes the datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

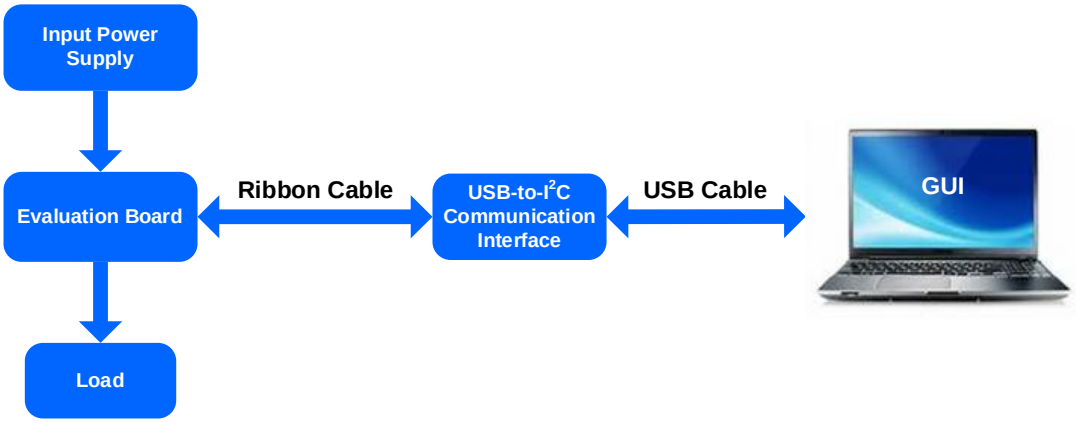
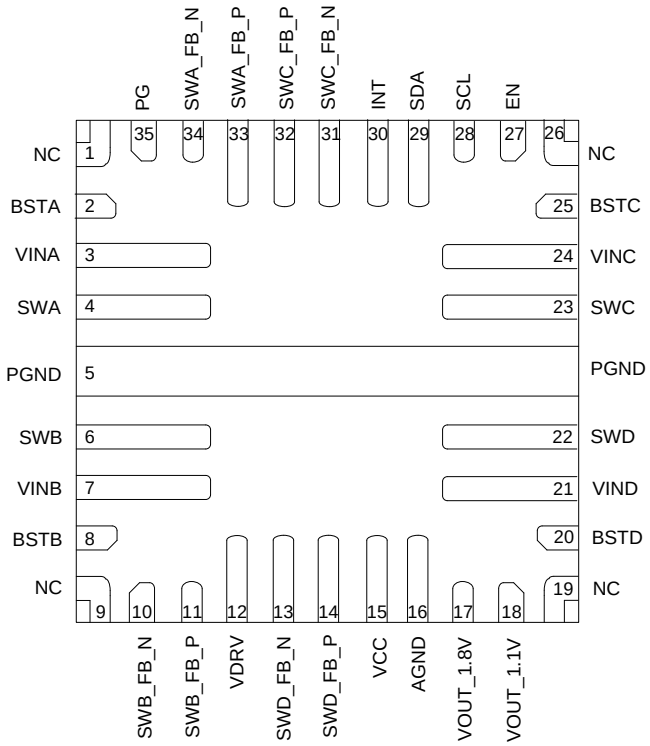


Figure 3: EVKT-5475 Evaluation Kit Set-Up

PACKAGE REFERENCE

TOP VIEW



QFN-35 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 9, 19, 26	NC	**No connection.**
2	BSTA	**Buck converter A (buck A) bootstrap.** Connect a capacitor between the SWA and BSTA pins to form a floating supply across buck A's high-side (HS) switch driver.
3	VINA	**Supply voltage input for buck A.** A ceramic capacitor is required to decouple the input rail. Connect the VINA pin using a wide PCB trace. VINA, VINB, VINC, and VIND must be connected to the same bus voltage.
4	SWA	**Buck A switch output.** Connect the SWA pin using a wide PCB trace.
5	PGND	**Power ground.** The PGND pin requires special consideration during PCB layout. Connect the PGND pin with copper traces and vias.
6	SWB	**Buck converter B (buck B) switch output.** Connect the SWB pin using a wide PCB trace.
7	VINB	**Supply voltage input for buck B.** A ceramic capacitor is required to decouple the input rail. Connect the VINB pin using a wide PCB trace.
8	BSTB	**Buck B bootstrap.** Connect a capacitor between the SWB and BSTB pins to form a floating supply across buck B's HS switch driver.
10	SWB_FB_N	**Negative feedback for buck B.** Kelvin connect the SWB_FB_N pin to the ground node of the output capacitor (C_{OUT}) on buck B.
11	SWB_FB_P	**Positive feedback for buck B.** Connect buck B's output to the SWB_FB_P pin directly.
12	VDRV	**3.3V supply input to the power management IC (PMIC).** Connect a 3.3V power supply to the VDRV pin. If there is no external 3.3V power supply, connect this pin to VCC.
13	SWD_FB_N	**Remote sense ground for buck converter D (buck D).** Kelvin connect the SWD_FB_N pin to the ground node of C_{OUT} on buck D.
14	SWD_FB_P	**Positive feedback for buck D.** Connect buck D's output to the SWD_FB_P pin directly.
15	VCC	**Internal 3.3V low-dropout (LDO) output.** The driver and control circuits are powered from the VCC pin voltage (V_{CC}). Decouple VCC with a 1µF ceramic capacitor placed as close to the pin as possible. Ceramic capacitors with X7R or X5R dielectrics are recommended due to their stable temperature characteristics.
16	AGND	**Analog ground.** Connect AGND to the power ground pin.
17	VOUT_1.8V	**1.8V LDO output from the PMIC.**
18	VOUT_1.1V	**1.1V LDO output from the PMIC.**
20	BSTD	**Buck D bootstrap.** Connect a capacitor between SWD and BSTD pins to form a floating supply across buck D's HS switch driver.
21	VIND	**Supply voltage input for buck D.** A ceramic capacitor is required to decouple the input rail. Connect the VIND pin using a wide PCB trace.
22	SWD	**Buck D switch output.** Connect the SWD pin using a wide PCB trace.
23	SWC	**Buck converter C (buck C) switch output.** Connect the SWC pin using a wide PCB trace.
24	VINC	**Supply voltage input for buck C.** A ceramic capacitor is required to decouple the input rail. Connect the VINC pin using a wide PCB trace.
25	BSTC	**Buck C bootstrap.** Connect a capacitor between the SWC and BSTC pins to form a floating supply across the buck C's HS switch.
27	EN	**Enable control.** Apply a logic low-to-high transition to the EN pin to enable the PMIC.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
28	SCL	**I²C bus clock.**
29	SDA	**I²C bus data.**
30	INT	**General status interrupt.** The INT pin is an open-drain output. The MP5475 asserts INT low to communicate any single (or more) critical event(s) to the host. INT remains asserted until the appropriate registers are explicitly cleared, or the MP5475 is reset.
31	SWC_FB_N	**Remote-sense ground for buck C.** Kelvin connect the SWC_FB_N pin to the ground node of C_{OUT} on buck C.
32	SWC_FB_P	**Positive feedback for buck C.** Connect buck C's output to the SWC_FB_P pin directly.
33	SWA_FB_P	**Positive feedback for buck A.** Connect buck A's output to the SWA_FB_P pin directly. SWA_FB_P is the feedback input of the dual-phase buck when buck A and buck B are set to dual-phase interleaving mode.
34	SWA_FB_N	**Remote-sense ground of buck A and buck B.** Kelvin connect the SWA_FB_N pin to ground node of C_{OUT} on buck A and buck B.
35	PG	**Open-drain power good (PG) output.** Pull the PG pin low when any enabled regulator falls below its under-voltage (UV) threshold. Pull PG low when all regulators are disabled.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{INx}) 18V
V_{SWx_DC} .....-0.3V to V_{IN} + 0.3V
V_{BSTx} ..... V_{SW} + 4V
V_{CC} 4.3V
All other pins ..... -0.3V to VCC
Junction temperature (T_J) .....170°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +170°C

ESD Ratings (2)

Human body model (HBM) ..... ±2000V
Charged-device model (CDM).....±750V

Recommended Operating Conditions (3)

Supply voltage (V_{INx}) (x = A, B, C, or D).....
.....3V to 16V
V_{IN_DC} - V_{SW_DC} (4).....-0.3V to V_{IN} + 0.3V
V_{SW_DC} (4) .....-0.3V to V_{IN} + 0.3V
Output voltage (V_{OUTx}) (x = A, B, C, or D) .....
…….Refer to the I²C setting
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-35 (5mmx5mm)
EV5475-U-00A (5)..... 25.....2.5 .. °C/W
JESD51-7 (6) ..... 29.....18.1 . °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AECQ100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
3) The device is not guaranteed to function outside of its operating conditions.
4) The voltage rating can be between -3V and +23V for a period of 25ns or shorter with a maximum repetition rate of 1000kHz when V_{IN} is 16V.
5) Measured on the EV5475-U-00A, 4-layer PCB.
6) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Default switching frequency	f_{SW}		850	1000	1150	kHz
EN rising threshold	V_{EN}		1.21	1.25	1.29	V
EN hysteresis	V_{EN_HYS}			220		mV
EN pull-down resistor	R_{EN}			2.2		MΩ
Step-Down Regulators						
V_{INx} under-voltage lockout (UVLO) rising threshold (where x = A, B, C, or D)	$V_{INx\_UVLO\_R}$		2.75	2.85	2.95	V
V_{INx} UVLO hysteresis	$V_{INx\_UVLO\_HYS}$			250		mV
V_{INx} over-voltage (OV) rising threshold			16	16.6	17.5	V
V_{INx} OV hysteresis				650		mV
Feedback (FB) voltage accuracy	V_{FB1}	Default output of buck converter A (buck A), T_J = 25°C	-1%	1.1	+1%	V
	V_{FB2}	Default output of buck converter B (buck B), T_J = 25°C	-1%	1.1	+1%	V
	V_{FB3}	Default output of buck converter C (buck C), T_J = 25°C	-1%	1.1	+1%	V
	V_{FB4}	Default output of buck converter D (buck D), T_J = 25°C	-1%	1.8	+1%	V
FB under-voltage (UV) threshold 1 (low to high) (7)		Hiccup entry (FB UV with OC for 50 cycles)		80		% of V_{REF}
FB UV threshold 2 (high to low) (7)		Hiccup entry (FB UV with 2.5µs deglitch)		75		% of V_{REF}
Buck A, Buck B, Buck C, and Buck D						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS1}$	For buck A/B/C/D		15		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS1}$	For buck A/B/C/D		5		mΩ
Switch leakage	SW_{ILK1}	T_J = 25°C		0	1	µA
Low-side (LS) current limit (source)	$I_{LS\_VALLEY1}$	Valley limit is independent of the high-side (HS) peak current limit	6	7	8	A
Negative current limit	I_{NOCP}	Forced pulse-width modulation (PWM)/OVP discharge		-5		A
Minimum on time (7)	t_{ON_MIN1}			20		ns
Minimum off time (7)	t_{OFF_MIN1}			100		ns
Output over-voltage protection (OVP) rising threshold	V_{OVP1_H}		117	122	127	% of V_{REF}
Output OVP recovery threshold	V_{OVP1_L}			110		% of V_{REF}
Buck A soft-start time	t_{SS_B1}	Default, V_{OUT} = 10% to 90%		0.88		ms
Buck B soft-start time	t_{SS_B2}	Default, V_{OUT} = 10% to 90%		0.88		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Buck C soft-start time	t_{SS_B3}	Default, V_{OUT} = 10% to 90%		0.88		ms
Buck D soft-start time	t_{SS_B4}	Default, V_{OUT} = 10% to 90%		1.44		ms
Low-Dropout (LDO) Regulator						
VDRV voltage (V_{DRV}) UVLO rising threshold			2.8	3	3.2	V
V_{DRV} UVLO falling threshold			2.6	2.8	3	V
V_{DRV} OV rising threshold			3.4	3.6	3.8	V
V_{DRV} OV hysteresis				250		mV
50mA, 1.1V Low-Dropout (LDO) Regulator						
Default output voltage	V_{1V1}	I_{OUT} = 0A to 20mA, power-on state	-5%	1.1	+5%	V
Current limit	I_{LIM_1V1}		50	70		mA
50mA, 1.8V Low-Dropout (LDO) Regulator						
Default output voltage	V_{1V8}	I_{OUT} = 0A to 20mA, power-on state	-5%	1.8	+5%	V
Current limit	I_{LIM_1V8}		50	70		mA
Power Good (PG) and Interrupt (INT)						
PG UV rising threshold	$V_{PG\_UV\_R}$		86	90	94	% of V_{REF}
PG UV falling threshold	$V_{PG\_UV\_F}$			78		% of V_{REF}
PG OV rising threshold	$V_{PG\_OV\_R}$		117	122	127	% of V_{REF}
PG OV falling threshold	$V_{PG\_OV\_F}$			110		% of V_{REF}
PG rising delay (7)	$t_{PG\_R\_DLY}$			500		µs
PG falling delay (7)	$t_{PG\_F\_DLY}$			50		µs
PG output port sink current capability	V_{PG_SINK}	Sink 1mA			0.4	V
INT output port sink current capability	V_{INT_SINK}	Sink 1mA			0.4	V
VCC Regulator						
VCC voltage	V_{CC}	I_{CC} = 25mA		3.5		V
VCC voltage regulation	V_{CC_RG}	I_{CC} = 0mA to 25mA		1		%
Temperature Protection						
Thermal shutdown (7)	T_{OTP_R}			150		°C
Thermal hysteresis (7)	T_{HYS}			20		°C
I²C Signals						
Input high voltage (SDA or SCL)	V_{IH}		1.4			V
Input low voltage (SDA or SCL)	V_{IL}				0.4	V

I²C PORT SIGNAL CHARACTERISTICS (7)

Parameter	Symbol	Condition	C_B = 100pF		C_B = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start command	t_{SU_STA}		160		600		ns
Hold time for a (repeated) start command	t_{HD_STA}		160		600		ns
Low period of the SCL clock	t_{LOW}		160		1300		ns
High period of the SCL clock	t_{HIGH}		60		600		ns
Data set-up time	t_{SU_DAT}		0	10			ns
Data hold time	t_{HD_DAT}		0	70			ns
Rising time of the SCLH signal	t_{R_CL}		10	40	20 x $0.1C_B$	300	ns
Rising time of the SCLH signal after a repeated start command and an acknowledge bit	t_{F_CL1}		10	80	20 x $0.1C_B$	300	ns
Falling time of the SCLH signal	t_{F_CL}		10	40	20 x $0.1C_B$	300	ns
Rising time of the SDAH signal	t_{F_DA}		10	80	20 x $0.1C_B$	300	ns
Falling time of the SDAH signal	t_{F_DA}		10	80	20 x $0.1C_B$	300	ns
Set-up time for stop command	t_{SU_STO}		160		600		ns
Bus free time between a stop and start command	t_{BUF}		160		1300		ns
Data valid time	t_{VD_DAT}			16		90	ns
Data valid acknowledge time	t_{VD_ACK}			160		900	ns
Capacitive load for each bus line	C_B	SDAH and SCLH line		100		400	pF
		SDAH + SDA line, SCLH + SCL line		400		400	pF

Note:

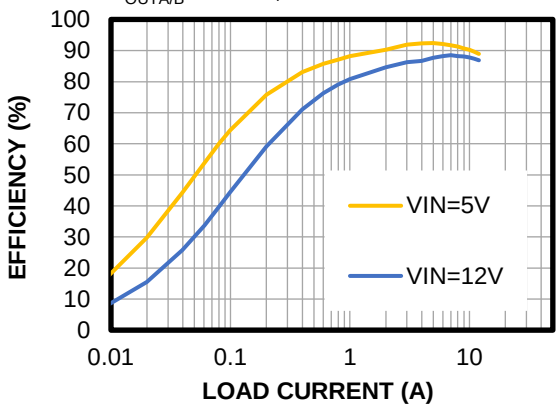
7) Guaranteed by design.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

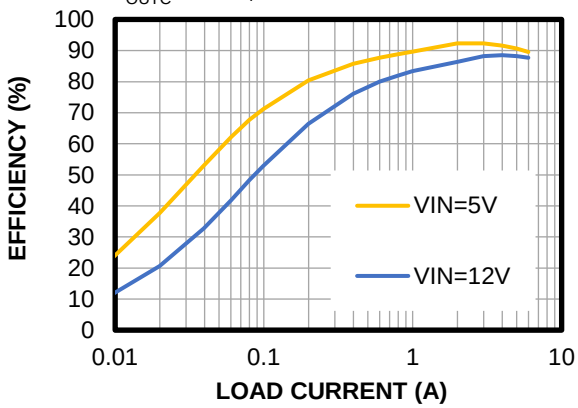
Efficiency vs. Load Current

$V_{OUTA/B}$ = 0.86V, PFM mode



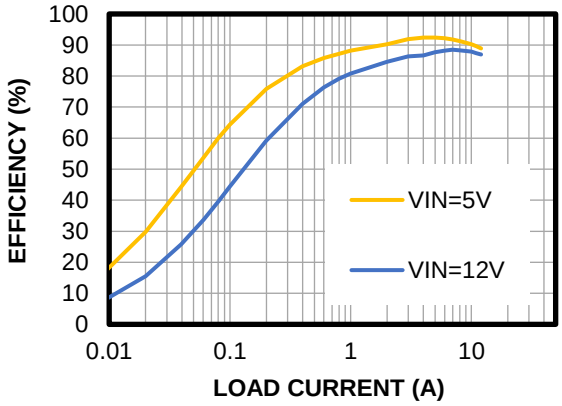
Efficiency vs. Load Current

V_{OUTC} = 0.9V, PFM mode



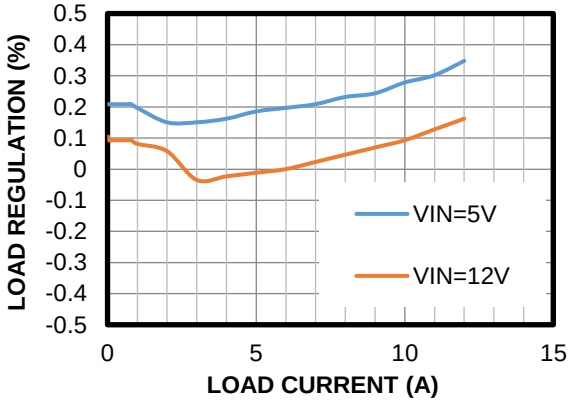
Efficiency vs. Load Current

V_{OUTD} = 0.9V, PFM mode



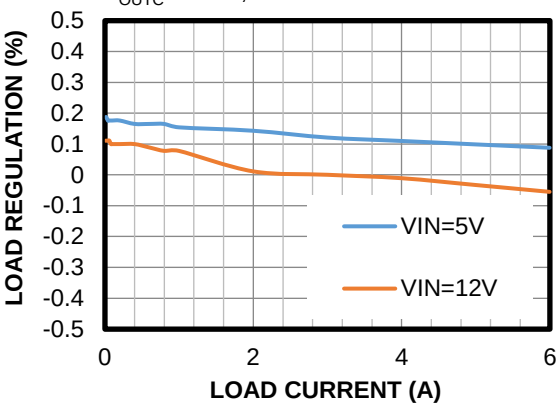
Load Regulation

$V_{OUTA/B}$ = 0.86V, PFM mode



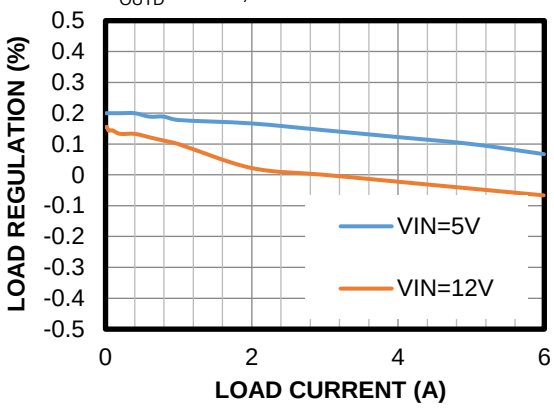
Load Regulation

V_{OUTC} = 0.9V, PFM mode



Load Regulation

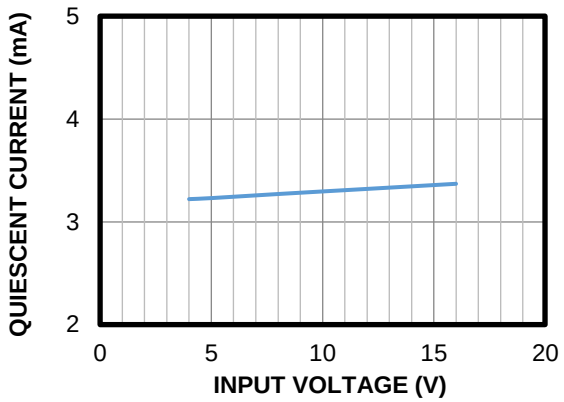
V_{OUTD} = 0.9V, PFM mode



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Quiescent Current vs. Input Voltage

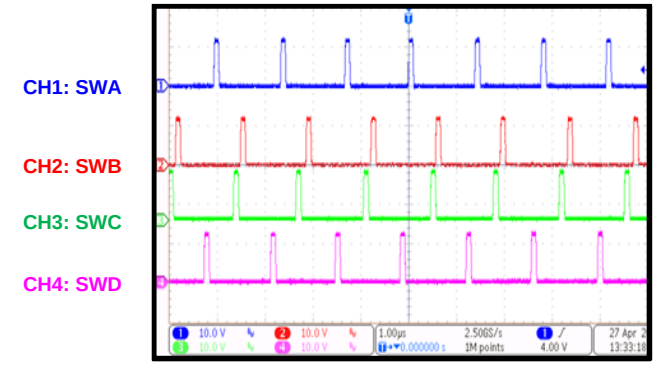


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

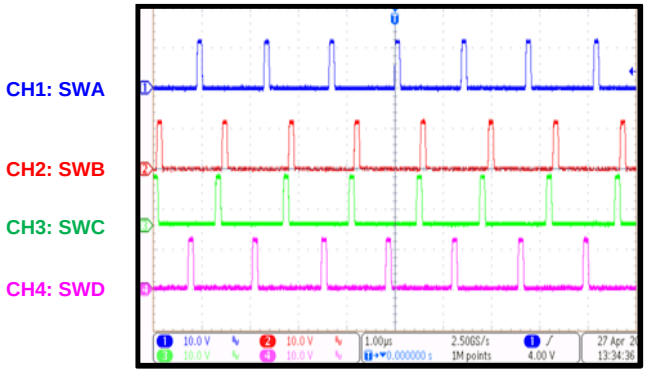
Steady State

Each buck channel with half load



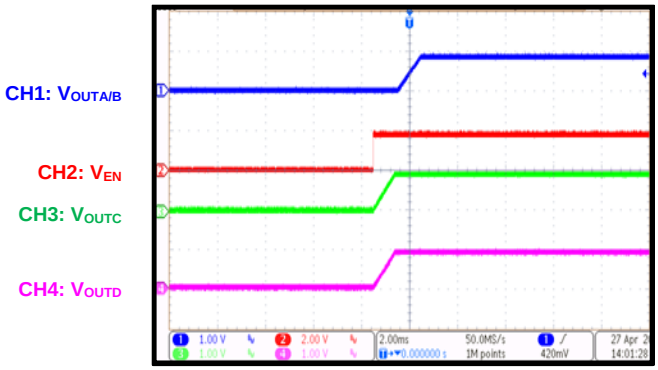
Steady State

Each buck channel with full load



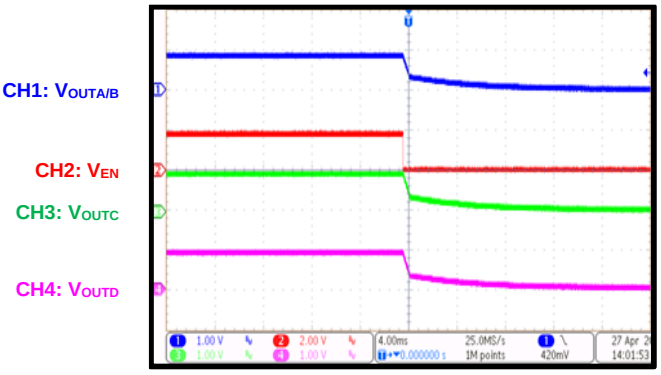
Start-Up through EN

Each buck channel without load



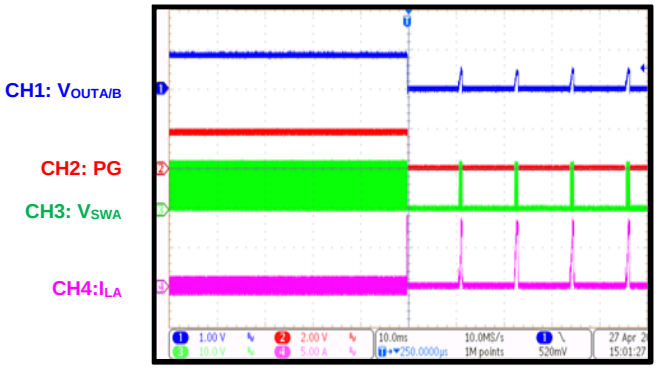
Shutdown through EN

Each buck channel without load



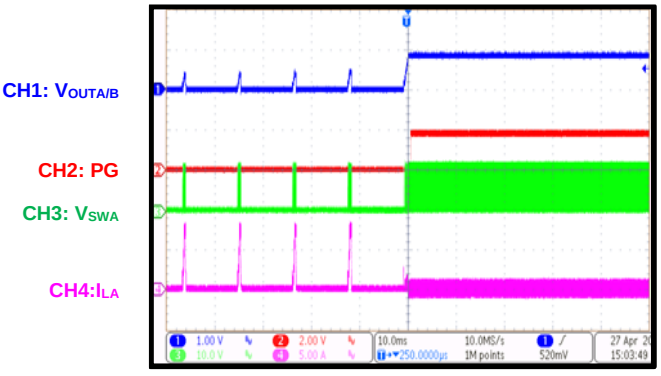
SCP Entry

Buck A/B output = 0.86V, I_{OUT} = 0A



SCP Recovery

Buck A/B output = 0.86V, I_{OUT} = 0A

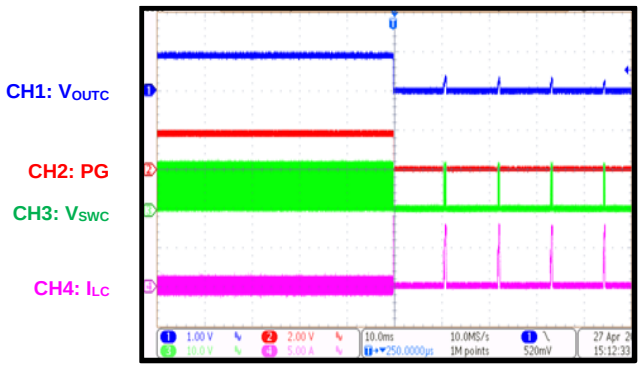


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

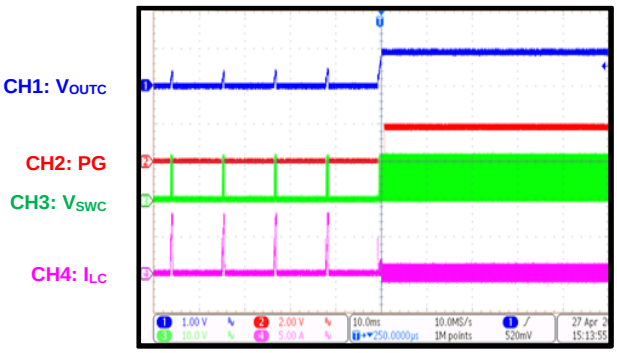
SCP Entry

Buck C output = 0.9V, I_{OUT} = 0A



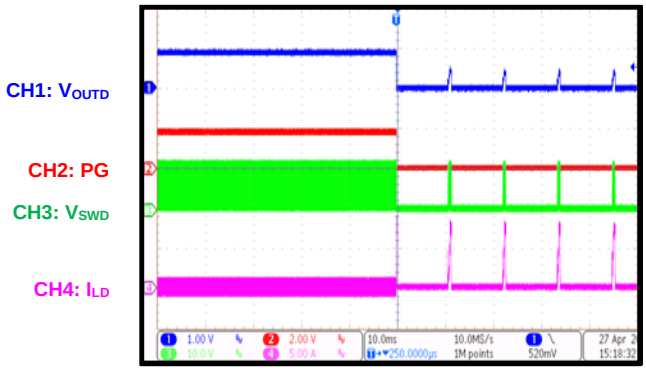
SCP Recovery

Buck C output = 0.9V, I_{OUT} = 0A



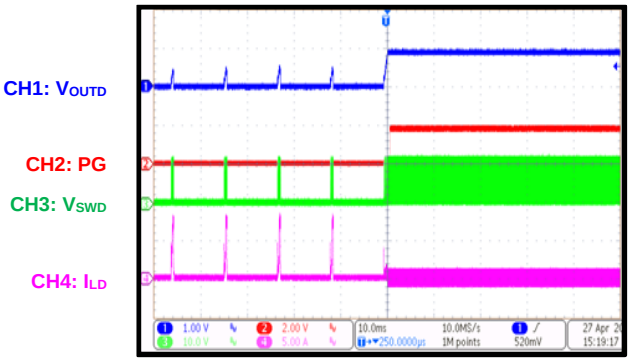
SCP Entry

Buck D output = 0.9V, I_{OUT} = 0A



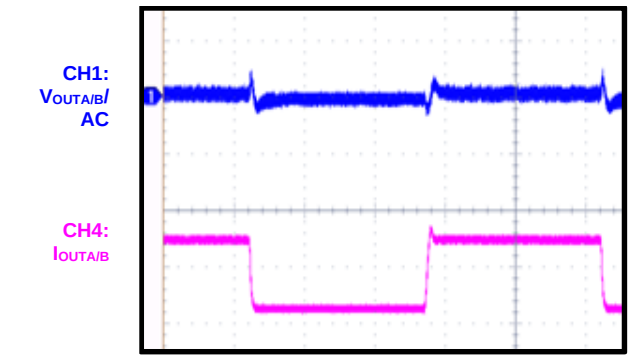
SCP Recovery

Buck D output = 0.9V, I_{OUT} = 0A



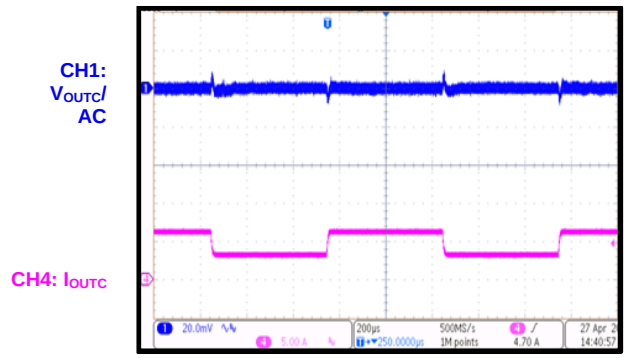
Load Transient Reponse

I_{OUT} = 6A to 12A, slew rate is 2.5A/µs by e-load



Load Transient Response

I_{OUT} = 3A to 6A, slew rate is 2.5A/µs by e-load

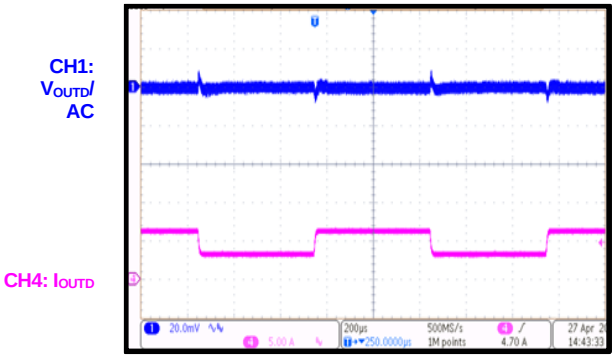


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Load Transient Response

I_{OUT} = 3A to 6A, slew rate is 2.5A/µs by e-load



FUNCTIONAL BLOCK DIAGRAM

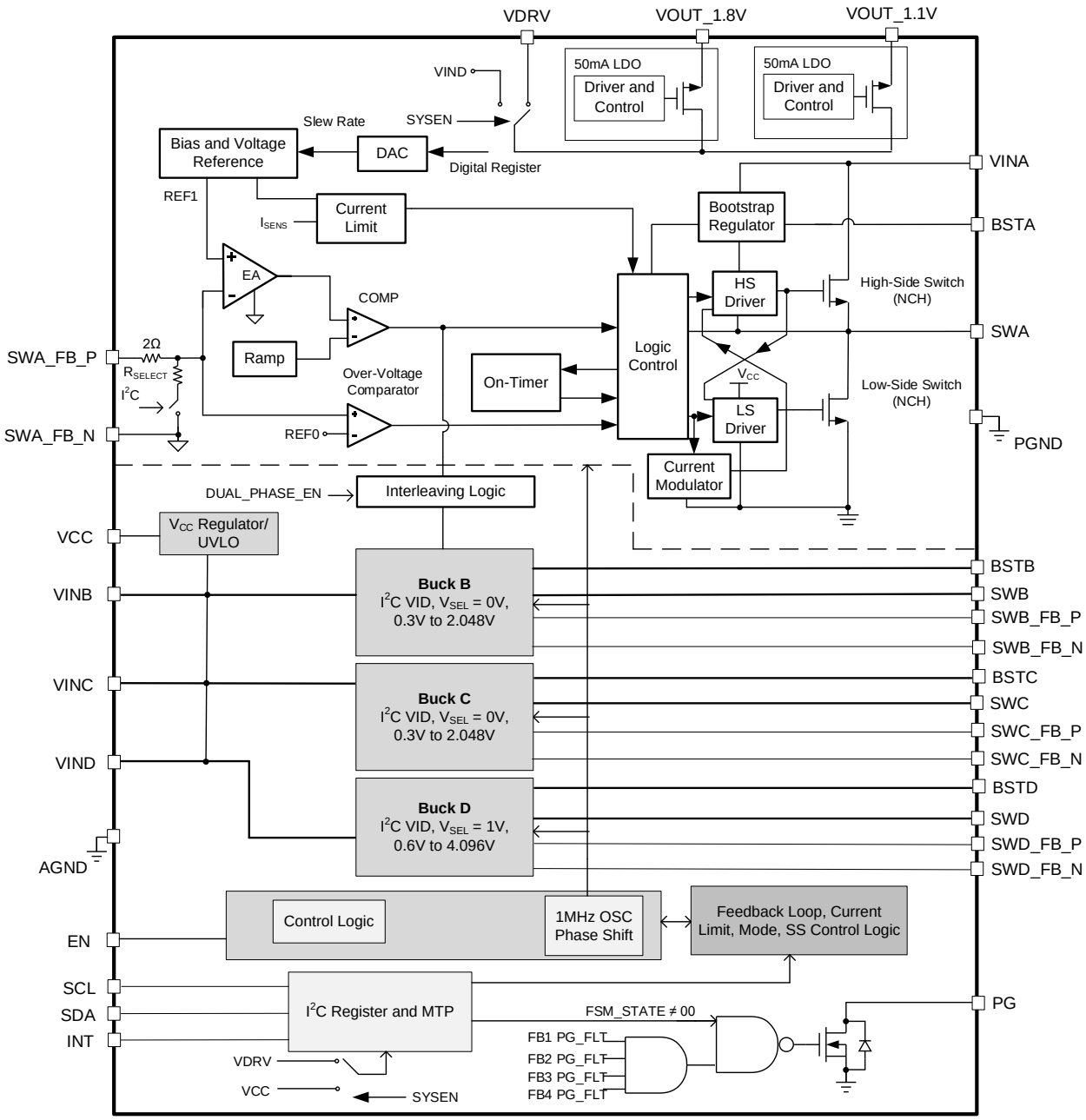


Figure 4: Functional Block Diagram

OPERATION

High-Efficiency Buck Converters

Buck converter A (buck A), buck converter B (buck B), buck converter C (buck C), and buck converter D (buck D) are synchronous, step-down DC/DC converters with built-in soft-start (SS), compensation, and current-limit protection with hiccup mode. Fixed-frequency constant-on-time (COT) control provides fast transient response. The switching clock is locked and phase-shifted from buck A to buck D in continuous conduction mode (CCM).

POWER CONTROL

State Machine Diagram

The state machine has a number of statuses, described below (see Figure 5).

No Supply

The MP5475's input pin has an under-voltage lockout (UVLO) detection circuit. If the input voltage (V_{INx}) (where x = A, B, C, or D) and the VDRV voltage (V_{DRV}), are below their respective UVLO rising thresholds, all the MP5475's functions are disabled.

Management State

After V_{DRV} exceeds its UVLO threshold, and before SYSEN is set, the MP5475 enters the management state. In the management state, the V_{INx} range is defined by V_{DRV}. The two low-dropout (LDO) regulator outputs, VOUT_1.8V and VOUT_1.1V, are enabled automatically when V_{DRV} reaches its UVLO rising threshold.

Power Off

If an over-temperature (OT) condition is triggered when V_{IN} exceeds its rising UVLO threshold, the MP5475 enters the power-off state. The MP5475 always monitors the power-on factor. If the power-on factor is detected after the MP5475's temperature drops below the falling threshold while in the power-off state, then the MP5475 enters the power-on sequence state.

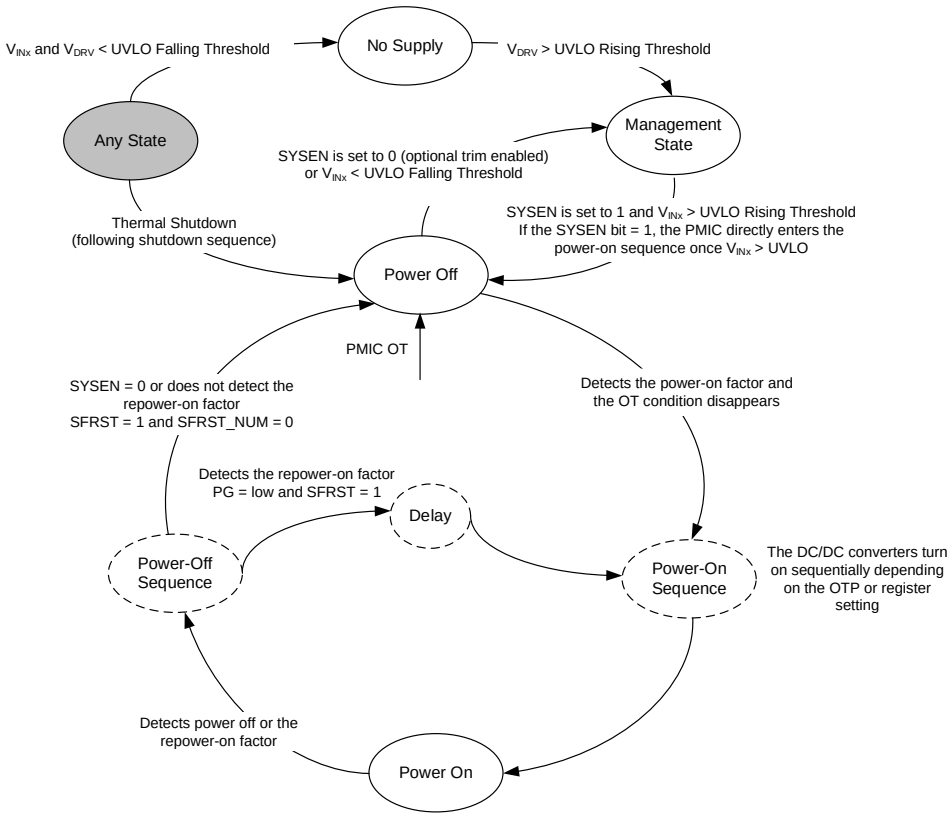


Figure 5: Power Control State Machine Diagram

Power Supply and Under-Voltage Lockout (UVLO)

V_{INA} is the power supply for buck A; V_{INB} is the power supply for buck B; V_{INC} is the power supply for buck C; V_{IND} is the power supply for buck D. It is recommended to connect the VINA, VINB, VINC, and VIND pins together during application. When V_{INx} exceeds its UVLO rising threshold, the corresponding buck starts up. The buck shuts down when V_{INx} drops below the UVLO falling threshold. See Figure 5 on page 19 for more details regarding the power-on sequence state.

Power-On Sequence

The DC/DC converters turn on sequentially according to the pre-configured order set via the multiple-time programmable (MTP) memory.

Power On

The DC/DC converter turns on. In this state, the MP5475 is always monitoring the power-off factor or repower-on factor.

Power-Off Sequence

The MP5475 initiates the power-off sequence when it detects the power-off factor or repower-on factor in the power-on state. Set the SFRST bit to 1 when the PG pin goes low, then the DC/DC converters shut down sequentially following the power-off sequence. After the power-off sequence is completed, the PMIC automatically enters the power-on sequence after a timer delay.

Set the SFRST bit to 1 when PG is high, then wait until PG goes low for the DC/DC converters to shut down sequentially following the power-off sequence.

Shutdown Event

If the PMIC detects that both V_{INx} and V_{DRV} have fallen below their respective UVLO thresholds, the MP5475 changes to a no supply state, regardless of the current state.

Power-On Factors

After V_{INx} and V_{DRV} exceed their respective ULVO thresholds, apply a logic low-to-high transition to the EN pin. The MP5475 has a few power-on factors, described below.

SYSEN

SYSEN is 1 data bit in the I²C register. If it is set to 1, the system changes from the power-off state to the power-on sequence. There are two ways to set SYSEN from 0 to 1:

- If the SYSEN bit is set to 1 via the MTP, the system automatically loads the SYSEN bit into the SYSEN I²C register when V_{INx} crosses its UVLO threshold.
- After the MP5475 enters the management state, write the SYSEN bit to 1 via the I²C to enable the buck converter.

Thermal Protection Recovery

If the MP5475 is in a power-off state due to the die temperature exceeding the thermal protection threshold, then the MP5475 enters the power-on sequence automatically once the die temperature decreases.

Power-On Sequence

There are 8 slots for power-on sequence timing. All the converters can be configured to time slots 0 to 7 via the MTP. The delay time between each time slot is configured by the 3-bit register TS_INTERVAL (see Table 1).

Table 1: Slot Time Interval

TS_INTERVAL	Time Delay between Each Slot
000	10ms
001	5ms
010	2ms
011	1ms
100	500µs
101	200µs

Figure 6 on page 21 and Figure 7 on page 22 show the MP5475's power-on sequence when power is first applied. The platform may power up V_{INx} and V_{DRV} supplies in any sequence.

Figure 6 on page 21 shows V_{INx} supply ramping before the V_{DRV} supply.

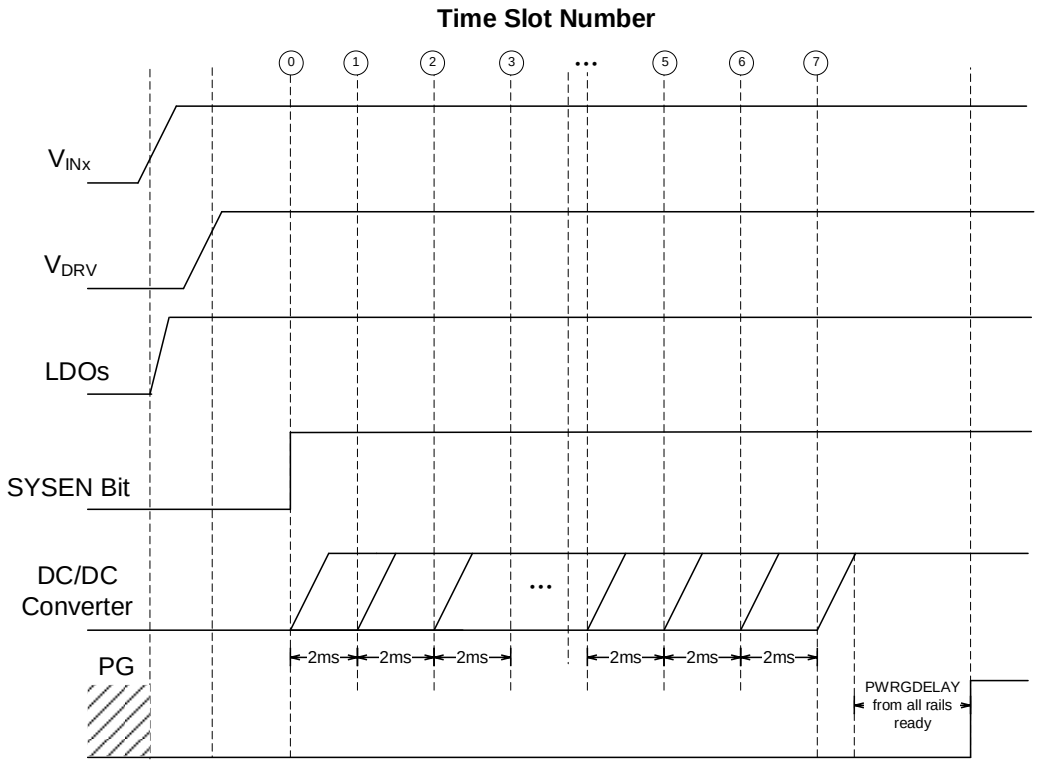


Figure 6: Power-On Sequence (V_{INx} Ready before V_{DRV})

Figure 7 on page 22 shows the V_{DRV} supply ramping up before the V_{INx} supply. The PMIC does not mandate any specific timing relationship between the V_{INx} and V_{DRV} supplies.

Once either the V_{INx} or V_{DRV} supply is valid and stable, the MP5475 drives the LDO output supplies, VOUT_1.8V and VOUT_1.1V, to the load devices for LDO (SPD, TS, and RCD).

The PMIC has an automatic internal supply switch-over function from the V_{DRV} input supply to the V_{INx} input supply. The input supply switch-over function is only applicable after the MP5475 has registered the SYSEN command. The MP5475 triggers the switch-over to the V_{INx} input supply when the V_{DRV} input drops below the 3V threshold. The internal input supply switch-over is for the MP5475's LDO outputs (VOUT_1.8V and VOUT_1.1V) and its I²C. The PMIC's I²C stays active when the MP5475 switches over to the V_{INx} input supply.

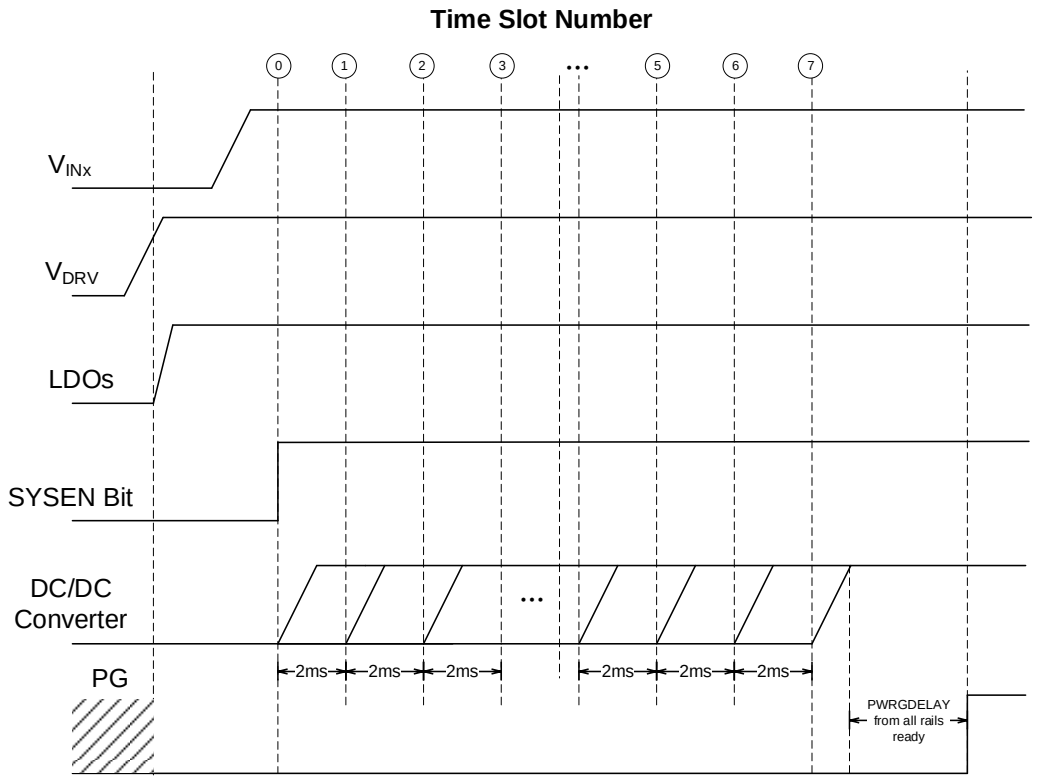


Figure 7: Power-On Sequence (V_{DRV} Ready before V_{INx})

Power-Off Factors

SYSEN – Software-Initiated Power Off (Trim Enable Function)

The MP5475 supports a software-controlled power off via the I²C interface. The SYSEN is 1 data bit in the I²C register. If the SYSEN bit is set to 0, the system enters a power-off sequence (trim enabled).

Thermal Protection Entry

If the MP5475's silicon die temperature exceeds the thermal protection threshold, the system enters a power-off state. In this scenario, the MP5475 enters the shutdown sequence instead of the power-off sequence and finally remains in the power-off state. For more details, see the Shutdown Sequence section on page 25.

V_{INx} Under-Voltage Lockout (UVLO)

If the MP5475's V_{INx} falls below its UVLO falling threshold while V_{DRV} is still active, the system enters a power-off state. In this scenario, the MP5475 enters the shutdown sequence instead of the power-off sequence and finally remains in the power-off state. For more details, see the Shutdown Sequence section on page 25.

Power-Off Sequence (Enabled by the Trim SYSEN Off Function)

The PG pin pulls low before the DC/DC converter initiates shutdown. The converter's power-off sequence is determined by the shutdown delay registers (11h, 19h, 21h, and 29h).

Figure 8 on page 23 shows the power-off sequence via the SYSEN bit when V_{DRV} turns off before V_{INx}. Figure 9 on page 23 shows the power-off sequence via the SYSEN bit when V_{INx} turns off before V_{DRV}.

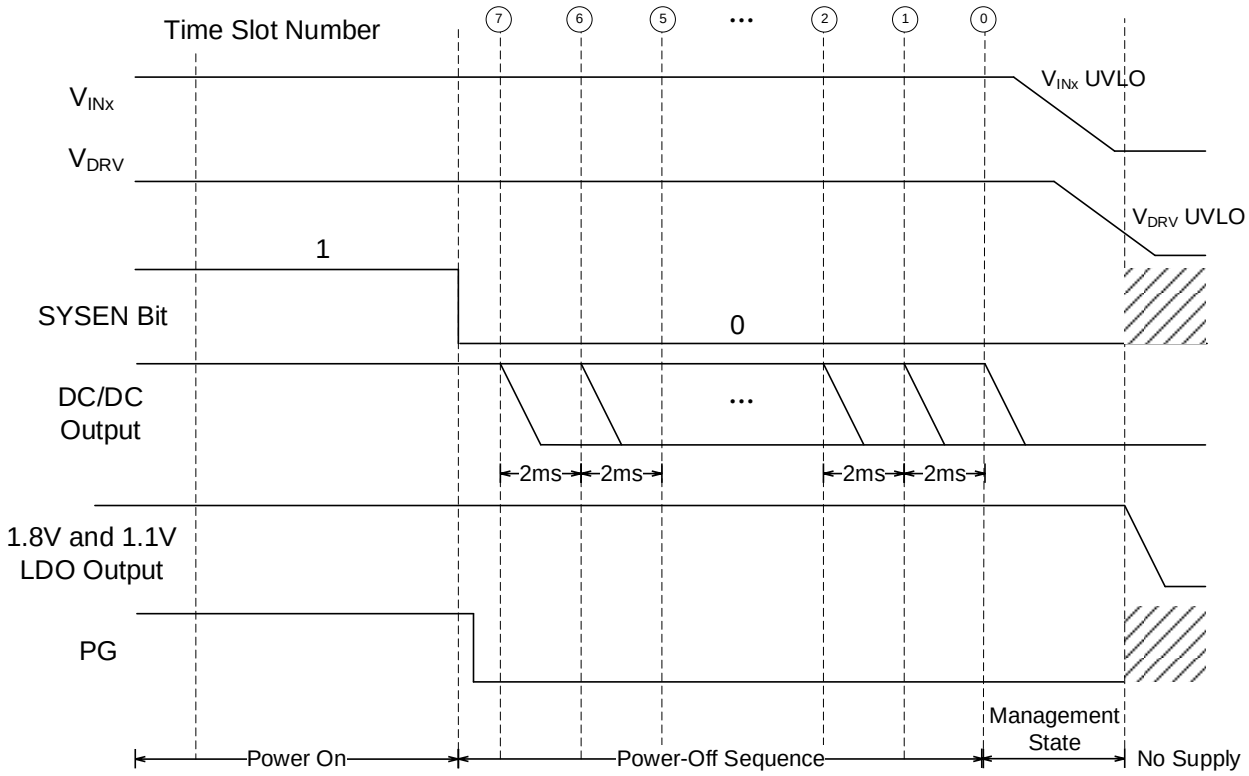


Figure 8: Power-Off Sequence via the SYSEN Bit (V_{INx} Off before V_{DRV})

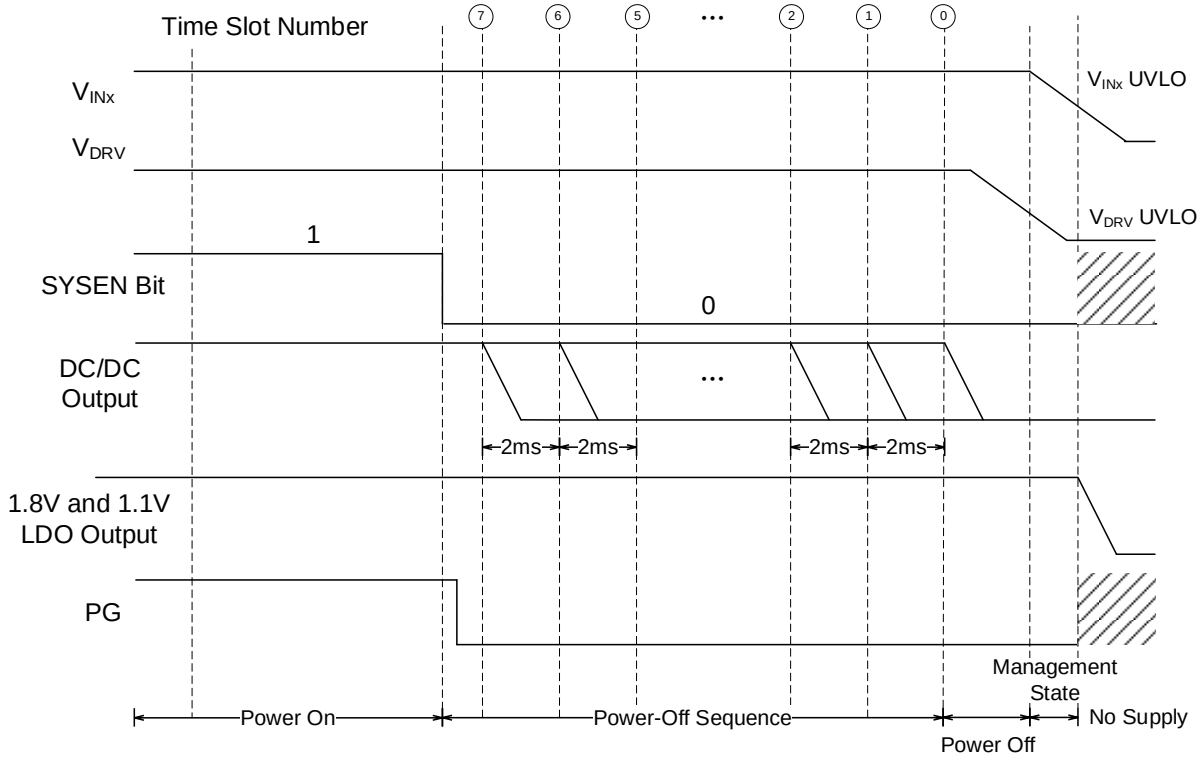


Figure 9: Power-Off Sequence via the SYSEN Bit (V_{DRV} Off before V_{INx})

Repower-On Factor

Manual Reset (SFRST)

It is possible to manually reset the device with a software reset. If the SFRST bit is set to 1 via the I²C and the PG pin is low, the system detects this as a repower-on factor.

Repower-On Sequence (Software-Initiated Power Cycle)

The MP5475 supports a software-controlled power reset via the I²C interface.

When using the software-controlled method, the SFRST bit is set high when the PG pin is low, The MP5475 waits for 200µs, then powers off the system. If the SFRST_NUM bit is not set to 0 after the delay time (set via the OFF_TIME register), then all the power rails power on again (see Figure 10).

When setting the SFRST bit high while PG is high, the MP5475 does not enter the repower-on sequence until PG goes low (see Figure 11).

After the repower-on sequence finishes, the SFRST_NUM value is set by register 43h, bits[2:0] - 1. If SFRST_NUM drops to 0 during the repower-on sequence, the MP5475 remains in the power-off state the next time a repower-on event occurs. There are two ways to restart the MP5475:

- Toggle V_{INx} to below its UVLO threshold and ramp up.
- Configure SFRST_NUM to a non-zero value.

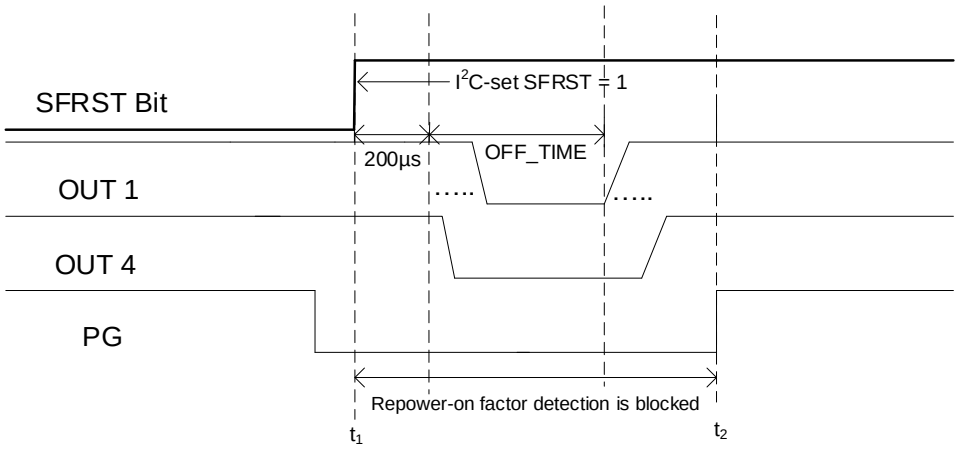


Figure 10: Repower-On Sequence (Set the SFRST Bit while PG Is Low)

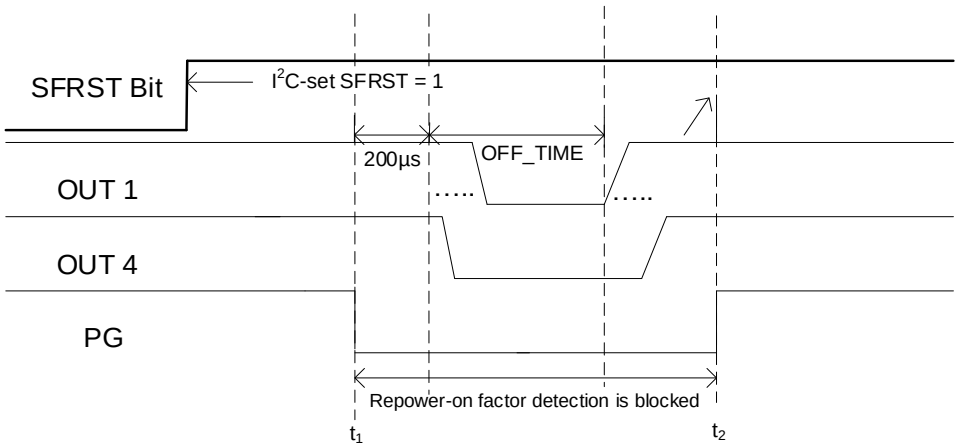


Figure 11: Repower-On Sequence (Set the SFRST Bit while PG Is High)

Shutdown Sequence

When V_{INx} drops below its UVLO falling threshold or the MP5475 has an OT condition, the MP5475 enters the shutdown sequence directly, All the DC/DC converters turn off at the same time following the soft-stop ramping down slew rate (see Figure 12).

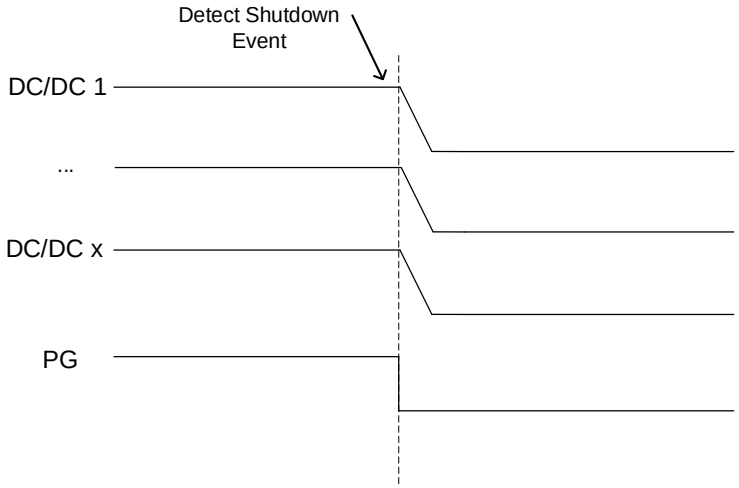


Figure 12: Shutdown Sequence

Thermal Shutdown

The MP5475 employs thermal shutdown by internally monitoring the IC's junction temperature (T_J). If T_J exceeds the 150°C threshold, the converter shuts off following the soft-stop ramping down slew rate. This is a non-latch protection. There is a 20°C hysteresis. Once T_J drops to about 130°C, the MP5475 initiates a soft start.

Pre-Biased Start-Up

The MP5475 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a set voltage during start-up, the internal bootstrap (BST) voltage (V_{BST}) is refreshed and charged, as well as the voltage on the internal soft-start capacitor (C_{SS}). If V_{BST} exceeds its rising threshold and the C_{SS} voltage exceeds the sensed output voltage (V_{OUTx}) (where x = A, B, C, or D) at the FB pin, then the MP5475 starts to work normally.

Power Good (PG)

The MP5475 provides a power good (PG) output to indicate whether the enabled buck's V_{OUTx} is ready. The PG pin is an open-drain output. Connect the PG pin to VCC or another voltage source through a pull-up resistor (e.g. 10kΩ).

If the FB voltage (V_{FB}) exceeds 92% of the reference voltage (V_{REF}), the PG pin pulls high after a 500μs default time (or another MTP-configured delay time). During normal operation, the PG pin pulls low when any enabled regulator falls below the UV threshold with a 50μs delay. The PG pin pulls low when all converters are disabled.

If UVLO occurs, SYSEN = 0, or over-temperature protection (OTP) occurs, then the PG pin pulls low immediately. If an over-current (OC) condition occurs, the PG pin pulls low when V_{FB} drops below 87% of V_{REF} after a 50μs delay.

General Status Interrupt (INT)

The MP5475 provides an interrupt control unit that is responsible for asserting and de-asserting the INT pin to the application host.

If the related interrupt is unmasked, it propagates to the INT pin. If the related interrupt is masked, the assertion of an interrupt from the masked register does not cause the IRQ signal to assert.

INT asserts low until all the interrupt events are removed. Figure 13 on page 26 shows the IRQ architecture block diagram.

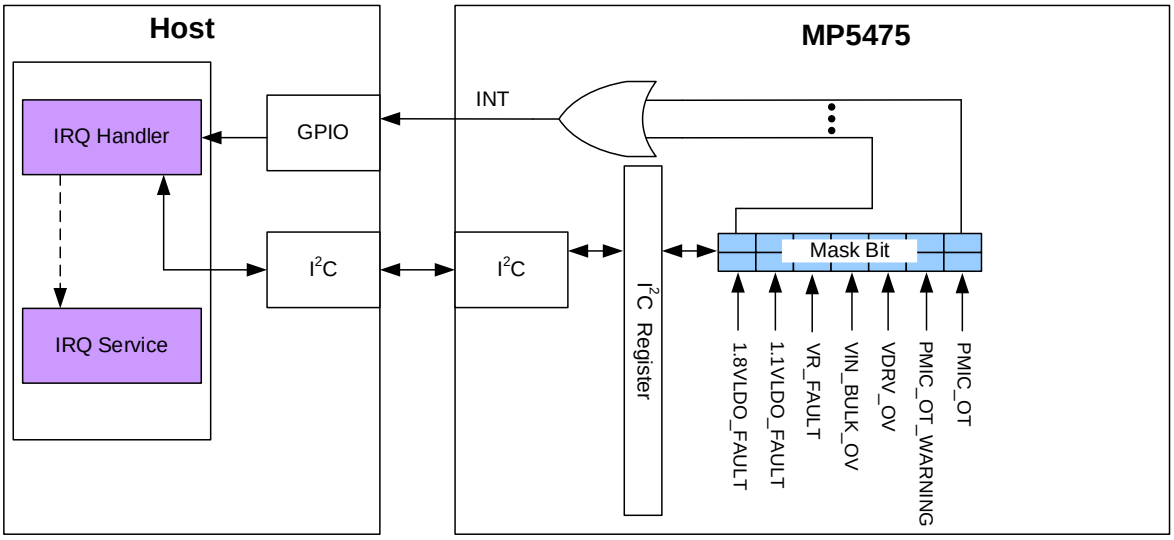


Figure 13: IRQ Architecture Block Diagram

Output Over-Voltage Protection (OVP)

The MP5475 monitors V_{OUTx} and enters over-voltage protection (OVP) discharge mode once V_{OUTx} exceeds 122% of its regulation voltage for longer than 2µs. In OVP discharge mode, the low-side MOSFET (LS-FET) turns on and stays on until the LS-FET's current reaches the negative current limit. This discharges the output to keep V_{OUTx} within its normal range. If the OV condition still exists, the LS-FET turns on again after a fixed delay to repeat the discharge behavior.

The MP5475 exits this discharge mode when V_{FB} drops below 110% of V_{REF}.

If the MP5475's V_{INx} exceeds the input OVP threshold by 14.5V during OVP discharge mode, then the MP5475 shuts down until V_{INx} drops below 14.2V, after which the MP5475 restarts. Input OVP is only active when under an output OV condition.

OVP can be enabled or disabled via the I²C and MTP interface.

Input Over-Voltage Protection (OVP)

The MP5475 monitors V_{INx} and enters OVP mode once V_{INx} exceeds 16.6V. In OVP mode, the MP5475 cannot enter forced continuous conduction mode (FCCM), which means that there is no soft shutdown when the device shuts down.

The MP5475 exits this mode when V_{INx} drops below 16V.

Output Discharge

To discharge the energy of the output capacitor (C_{OUT}) during the power-off sequence or shutdown sequence, there are discharge paths both from the SWx and FBx pins to ground. The discharge function can be enabled or disabled via the I²C and MTP interface.

Soft Start (SS) and Soft Shutdown

The MP5475 employs a soft-start and soft shutdown mechanism to ensure a smooth output during start-up and shutdown.

When the MP5475 is enabled and V_{BST} reaches its rising threshold, the internal digital-to-analog converter (DAC) outputs a ramp voltage (V_{REF}). V_{OUTx} smoothly ramps up with V_{REF}. Once the DAC output reaches the final voltage, it maintains a steady voltage. At this point, soft start finishes, and the MP5475 enters steady state operation.

When the MP5475 is disabled, the internal DAC ramps down V_{REF}. V_{OUTx} follows the soft-shutdown slew rate with V_{REF} until the output drops to 0.3V. Then soft shutdown stops and the MP5475's output is discharged by the FB pin's discharge FET, if the discharge function is enabled.

The start-up delay, shutdown delay, soft-start and soft-shutdown slew rate can be configured via the MTP.

Out-of-Phase Operation

Buck A, buck B, buck C, and buck D are frequency-locked and phase-shifted. Figure 14 shows the phase shift's default definition, which can also be changed via the MTP.

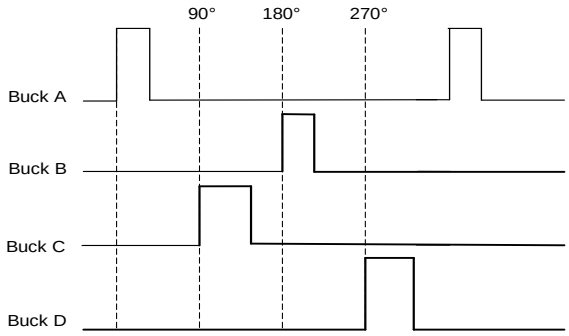


Figure 13: Phase-Shift Functional Diagram

Interleaving for Dual-Rail Mode

When interleaving mode is enabled, the MP5475's buck A/B and buck C/D operate with dual-phase interleaving (see Figure 14).

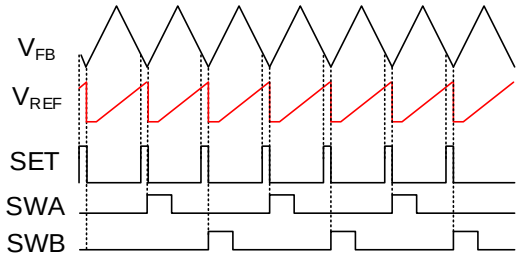


Figure 14: Interleaving for Dual-Rail Mode Diagram

The SET signal is triggered by comparing V_{FB} and V_{REF}. When the SET signal goes high, only one phase's pulse-width modulation (PWM) output becomes high; the next time SET goes high, the next phase's PWM output goes high. This achieves interleaving.

Current Balancing

When buck A and buck B work in dual-phase interleaving mode, the MP5475 senses two phase currents and auto-tunes buck A and buck B's on time (t_{ON}) to achieve current balancing.

Active Voltage Positioning (AVP)

When buck A and buck B (or buck C and buck D) work in dual-phase interleaving mode, the MP5475 supports active voltage positioning (AVP) by setting the AVP_EN bit to 1 via the I²C. An internal current-sense circuit generates the droop current (I_{DROOP}) source, which is proportional to the internal sensing current. I_{DROOP} is injected into the FB pin to produce the feedback (FB) voltage (V_{FBx}) with a droop voltage.

VCC Regulator

A 3.5V internal regulator powers most of the internal circuitry. A decoupling capacitor is required to stabilize the regulator and reduce the ripple. This regulator takes the VINA input and operates across the full V_{INA} range.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP5475 provides valley current limit control. While the LS-FET turns on, the inductor current (I_L) is monitored. If the sensed I_L exceeds the valley current limit threshold, the device enters over-current protection (OCP) mode. The high-side MOSFET (HS-FET) cannot turn on until the valley current limit disappears. Meanwhile, V_{OUTx} drops until it falls below the under-voltage (UV) threshold.

If an UV and OC condition are both triggered, the MP5475 enters hiccup mode to periodically restart the related power rail. The hiccup duty cycle is very small to reduce the power dissipation during a short-circuit condition. During OCP, the device tries to recover from the OC fault with hiccup mode. That means that the chip disables the output power stage, discharges C_{SS}, and then automatically tries to soft start again. If the OC condition still exists when soft start elapses, the device repeats this operation. OCP is a non-latch protection.

Multiple-Time Programmable (MTP) Configuration

The I²C and MTP blocks are active once V_{DRV} exceeds its UVLO rising threshold.

When V_{DRV} starts up the MP5475, the MTP data is loaded into the corresponding I²C registers during the first start-up, and the I²C registers directly control buck A to buck D's parameters. The I²C register and MTP table share the same register address.

After the MP5475's V_{DRV} and V_{INx} start up, the system-on-chip (SoC) configures the MP5475's I²C register and MTP.

When the SoC writes to the I²C register, the I²C register takes effect immediately; this setting can also be burned into the MTP. During normal buck

operation, the I²C master can read and write to the register's data online.

Safety Considerations for Writing to the MTP

Several protection items can reduce the failure rate of MTP writing. Figure 15 shows how to configure the MTP, and follow the three steps below to write to the MTP registers:

1. Set MTP_PROGRAM to 1. The I²C register is locked to prevent write operations until MTP configuring finishes, but the SoC can read the I²C register during this period.
2. The MP5475 checks the MTP's burning power supply. If this supply exceeds 5.1V, MTP writing continues; otherwise, abort and unlock the I²C write protection.
3. The MP5475 calculates the sum of all related I²C registers that are burnt into the MTP register, then generates 8-bit checksum data. The sum is not a true sum of all I²C registers. Rather, it is an arithmetic to combine all the data. The checksum result is written to the MTP register as well.

After MTP write operation finishes (typically after about 100ms), the MP5475 sets MTP_PROGRAM to 0. I²C register write protection is unlocked. The MTP device configuration specification is up to 0.5mA/bit for 50ms. This means that two configuration cycles with less current requires about 100ms.

The SoC can read the register; if the MTP_PROGRAM goes to 0, this indicates that the MTP configuration is done.

After MTP write operation finishes, the system SoC can read the MTP register data to confirm that the correct value is saved to the MTP registers. If anything is wrong, the SoC writes to the MTP again.

During V_{IN} start-up, before loading the MTP data into the I²C register, the MP5475 executes a checksum calculation for all related MTP registers, then compare this value with the checksum byte. If they match, then MTP data is loaded to the I²C register; Otherwise, the I²C register uses a hard-coded default value. An I²C/register flag bit is available to indicate whether this is a checksum error.

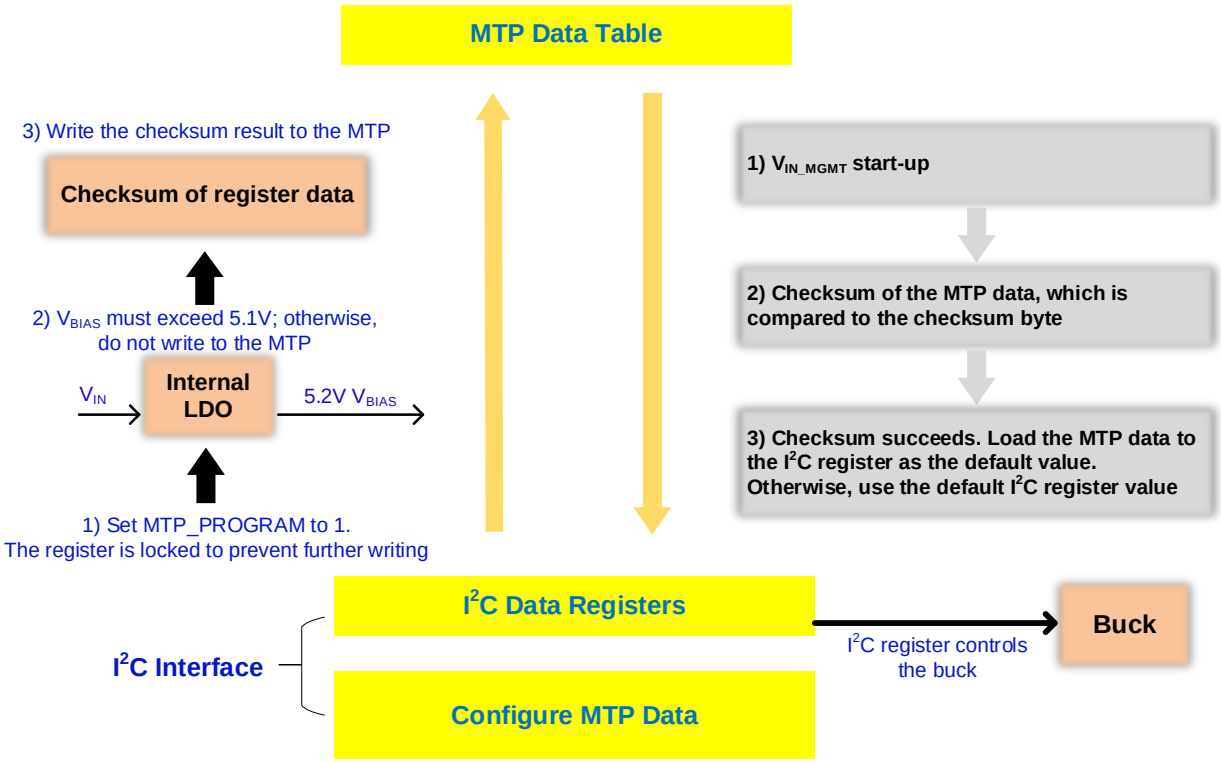


Figure 15: MTP Configuration

I²C INTERFACE

I²C Serial Interface

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The MP5475 interface is an I²C slave. The I²C adds flexibility to the power supply solution. V_{OUTx}, the transition slew rate, and other parameters can be controlled by the I²C instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the clock's high period. The high or low state of the data line can only change after the clock signal on the SCL line stays low for no shorter than maximum data hold time (t_{HD_DAT}), and also no longer than the maximum data set-up time (t_{SU_DAT}) before the next SCL clock starts (see Figure 16).

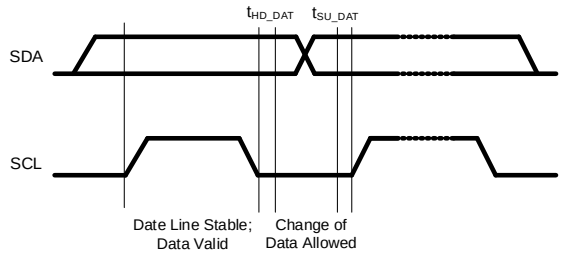


Figure 16: Bit Transfer on the I²C Bus

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start command is defined as the SDA signal transitioning from high to low while SCL is high. A stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 17).

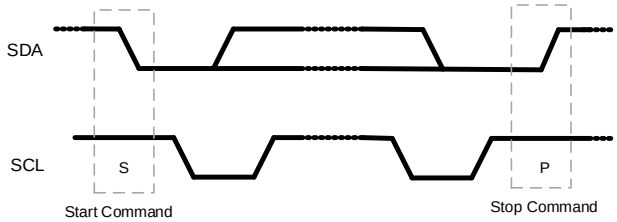


Figure 17: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is busy after the start condition, and it is considered to be free again after the stop command. The bus remains busy if a repeated start (Sr) is generated instead of a stop command. The start and repeated start commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte has to be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the clock pulse's high period.

Figure 18 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. If the master still wants to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

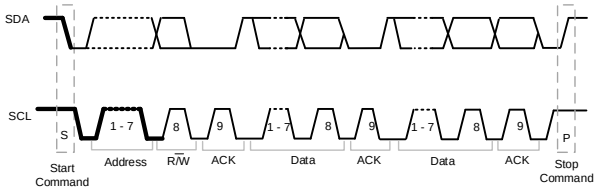


Figure 18: A Complete Data Transfer

Figure 19 on page 30 shows an I²C write example for a single register. Figure 20 on page 30 shows an I²C read example for a single register.

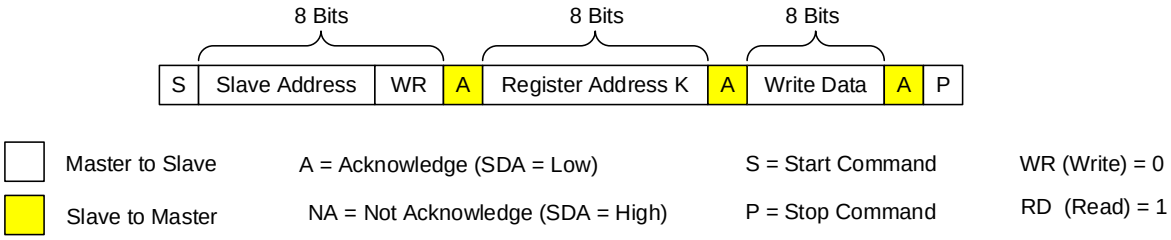


Figure 19: I²C Write Singe Register Example

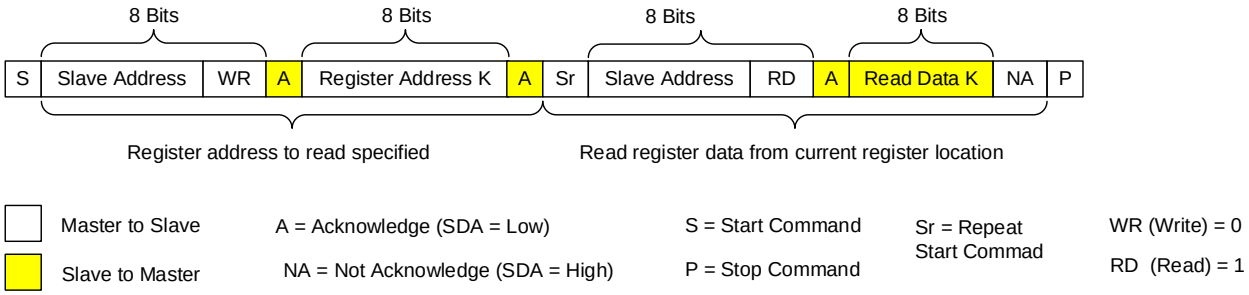


Figure 20: I²C Read Singe Register Example

REGISTER MAP

MTP CONFIGURATION TABLE

Scope	REG (0x)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Buck A	10 (WR)	DUAL_ PHASE_ ENA	SOFT_START_DELAYA			SOFT_START_TIMEA			
	11 (WR)	SHUTDOWN_DELAYA			SOFT_STOP_TIMEA		VOUT_TRANSITION_RATEA		
	12 (WR)	VOUT_ LIMIT_ENA	MODEA	CURRENT_LIMITA		VOUT_ OVP_ENA	PHASE_DELAY_ SELECTA		VOUT_ DIS_ENA
	13 (WR)	VOUT_ SELECTA	RESERVED					V_REFA_HIGH	
	14 (WR)	V_REFA_LOW							
	15 (WR)	RESERVED							
	16 (WR)	RESERVED							
	17 (WR)	AVP_ENA	AVP_GAINA		AVP_TRIMA				
Buck B	18 (WR)	RESERVED	SOFT_START_DELAYB			SOFT_START_TIMEB			
	19 (WR)	SHUTDOWN_DELAYB			SOFT_STOP_TIMEB		VOUT_TRANSITION_RATEB		
	1A (WR)	VOUT_ LIMIT_ENB	MODEB	CURRENT_LIMITB		VOUT_ OVP_ENB	PHASE_DELAY_ SELECTB		VOUT_ DIS_ENB
	1B (WR)	VOUT_ SELECTB	RESERVED					V_REFB_HIGH	
	1C (WR)	V_REFB_LOW							
	1D (WR)	RESERVED							
	1E (WR)	RESERVED							
Buck C	20 (WR)	DUAL_ PHASE_ ENC	SOFT_START_DELAYC			SOFT_START_TIMEC			
	21 (WR)	SHUTDOWN_DELAYC			SOFT_STOP_TIMEC		VOUT_TRANSITION_RATEC		
	22 (WR)	VOUT_ LIMIT_ENC	MODEC	CURRENT_LIMITC		VOUT_ OVP_ENC	PHASE_DELAY_ SELECTC		VOUT_ DIS_ENC
	23 (WR)	VOUT_ SELECTC	RESERVED					V_REFC_HIGH	
	24 (WR)	V_REFC_LOW							
	25 (WR)	RESERVED							
	26 (WR)	RESERVED							
	27 (WR)	AVP_ENC	AVP_GAINC		AVP_TRIMC				
Buck D	28 (WR)	RESERVED	SOFT_START_DELAYD			SOFT_START_TIMED			
	29 (WR)	SHUTDOWN_DELAYD			SOFT_STOP_TIME4		VOUT_TRANSITION_RATED		
	2A (WR)	VOUT_ LIMIT_END	MODED	CURRENT_LIMITD		VOUT_ OVP_END	PHASE_DELAY_ SELECTD		VOUT_ DIS_END
	2B (WR)	VOUT_ SELECTD	RESERVED					V_REFD_HIGH	
	2C (WR)	V_REFD_LOW							
	2D (WR)	RESERVED							
	2E (WR)	RESERVED							

REGISTER MAP *(continued)*

MTP CONFIGURATION TABLE

Scope	REG (0x)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
System	40 (WR)	SYSEN	RESERVED	ENA	ENB	ENC	END	RESERVED	SFRST
	41 (WR)	RESERVED	I2C_SLAVE_ADDRESS						
	42 (WR)	FREQ (500kHz/750kHz/1000kHz/1.25MHz/ 1.5MHz/2MHz)			TS_INTERVAL			PWRG_DELAY	
	43 (WR)	UVLO	MTP_ PROGRAM	SHUTDOWN_ DELAY_EN	OFF_TIME		SFRST_NUM		
	44 (WR)	RESERVED	RESERVED		WP_EN	RESERVED	RESERVED	PWR_GOOD_CFG	
	45 (WR)	RESERVED	1.8VLDO_ FAULT_MSK	1.1VLDO_ FAULT_MSK	VR_FAULT_ MSK	VBULK_OV_ MSK	VDRV_ OV_MSK	PMIC_ HIGH_ TEMP_ WARNING_ MSK	PMIC_ HIGH_ TEMP_ SHUTDOWN_ MSK
	50 (WR)	MTP_CONFIGURE_CODE							
	51 (WR)	MTP_REVISION_NUMBER							

MTP TABLE DESCRIPTION

DUAL_PHASE_EN1 and DUAL_PHASE_EN3 (from Registers 10h and 20h)

The DUAL_PHASE_ENx bits set whether buck A and buck B (or buck C and buck D) operate in dual-phase interleaving mode or in independent, single-phase mode.

Bits	Access	Bit Name	Default	Reset Condition	Description
7	WR	DUAL_PHASE_ENA DUAL_PHASE_ENC	DUAL_PHASE_ENA = 1 DUAL_PHASE_ENC = 0	V_{CC} < 2V, V_{DRV} < 2V	Sets whether buck A and buck B (or buck C and buck D) operate in dual-phase interleaving mode or in independent, single-phase mode. The dual-phase enable bit only takes effect in MTP. 0: Independent, single-phase operation 1: Dual-phase interleaving operation

SOFT_START_DELAYx and SOFT_START_TIMEx (from Registers 10h, 18h, 20h, and 28h)

The SOFT_START_DELAYx and SOFT_START_TIMEx (where x = A, B, C, and D) bits set the soft-start delay time and soft-start time for buck A, buck B, buck C, and buck D.

Bits	Access	Bit Name	Default	Reset Condition	Description
6:4	WR	SOFT_START_DELAYx	00	V_{CC} < 2V, V_{DRV} < 2V	Sets the time delay between when the input voltage (V_{INx}) exceeds UVLO threshold, the LDOs are ready, and SYSEN = high to when the related buck's output voltage starts to ramp up. There are 8 different values. For more details, see Figure 6 on page 21 and Figure 7 on page 22. 000: Time slot 0 001: Time slot 1 010: Time slot 2 011: Time slot 3 100: Time slot 4 101: Time slot 5 110: Time slot 6 111: Time slot 7
3:0	WR	SOFT_START_TIMEx	0111	V_{CC} < 2V, V_{DRV} < 2V	Sets the soft-start slew rate for each buck. The values below are the potential internal reference voltage (V_{REF}) slew rates. If the relevant VOUT_SELECT bit is set, the output voltage (V_{OUTx}) (where x = A, B, C, and D) slew rate is 2 times the value listed below. 0000: 8mV/µs 0001: 4mV/µs 0010: 2.7mV/µs 0011: 2mV/µs 0100: 1.6mV/µs 0101: 1.3mV/µs 0110: 1.14mV/µs 0111: 1mV/µs 1000: 0.89mV/µs 1001: 0.67mV/µs 1010: 0.5mV/µs 1011: 0.4mV/µs 1100: 0.33mV/µs 1101: 0.25mV/µs 1110: 0.2mV/µs 1111: 0.167mV/µs

SHUTDOWN_DELAYx, SOFT_STOP_TIMEx, and VOUT_TRANSITION_RATEx (from Registers 11h, 19h, 21h, and 29h)

The SHUTDOWN_DELAYx, SOFT_STOP_TIMEx, and VOUT_TRANSITION_RATEx (where x = A, B, C, or D) bits set the shutdown time, soft-stop time, and V_{OUTx} transition rate for buck A, buck B, buck C, and buck D.

Bits	Access	Bit Name	Default	Reset Condition	Description
7:5	WR	SHUTDOWN_ DELAYx	00	V_{CC} < 2V, V_{DRV} < 2V	Sets the delay time to SYSEN = 0 or SFRST = 0 and the buck V_{OUTx} starting to ramp down. The 3 bits can set 8 different values: 000: Time slot 0 001: Time slot 1 010: Time slot 2 011: Time slot 3 100: Time slot 4 101: Time slot 5 110: Time slot 6 111: Time slot 7
4:3	WR	SOFT_STOP_ TIMEx	10	V_{CC} < 2V, V_{DRV} < 2V	Sets the soft-shutdown slew rate for each buck. The slew rates below are the internal V_{REF} slew rates. If the relevant VOUT_SELECT bit is set, the soft-shutdown slew rate is 2 times the value listed below. 00: 4mV/µs 01: 2mV/µs 10: 1mV/µs 11: 0.5mV/µs
2:0	WR	VOUT_ TRANSITION_ RATEx	011	V_{CC} < 2V, V_{DRV} < 2V	Sets the V_{OUTx} transition slew rate for each buck. The value below is the internal V_{REF} slew rate. If the relevant VOUT_SELECT bit is set, the V_{OUT} slew rate is 2 times the value listed below. 000: 1.6mV/µs 001: 1.3mV/µs 010: 1.14mV/µs 011: 1mV/µs 100: 0.89mV/µs 101: 0.67mV/µs 110: 0.5mV/µs 111: 0.4mV/µs

VOUT_LIMIT_ENx, MODEX, CURRENT_LIMITX, VOUT_OVP_ENx, PHASE_DELAY_SELECTx, and VOUT_DIS_ENx (from Registers 12h, 1Ah, 22h, 2Ah)

The VOUT_LIMIT_ENx, MODEX, CURRENT_LIMITX, VOUT_OVP_ENx, PHASE_DELAY_SELECTx, and VOUT_DIS_ENx (where x = A, B, C, or D) bits set the pulse-width modulation (PWM) mode, maximum V_{OUTx}, current limit, phase delay, and enable other protection functions, such as over-voltage protection (OVP) and passive output discharge.

Bits	Access	Bit Name	Default	Reset Condition	Description
7	WR	VOUT_LIMIT_ENx	0	V_{CC} < 2V, V_{DRV} < 2V	Limits the maximum V_{OUTx} of each buck's rail. 0: The maximum V_{OUTx} has no limit; the value depends on the I²C V_{OUTx} setting maximum duty cycle or absolute voltage limit 1: The maximum V_{OUTx} is limited to V_{REF} x 1 if the relevant VOUT_SELECT bit = 1

6	WR	MODEx	0	V_{CC} < 2V, V_{DRV} < 2V	Select the mode between automatic pulse-frequency modulation (PFM)/PWM mode and forced PWM mode. 0: Automatic PFM/PWM mode 1: Forced PWM mode
5:4	WR	CURRENT_LIMITx	11	V_{CC} < 2V, V_{DRV} < 2V	Sets the current limit of each buck, with 15% accuracy. 00: 4A valley current limit for 3A output current (I_{OUT}) applications 01: 5A valley current limit for 4A I_{OUT} applications 10: 6A valley current limit for 5A I_{OUT} applications 11: 7A valley current limit for 6A I_{OUT} applications
3	WR	VOUT_OVP_ENx	1	V_{CC} < 2V, V_{DRV} < 2V	Enables each buck's output OVP. 0: Disabled 1: Enabled
2:1	WR	PHASE_DELAY_SELECTx	PHASE_DELAY_SELECTA = 00 (fixed) PHASE_DELAY_SELECTB = 10 PHASE_DELAY_SELECTC = 01 PHASE_DELAY_SELECTD = 11	V_{CC} < 2V, V_{DRV} < 2V	Sets the phase delay for each buck. Buck A is fixed to 00. 00: 0° delay 01: 90° delay 10: 180° delay 11: 270° delay
0	WR	VOUT_DIS_ENx	1	V_{CC} < 2V, V_{DRV} < 2V	Enables the passive discharge function. Soft shutdown finishes until the buck V_{OUTx} discharges to 0.3V. The passive discharge resistor is then connected to the buck V_{OUTx} to further discharge the buck V_{OUTx}. This bit also enables buck A to buck D's output passive discharge function. 0: Disabled 1: Enabled

VOUT_SELECTx and V_REFx_HIGH (from Registers 13h, 1Bh, 23h, and 2Bh)

The VOUT_SELECTx and V_REFx_HIGHx (where x = A, B, C, or D) bits set the buck's V_{OUTx}, the internal feedback divider ratio, and the high bit to set the internal V_{REF}.

Bits	Access	Bit Name	Default	Reset Condition	Description
7	WR	VOUT_SELECTx	VOUT_SELECTA = 0 VOUT_SELECTB = 0 VOUT_SELECTC = 0 VOUT_SELECTD = 1	V_{CC} < 2V, V_{DRV} < 2V	Sets the internal feedback divider ratio. 0: V_{FB} is directly fed to the error amplifier; V_{FB} is equal to V_{REF} 1: V_{FB} is divided by 2, then compared to V_{REF}; V_{FB} is equal to 2 times of V_{REF}, and is between 0.6V and 4.096V
6:2	RO	RESERVED	5'b000000	V_{CC} < 2V, V_{DRV} < 2V	Reserved.

1:0	WR	V_REFx_HIGH	VREFA = 10 VREFB = 10 VREFC = 10 VREFD = 01	V_{CC} < 2V, V_{DRV} < 2V	These high bits set the internal V_{REF}. The MP5475 does not execute V_{REF} until the V_REFx_LOW bits are configured. Configure V_REFx_HIGH first, then configure V_REFx_LOW.

V_REFx_LOW (from Registers 14h, 1Ch, 24h, and 2Ch)

The V_REFx_LOW bits set the internal V_{REF}.

Bits	Access	Bit Name	Default	Reset Condition	Description
7:0	WR	V_REFx_LOW	VREFA = 00100110 VREFB = 00100110 VREFC = 00100110 VREFD = 11000010	V_{CC} < 2V, V_{DRV} < 2V	These low bits set the internal V_{REF} between 300mV and 2.048V, with 2mV per step. {V_REFx_HIGH, V_REFx_LOW} = 00_1001_0110: 300mV {V_REFx_HIGH, V_REFx_LOW} = 00_1001_0111: 302mV ... {V_REFx_HIGH, V_REFx_LOW} = 11_1111_1111: 2.048V Others: 0mV Note that the MP5475 does not execute V_{REF} until the V_REFx_LOW bits are configured. The user must configure V_REFx_HIGH first, then configure V_REFx_LOW.

SYSTEM (40h)

The SYSTEM command enables system settings, including the overall system, each buck regulator, and software restart.

Bits	Access	Bit Name	Default	Reset Condition	Description
7	WR	SYSEN	1'b0	V_{CC} < 2V, V_{DRV} < 2V	Enables the system. When the MP5475 detects a power-on event, it sets this bit to 1. Then the power-on sequence starts. The DC/DC converters turn on sequentially according to the corresponding enable bit (e.g. ENA = 1 for buck A) and power-on delay (SOFT_START_DELAY1) setting. Set this bit from 1 to 0 to trigger the power-off sequence. Other I²C registers are not reset when the I²C-set SYSEN transitions from 1 to 0.
6	WR	RESERVED	1'b1	V_{CC} < 2V, V_{DRV} < 2V	Reserved.
5:2	WR	ENx	ENA = 1 ENB = 1 ENC = 1 END = 1	V_{CC} <2V, V_{DRV} < 2V	Enables each buck regulator. 1: Enabled 0: Disabled
0	WR	SFRST	1'b1	V_{CC} < 2V, V_{DRV} < 2V	Enables software restart. 0: Software restart is disabled 1: Software restart is enabled. The MP5475 initiates a repower-on event when PG low is detected during the power-on state

AVP_ENx, AVP_GAINx, and AVP_TRIMx (from Registers 17h and 27h)

The AVP_EN, AVP_GAIN, and AVP_TRIM bits configure active voltage positioning (AVP) for buck A and buck B (or buck C and buck D).

Bits	Access	Bit Name	Default	Reset Condition	Description
7	WR	AVP_ENx	AVP_ENA = 0 AVP_ENC = 0	V_{CC} < 2V, V_{DRV} < 2V	Enables buck A and buck C's AVP function. 0: The AVP function is disabled 1: The AVP function is enabled
6:5	WR	AVP_GAINx	AVP_GAINA = 01 AVP_GAINC = 01	V_{CC} < 2V, V_{DRV} < 2V	Sets the AVP gain. 00: 2.5mV/A 01: 2mV/A 10: 1mV/A 11: 0.5V/A
4:0	WR	AVP_TRIMx	AVP_TRIMA = 0_0000 AVP_TRIMC = 0_0000	V_{CC} < 2V, V_{DRV} < 2V	Sets the DC offset voltage to the V_{OUTx} command value when AVP is enabled between -28mV and +28mV, with 2mV per step. x_0000 : 0mV 0_0001 : 2mV … 0_1111: 28mV 1_0001: -2mV … 1_1111: -28mV

I2C_SLAVE_ADDRESS (from Register 41h)

The I2C_SLAVE_ADDRESS bits configures the slave address.

Bits	Access	Bit Name	Default	Reset Condition	Description
6:0	WR	I2C_SLAVE_ADDRESS	6'b1100 000	V_{CC} < 2V, V_{DRV} < 2V	Sets the MP5475's I²C slave address. Note that the I²C slave address bits only take effect in the multiple-time programmable (MTP) memory.

FREQ, TS_INTERVAL, and PWRG_DELAY (from Register 42h)

The FREQ, TS_INTERVAL, and PWRG_DELAY bits configure the system setting, including frequency, TS_INTERVAL, and PG delay time.

Bits	Access	Bit Name	Default	Reset Condition	Description
7:5	WR	FREQ	3'b010: 1000kHz	V_{CC} < 2V, V_{DRV} < 2V	Sets the frequency of the buck regulator. The switching frequency (f_{SW}) of buck A to buck D remains constant. 000: 500kHz 001: 750kHz 010: 1000kHz 011: 1250kHz 100: 1500kHz 101: 2000kHz

4:2	WR	TS_INTERVAL	3'b011	V_{CC} < 2V, V_{DRV} < 2V	Determines the delay time between each time slot during the start-up delay and shutdown delay. 000: 10ms 001: 5ms 010: 2ms 011: 1ms 100: 500µs 101: 200µs
1:0	WR	PWRG_DELAY	2'b01	V_{CC} < 2V, V_{DRV} < 2V	Sets the PG delay timer after the MP5475's start-up delay finishes. 00: 0.5ms 01: 1ms 01: 10ms 10: 25ms

UVLO, SHUTDOWN_DELAY_EN, OFF_TIME, and SFRST_NUM (from Register 43h)

The UVLO, SHUTDOWN_DELAY_EN, OFF_TIME, and SFRST_NUM bits configure the system, including V_{IN} under-voltage lockout (UVLO), shutdown delay enable, off time during the repower-on sequence for software restart, and the number of repower times for software restart.

Bits	Access	Bit Name	Default	Reset Condition	Description
7	WR	UVLO	1'b0	V_{CC} < 2V, V_{DRV} < 2V	Sets the V_{IN} UVLO threshold. 0: 3.7V rising UVLO threshold, and 3.48V falling UVLO threshold (default) 1: 2.85V rising UVLO threshold, and 2.6V falling UVLO threshold Note that the UVLO control bit only takes effect in the MTP.
5	WR	SHUTDOWN_ DELAY_EN	1'b1	V_{CC} < 2V, V_{DRV} < 2V	The MP5475 offers two types of shutdown sequences when SYSEN = 0 or during software reset. The first type of shutdown sequence is where buck A to buck D follow the shutdown sequence. The second type of shutdown sequence is where the buck A to buck D shutdown sequences occur at the same time. For more details, see the SHUTDOWN_DELAYx bit configuration (from registers 11h, 19h, 21h, and 29h). 0: Shuts down at the same time 1: The shutdown sequence follows the SHUTDOWN_DELAYx bit configuration (from registers 11h, 19h, 21h, and 29h)
4:3	WR	OFF_TIME	2'b00	V_{CC} < 2V, V_{DRV} < 2V	Sets the off time during repower sequence for software restart. 00: 10ms 01: 25ms 10: 50ms 11: 100ms

2:0	WR	SFRST_NUM	3'b111	V_{CC} < 2V, V_{DRV} < 2V || V_{INx} < UVLO	Sets the number of repower times for software restart. 111: Repowers when SFRST is set, and PG low is detected 110: Repower times set to 5 101: Repower times set to 4 100: Repower times set to 3 011: Repower times set to 2 010: Repower times set to 1 001: Repower times set to 0 000: Repower times set to 0

PWR_GOOD_CFG (from Register 44h)

The PWR_GOOD_CFG bits configure the mask bit for the PWR_GOOD signal.

Bits	Access	Bit Name	Default	Reset Condition	Description
1:0	WR	PWR_GOOD_ CFG	2'b00	V_{CC} < 2V, V_{DRV} < 2V	Sets the mask bit for the PWR_GOOD signal. 00: PWR_GOOD automatic mode 01: Reserved 10: Forces PWR_GOOD to 0 11: Forces PWR_GOOD to 1

XXX_MSK (from Register 45h)

The XXX_MSK bits (1.8VLDO_FAULT_MSK, 1.1VLDO_FAULT_MSK, VR_FAULT_MSK, VBULK_OV_MSK, VDRV_OV_MSK, PMIC_HIGH_TEMP_WARNING_MSK, or PMIC_HIGH_TEMP_SHUTDOWN_MSK) set the mask or unmask for the 1.8VLDO_FAULT, 1.1VLDO_FAULT, VR_FAULT, VBULK_OV, VDRV_OV, PMIC_HIGH_TEMP_WARNING, or PMIC_HIGH_TEMP_SHUTDOWN signal.

Bits	Access	Bit Name	Default	Reset Condition	Description
6:0	WR	XXX_MSK	6'b000000	V_{CC} < 2V, V_{DRV} < 2V	Sets the interrupt mask bit for the 1.8VLDO_FAULT, 1.1VLDO_FAULT, VR_FAULT, VBULK_OV, VDRV_OV, PMIC_HIGH_TEMP_WARNING, or PMIC_HIGH_TEMP_SHUTDOWN signal. 0: Unmask is off for the related interrupt 1: Masks the related interrupt

MTP_CONFIGURE_CODE (from Register 50h)

The MTP_CONFIGURE_CODE bits set the MTP configure code.

Bits	Access	Bit Name	Default	Reset Condition	Description
7:0	WR	MTP_ CONFIGURE_ CODE	N/A	V_{CC} < 2V, V_{DRV} < 2V	Sets the MTP configure code, which is used to identify different MTP configurations.

MTP_REVISION_NUMBER (from Register 51h)

The MTP_REVISION_NUMBER bits set the MTP revision number.

Bits	Access	Bit Name	Default	Reset Condition	Description
7:0	WR	MTP_REVISION_ NUMBER	N/A	V_{CC} < 2V, V_{DRV} < 2V	Sets the MTP revision number, which is used to track multiple MTP revisions.

I²C REGISTER MAP

Scope	Reg (0x)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
System	05 (RO)	RESERVED				FSM_STATE		PMR_GOOD	PMR_GOOD_RAW
	06 (RO)	BUCKA_PG_FILT	BUCKB_PG_FILT	BUCKC_PG_FILT	BUCKD_PG_FILT	BUCKA_PG_RAW	BUCKB_PG_RAW	BUCKC_PG_RAW	BUCKD_PG_RAW
	07 (RC)	BUCKA_UV	BUCKB_UV	BUCKC_UV	BUCKD_UV	BUCKA_OV	BUCKB_OV	BUCKC_OV	BUCKD_OV
	08 (RC)	BUCKA_OC	BUCKB_OC	BUCKC_OC	BUCKD_OC	BUCKA_OC_WARNING	BUCKB_OC_WARNING	BUCKC_OC_WARNING	BUCKD_OC_WARNING
	09 (WC)	RESERVED	1.8VLDO_FAULT	1.1VLDO_FAULT	VR_FAULT	VBULK_OV	VDRV_OV	PMIC_HIGH_TEMP_WARNING	PMIC_HIGH_TEMP_SHUTDOWN
Buck A	10 (WR)	DUAL_PHASE_ENA	SOFT_START_DELAYA			SOFT_START_TIMEA			
	11 (WR)	SHUTDOWN_DELAYA			SOFT_STOP_TIMEA	VOUT_TRANSITION_RATEA			
	12 (WR)	VOUT_LIMIT_ENA	MODEA	CURRENT_LIMITA		VOUT_OVP_ENA	PHASE_DELAY_SELECTA		VOUT_DIS_ENA
	13 (WR)	VOUT_SELECTA	RESERVED					V_REFA_HIGH	
	14 (WR)	V_REFA_LOW							
	15 (WR)	RESERVED							
	16 (WR)	RESERVED							
	17 (WR)	AVP_ENA	AVP_GAINA		AVP_TRIMA				
Buck B	18 (WR)	RESERVED	SOFT_START_DELAYB			SOFT_START_TIMEB			
	19 (WR)	SHUTDOWN_DELAYB			SOFT_STOP_TIMEB	VOUT_TRANSITION_RATEB			
	1A (WR)	VOUT_LIMIT_ENB	MODEB	CURRENT_LIMITB		VOUT_OVP_ENB	PHASE_DELAY_SELECTB		VOUT_DIS_ENB
	1B (WR)	VOUT_SELECTB	RESERVED					V_REFB_HIGH	
	1C (WR)	V_REFB_LOW							
	1D (WR)	RESERVED							
	1E (WR)	RESERVED							
Buck C	20 (WR)	DUAL_PHASE_ENC	SOFT_START_DELAYC			SOFT_START_TIMEC			
	21 (WR)	SHUTDOWN_DELAYC			SOFT_STOP_TIMEC	VOUT_TRANSITION_RATEC			
	22 (WR)	VOUT_LIMIT_ENC	MODEC	CURRENT_LIMITC		VOUT_OVP_ENC	PHASE_DELAY_SELECTC		VOUT_DIS_ENC
	23 (WR)	VOUT_SELECTC	RESERVED					V_REFC_HIGH	
	24 (WR)	V_REFC_LOW							
	25 (WR)	RESERVED							
	26 (WR)	RESERVED							
	27 (WR)	AVP_ENC	AVP_GAINC		AVP_TRIMC				

I²C REGISTER MAP *(continued)*

Scope	Reg (0x)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Buck D	28 (WR)	RESERVED	SOFT_START_DELAYD			SOFT_START_TIMED			
	29 (WR)	SHUTDOWN_DELAYD			SOFT_STOP_TIMED	VOUT_TRANSITION_RATED			
	2A (WR)	VOUT_LIMIT_END	MODED	CURRENT_LIMITD		VOUT_OVP_END	PHASE_DELAY_SELECTD		VOUT_DIS_END
	2B (WR)	VOUT_SELECTD	RESERVED					V_REFD_HIGH	
	2C (WR)	V_REFD_LOW							
	2D (WR)	RESERVED							
	2E (WR)	RESERVED							
System	40 (WR)	SYSEN	RESERVED	ENA	ENB	ENC	END	RESERVED	SFRST
	41 (WR)	RESERVED	SLAVE_ADDRESS						
	42 (WR)	FREQ (500k/750k/1000k/1.25M/1.5M/2M)			TS_INTERVAL			PWRG_DELAY	
	43 (WR)	UVLO	MTP_PROGRAM	SHUTDOWN_DELAY_EN	OFF_TIME		SFRST_NUM		
	44 (WR)	RESERVED	RESERVED		WP_EN	RESERVED	RESERVED	PWR_GOOD_CFG	
	45 (WR)	RESERVED	1.8VLDO_FAULT_MSK	1.1VLDO_FAULT_MSK	VR_FAULT_MSK	VBULK_OV_MSK	VDRV_OV_MSK	PMIC_HIGH_TEMP_WARNING_MSK	PMIC_HIGH_TEMP_SHUTDOWN_MSK
	50 (WR)	MTP_CONFIGURE_CODE							
	51 (WR)	MTP_REVISION_NUMBER							
	52 (WR)	MTP_PROGRAM_PASSWORD							
	54 (WR)	REVISION_ID_MAJOR_STEPPING				REVISION_ID_MINOR_STEPPING			
	55 (WR)	VENDER_ID_BYTE0							
	56 (WR)	VENDER_ID_BYTE1							

Register Bits Description

Most of the register bits share the same description as the MTP table. Only the description of different register bits are included below.

The I²C register's default value is determined by the MTP table.

All I²C registers are reset at the V_{CC} UVLO threshold, V_{IN} < UVLO, or the EN pin going low.

OTP does not reset via the I²C register.

The below I²C register bits can only take effect after MTP:

1. DUAL_PHASE_EN1 (bit[7] of register 10h)
2. DUAL_PHASE_EN3 (bit[7] of register 20h)
3. I²C slave address (bits[6:0] of register 41h)
4. UVLO (bit[7] of register 43h)

FSM_STATE, PWR_GOOD, and PWR_GOOD_RAW (from Register 05h)

The FSM_STATE, PWR_GOOD, and PWR_GOOD_RAW bits control certain system configurations, including the state, PWR_GOOD_RAW signal, and the output for all the BUCK_PG_FILT states.

Bits	Access	Bit Name	Default	Description
3:2	RO	FSM_STATE	2'b00	00: Management state 01: Power-on state
1	RO	PWR_GOOD	1'b0	Sets the PWR_GOOD_RAW signal, which is filtered by the FSM_STATE signal. When PWR_GOOD_RAW is high and the MP5475 is not in management state, PWR_GOOD is high. 0: PWR_GOOD outputs low 1: PWR_GOOD outputs high
0	RO	PWR_GOOD_RAW	1'b0	Sets the output for all the BUCK_PG_FILT signals. 0: PWR_GOOD_RAW outputs low 1: PWR_GOOD_RAW outputs high

BUCKx_PG_FILT and BUCKx_PG_RAW (from Register 06h)

The BUCKx_PG_FILT and BUCKx_PG_RAW bits set each buck's PG output and the filter's PG output.

Bits	Access	Bit Name	Default	Description
7:4	RO	BUCKx_PG_FILT	4'b1111	Sets buck x's (where x = A, B, C, or D) PG output filter when working with the EN signal. 0: The filter's PG output is low (the selected rail's output is out of ±20% nominal output) 1: The filter's PG output is high (the selected rail's output is out of ±20% nominal output, or the rail is disabled)
3:0	RO	BUCKx_PG_RAW	4'b0000	Sets buck x's (where x = A, B, C, or D) raw PG output. 0: The PG raw output is low (the selected rail's output is out of ±20% nominal output) 1: The PG raw output is high (the selected rail output is within ±20% nominal output)

BUCKx_UV and BUCKx_OV (from Register 07h)

The BUCKx_UV and BUCKx_OV bits indicate each buck's over-voltage (OV) or under-voltage (UV) status.

Bits	Access	Bit Name	Default	Description
7:4	RC	BUCKx_UV	4'b0000	Indicates buck x's (where x = A, B, C, or D) output UV status. 0: No UV condition on buck x 1: UV condition on buck x (below 20% of nominal output window)
3:0	RC	BUCKx_OV	4'b0000	Indicates buck x's (where x = A, B, C, or D) output OV status. 0: No OV condition on buck x 1: OV condition on buck x (above 20% of nominal output window)

BUCKx_OC and BUCKx_OC_WARNING (from Register 08h)

The BUCKx_OC and BUCKx_OC_WARNING bits indicate each buck's over-current (OC) status as well as the high current consumption warning status.

Bits	Access	Bit Name	Default	Description
7:4	RC	BUCKx_OC	4'b0000	Indicates buck x's (where x = A, B, C, or D) OC status. 0: No buck x OC condition 1: Buck x over-current protection (OCP) has occurred

3:0	RC	BUCKx_OC_ WARNING	4'b0000	Indicates buck x's (where x = A, B, C, or D) high current consumption warning status (the output current exceeds 85% of the threshold). 0: No high current consumption warning 1: High current consumption warning

SYSTEM (09h)

The SYSTEM command indicates error statuses, such as 1.8V LDO and 1.1V LDO faults, voltage regulator (VR) faults, and V_{INx} OV faults, as well as PMIC high-temperature warnings and high-temperature shutdown, where the temperature is between 125°C and 150°C.

Bits	Access	Bit Name	Default	Description
6	WC	1.8VLDO_FAULT	1'b0	Indicates the 1.8VLDO's output PG status. 0: The 1.8VLDO output is within ±15% of the nominal output window 1: The 1.8VLDO output is not within ±15% of the nominal output window
5	WC	1.1VLDOX_FAULT	1'b0	Indicates the 1.1VLDO's output PG status. 0: The 1.1VLDO output is within ±15% of the nominal output window 1: The 1.1VLDO output is not within ±15% of the nominal output window
4	WC	VR_FAULT	1'b0	Indicates the overall buck's PG status. 0: All buck outputs are within ±20% of the nominal range 1: One (or more) buck output(s) are outside of the ±20% nominal range
3	WC	VBULK_OV	1'b0	Indicates the V_{INx} OV status. 0: V_{INx} is below 14.2V 1: V_{INx} exceeds 14.5V
2	WC	VDRV_OV	1'b0	Indicates V_{DRV}'s OV status. 0: V_{DRV} is below 3.5V 1: V_{DRV} exceeds 3.6V
1	WC	PMIC_HIGH_TEMP_ WARNNING	1'b0	Indicates whether the PMIC has a high-temperature warning. 0: No high-temperature warning 1: The PMIC's silicon temperature exceeds 125°C
0	WC	PMIC_HIGH_TEMP_ SHUTDOWN	1'b0	Indicates the PMIC's high-temperature shutdown status. 0: No high temperature shutdown 1: The PMIC's silicon temperature exceeds 150°C

MTP_PROGRAM (from Register 43h)

The MTP_PROGRAM bits control MTP configuration.

Bits	Access	Bit Name	Default	Reset Condition	Description
6	WR	MTP_PROGRAM	1'b0	Automatic	Controls MTP configuration. Once this bit is set, the I²C register is written to the MTP table. During MTP writing, I²C write operation is locked and not acknowledged (NACK), but read operation is not locked until MTP write operation finishes. Then the system automatically resets this bit.

WP_EN (from Register 44h)

The WP_EN bit enables I²C write protection.

Bits	Access	Bit Name	Default	Reset Condition	Description
4	WR	WP_EN	1'b0	V_{CC} < 2V, V_{DRV} < 2V	Enables I²C write protection. 0: No write protection 1: Only allowed to write to the I²C register while in the management state

MTP_PROGRAM_PASSWORD(from Register 52h)

The MTP_PROGRAM_PASSWORD bits set the correct password for MTP configuration.

Bits	Access	Bit Name	Default	Reset Condition	Description
7:0	WR	MTP_ PROGRAM_ PASSWORD	8'b0000 0000	V_{CC} < 2V, V_{DRV} < 2V	Sets the correct password for MTP configuration. These bits controls access to the MTP_PROGRAM bit.

REVISION_ID_MAJOR_STEPPING and REVISION_ID_MINOR_STEPPING (from Register 54h)

The REVISION_ID_MAJOR_STEPPING and REVISION_ID_MINOR_STEPPING bits set the major and minor revision.

Bits	Access	Bit Name	Default	Reset Condition	Description
7:4	WR	REVISION_ID_ MAJOR_ STEPPING	4'b0000	V_{CC} < 2V, V_{DRV} < 2V	Sets the major revision. All other encodings are reserved. 0000: Reserved 0001: Revision 1 0010: Revision 2 0011: Revision 3
3:0	WR	REVISION_ID_ MINOR_ STEPPING	4'b0000	V_{CC} < 2V, V_{DRV} < 2V	Sets the minor revision. All other encodings are reserved. 0000: Reserved 0001: Revision 1 0010: Revision 2 0011: Revision 3

VENDOR_ID_BYTE0 (from Register 55h)

The VENDOR_ID_BYTE0 bits set the lower byte of the vendor's ID.

Bits	Access	Bit Name	Default	Reset Condition	Description
7:0	WR	VENDOR_ID_ BYTE0	8'b0000 0000	V_{CC} < 2V, V_{DRV} < 2V	Sets the lower byte of the vendor's ID.

VENDOR_ID_BYTE1 (from Register 56h)

The VENDOR_ID_BYTE1 bits set the higher byte of the vendor's ID.

Bits	Access	Bit Name	Default	Reset Condition	Description
7:0	WR	VENDOR_ID_ BYTE1	8'b0000 0000	V_{CC} < 2V, V_{DRV} < 2V	Sets the higher byte of the vendor's ID.

APPLICATION INFORMATION

Selecting the Inductor

MPL Optimized Performance with MPS Inductor MPL4020 Series

Choose a 0.22µH to 2µH inductor with a minimum DC current rating exceeding 25% of the maximum load current for most applications. To optimize efficiency, use an inductor with a DC resistance below 15mΩ. For most designs, the inductance (L1) can be calculated with Equation (1):

$$L1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current (I_{L_MAX}) can be estimated with Equation (2):

$$I_{L\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Use a larger-value inductor to achieve improved efficiency under light-load conditions (below 100mA).

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 shows the MPS power inductor recommendations, where the part number can be selected based on the design requirements.

Table 2: Selecting the Power Inductor

Part Number	Inductance	Manufacturer
MPL-AL4020-R47	0.47µH	MPS
MPL-AL4020-R68	0.68µH	MPS
MPL-AL4020-1R0	1µH	MPS
MPL-AL4020-1R5	1.5µH	MPS

For more information, visit the Inductors page on the MPS website.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended for the best results due to their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor (C_{IN}) (I_{C1}) can be calculated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, which can be estimated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose C_{IN} with an RMS current rating that is greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure there is enough capacitance to provide sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Output Capacitor for the Step-Down Regulator

The output capacitor (C_{OUT}) for the step-down converter maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (6)$$

Where L1 is the inductance, and R_{ESR} is the equivalent series resistance (ESR) of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}.

For simplification, ΔV_{OUT} can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The C_{OUT} characteristics also affect the stability of the regulation system.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 21 and follow the guidelines below:

1. Connect the input ground to the ground with the shortest and widest trace possible.
2. Connect C_{IN} to the VINx pin (where x = A, B, C, or D) with the shortest and widest trace possible.
3. Ensure all FB connections are short and direct.
4. Place the FB resistors and compensation components as close to the chip as possible.
5. Route the SWx pin (where x = A, B, C, or D) away from sensitive analog areas, such as FB.
6. Place the VCC decoupling capacitor close to the VCC and AGND pins.
7. Keep an open space around the PMIC and ensure that the airflow is at least 200FPM to 400FPM on the PMIC surface and the other side of the DIMM board. Airflow is required for PMIC heat dissipation.

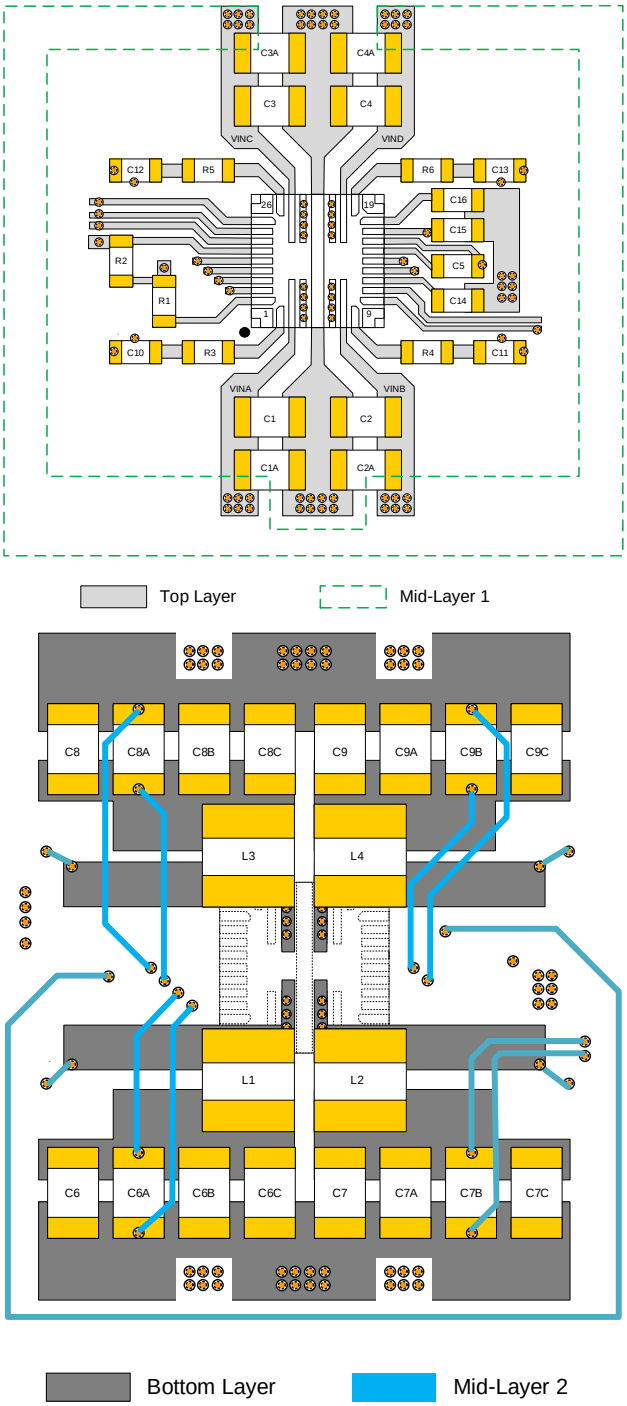


Figure 21: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

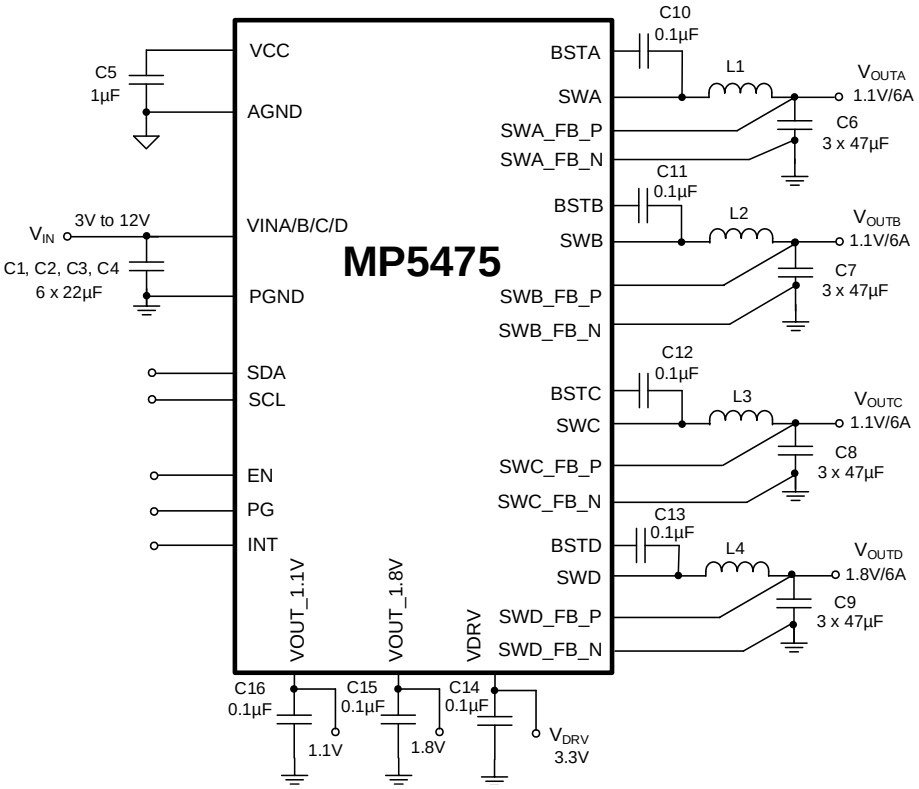


Figure 22: Typical Application Circuit (Buck A and Buck B in Single-Phase Regulator Mode)

TYPICAL APPLICATION CIRCUITS *(continued)*

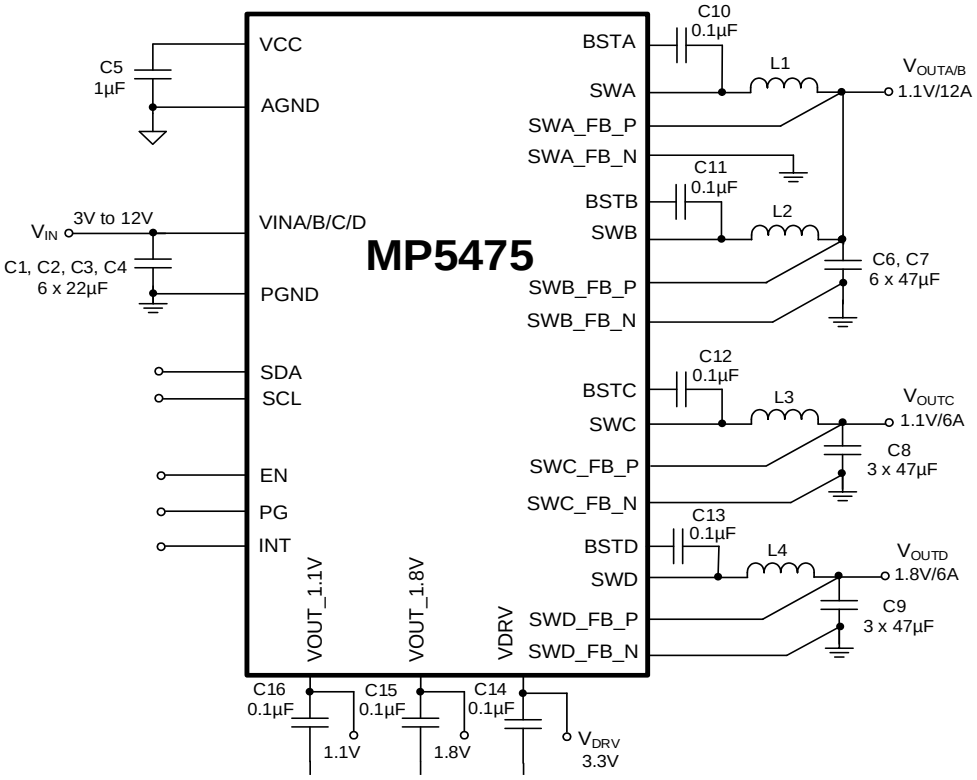
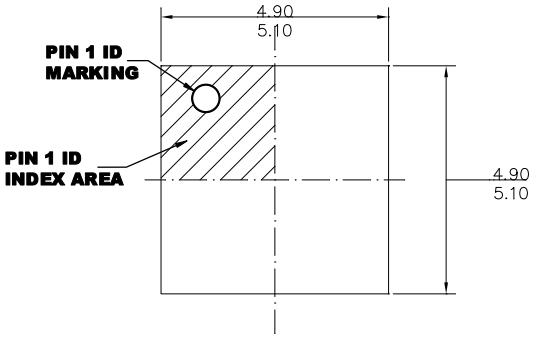


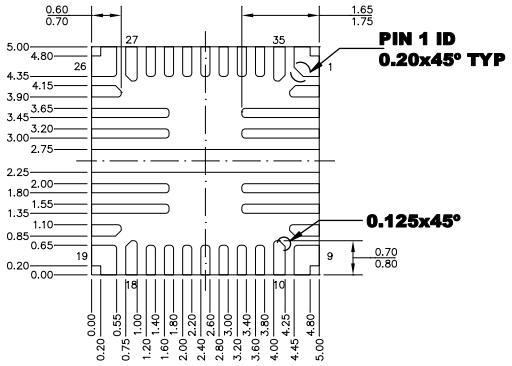
Figure 23: Typical Application (Buck A and Buck B in Dual-Phase Regulator Mode)

PACKAGE INFORMATION

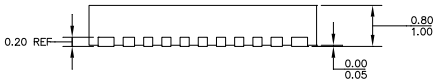
QFN-35 (5mmx5mm)



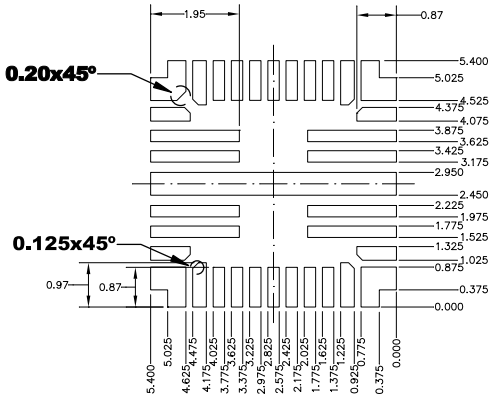
TOP VIEW



BOTTOM VIEW



SIDE VIEW

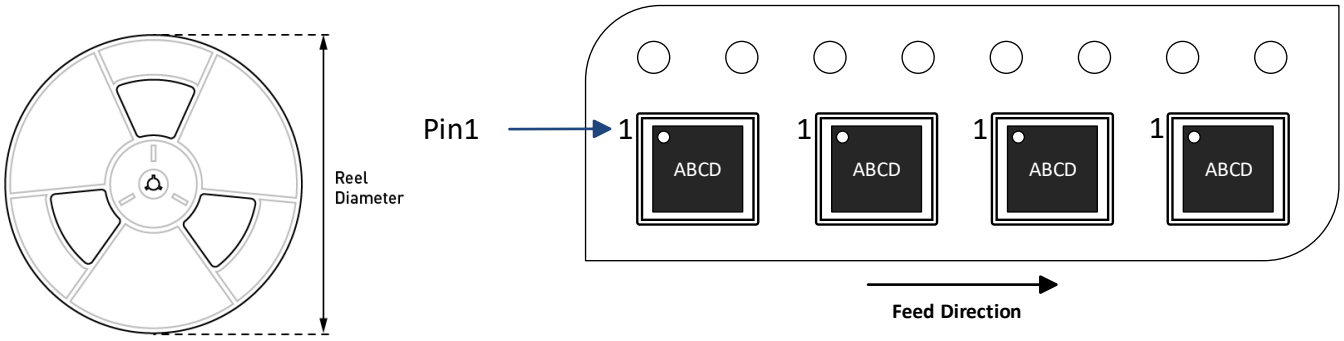


RECOMMENDED LAND PATTERN

NOTE:

1)ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-333.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5475GU-xxxx-Z	QFN-35 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/7/2024	Initial Release	-