

REG710xx Buck-Boost Charge Pump with up to 60-mA Output Current

1 Features

- Wide Input Voltage Range: 1.8 V to 5.5 V
- Automatic Step-Up and Step-Down Operation
- Low Input Current Ripple
- Low Output Voltage Ripple
- Minimum Number of External Components—No Inductors
- 1-MHz Internal Oscillator Allows Small Capacitors
- Shutdown Mode
- Thermal and Current Limit Protection
- Six Fixed Output Voltages Available:
 - 2.5 V, 2.7 V, 3 V, 3.3 V, 5 V, 5.5 V

2 Applications

- White LED Driver
- Smart Card Readers
- SIM Cards
- Handheld devices
- Modems
- PCMCIA Cards
- LCD Displays
- Battery Backup Supplies

3 Description

The REG710 family of devices are switched capacitor voltage converters that generate regulated, low-ripple output voltage from an unregulated input voltage. A wide input supply voltage from 1.8 V to 5.5 V makes the REG710 family of devices ideal for a variety of battery sources, such as single-cell Li-Ion, or 2-cell and 3-cell nickel-based or alkaline-based chemistries.

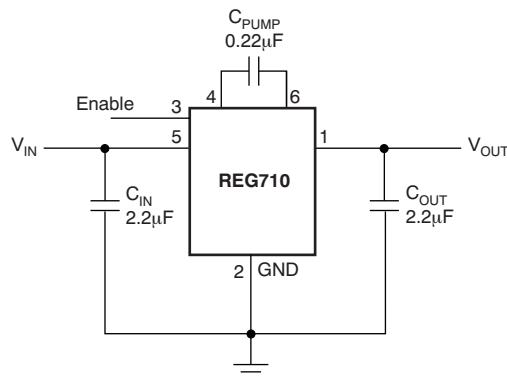
The input voltage may vary above and below the output voltage and the output remains in regulation. The device works as step-up or step-down converters without the need of an inductor, providing low EMI DC-DC conversion. The high switching frequency allows the use of small surface-mount capacitors, saving board space and reducing cost. The REG710 device is thermally protected and current limited, protecting the load and the regulator during fault conditions. Typical ground pin current (quiescent current) is 65 μ A with no load, and less than 1 μ A in shutdown mode.

Device Information⁽¹⁾

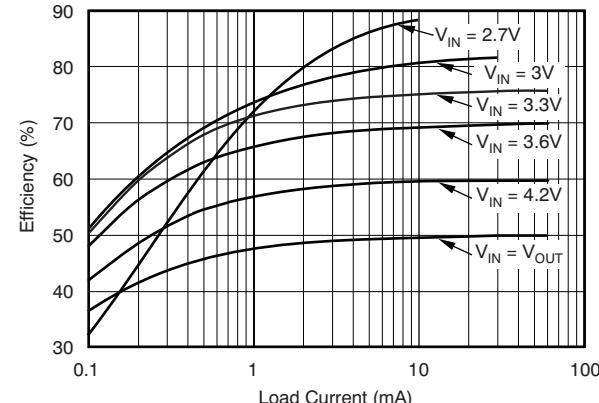
PART NUMBER	PACKAGE	BODY SIZE (NOM)
REG710	SOT-23 (6)	2.90 mm x 1.60 mm
REG71050	SOT (6)	2.90 mm x 1.60 mm
	SON (6)	2.00 mm x 2.00 mm
REG71055	SOT-23 (6)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Operating Circuit



Efficiency vs Load Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2009) to Revision H	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

5 Device Comparison Table

ORDER NUMBER	OUTPUT VOLTAGE
REG71055	5.5 V
REG710NA-5	5 V
REG71050	
REG710NA-3.3	3.3 V
REG710NA-3	3 V
REG710NA-2.7	2.7 V
REG710NA-2.5	2.5 V

6 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DDC/DBV	DRV		
C_{pump-}	4	3	–	Connect to the flying capacitor
C_{pump+}	6	1	–	Connect to the flying capacitor
Enable	3	5	I	Hardware Enable/Disable pin (high=enable)
GND	2	4	–	Ground
V_{in}	5	2	I	Input supply pin. Connect the input capacitor to this pin.
V_{out}	1	6	O	Output supply. Connect the output capacitor to this pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply voltage	-0.3	6	V
Enable	Enable input	-0.3	V_{IN}	
	Output short-circuit duration	Indefinite		
T_A	Operating ambient temperature	-55	125	°C
T_J	Operating ambient temperature	-55	150	
T_{stg}	Storage temperature	-55	150	

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
INPUT VOLTAGE					
Tested Startup ⁽¹⁾	REG71055	3	5.5	V	
	REG710-5	2.7	5.5	V	
	All other models	1.8	5.5	V	
T _A	Operating ambient temperature range	-40	85	°C	

(1) See conditions under Output Voltage with a resistive load no lower than typical V_{OUT}/I_{OUT} in [Electrical Characteristics](#).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		REG710			UNIT
		DRV	DDC	DBV	
		6 PINS	6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	119.1	204.6	184.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	110.5	50.5	124.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	88.7	54.3	30.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	7.7	0.8	22.1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	89	52.8	30.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	61.8	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted), V_{IN} = (V_{OUT} / 2 + 0.75 V), I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 2.2 μF, C_{PUMP} = 0.22 μF, and V_{ENABLE} = 1.3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY					
V _{IN}	Input voltage range. Tested Startup.				
REG71055	See conditions under Output Voltage with a resistive load no lower than typical V _{OUT} /I _{OUT} .	3	5.5		V
REG710-5		2.7	5.5		
All other models		1.8	5.5		
I _Q	I _{OUT} = 0 mA, T _A = 25°C		65	100	μA
I _{SD}	V _{IN} = 1.8 V to 5.5 V, Enable = 0 V, T _A = 25°C		0.01	1	μA
CONTROL SIGNALS (ENABLE)					
Logic high input voltage	V _{IN} = 1.8 V to 5.5 V	1.3	V _{IN}		V
Logic low input voltage	V _{IN} = 1.8 V to 5.5 V	-0.2	0.4		V
Logic high input current	V _{IN} = 1.8 V to 5.5 V, T _A = 25°C		100	nA	
Logic low input current	V _{IN} = 1.8 V to 5.5 V, T _A = 25°C		100	nA	
OSCILLATOR FREQUENCY⁽¹⁾					
			1		MHz

(1) The converter regulates by enabling and disabling periods of switching cycles. The switching frequency is the oscillator frequency during an active period.

Electrical Characteristics (continued)

$T_A = -40^\circ\text{C}$ to 85°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted), $V_{IN} = (V_{OUT} / 2 + 0.75 \text{ V})$, $I_{OUT} = 10 \text{ mA}$, $C_{IN} = C_{OUT} = 2.2 \mu\text{F}$, $C_{PUMP} = 0.22 \mu\text{F}$, and $V_{ENABLE} = 1.3 \text{ V}$, unless otherwise noted.

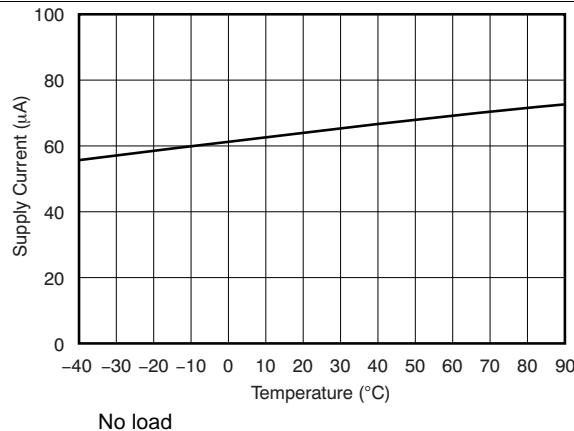
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT					
REG71055	$I_{OUT} \leq 10 \text{ mA}, 3 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	5.2	5.5	5.8	V
	$I_{OUT} \leq 30 \text{ mA}, 3.25 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	5.2	5.5	5.8	V
REG710-5, REG71050	$I_{OUT} \leq 10 \text{ mA}, 2.7 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	4.7	5	5.3	V
	$I_{OUT} \leq 30 \text{ mA}, 3 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	4.7	5	5.3	V
REG710-3.3	$I_{OUT} \leq 60 \text{ mA}, 3.3 \text{ V} \leq V_{IN} \leq 4.2 \text{ V}$	4.6	5	5.4	V
	$I_{OUT} \leq 10 \text{ mA}, 1.8 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	3.1	3.3	3.5	V
REG710-3	$I_{OUT} \leq 30 \text{ mA}, 2.2 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	3.1	3.3	3.5	V
	$I_{OUT} \leq 10 \text{ mA}, 1.8 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	2.82	3	3.18	V
REG710-2.7	$I_{OUT} \leq 30 \text{ mA}, 2 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	2.82	3	3.18	V
	$I_{OUT} \leq 10 \text{ mA}, 1.8 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	2.54	2.7	2.86	V
REG710-2.5	$I_{OUT} \leq 30 \text{ mA}, 2 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	2.54	2.7	2.86	V
	$I_{OUT} \leq 10 \text{ mA}, 1.8 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$	2.35	2.5	2.65	V
I_{out}	Nominal output current	$T_A = 25^\circ\text{C}$	30		mA
I_{sc}	Short circuit output current	$T_A = 25^\circ\text{C}$		100	mA
RIPPLE VOLTAGE⁽²⁾					
$I_{OUT} = 30 \text{ mA}, T_A = 25^\circ\text{C}$					
EFFICIENCY⁽³⁾					
$I_{OUT} = 10 \text{ mA}, V_{IN} = 1.8 \text{ V}, \text{REG710-3.3}, T_A = 25^\circ\text{C}$					
THERMAL SHUTDOWN					
Shutdown temperature					
Shutdown recovery					

(2) Effective series resistance (ESR) of capacitors is < 0.1 Ω .

(3) See efficiency curves for other V_{IN}/V_{OUT} configurations.

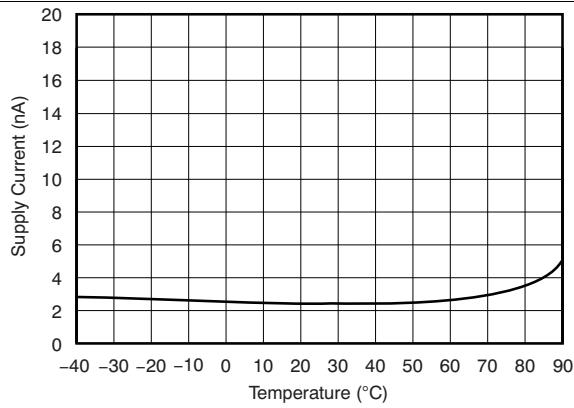
7.6 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_{IN} = (V_{OUT} / 2 + 0.75 \text{ V})$, $I_{OUT} = 5 \text{ mA}$, $C_{IN} = C_{OUT} = 2.2 \mu\text{F}$, $C_{PUMP} = 0.22 \mu\text{F}$, and $V_{ENABLE} = 1.3 \text{ V}$, unless otherwise noted.



No load

Figure 1. Supply Current vs Temperature



Not enabled

Figure 2. Supply Current vs Temperature

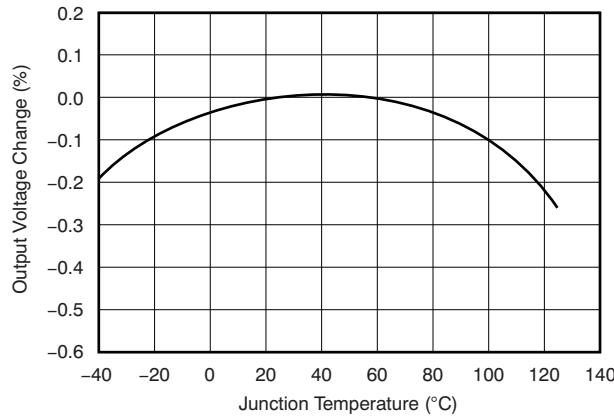


Figure 3. Output Voltage vs Temperature

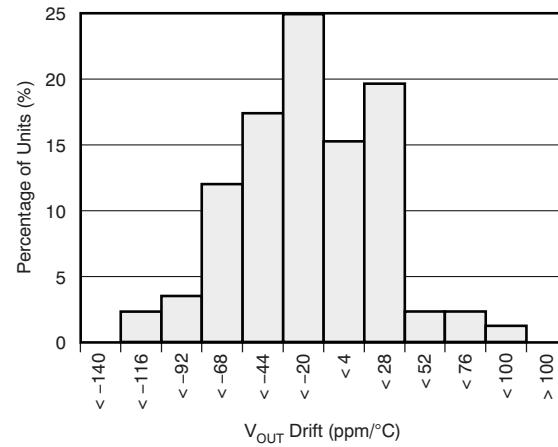


Figure 4. Output Voltage Drift Histogram

8 Detailed Description

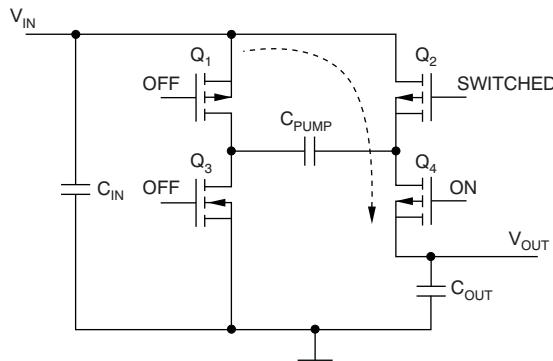
8.1 Overview

The REG710 regulated charge pump provides a regulated output voltage for input voltages which are not regulated with a value that can be lower or higher than the regulated output voltage. This is accomplished by automatic mode switching within the device. When the input voltage is greater than the required output, the device operates as a variable frequency switched-mode regulator. This operation is shown in [Figure 5](#). Transistors Q₁ and Q₃ are held off, Q₄ is on, and Q₂ is switched as needed to maintain a regulated output voltage.

When the input voltage is less than the required output voltage, the device switches to a step-up or boost mode of operation, as shown in [Figure 6](#).

A conversion clock of 50% duty cycle is generated. During the first half cycle the FET switches are configured as shown in [Figure 6](#) (A), and C_{PUMP} charges to V_{IN}.

During the second half cycle the FET switches are configured as shown in [Figure 6](#) (B), and the voltage on C_{PUMP} is added to V_{IN}. The output voltage is regulated by skipping clock cycles as necessary.



Step-Down (Buck) Mode

Figure 5. Simplified Schematic of the REG710 Operating in the Step-Down Mode

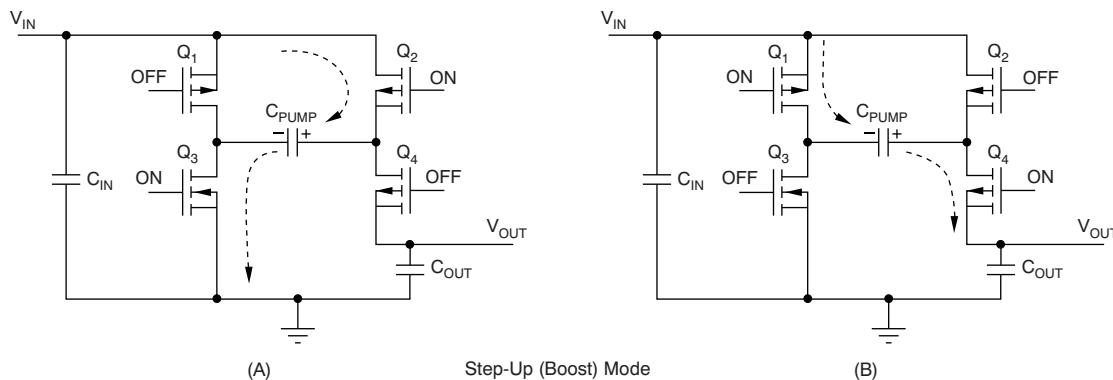
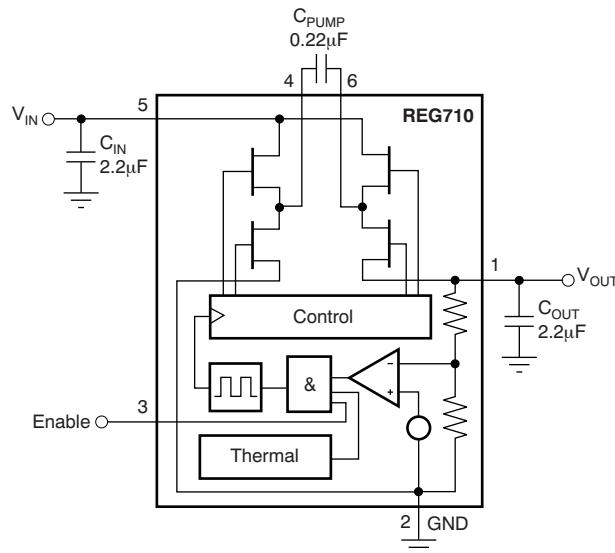


Figure 6. Simplified Schematic of the REG710 Operating in the Step-Up or Boost Mode

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Shutdown Mode

The EN pin enables the IC when pulled high and places it into energy-saving shutdown mode when pulled low. When in shutdown mode, the output is disconnected from the input and the quiescent current is reduced to 0.01 μA typical. This shutdown mode functionality is only valid when V_{IN} is above the minimum recommended operating voltage. The EN pin cannot be left floating and must be actively terminated either high or low.

8.3.2 Protection

The regulator includes thermal shutdown circuitry protecting the device from damage caused by overload conditions. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is automatically reenabled. Continuously operating the regulator into thermal shutdown can degrade reliability. The regulator also provides current limit to protect itself and the load.

8.4 Device Functional Modes

8.4.1 Peak Current Reduction

In normal operation, the charging of the pump and the output capacitors usually leads to relatively high peak input currents which can be much higher than the average load current. The regulator incorporates circuitry to limit the input peak current, lowering the total EMI emission and lowering the output voltage ripple and the input current ripple. The Input capacitor (C_{IN}) supplies most of the charge required by the input current peaks.

8.4.2 Efficiency

The efficiency of the charge pump regulator varies with the output voltage version, the applied input voltage, the load current, and the internal operation mode of the device.

The approximate efficiency is given by:

Device Functional Modes (continued)

$$\text{Efficiency (\%)} = V_{\text{OUT}} / (2 \times V_{\text{IN}}) \times 100$$

(step-up operating mode)

or

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} \times 100$$

(step-down operating mode)

(1)

Table 1. Operating Mode Change versus V_{IN}

PRODUCT	OPERATING MODE CHANGES AT V_{IN} OF
REG710-2.5	> 3.2 V
REG710-2.7	> 3.4 V
REG710-3	> 3.7 V
REG710-3.3	> 4.0 V
REG710-5, REG71050, REG71055	Step-up only

Table 1 lists the approximate values of the input voltage at which the device changes internal operating mode. See efficiency curves in *Typical Characteristics* for various loads and input voltages.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The REG710 is a switched capacitor voltage converter that produces a regulated, low-ripple output voltage from an unregulated input voltage range from 1.8 V to 5.5 V. The high switching frequency allows the use of small surface-mount capacitors. The following section gives guidance to choose external components to complete the power supply design. Application curves are included for the typical application shown below.

9.2 Typical Applications

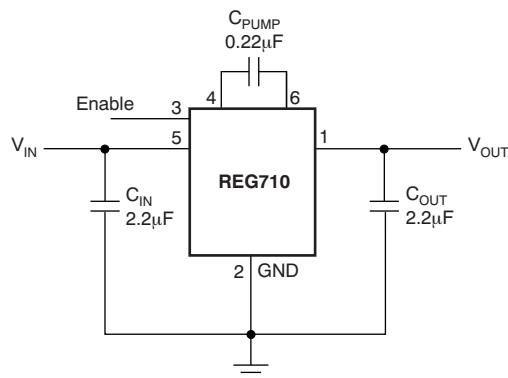


Figure 7. Typical Operating Circuit

9.2.1 Design Requirements

The REG710 family of switched capacitor voltage converters offers a variety of regulated fixed output voltages. This family supports unregulated input voltages which can have values that are lower or higher than the regulated output voltage. Only input and output capacitors as well as a pump capacitor are required to have a fully functional converter. The following design procedure is adequate for the whole V_{IN} , V_{OUT} and load current range of REG710.

9.2.2 Detailed Design Procedure

9.2.2.1 Capacitor Selection

For minimum output voltage ripple, the output capacitor C_{OUT} should be a ceramic, surface-mount type. Tantalum capacitors generally have a higher effective series resistance (ESR) and may contribute to higher output voltage ripple. Leaded capacitors also increase ripple due to the higher inductance of the package itself. To achieve best operation with low input voltage and high load current, the input and pump capacitors (C_{IN} and C_{PUMP} , respectively) should also be surface-mount ceramic types. In all cases, X7R or X5R dielectric are recommended. See the typical operating circuit shown in [Figure 7](#) for component values.

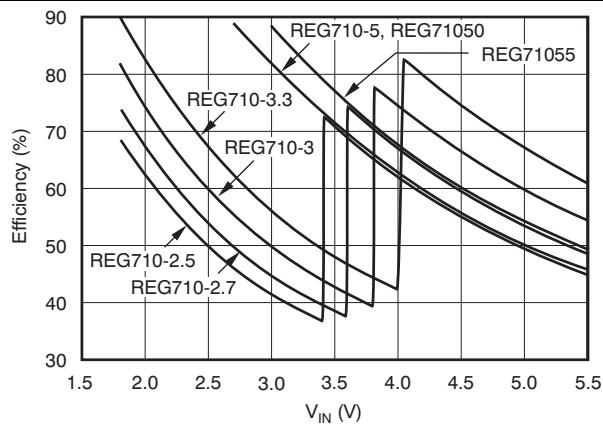
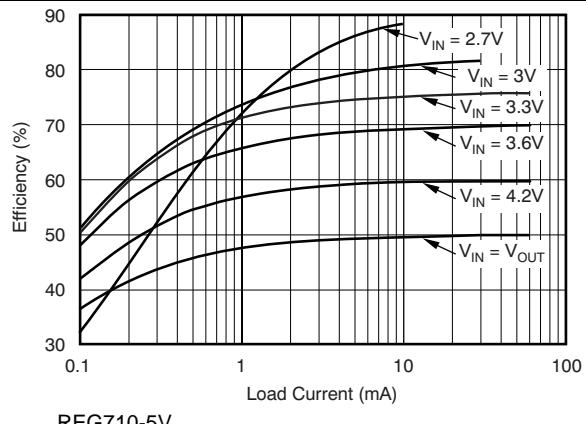
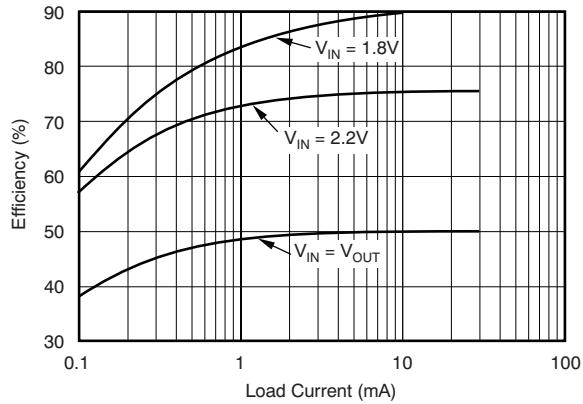
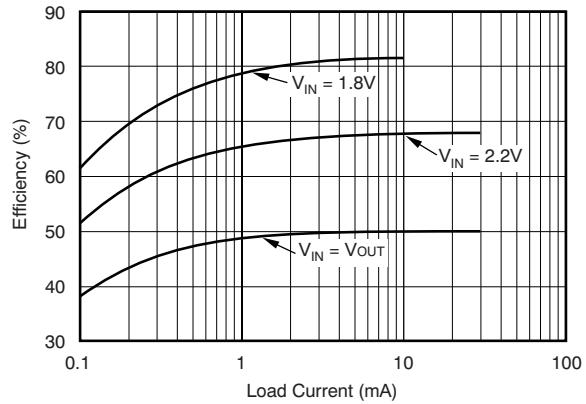
With light loads or higher input voltage, a smaller 0.1- μ F pump capacitor (C_{PUMP}) and smaller 1- μ F input and output capacitors (C_{IN} and C_{OUT} , respectively) can be used. To minimize output voltage ripple, increase the output capacitor, C_{OUT} , to 10 μ F or larger.

The capacitors listed in [Table 2](#) can be used with the REG710. This table is only a representative list of compatible parts.

Table 2. Suggested Capacitors

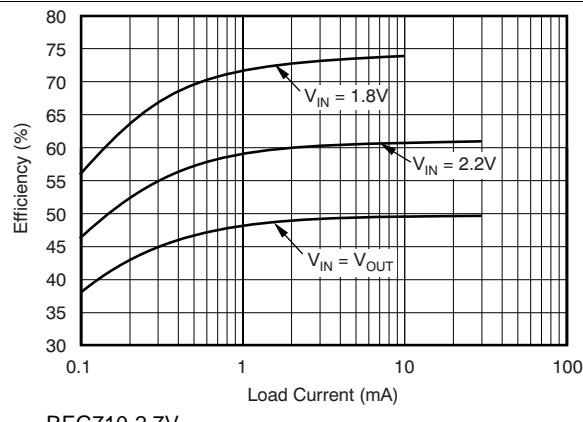
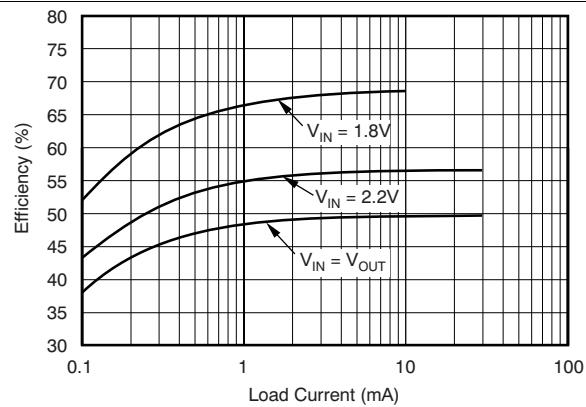
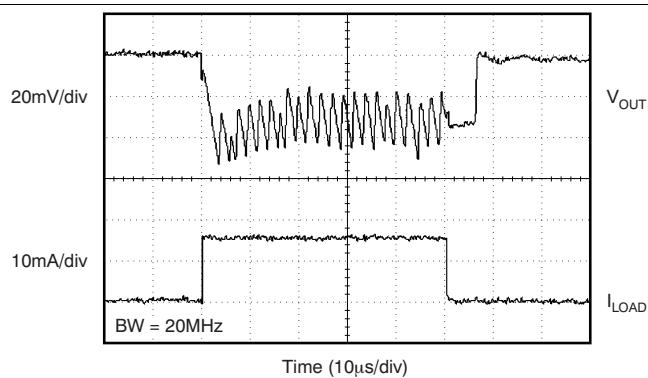
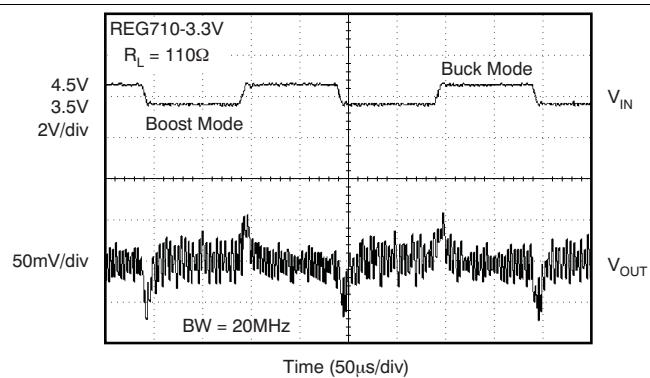
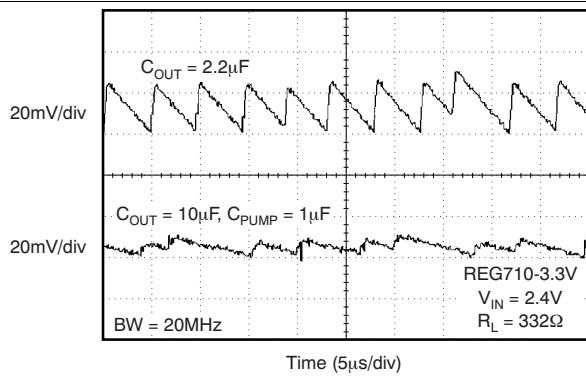
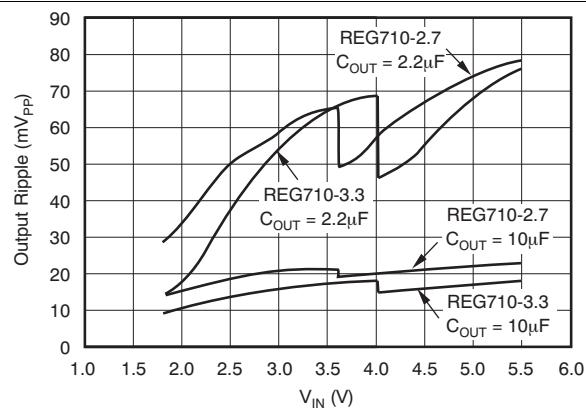
MANUFACTURER	PART NUMBER	VALUE	TOLERANCE	DIELECTRIC MATERIAL	PACKAGE SIZE	RATED WORKING VOLTAGE
Kemet	C1206C255K8RAC	2.2 μ F	$\pm 10\%$	X7R	1206	10 V
	C1206C224K8RAC	0.22 μ F	$\pm 10\%$	X7R	1206	10 V
Panasonic	ECJ-2YBOJ225K	2.2 μ F	$\pm 10\%$	X5R	805	6.3 V
	ECJ-2VBIC224K	0.22 μ F	$\pm 10\%$	X7R	805	16 V
	ECJ-2VBIC104	0.1 μ F	$\pm 10\%$	X7R	805	16 V
Taiyo Yuden	EMK316BJ225KL	2.2 μ F	$\pm 10\%$	X7R	1206	16 V
	TKM316BJ224KF	0.22 μ F	$\pm 10\%$	X7R	1206	25 V

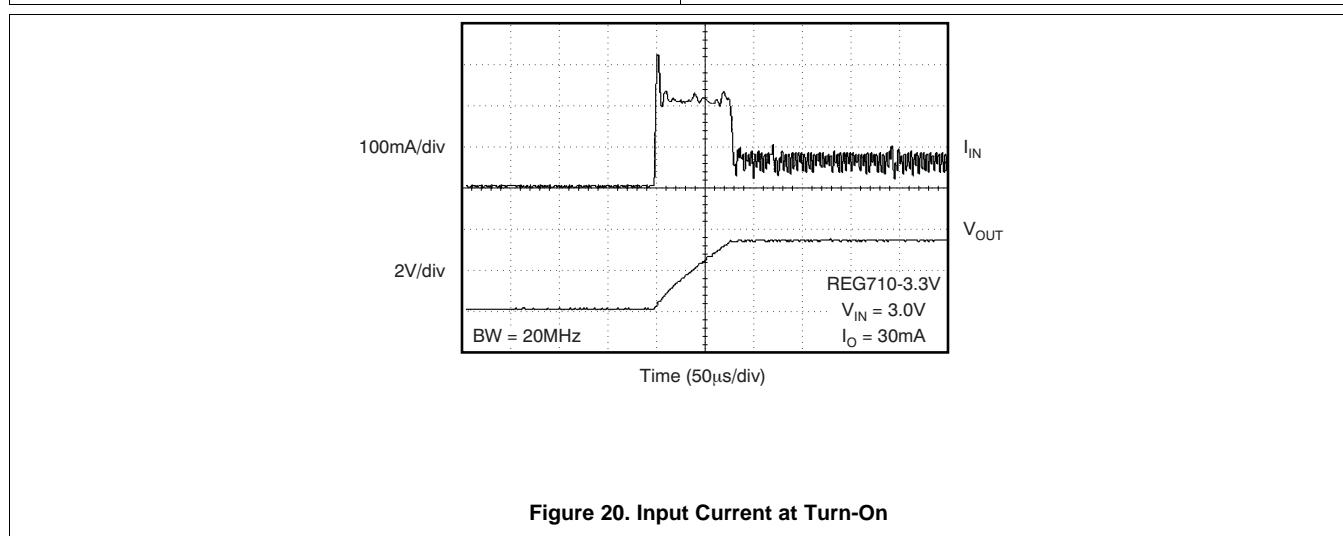
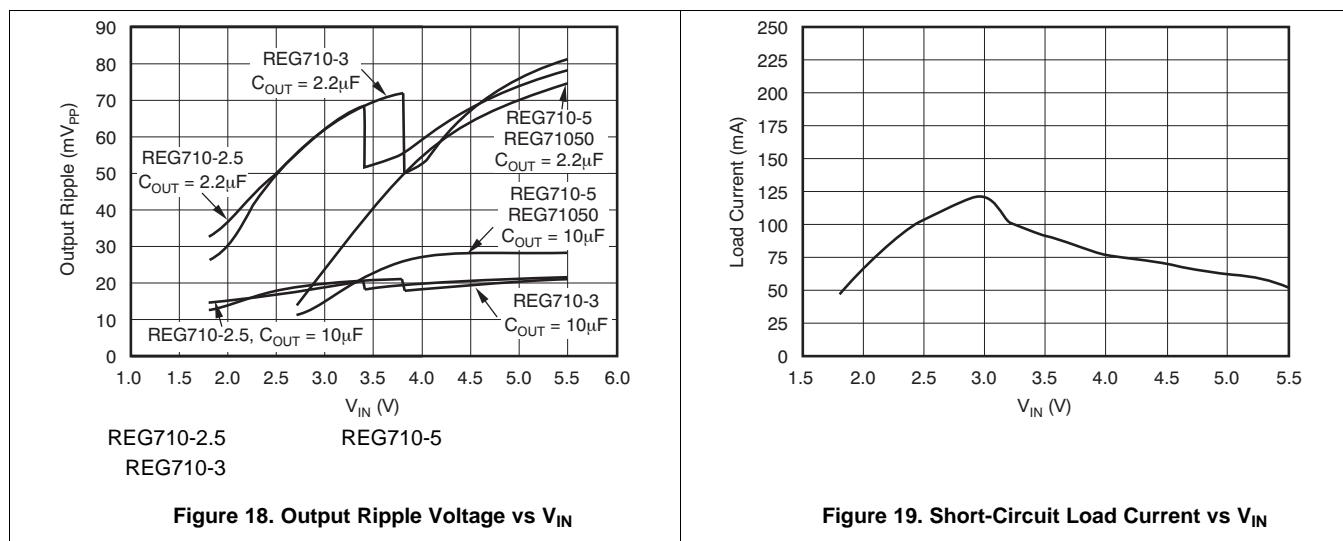
9.2.3 Application Curves


Figure 8. Efficiency vs V_{IN}

Figure 9. Efficiency vs Load Current

REG710-3.3V

Figure 10. Efficiency vs Load Current
Figure 11. Efficiency vs Load Current

REG71050, REG71055, REG710

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Figure 12. Efficiency vs Load Current

Figure 13. Efficiency vs Load Current

Figure 14. Load Transient Response

Figure 15. Line Transient Response

Figure 16. Output Ripple Voltage

Figure 17. Output Ripple Voltage vs V_{IN}



9.3 System Examples

9.3.1 1.8 V to 5.0 V With 10-mA Output Current

The REG710 family of charge pumps can be cascaded to reach higher output voltages, as shown in Figure 21.

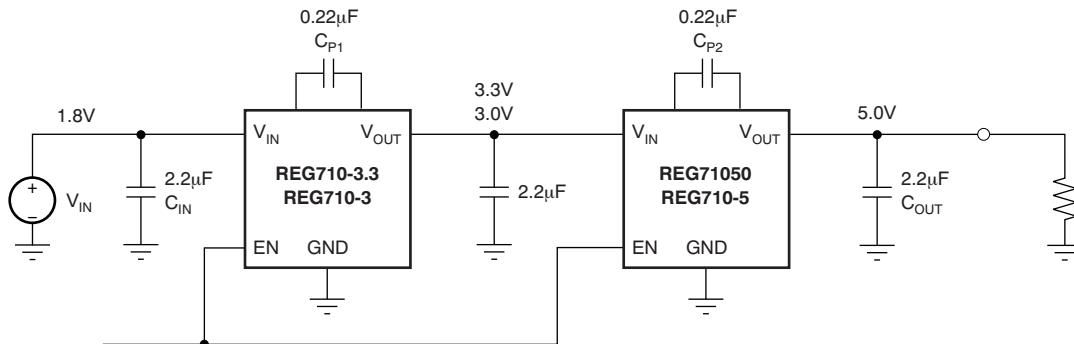


Figure 21. REG710 Circuit for Step-Up Operation From 1.8 V to 5 V With 10-mA Output Current

This application circuit operates from 1.8 V input voltage and generates 5 V output voltage supporting 10 mA load current.

Higher output voltages can be achieved when two REG710 devices are connected in cascade. When cascading two devices from the REG710 family, the relationship between output current and input voltage must be taken into account. (see [Electrical Characteristics](#)). In this case, REG710 can deliver a maximum of 10 mA. REG710-3.3 or REG710-3 can be used. A second charge pump, REG71050 or REG710-5, steps up the voltage from 3 V or 3.3 V to 5 V. Connect both Enable pins together.

System Examples (continued)

9.3.2 Doubling the Output Current

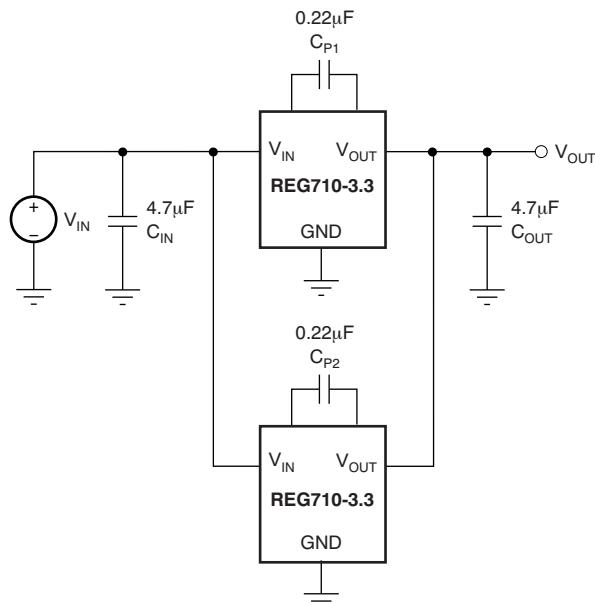


Figure 22. REG710 Circuit for Doubling the Output Current

When higher output currents are required, the REG710 family can be paralleled to double the output current. When paralleling two devices the relationship between output current and input voltage must be taken into account (see [Electrical Characteristics](#)).

This particular application can deliver 20 mA for an input voltage from 1.8 V to 5.5 V, or 60-mA output for an input voltage from 2.2 V to 5.5 V. The output voltage is 3.3 V.

9.3.3 Driving LEDs

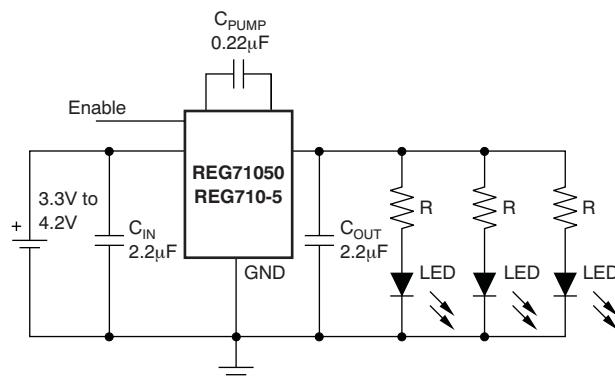


Figure 23. REG710 Circuit for Driving LEDs

The REG710 family can be used to drive LEDs. The feed forward voltage of the chosen LED determines the required output voltage. In this application, the charge pump can drive multiple LEDs up to 60 mA in total.

$$R = \frac{5V - V_{LED}}{I_{LED}} \quad (2)$$

10 Power Supply Recommendations

The input supply to the REG710 must have a current rating according to the supply voltage, output voltage and output current of the REG710.

11 Layout

11.1 Layout Guidelines

Large transient currents flow in the V_{IN} , V_{OUT} , and GND traces. To minimize both input and output ripple, keep the capacitors as close as possible to the regulator using short, direct circuit traces.

A suggested printed-circuit-board (PCB) routing is shown in Figure 24. The trace lengths from the input and output capacitors have been kept as short as possible.

11.2 Layout Example

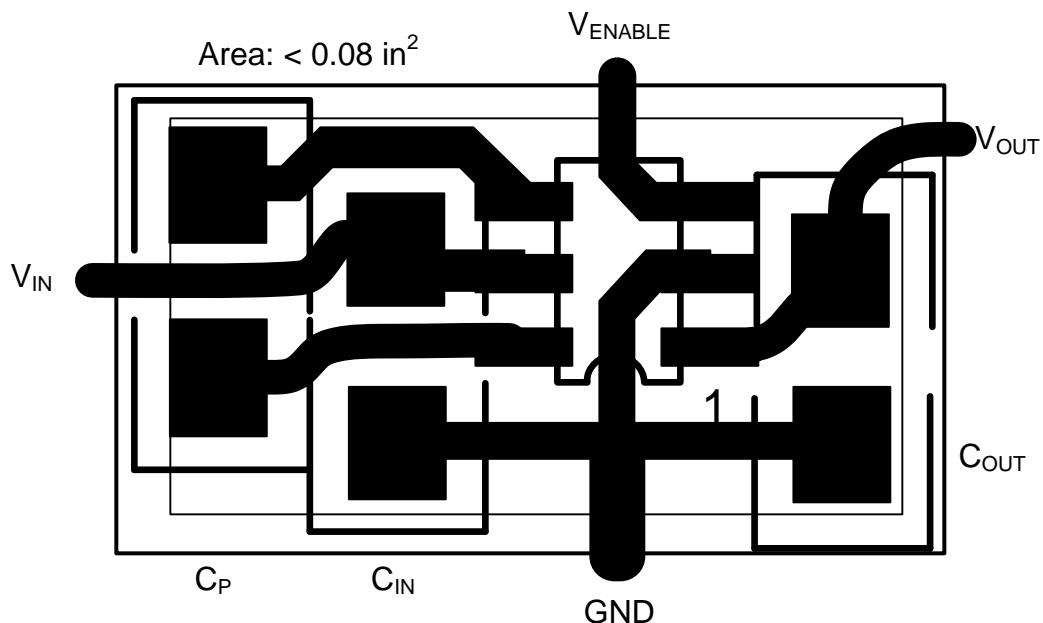


Figure 24. Suggested PCB Design for Minimum Ripple

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
REG71050	Click here				
REG71055	Click here				

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022 — TI Glossary.](#)

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG71050DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GAAI	Samples
REG71050DDCRG4	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GAAI	Samples
REG71050DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GAAI	Samples
REG71050DDCTG4	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GAAI	Samples
REG71050DRVVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CFF	Samples
REG71050DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CFF	Samples
REG71055DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10H	Samples
REG71055DDCRG4	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10H	Samples
REG71055DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10H	Samples
REG71055DDCTG4	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10H	Samples
REG710NA-2.5/250	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10G	Samples
REG710NA-2.7/250	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10F	Samples
REG710NA-3.3/250	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10C	Samples
REG710NA-3.3/250G4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10C	Samples
REG710NA-3.3/3K	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10C	Samples
REG710NA-3/250	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10D	Samples
REG710NA-3/3K	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10D	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG710NA-5/250	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10B	Samples
REG710NA-5/250G4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10B	Samples
REG710NA-5/3K	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10B	Samples
REG710NA-5/3KG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R10B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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www.ti.com

PACKAGE OPTION ADDENDUM

24-Aug-2018

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF REG71055 :

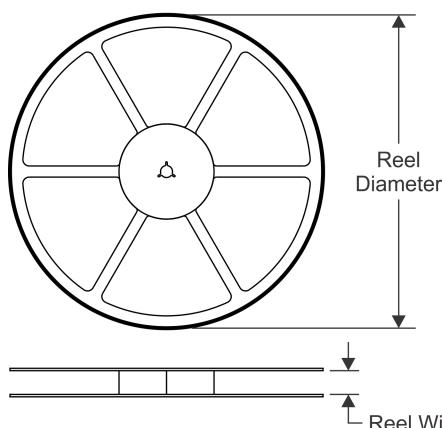
- Automotive: [REG71055-Q1](#)

NOTE: Qualified Version Definitions:

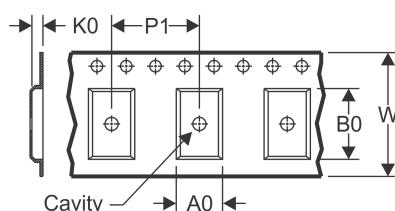
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

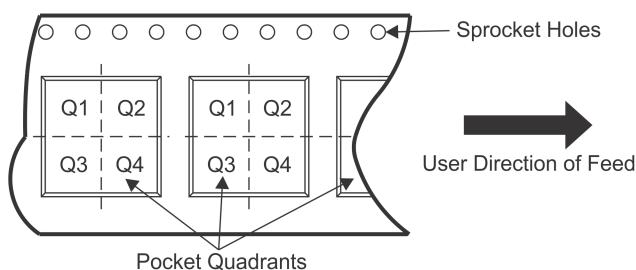


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

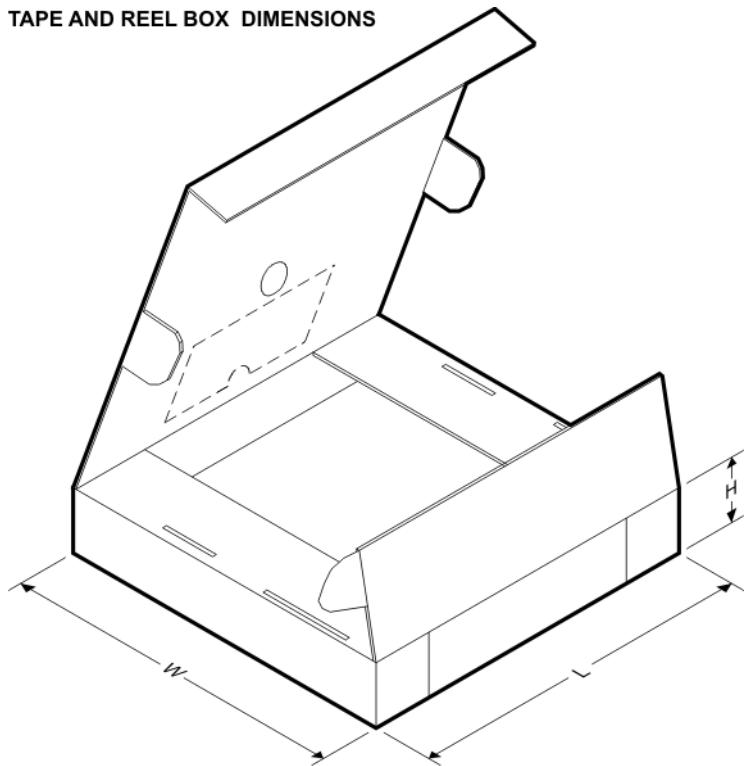
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG71050DDCR	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG71050DDCT	SOT-23-THIN	DDC	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG71050DRVVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
REG71050DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
REG71055DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG71055DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG710NA-2.5/250	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG710NA-2.7/250	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG710NA-3.3/250	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG710NA-3.3/3K	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG710NA-3.3/3K	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG710NA-3/250	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG710NA-3/250	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG710NA-3/3K	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG710NA-3/3K	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG710NA-5/250	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG710NA-5/250	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG710NA-5/3K	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG710NA-5/3K	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG71050DDCR	SOT-23-THIN	DDC	6	3000	203.0	203.0	35.0
REG71050DDCT	SOT-23-THIN	DDC	6	250	203.0	203.0	35.0
REG71050DRV	WSON	DRV	6	3000	195.0	200.0	45.0
REG71050DRV	WSON	DRV	6	250	195.0	200.0	45.0
REG71055DDCR	SOT-23-THIN	DDC	6	3000	203.0	203.0	35.0
REG71055DDCT	SOT-23-THIN	DDC	6	250	203.0	203.0	35.0
REG710NA-2.5/250	SOT-23	DBV	6	250	203.0	203.0	35.0
REG710NA-2.7/250	SOT-23	DBV	6	250	203.0	203.0	35.0
REG710NA-3.3/250	SOT-23	DBV	6	250	180.0	180.0	18.0
REG710NA-3.3/3K	SOT-23	DBV	6	3000	180.0	180.0	18.0
REG710NA-3.3/3K	SOT-23	DBV	6	3000	203.0	203.0	35.0
REG710NA-3/250	SOT-23	DBV	6	250	180.0	180.0	18.0
REG710NA-3/250	SOT-23	DBV	6	250	203.0	203.0	35.0

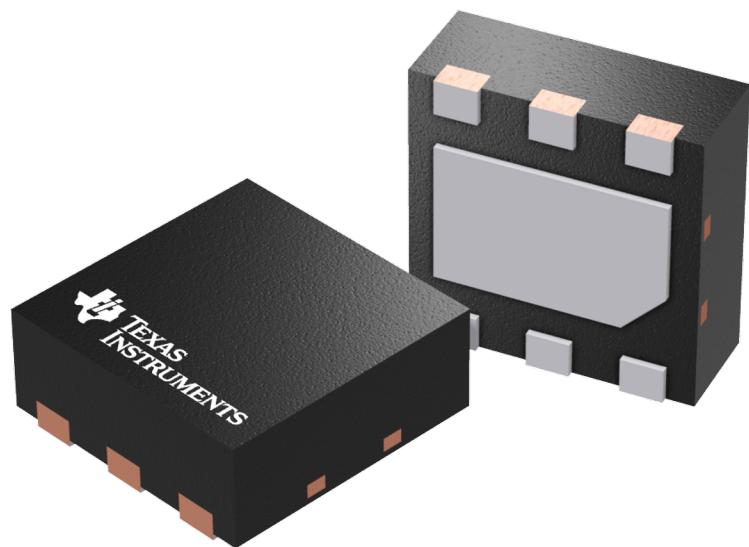
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG710NA-3/3K	SOT-23	DBV	6	3000	180.0	180.0	18.0
REG710NA-3/3K	SOT-23	DBV	6	3000	203.0	203.0	35.0
REG710NA-5/250	SOT-23	DBV	6	250	180.0	180.0	18.0
REG710NA-5/250	SOT-23	DBV	6	250	203.0	203.0	35.0
REG710NA-5/3K	SOT-23	DBV	6	3000	180.0	180.0	18.0
REG710NA-5/3K	SOT-23	DBV	6	3000	203.0	203.0	35.0

GENERIC PACKAGE VIEW

DRV 6

WSON - 0.8 mm max height

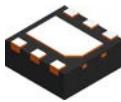
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4206925/F

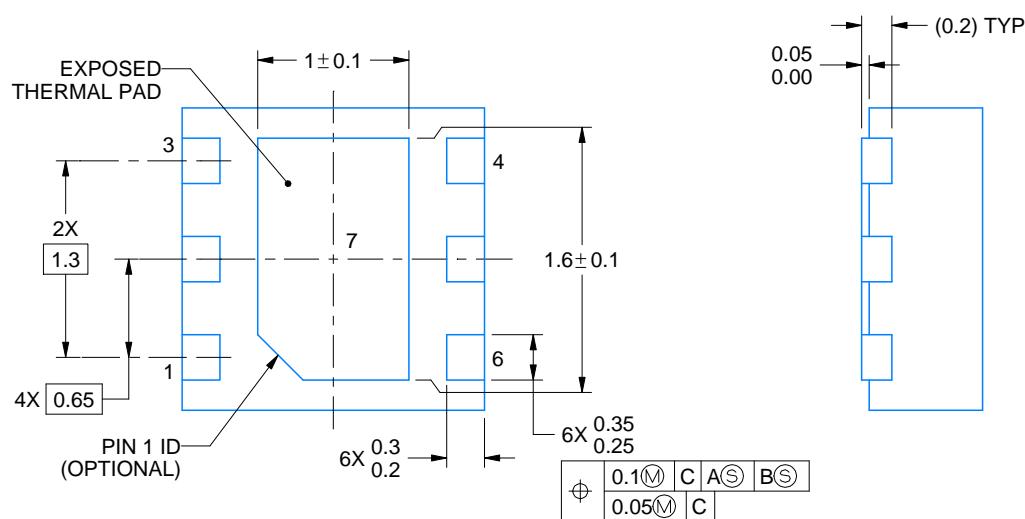
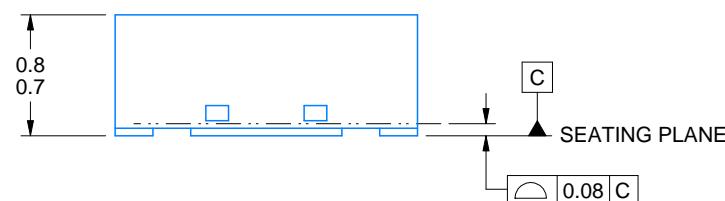
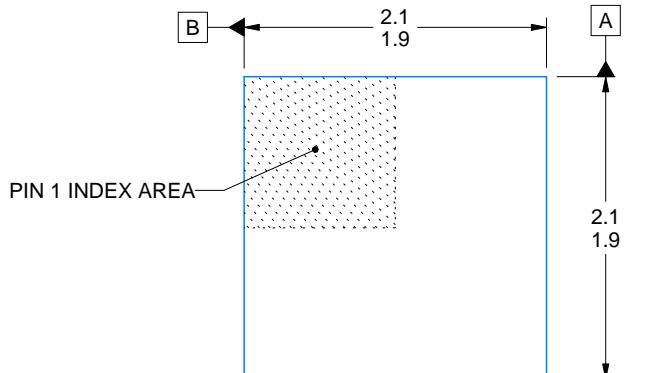
DRV0006A



PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222173/B 04/2018

NOTES:

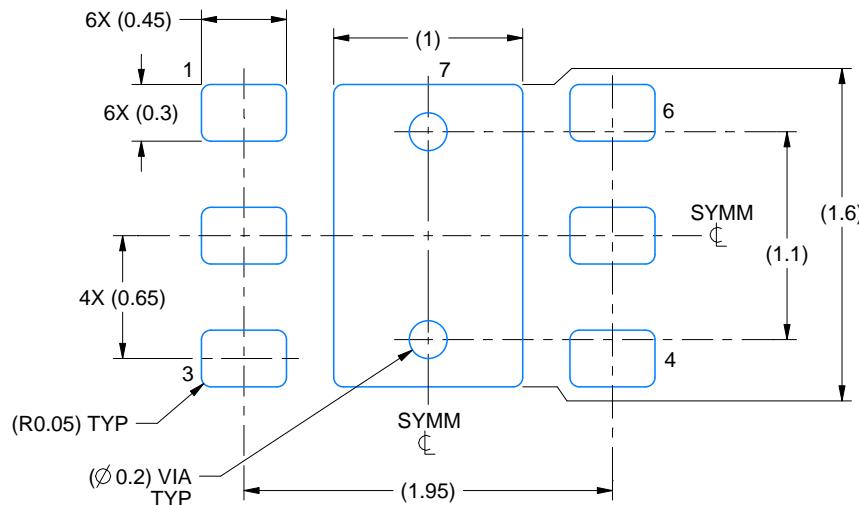
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DRV0006A

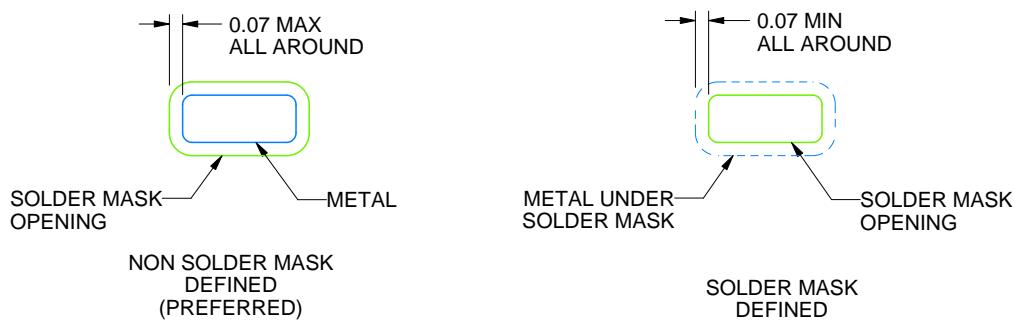
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE

SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

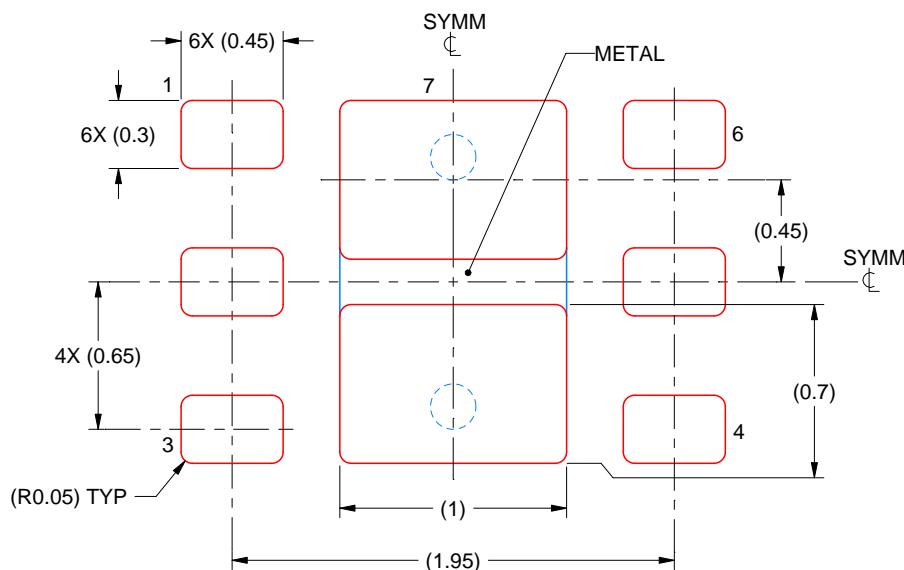
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

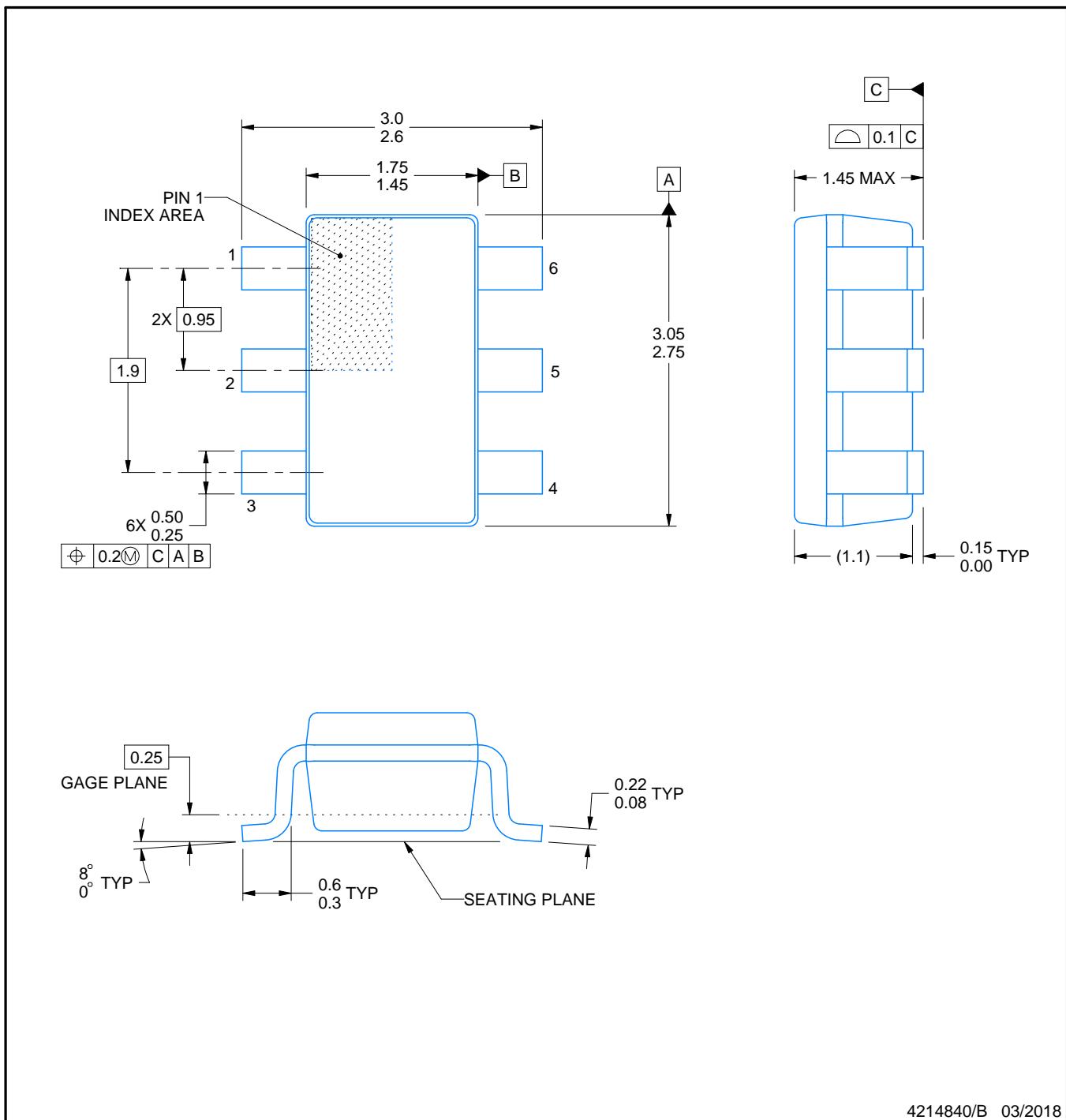
PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

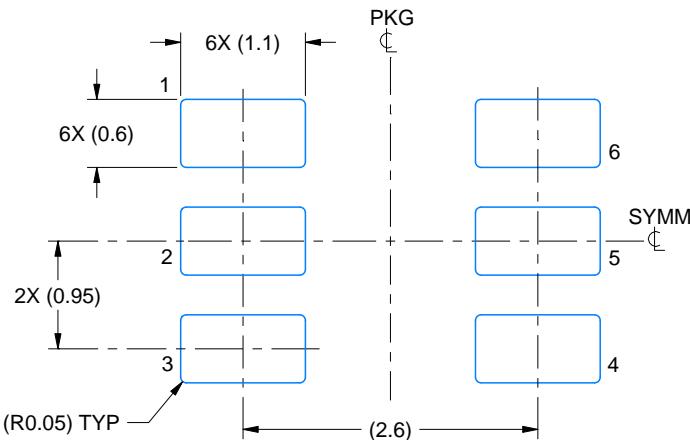
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

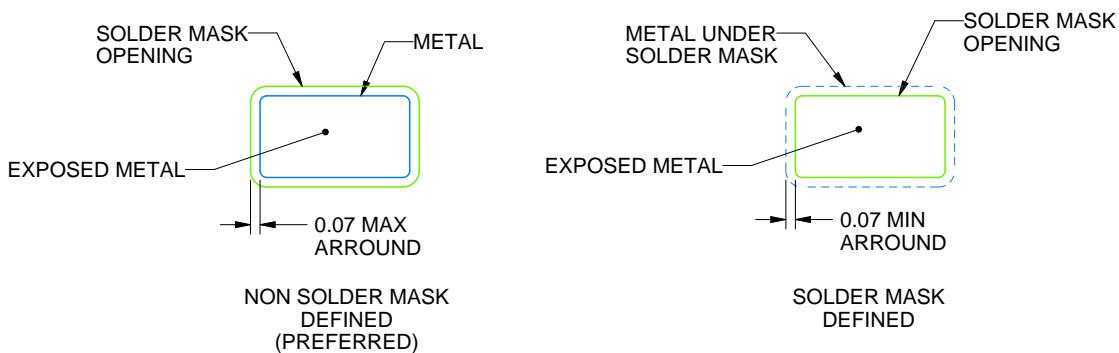
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

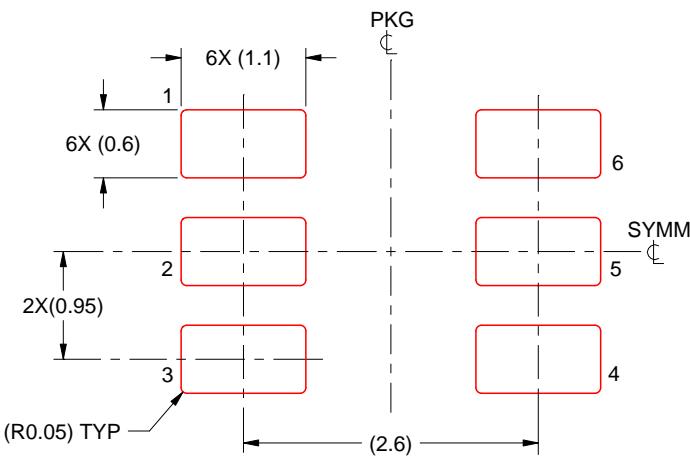
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

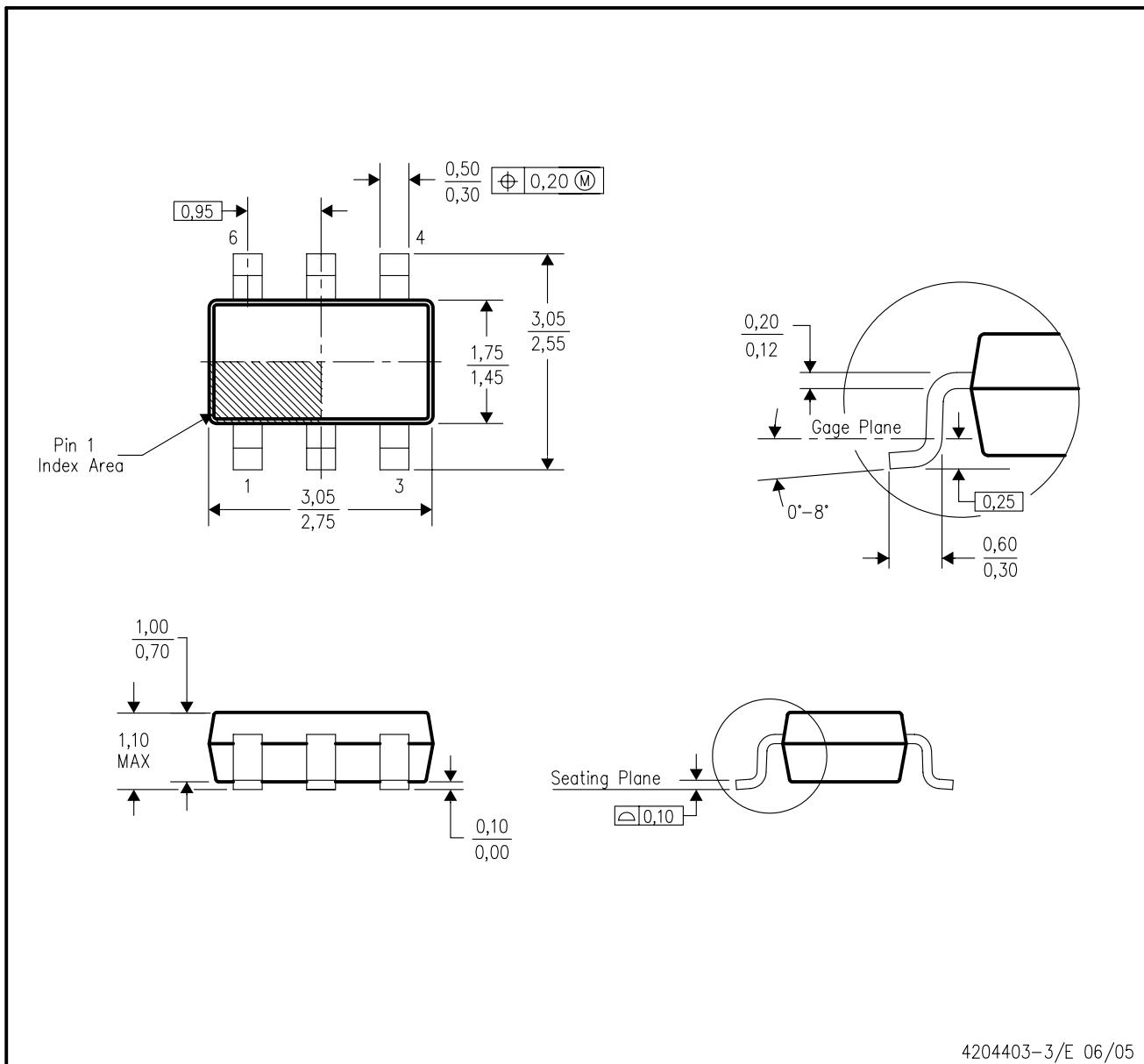
4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DDC (R-PDSO-G6)

PLASTIC SMALL-OUTLINE



4204403-3/E 06/05

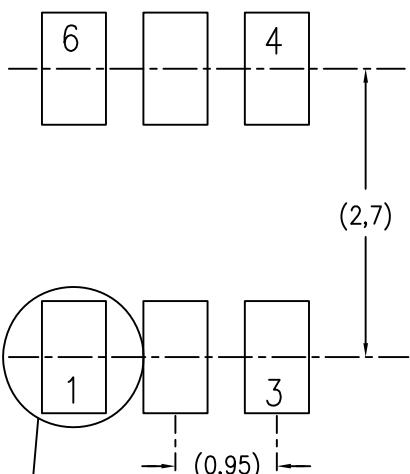
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-193 variation AA (6 pin).

LAND PATTERN DATA

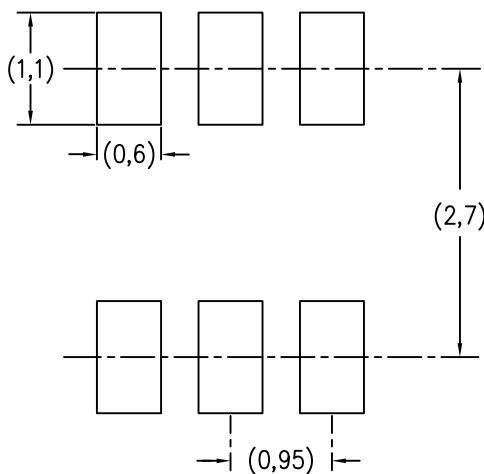
DDC (R-PDSO-G6)

PLASTIC SMALL OUTLINE

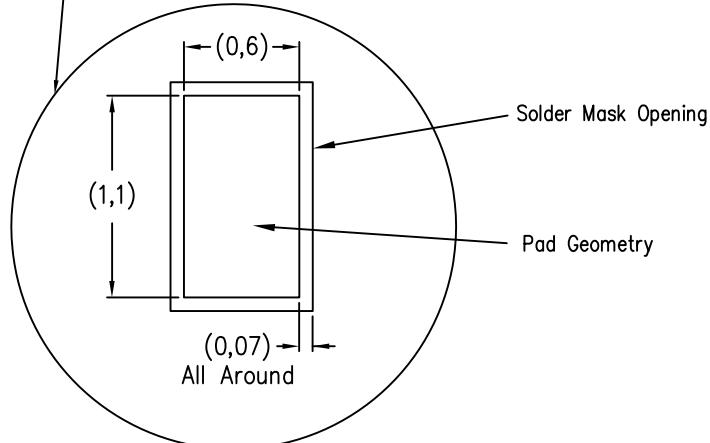
Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(Note D)



Example
Non Soldermask Defined Pad



4218552-3/A 05/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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