# A 13.56-Mbps Pulse Delay Modulation Based Transceiver for Simultaneous Near-Field Data and Power Transmission

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***Abstract*—A fully-integrated near-field wireless transceiver has been presented for simultaneous data and power transmission across inductive links, which operates based on pulse delay modulation (PDM) technique. PDM is a low-power carrier-less modulation scheme that offers wide bandwidth along with robustness against strong power carrier interference, which makes it suitable for implantable neuroprosthetic devices, such as retinal implants. To transmit each bit, a pattern of narrow pulses are generated at the same frequency of the power carrier across the transmitter (Tx) data coil with specific time delays to initiate decaying ringing across the tuned receiver (Rx) data coil. This ringing shifts the zero-crossing times of the undesired power carrier interference on the Rx data coil, resulting in a phase shift between the signals across Rx power and data coils, from which the data bit stream can be recovered. A PDM transceiver prototype was fabricated in a 0.35-$\mu$m standard CMOS process, occupying 1.6 $\mathrm{mm}^2$. The transceiver achieved a measured 13.56 Mbps data rate with a raw bit error rate (BER) of $4.3 \times 10^{-7}$ at 10 mm distance between figure-8 data coils, despite a signal-to-interference ratio (SIR) of −18.5 dB across the Rx data coil. At the same time, a class-D power amplifier, operating at 13.56 MHz, delivered 42 mW of regulated power across a separate pair of high-Q power coils, aligned with the data coils. The PDM data Tx and Rx power consumptions were 960 pJ/bit and 162 pJ/bit, respectively, at 1.8 V supply voltage.**

***Index Terms*—Implantable medical devices, impulse radio, inductive coupling, near-field transceiver, neuroprostheses, pulse delay modulation, wireless power transmission.**

## I. Introduction

INDUCTIVE links have been used extensively for wireless data and power transmission to a group of implantable medical devices (IMDs), known as neuroprostheses, which substitute sensory or motor modalities that are lost due to an injury or a disease [1]. Well known examples are the cochlear implants and visual prostheses, which need a large volume of data from external artificial sensors to the IMD [2]–[7]. We refer to this communication direction as the downlink. There are also IMDs, such as invasive brain-computer interfaces (iBCI), in which large amount of information is collected from the central nervous system and sent to outside of the body for further processing [8]–[13]. This is called the uplink. Most radio frequency identification (RFID) applications also utilize inductive links to not only energize the ultra-low power battery-less RFID tags, but also interrogate them to read their stored information [14]–[16].

The main challenges involved in designing transcutaneous data and power transmission links relate to the extremely limited space and power available to the IMD for establishing a wideband and robust connection. Because of the electro-magnetic field absorption in the tissue, which increases at a rate of carrier frequency squared, $f^2$, within the frequency bands of interest, high data rate must be achieved at the lowest possible carrier frequencies [17]. This requirement rules out the majority of established wideband wireless protocols, such as Bluetooth or WiFi, which operate at 2.4 GHz. There are also dedicated bands, such as the Medical Implant Communication Service (MICS), operating in the 402∼405 MHz range, which can only offer a limited bandwidth (300 kHz) [18]. Therefore, inductive coupling within 1–20 MHz band is the most common method that has been utilized for establishing wideband data telemetry and efficient power transmission to neuroprostheses.

The majority of modulation techniques that have been devised for near-field data transmission modify the amplitude, frequency, or phase of a sinusoidal carrier signal based on the data to be transferred across the inductive link. Amplitude shift-keying (ASK), frequency shift keying (FSK), load shift keying (LSK), and binary/quadrature phase shift keying (BPSK/QPSK) are examples of such methods [17], [19]–[24]. The use of power carrier signal along with these methods was attractive in the early IMDs because the same inductive link could be used for both power and data transmission.

In high-performance IMDs that require wider bandwidth, however, a separate power carrier from the data carrier is preferred because increasing the frequency of the high amplitude power carrier can lead to unsafe temperature elevation due to excessive power loss in the tissue. To achieve high power transfer efficiency (PTE) and high data rate, a high frequency carrier (>50 MHz) is required for the data link while the power carrier frequency, $f_p$, should be kept below 20 MHz [25]. This has led to the use of dual-carrier power/data links with each carrier linking a separate pair of coils [22]–[25].

A major challenge in dual-carrier designs is the cross-coupling between the two pairs of coils, which need to be minia-

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turized and co-located inside the IMD. In particular, the strong power carrier interference can dwarf the weak data signal on the receiver (Rx) side and make data recovery quite difficult, if not impossible. In other words, to achieve a low bit-error-rate (BER), a large signal-to-interference ratio (SIR) is needed. While innovative coil designs can help with reducing the coils' cross-coupling [26]–[28], it is still necessary to filter out the power carrier interference at the Rx input electronically at the cost of adding to the power consumption and complexity of the IMD [29]. Moreover, achieving high data rates via traditional modulation schemes requires power consuming frequency-stabilization RF circuits, such as phase-locked loops (PLL), which are not desired on the IMD side.

The data carrier was recently substituted with a series of narrow pulses in near-field, similar to far-field impulse radio ultra-wideband (IR-UWB), to further reduce the transmitter (Tx) power consumption and increase the data rate [30], [31]. We also demonstrated a pulse-based data transmission method, called pulse harmonic modulation (PHM), to further push the limits of power consumption and data rate in near-field telemetry links [32]–[34]. Unfortunately none of these methods are robust against strong power carrier interference, i.e. they operate only when the SIR at Rx input is high. Hence, there is a need for low-power, wideband, and low BER data transmission links that can withstand simultaneous power transmission within the small space available inside the IMD.

This was the motivation behind a new carrier-less data transmission scheme, called Pulse Delay Modulation (PDM), for near-field simultaneous data and power transmission. This is fundamentally different from the PHM technique, in which two pulses per bit are transmitted through the Tx coil in order to initiate and suppress ringing across a high-Q Rx LC-tank circuit and minimize crosstalk. The novel aspect in the PDM, however, is utilization of undesired power carrier interference across the Rx input to deliver the data bits. The proposed method saves the power and space needed for filtering out the power carrier interference on the Rx side, and at the same time enjoys power saving properties of the near-field IR-UWB, particularly on the Tx side, by eliminating the data carrier.

We recently described the PDM concept and theoretical basis in [35]. In this paper, we present the first fully-integrated PDM-based transceiver prototype, which block diagram is shown in Fig. 1. We have also characterized the PDM-based power/data link extensively, including BER measures in various conditions to demonstrate the PDM feasibility. The key improvements compared to the state-of-the-art in simultaneous wireless data and power transmission across an inductive link include: 1) increasing data rate, 2) reducing both Tx and Rx power consumption and die area, and 3) improving robustness against power carrier interference by reducing the required SIR to achieve the same BER. A brief overview of the PDM architecture with respect to the inductive links and its theory are included in Section II. Section III describes the PDM transceiver circuit. Section IV presents the PDM transceiver characterization and measurement results, followed by the discussion in Section V and concluding remarks in Section VI.

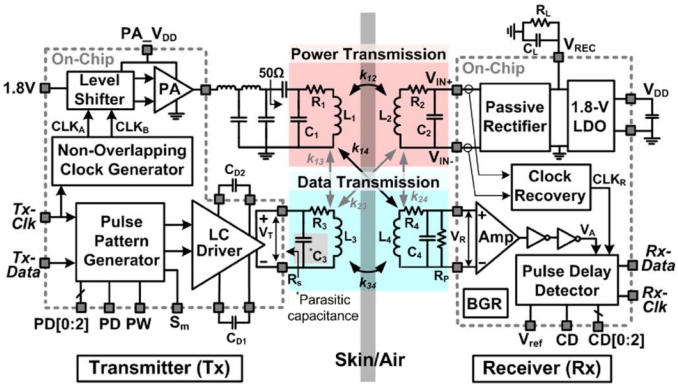


Fig. 1. Block diagram of the wireless power and data transmission circuit across a dual-band inductive link using the Pulse Delay Modulation (PDM) scheme. The first prototype PDM transceiver ASIC includes all the blocks inside the Tx and Rx dashed boxes. Direct ($k_{12}$ and $k_{34}$) and cross ($k_{13}$, $k_{14}$, $k_{23}$, and $k_{24}$) couplings across two pairs of coils are also presented.

## II. PDM Theory and Operation

### A. PDM Operation

Inside the PDM Tx, shown in the left dashed box in Fig. 1, a clock generator block creates two non-overlapping clocks from an external master clock signal, Tx-Clk, at the desired carrier frequency, $f_p$, for a class-D power amplifier (PA), which generates the power carrier signal at a desired output power level that can be adjusted by its supply voltage, $\mathrm{PA\_V_{DD}}$. The power carrier is delivered to $L_1$ after passing through a 50 Ω matching circuit to induce current in $L_2$. Using the same Tx-Clk, a pulse pattern generator (PPG) generates two narrow pulses, which are in sync with the power carrier and spaced by half a power carrier cycle, $T_p/2$, for each Tx-Data bit "1". No pulses are generated for Tx-Data bit "0". The LC driver circuit transmits each pulse across $L_3 - L_4$ data link. Each data pulse generates a decaying ringing response at a carrier harmonic frequency that the $\mathrm{L_4C_4}$-tank is tuned at. Within every data bit "1" period, ringing from these two pulses alter the timing of the power carrier interference zero-crossings across $\mathrm{L_4C_4}$-tank, which is induced through $k_{14}$ and $k_{24}$ cross couplings.

Inside the Rx block, which is the right dashed box in Fig. 1, a passive full-wave rectifier is followed by a 1.8 V low drop-out (LDO) regulator to provide the IMD power supply, $V_{DD}$. A clock recovery circuit extracts the internal IMD clock, $CLK_R$, from the received power carrier across $\mathrm{L_2C_2}$-tank. $V_R$ is the Rx input signal across $\mathrm{L_4C_4}$-tank and the superposition of the power carrier interference through $k_{14}$ and $k_{24}$ and PDM pulses through $k_{34}$. $V_R$ is amplified to create a square waveform, $V_A$, and then a pulse delay detector integrates the time shifts between $V_A$ and $CLK_R$ to recover the received data bit stream.

### B. Inductive Link Impulse Response

In the PDM data link in Fig. 1, since $k_{34}$ is relatively small, we can neglect the effect of the $\mathrm{L_4C_4}$-tank on the $\mathrm{L_3C_3}$-tank to simplify our equations. The pulse generator in Fig. 1 can be modeled by a voltage source in series with output resistance, $R_s$, driving $\mathrm{L_3C_3}$-tank. $\mathrm{L_4C_4}$-tank is tuned at $f_d$, while the

$L_3C_3$-tank can be either tuned at $f_d$ to increase the received signal amplitude or left at its self-resonance frequency (SRF) to reduce the Tx power consumption, in which case $C_3$ in Fig. 1 represents the parasitic capacitance of $L_3$ [33]. The inductive data link transfer function in the S-domain i.e. the ratio of the voltage across the $L_4C_4$-tank, $V_R$, to the LC driver output, $V_T$, can be described as, [See (1) at bottom of page] where all circuit parameters are the lumped elements in Fig. 1 and $M_{34} = k_{34} \times (L_3L_4)^{0.5}$ is the mutual inductance between $L_3$ and $L_4$. $H_{34}(s)$ is composed of two second order terms, one originating from the data Tx and the other from the data Rx tanks, each of which can be expressed as

$$\frac{1}{s^2+2\zeta\omega_n s+\omega_n^2}=\frac{1}{(s+s_1)(s+s_1^*)}, \quad s_1=\zeta\omega_n+j\omega_{nd}, 0\le\zeta<1 \tag{2}$$

where $\zeta$ is the damping ratio, $\omega_n$ is the natural frequency, and $\omega_{nd} = \omega_n \times (1-\zeta^2)^{1/2}$ is the natural damping frequency of the system. From (1) and (2), these second order system parameters can be expressed in terms of the lumped circuit elements in Fig. 1

$$\zeta_1\omega_{n_1}=\frac{(R_sR_3C_3+L_3)}{2R_sL_3C_3}\cong\frac{1}{2R_sC_3}, \omega_{n_1}^2=\frac{R_s+R_3}{R_sL_3C_3}\cong\frac{1}{L_3C_3}, \tag{3}$$

$$\zeta_2\omega_{n_2}=\frac{R_4}{2L_4}, \omega_{n_2}^2=\frac{1}{L_4C_4}. \tag{4}$$

Assuming both second order systems are under damped, $\zeta_1 < 1$ and $\zeta_2 < 1$, which is often the case for LC-tanks used in data telemetry links, (1) can be rearranged as

$$H_{34}(s)=\frac{M_{34}s}{R_sL_3C_3(s+s_1)(s+s_1^*)\times L_4C_4(s+s_2)(s+s_2^*)}, \quad s_j=\zeta_j\omega_{n_j}+j\omega_{nd_j}, j=1,2. \tag{5}$$

Now we can break $H_{34}(s)$ up into the sum of its first order components

$$H_{34}(s)=\left[\frac{A_1}{(s+s_1)}+\frac{A_1^*}{(s+s_1^*)}+\frac{A_2}{(s+s_2)}+\frac{A_2^*}{(s+s_2^*)}\right] \tag{6}$$

where

$$A_1=\frac{-M_{34}s_1}{R_sL_3C_3(s_1^*-s_1)\times L_4C_4(s_2-s_1)(s_2^*-s_1)}=a_1+jb_1, \tag{7}$$

$$A_2=\frac{-M_{34}s_2}{R_sL_3C_3(s_1-s_2)(s_1^*-s_2)\times L_4C_4(s_2^*-s_2)}=a_2+jb_2 \tag{8}$$

and apply the inverse Laplace transform to find the impulse response for the inductive link

$$h_{34}(t)=2e^{-\zeta_1\omega_{n_1}t}(a_1\cos(\omega_{nd_1}t)+b_1\sin(\omega_{nd_1}t)) +2e^{-\zeta_2\omega_{n_2}t}(a_2\cos(\omega_{nd_2}t)+b_2\sin(\omega_{nd_2}t)). \tag{9}$$

As shown in more detail in [32], this response is a ringing, which envelope builds up rapidly with $1/\zeta_1\omega_{n1}$ but decays slowly with $1/\zeta_2\omega_{n2}$.

The impulse response of the power interference link due to $k_{14}$, i.e. $H_{14}(s)$, can be found from (5) by substituting $L_3C_3$-tank circuits parameters and $M_{34}$ with $L_1C_1$-tank parameters and $M_{14}$, respectively. Because the voltage across $L_1$ is much larger than that of $L_2$, we can safely neglect the effect of $L_2C_2$-tank on the $L_4C_4$-tank through $k_{24}$ [32]. Therefore, the amplitude and phase of the power carrier interference across the $L_4C_4$-tank, i.e. the power carrier component of $V_R$, can be calculated using $|H_{14}(j\omega_p)|$ and $\angle H_{14}(j\omega_p)$, respectively, where $\omega_p = 2\pi f_p$.

### C. Pulse Delay Modulation

Using the inductive link impulse responses from Section II-B, one can calculate $V_R$ in Fig. 1. Instead of a data carrier for each data bit "1", two narrow pulses, equal but opposite in amplitudes with $t_{pw} \le \sqrt{2}/\pi f_d$ and spaced by $T_p/2 = 1/2f_p$, are transmitted across $L_3C_3$-tank. These pulses initiate ringing patterns across $L_4C_4$-tank based on (9), as shown in Fig. 2. To minimize inter-symbol-interference (ISI) within consecutive "1"s, it is important for these ringing to dampen quickly. It can be seen from (9) and (4) that increasing $\zeta_2\omega_{n2}$, which is proportional to $R_4$, helps damping the ringing faster. Therefore, $Q_4$ of the $L_4C_4$-tank in Fig. 1 is intentionally reduced by increasing $R_4$.

When present, the abovementioned data pulse ringing change the shape of the received power carrier interference across $L_4C_4$-tank. To facilitate the detection of these changes, our solution is to select the timing of the data pulses at $V_T$ in a way that they alter the zero-crossing times of the interfering sinusoidal power carrier, which are the most sensitive points of the signal to an external disturbance. Hence, the Tx pulses for every bit "1" are applied at the beginning and in the middle of every bit period in sync with the power carrier, and after a specific delay, $t_d$, which is selected such that the voltage peaks of the data ringing at $V_R$ coincide with the original zero-crossing times of the power carrier interference at $V_R$. The result is a

$$H_{34}(s)=\frac{M_{34}s}{(R_sL_3C_3s^2+(R_sR_3C_3+L_3)s+R_s+R_3)(L_4C_4s^2+R_4C_4s+1)} \tag{1}$$

TABLE I
MEASURED POWER AND DATA COILS SPECIFICATIONS

| Link | Coil | Size (mm) | #Turns | Line Width (mm) | $L$ (nH) | $^{**}R$ (Ω) | $f$ (MHz) | $Q$ | $SRF$ (MHz) | Mutual Coupling $(k)$ $\times 10^{-3}$ | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | $L_1$ | $L_2$ | $L_3$ | $L_4$ |
| Power | $L_1$ | 32 × 32 | 5 | 2 | 500 | 0.5 | 13.56 | 85.2 | 116 | - | 37 | 9 | 6.4 |
| | $^{*}L_2$ | 10 × 10 | 3 | 0.255 | 195 | 0.34 | 13.56 | 48.8 | 237 | 37 | - | 4.2 | 8.5 |
| Data | $L_3$ | 30 × 30 | 1 | 1 | 165 | 0.48 | 50 | 108 | 255 | 9 | 4.2 | - | 19 |
| | $L_4$ | 10 × 10 | 1 | 0.4 | 56.8 | 0.44 | 50 | $^{+}$40.5 | 550 | 6.4 | 8.5 | 19 | - |

$^{*}$ $L_2$ was an AWG30 wire-wound coil.
$^{**}$ From measurements at the operating frequency, $f$.
$^{+}$ $Q_4$ was reduced to 5 by adding $R_P = 100\ \Omega$.

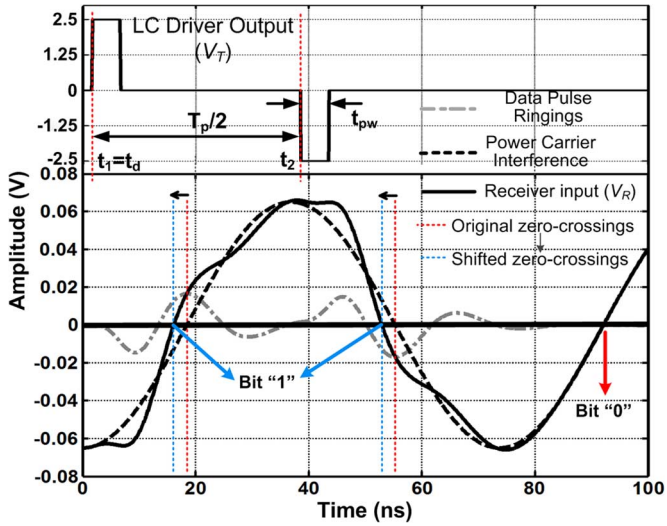


Fig. 2. PDM key waveforms simulated in MATLAB. On the Tx side, two narrow pulses have been generated for each data bit "1" after an adjustable delay of $t_d$ with respect to the power carrier. Each pulse creates a ringing across $L_4C_4$-tank in Fig. 1 that shifts the zero-crossing times of the induced power carrier interference. It can be seen that the superimposed signal, which is labeled as $V_R$, has 2.5 ns zero-crossing time shift to left for bit "1" and no shift for bit "0". The inductive link specifications can be found from Table I.

shift in the $V_R$ zero-crossings in a certain direction for bit "1", as shown Fig. 2. The PPG block in Fig. 1 sets $t_d$ at

$$t_d = nT_p + \frac{\angle H_{14}(j\omega_p)}{\omega_p} - \frac{\angle H_{34}(j\omega_d)}{\omega_d} - \frac{3}{4f_d} + t_{PA} \quad (10)$$

where $n$ is an integer number, $\angle H_{14}(j\omega_p)/\omega_p$ and $\angle H_{34}(j\omega_d)/\omega_d$ are the delays for power carrier interference and data pulses from $L_1$ to $L_4$ and $L_3$ to $L_4$, respectively, and $t_{PA}$ is the total delay from the Tx-Clk to the power carrier across $L_1C_1$-tank in Fig. 1.

Fig. 2 shows the transient simulation results of the simplified PDM model in Fig. 1, based on (9) and the dual-carrier inductive link specifications in Table I. The power carrier across $L_1C_1$-tank in this simulation was a 50 $V_{P-P}$ sinusoid with 90° phase shift at $f_p = 13.56$ MHz. $V_T$ in Fig. 1 is shown on the top trace in Fig. 2 with two $t_{pw} = 5$ ns pulses with equal but opposite 2.5 V amplitudes at $t_1 = t_d = 1.6$ ns and $t_2 = t_d + T_p/2 = 38.4$ ns delay times with respect to the negative peak of the power carrier interference. The resulting signal across $L_4C_4$-tank, shown in dashed gray, demonstrate how these $f_d = 50$ MHz ringing dampen rapidly by $t =\sim 35$ ns and

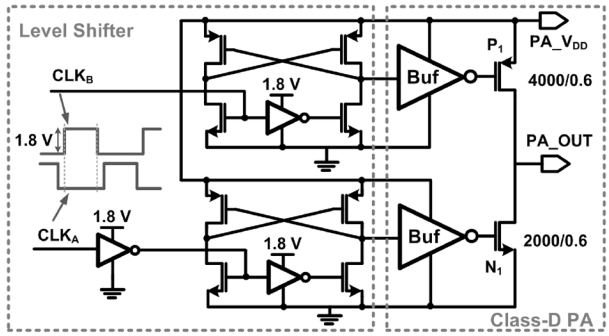


Fig. 3. Schematic diagram of the class-D PA followed by the level shifter. The maximum PA output power is 340 mW when $\mathrm{PA\_V_{DD}} = 5$ V.

$t =\sim 70$ ns before the beginning of the next pulse due to the lowered $Q_4 = 5$. See the inductive link specifications in Table I.

Without data pulse ringing, the induced power carrier interference across $L_4C_4$-tank is a clean sinusoid, which is the dashed black waveform labeled as Power Carrier Interference in Fig. 2. The actual received signal, $V_R$, however, which is shown in solid black, results from the superposition of the data and power components. It can be seen that PDM has shifted the zero-crossings of the superimposed waveform, $V_R$, for a bit "1" by 2.5 ns to the left from $t_{zc1(0)} = 18.4$ ns and $t_{zc2(0)} = 55.3$ ns in the dashed waveform to $t_{zc1(1)} = 15.9$ ns and $t_{zc2(1)} = 52.8$ ns in the solid waveform, respectively.

Considering that $L_1C_1$ and $L_2C_2$ tanks are both high-Q and tuned at $f_p$ for efficient power transmission, the induced power carrier on $L_2C_2$-tank is much stronger than that from $L_3C_3$ and $L_4C_4$ tanks. Therefore, the transmitted data pulses do not have any noticeable effects on the power link and the recovered clock signal, $CLK_R$. Since no pulses are transmitted for data bit "0", the delay between zero-crossings of signals across $L_4C_4$ and $L_2C_2$ tanks would be a clear representation of data bit "1", which can be detected by the pulse delay detector circuit in Fig. 1 to recover the serial data bit stream, Rx-Data.

Any detuning of power and data LC-tank circuits in Fig. 1 could affect data recovery in Rx by changing $\angle H_{14}(j\omega_p)$, $\angle H_{34}(j\omega_d)$, and $f_d$, which determine the timing of zero crossings of the power carrier interference and voltage peaks of the data pulse ringing. According to (10), such variations could be compensated by $t_d$, which is accurately adjustable.

## III. PDM TRANSCEIVER ARCHITECTURE

The PDM transceiver prototype was designed to operate at 13.56 MHz within the industrial-scientific-medical (ISM) band.

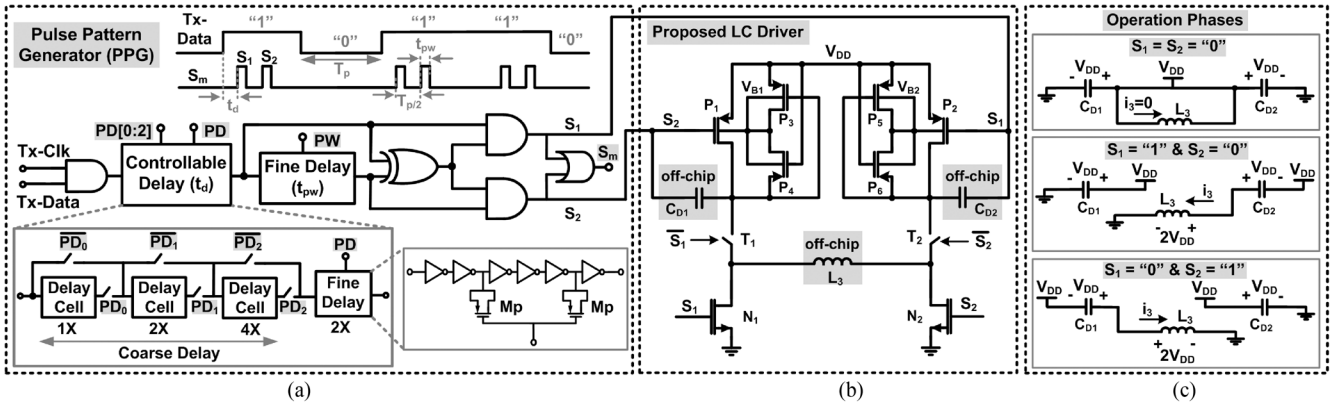


Fig. 4. Schematic diagram of the data Tx block in the PDM transceiver. (a) The pattern pulse generator (PPG) block generates two pulses with $T_p/2$ spacing, which width ($t_{pw}$) and delay ($t_d$) are adjustable. (b) The LC driver applies narrow pulses across $L_3$, which amplitudes are twice the conventional H-bridge drivers [30]. (c) Three operating phases of the proposed LC driver. $C_{D1}$ and $C_{D2}$ are 100 pF off-chip capacitors.

It should be noted that regulatory compliance due to Rx ringing at $f_d = 50$ MHz is not a concern in the near-field short-range communications, where the transmission range is short in comparison to far-field communications. Although, in this paper we have configured the transceiver for downlink, it can also be used for uplink.

### A. Transmitter Design

*1) Power Transmitter:* In the PDM power Tx, a class-D PA, which schematic diagram is shown in Fig. 3, drives $L_1$ through a 50 Ω matching circuit. To compensate for the mismatch between the signal paths that drive output stage transistors, $\mathrm{N}_1$ and $\mathrm{P}_1$, the PA is driven by a pair of non-overlapping clocks. This avoids instantaneous large currents in $\mathrm{N}_1$ and $\mathrm{P}_1$, which operate as switches with 4 Ω on resistance. The PA supply, $\mathrm{PA\_V_{DD}}$, is adjustable from 1.8 V to 5 V to control the PA output power up to 340 mW. A pair of level shifters at the PA input converts the non-overlapping clocks from 1.8 V to the $\mathrm{PA\_V_{DD}}$ level.

*2) Data Transmitter:* The PDM data transmitter, which schematic is shown in Fig. 4, includes a pulse pattern generator (PPG) and an LC driver. During each $T_p$ period, the PPG block in Fig. 4(a) generates two pulses ($S_1$ and $S_2$) with adjustable width and delay for data bit "1", which are spaced at $T_p/2$, and none for bit "0". Therefore, the data rate $(DR)$ in this PDM implementation is always the same as $f_p$. The width of data pulses, $t_{pw}$, is continuously adjustable from 3–8 ns via the PW input node. The data pulse delay, $t_d$, is accurately adjustable from 5–71 ns to compensate for process variations by a combination of a coarse delay, controlled by three binary-weighted bits $(\mathrm{PD}_{0-2})$ from 0–56 ns with 8 ns steps, and a fine delay, controlled by an analog input (PD), from 5–15 ns. The coarse delay is generated by accumulating propagation delays of a series of capacitively-loaded inverters. The parasitic capacitances of two PMOS transistors, $\mathrm{M_P}$, which vary with their gate voltage, PD, generate the fine delay. $S_1$ and $S_2$ are combined in an OR gate to generate $S_m$ in Fig. 4(a), which is used for monitoring.

Fig. 4(b) shows the schematic diagram of the novel LC driver, which is capable of quadrupling the supply voltage, $V_{DD}$, across the Tx data coil, $L_3$, which is twice the conventional H-bridge drivers. For each data bit "0", $S_1 = S_2 = 0$, $\mathrm{T}_{1,2}$ and $\mathrm{P}_{1,2}$ turn on, and $\mathrm{N}_{1,2}$ turn off. Therefore, both $L_3$ nodes are connected to $V_{DD}$ and off-chip $C_{D1}$ and $C_{D2}$ capacitors are charged to $V_{DD}$ via $\mathrm{P}_{1,2}$, as shown on the top of Fig. 4(c). In this condition, no current passes through $L_3$ and no voltage change is induced across the $\mathrm{L_4C_4}$-tank. For each data bit "1", after a delay of $t_d$, $S_1$ toggles to "1" for $t_{pw}$, during which $\mathrm{P}_2$ and $\mathrm{T}_1$ turn off, $\mathrm{N}_1$ turns on, and $C_{D2}$ is in series with $L_3$ while the left node of $L_3$ is connected to ground via $\mathrm{N}_1$. Therefore, as shown in the middle of Fig. 4(c), the voltage across $L_3$ increases to $2 \times V_{DD}$ and its current, $i_3$, starts ramping up (from right to left) at a rate of $di_3/dt = 2 \times V_{DD}/L_3$, if we ignore the voltage drops across $\mathrm{N}_1$ and $\mathrm{T}_2$ in this simplified analysis. The $di_3/dt$ is responsible for inducing a voltage across $\mathrm{L_4C_4}$-tank, which is the data part of $V_R = M_{34} di_3/dt \propto 2 \times V_{DD}$. To end the first pulse, $S_1$ is toggled back to "0", at which time $\mathrm{T}_1$ shorts the left node of $L_3$ to $V_{DD}$ and provides a path for $i_3$ to return back to zero without causing undesired oscillations. After a delay of $T_p/2$, $S_2$ toggles to "1", resulting in a current pulse in $L_3$, similar to that of $S_1$ but in the opposite direction (left to right), as shown in the bottom of Fig. 4(c). In the driver circuit, $\mathrm{P}_{3-6}$ dynamically bias the bulks of $\mathrm{P}_{1,2}$ to the highest voltage to avoid current flow in the bulk.

By doubling the voltage across $L_3$ in each direction, the proposed LC driver can improve the communication range and robustness of inductively powered telemetry links, especially those designed in low-voltage technology nodes. It should be noted that in this design, since $S_2$ is already out-of-phase with respect to $S_1$, resulting in $i_3$ flowing in opposite directions, the induced data pulse ringing across $\mathrm{L_4C_4}$-tank also have opposite polarity, and change the zero-crossing times of power carrier interference in the same direction, as shown in Fig. 2.

### B. Receiver Design

*1) Power Management:* Fig. 5 shows the schematic diagram of the full-wave passive rectifier in the PDM power receiver with self-threshold-cancellation scheme [36]. In this scheme, initially $V_{REC}$ reaches $V_{INR} - V_{Th(\mathrm{P2})}$ through $\mathrm{P}_2$, leading to $V_C = V_{REC} - V_{Th(P3)} = V_{INR} - 2V_{Th(\mathrm{P2,3})}$. Since $V_{SG(\mathrm{P1})} = V_{INR} - V_C = 2V_{Th(\mathrm{P2,3})} > V_{Th(\mathrm{P1})}$, $\mathrm{P}_1$ is pushed into triode, and $V_{REC}$ is charged up until $V_C$ becomes $V_{INR} - V_{Th(\mathrm{P1})}$. Therefore, $V_{REC}$ finally reaches $V_{INR} - V_{Th(\mathrm{P1})} + V_{Th(\mathrm{P3})}$, which means that $\mathrm{P}_{1-3}$ play the role of a

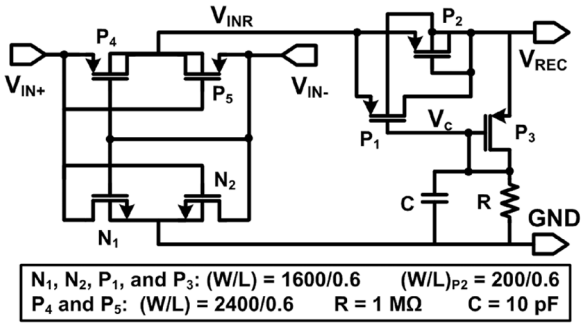


Fig. 5. Schematic diagram of the full-wave passive rectifier with self-threshold-cancellation scheme [36]. In this circuit, $\mathrm{P}_{1-3}$ play the role of a diode with effective voltage drop of $V_{Th(P1)} - V_{Th(P3)}$, which improves the PCE.

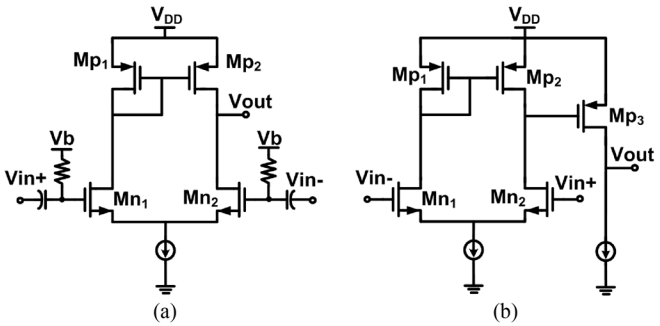


Fig. 7. Schematic diagrams of (a) Rx amplifier in Fig. 1 with 22.5 dB gain at $f_d = 50$ MHz. (b) Rx comparator in Fig. 6. The static power consumptions of the amplifier and comparator are 156 $\mu$A and 127 $\mu$A, respectively.

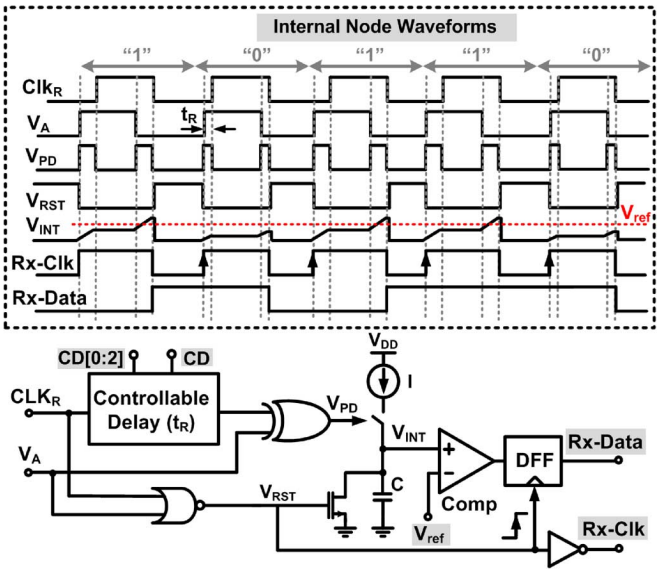


Fig. 6. Schematic diagram of the pulse delay detector with its operating waveforms to recover the data bit stream and clock. Rx-Data is ready to be sampled at the rising edge of the Rx-Clk as shown in the waveforms. A small delay $(t_R)$ between $CLK_R$ and $V_A$ is required to set the integrator output, $V_{INT}$, within the input common mode range of the comparator. $t_R$ is continuously adjustable from 5–71 ns to compensate for process variations by a combination of fine and coarse delays, controlled by CD and CD[0:2], respectively.

diode with effective voltage drop of $V_{Th(\mathrm{P1})} - V_{Th(\mathrm{P3})}$. This significant reduction in the threshold voltage improves the power conversion efficiency (PCE). $\mathrm{N}_1$, $\mathrm{N}_2$, $\mathrm{P}_4$, and $\mathrm{P}_5$ are used for full-wave rectification.

*2) Data Receiver:* In the data Rx block in Fig. 1, $V_R$ is amplified by a high gain amplifier followed by two inverters to create a square waveform, $V_A$. A pulse delay detector is then used to detect the phase shift (delay) between $V_A$ and the recovered clock from the $\mathrm{L_2C_2}$-tank $(CLK_R)$ to detect "1"s and "0"s in the data bit stream.

Fig. 6 shows the schematic diagram of the pulse delay detector with its key internal node waveforms. First, the delay between $V_A$ and $CLK_R$ is detected by an XOR gate, which is represented by $V_{PD}$. During one $T_p$, an integrator accumulates the energy inside $V_{PD}$ pulses by charging a capacitor, $C = 1.1$ pF, with $I = 100$ $\mu$A. The integrator output, $V_{INT}$, is then compared with an externally-adjustable reference voltage, $V_{ref}$, to detect data bit "1". $V_{ref}$ is adjusted such that the integrator output is greater than $V_{ref}$ for "1"s and smaller than $V_{ref}$ for "0"s. $V_A$ and $CLK_R$ are also combined in a NOR gate to generate the reset signal, $V_{RST}$, to discharge $C$ and prepare the integrator for the next data bit. To recover short pulses at the comparator output, a D-type flip flop is clocked at the rising edge of $V_{RST}$. Therefore, Rx-Data is ready to be sampled at the rising edge of the Rx-Clk.

Figs. 7(a) and 7(b) show the schematic diagrams of the PDM Rx amplifier in Fig. 1 and the high speed comparator in Fig. 6, respectively. Because nMOS differential pair is used in the comparator, a small delay between $CLK_R$ and $V_A$, $t_R$ in Fig. 6 inset, is required for the data bit "0" to set $V_{INT}$ within the input common mode range (ICMR) of the comparator. A controllable delay with a circuit diagram identical to the one in Fig. 4 generates $t_R$. The amplifier gain is 22.5 dB at $f_d = 50$ MHz and the static power consumptions of the amplifier and comparator are 156 $\mu$A and 127 $\mu$A, respectively.

## IV. Measurement Results

The PDM transceiver prototype, shown in Fig. 8, was fabricated in a 0.35-$\mu$m 2P4M standard CMOS process, occupying 1.6 $\mathrm{mm}^2$ of chip area. Two PDM chips were used in our experimental setup, shown in Fig. 9. They were wirebonded to QFN packages mounted on 2-layer FR4 printed circuit boards (PCBs). Each PCB included a planar figure-8 coil for data transmission as shown in Fig. 9 inset [26]. The geometries of a printed spiral coil in the Tx and a wire-wound coil in the Rx were optimized at 13.56 MHz for power transmission [37]. $L_1$ and $L_2$ were glued onto $L_3$ and $L_4$, respectively, following careful alignment to minimize undesired cross couplings between power and data coils, $k_{13}$ and $k_{24}$. The specifications of power and data coils are summarized in Table I.

At $\mathrm{PA\_V_{DD}} = 5$ V, which is the maximum voltage in this process, the class-D PA delivered 340 mW to a 50 $\Omega$ load with measured 61.8% power efficiency at $f_p = 13.56$ MHz. Fig. 10(a) shows the passive rectifier measured input and output voltage waveforms when loaded by $C_L = 10$ $\mu$F and $R_L = 0.4$ k$\Omega$. In this condition, for $V_{REC} = 2.5$ V, the peak of the 13.56 MHz carrier was 3.6 V. Fig. 10(a) also shows the regulator output, $V_{DD} = 1.8$ V, across a 10 $\mu$F capacitor. The maximum ripple on $V_{DD}$ was 50 mV, which was acceptable in our digital-based Rx. Fig. 10(b) shows the rectifier measured

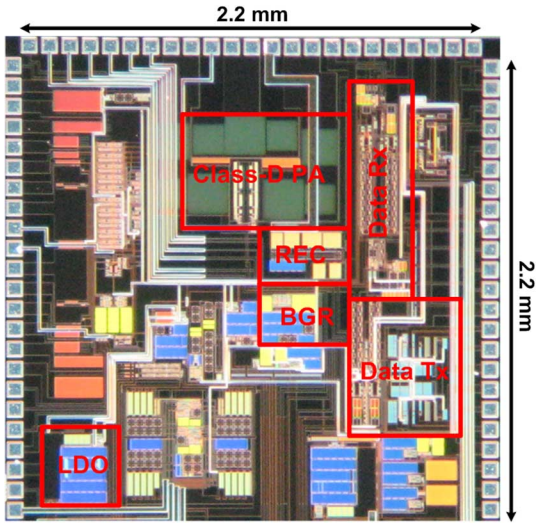


Fig. 8. PDM transceiver chip microphotograph occupying 1.6 $\mathrm{mm}^2$.

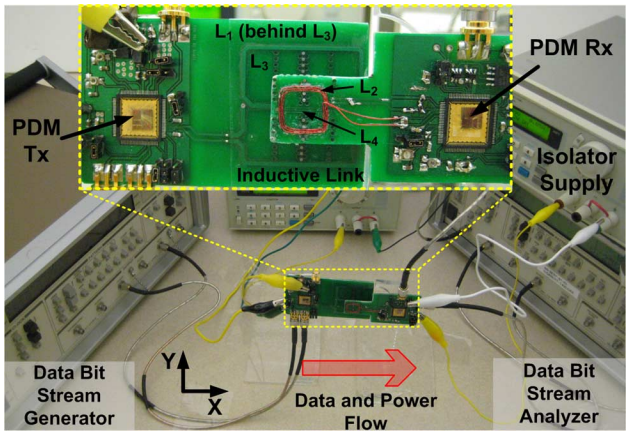


Fig. 9. PDM transceiver measurement setup. Inset: inductive links made of printed-spiral and wire-wound coils for power transmission ($L_1$ and $L_2$ in Fig. 1) [37] and a pair of planar figure-8 coils on FR4 PCB for data transmission ($L_3$ and $L_4$ in Fig. 1) [26]. $L_1$ was carefully aligned and glued behind $L_3$ to minimize $k_{13}$. $L_2$ was also glued over $L_4$ with careful alignment to minimize $k_{24}$.

PCE vs. $R_L$ at 13.56 MHz for different $V_{REC}$ values. As $R_L$ increases, the current flowing through, and the voltage dropping across the rectifier pass transistor, $\mathrm{P}_1$ in Fig. 5, reduces. This decreases the rectifier power loss and increases the PCE. At high $V_{REC}$ values, PCE is slightly increased because the rectifier voltage drop is relatively smaller. For a wide range of $R_L$, the rectifier PCE is >50%.

To measure the wireless link BER, the coils were held in parallel and perfectly aligned using Plexiglas sheets, as shown in Fig. 9. The surface-to-surface distance, $d$, between the two PCBs, each of which had 1.5 mm thickness, was 10 mm. Thus, the coupling distances for the data and power links were 10 mm and 13 mm, respectively. A pair of Tektronix GB1400 (GigaBERT) were used to generate the random serial data bit stream and synchronized clock, Tx-Data and Tx-Clk in Fig. 1, and measure the wireless link BER of the recovered data, Rx-Data, in real time.

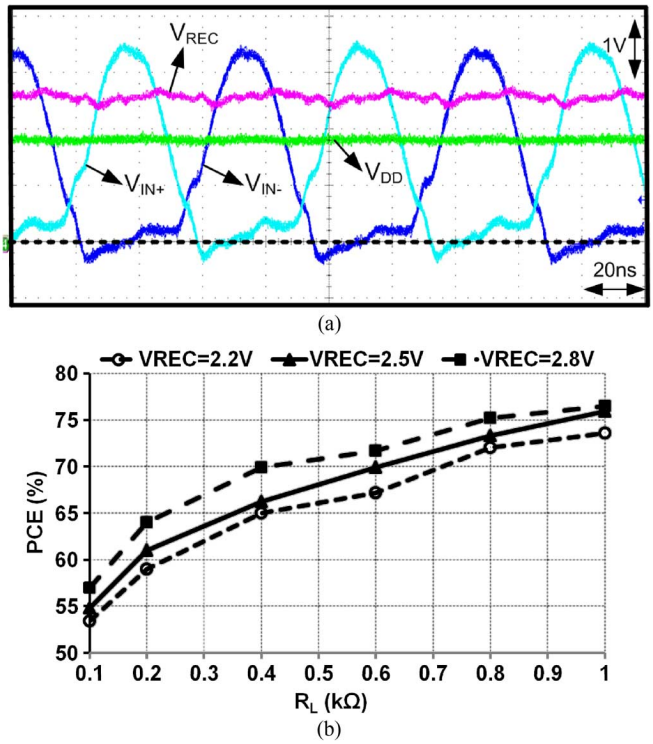


Fig. 10. (a) Passive rectifier measured input and output waveforms at 13.56 MHz when loaded by $C_L = 10\ \mu\mathrm{F}$ and $R_L = 0.4\ \mathrm{k}\Omega$. The regulator output at $V_{DD} = 1.8\ \mathrm{V}$ has also been shown. (b) Rectifier PCE vs. $R_L$ for different $V_{REC}$ values.

In order to test the link in a truly wireless setup and avoid any ground loops, we used a dual channel voltage isolator (Si8620, Silicon Labs, TX), which was supplied at 2.5 V on the Rx side, to deliver Rx-Data and Rx-Clk to the GigaBERT for BER measurements. The PDM Rx was inductively powered through the on-chip power management block, which generated the regulated $V_{DD}$ for the rest of the chip. Hence, the Rx PDM chip was completely isolated from the Tx chip.

In order to achieve the high data rate $(DR)$ of 13.56 Mbps, the data ringing across $\mathrm{L_4C_4}$-tank initiated by each Tx pulse had to be suppressed within $T_p/2 = 36.8$ ns. With a large $Q_4$, the data ringing will have a slow decaying pattern and multiple cycles should be dedicated during $T_p/2$ by tuning $\mathrm{L_4C_4}$-tank at $f_d \gg 2f_p$. However, this method makes PDM more sensitive to variations in $t_d$ as will be discussed in Section V.

$Q_4$ was reduced to 5 by adding $R_P = 100\ \Omega$ in parallel with $\mathrm{L_4C_4}$-tank (tuned at $f_d = 50$ MHz), as shown in Fig. 1, to limit the number of data ringing and avoid ISI. Fig. 11 from the top shows the transmitted data bits "1" and "0" at 13.56 Mbps, the PPG output ($S_m$ in Fig. 4), and different waveforms across the $\mathrm{L_4C_4}$-tank after 20 dB amplifications: data ringing when power carrier was not present, power carrier interference when data ringing were not present, and the superposition of data and power components in the received signal when both power carrier and data pulses are present. In this measurement, to avoid probing the inductive link directly, we used the discrete custom RF amplifier in [38]. The data ringing have shifted the zero-crossings of the power carrier to the left by 2.3 ns. In this measurement, $d = 10\ \mathrm{mm}$, $t_d = 28\ \mathrm{ns}$, and $\mathrm{PA\_V_{DD}} = 4\ \mathrm{V}$, power

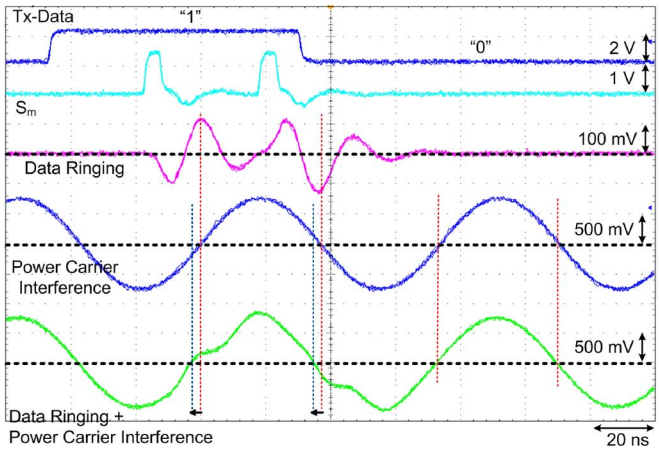


Fig. 11. Transmitter waveforms for data bits "1" and "0" at 13.56 Mbps and PPG output ($S_m$ in Fig. 4), and $L_4C_4$-tank waveforms after a 20 dB amplification by a discrete RF amplifier [38]. Data ringings were measured when power carrier interference was zero and vice versa. In the bottom trace, the superimposed data ringings have shifted the zero-crossings of the power carrier interference to the left by 2.3 ns. In this measurement, $d = 10$ mm, $t_d = 28$ ns, $t_{pw} = 5$ ns, PA_$V_{DD} = 4$ V, and SIR $= -18.5$ dB.

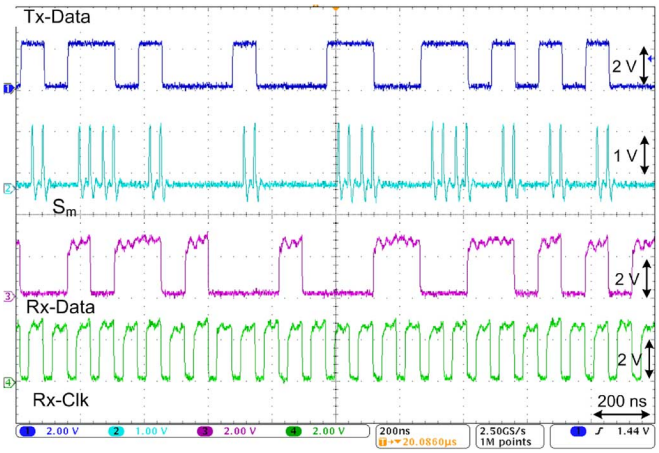


Fig. 12. PDM transceiver waveforms from the top: Transmitted serial data bit stream at 13.56 Mbps, the PPG output signal ($S_m$ in Fig. 4), recovered data bit stream, and recovered clock. Rx-Data and Rx-Clk were measured through an isolator that was supplied at 2.5 V. $d = 10$ mm, $t_d = 28$ ns, $t_{pw} = 5$ ns, PA_$V_{DD} = 4$ V, $V_{REC} = 2.5$ V, $V_{dd} = 1.8$ V, $V_{ref} = 0.9$ V, $t_R = 4$ ns, and SIR $= -18.5$ dB.

link was able to deliver 42 mW of regulated power to the Rx and measured SIR was $-18.5$ dB. It should be noted that SIR is defined as the ratio of the energy inside data pulse ringing for the data bit "1" to that inside the power carrier interference during one data bit period ($T_p$).

Fig. 12 shows a snapshot of the key measured waveforms in the PDM transceiver setup of Fig. 9. From top, the transmitted serial data bit stream at $DR = 13.56$ Mbps, PPG output ($S_m$ in Fig. 4), recovered serial data bit stream, and recovered clock are shown at $d = 10$ mm and SIR $= -18.5$ dB, when 42 mW of regulated power was delivered to a resistive load.

Fig. 13(a) shows the measured BER at 13.56 Mbps for various amounts of power delivered to the load (PDL), while changing $d$ from 4 to 10 mm. These results indicate that if the acceptable BER limit is considered $10^{-6}$, this PDM transceiver achieves

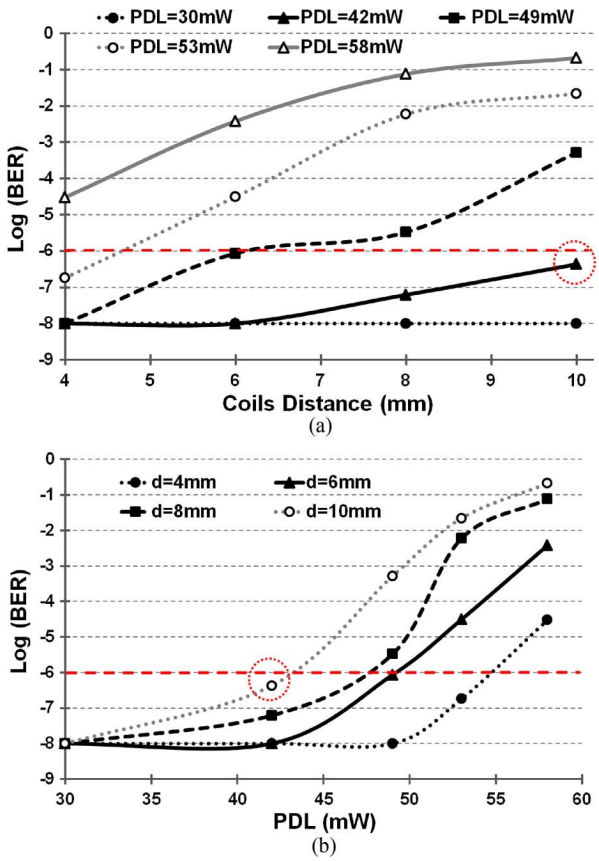


Fig. 13. Measured BER at 13.56 Mbps vs. (a) coupling distance, $d$, for different amounts of power delivered to the load (PDL); (b) PDL for different values of $d$. PA_VDD was swept between 3.3 V and 5 V to adjust PDL, while data Tx supply was constant at 1.8 V and $DR = 13.56$ Mbps.

$DR = 13.56$ Mbps while delivering 42 mW at $d = 10$ mm. Fig. 13(b) shows the measured BER values vs. PDL for different $d$. At $d = 10$ mm, for PDL $> 42$ mW, the SIR decreases and leads to higher BER. Fig. 13 implies that low SIR is the limiting factor in increasing the coil separation in PDM-based systems. To increase the distance >10 mm, as shown in Fig. 13(a), PDL should be decreased to <30 mW to reduce the power carrier interference. In these measurements, the data Tx and Rx supply voltages were constant at 1.8 V while the PA_$V_{DD}$ was swept between 3.3 V and 5 V to achieve different PDL values. The PDM data Tx and Rx power consumptions were 960 pJ/bit and 162 pJ/bit, respectively. Key specifications of the prototype PDM transceiver ASIC are summarized Table II.

Fig. 14(a) shows the changes in the BER due to coil misalignments along the X and Y axes at $d = 10$ mm and PDL $= 42$ mW. These curves show that figure-8 coils are more robust against misalignments along the X-axis (lower BER at the same misalignment) compared to the Y-axis, which is in agreement with our earlier observations in [26], based on variations in the coils' coupling. Fig. 14(b) shows the measured BER vs. SIR across $L_4C_4$-tank, indicating that for an acceptable BER of $10^{-6}$, minimum required SIR for this PDM receiver is about $-18.5$ dB. At lower SIR, data ringing across $L_4C_4$-tank have less effect on shifting the zero-crossings of the power carrier interference, leading to smaller variations on the integrator output in Fig. 6 for the data bit "1" and higher BER.

TABLE II
PDM-BASED TRANSCEIVER SPECIFICATIONS

| | | |
|---|---|---|
| Technology (TSMC) | | 0.35-µm 2P4M CMOS |
| Data transceiver supply voltage, $V_{dd}$ | | 1.8 V |
| Class-D PA supply voltage, PA_$V_{DD}$ | | 1.8-5 V |
| Power carrier frequency, $f_p$ | | 13.56 MHz |
| Data rate, $DR$ | | 13.56 Mbps |
| Pulse specs: $t_d$ / $t_{pw}$ | | 28 ns / 5 ns |
| Bit-error-rate (BER) | | $4.3\times10^{-7}$ |
| Nominal coils distance, $d$ | | 10 mm |
| Nominal delivered power to the load | | 42 mW |
| Power consumption (Data) | Tx | 960 pJ/bit |
| | Rx | 162 pJ/bit |
| Area on chip (Power and Data) | Tx | 0.88 mm$^2$ |
| | Rx | 0.72 mm$^2$ |

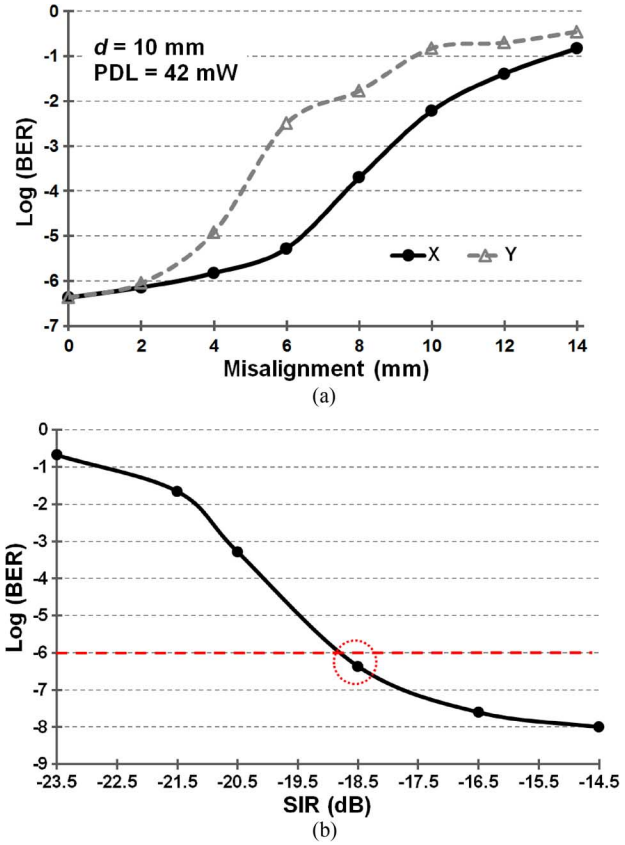


Fig. 14. Measured BER vs. (a) misalignment along X and Y axes (see Fig. 9) at $d = 10$ mm and $DR = 13.56$ Mbps while 42 mW was delivered to the Rx via $L_1 - L_2$ link, and (b) SIR across $L_4C_4$-tank. For an acceptable BER of $10^{-6}$, minimum required SIR for this PDM receiver is about $-18.5$ dB.

Table III benchmarks PDM against recent methods for simultaneous power and data transmission. To the best of our knowledge, PDM is the first pulse-based technique for simultaneous power and data transmission at high data rates. Our current PDM transceiver can achieve a data rate of 13.56 Mbps with a BER of $4.3 \times 10^{-7}$ across a 10 mm inductive link. Data Tx and Rx power consumptions under these conditions are only 960 and 162 pJ/bit, respectively, while a separate power link delivers 42 mW of regulated power to the load. Compared to the state-of-the-art [29], we have not only increased the data rate by a factor of 6.7 but also reduced the data Rx power consumption 19 folds. This power reduction is important in inductively powered IMDs, where received regulated power is quite precious. It should be noted that in [24], a first order off-chip low-pass filter (LPF) has been used to improve the SIR to $-6$ dB while the required SIR for the PDM receiver is $-18.5$ dB. A second order LPF has also been used in [29] to further suppress the power carrier interference. The LSK data link in [21] achieved 2.8 Mbps with smaller Tx power consumption. However, LSK can only be used for the uplink while PDM can be used for both up and downlink. Moreover, LSK consumes low power for data transfer at the cost of reducing the PDL by up to 50% at high data rates.

## V. DISCUSSION

For successful data recovery in the PDM, $t_d$ needs to be adjusted based on the delay between data ringing and power carrier interference zero-crossing times across the $L_4C_4$-tank. According to (10), the jitter in Tx-Clk and any changes in the link impulse response due to coupling variations can vary the optimal $t_d$. In all measurements, $t_d$ was set to 28 ns and $t_d$ variations were less than 1 ns.

PDM is reasonably robust against such $t_d$ variations because: 1) Variations of the phase delay resulted from the changes in $k_{14}$ (power interference path) and $k_{34}$ (data path), which are the 2nd and 3rd terms in (10), respectively, tend to cancel out each other. This will maintain $t_d$ fairly constant considering the fact that $L_1$ and $L_3$ move together. 2) Small variations in $t_d$ slightly shift the voltage peaks of the data ringing in Fig. 2. This can reduce zero-crossing shifts of the received signal across the $L_4C_4$-tank. It can be proven that if $t_d$ varies by $\Delta t_d$, shifts in zero crossings would be equal to data ringing with $\cos(\omega_d \Delta t_d)$ times smaller amplitude. This is the equivalent of $\sim$3 dB reduction in SIR if $\Delta t_d = 1/8 f_d$=2.5 ns. We chose $f_d = 50$ MHz to reduce the sensitivity of shifts in zero crossings to $t_d$ variations. Fig. 15 shows the measured BER values when $t_d$ was changed up to $\pm 4$ ns around its optimal value of $t_d = 28$ ns by controlling the PD signal in Fig. 4. The drop in zero-crossing shifts has significantly increased the BER for $\Delta t_d > 2$ ns. The use of crystal-based oscillators with sub-nanosecond jitter is feasible in the external power Tx due to its relatively relaxed size constraints. In systems with high jitter oscillators, PDL should be reduced to increase the amount of zero-crossing shifts or SIR to keep the BER low (see Figs. 13(b) and 14(b)). Furthermore, in a complete system, the data Tx block can actively adjust $t_d$ in a closed loop to maintain its optimal value for the lowest BER.

An automatic gain control (AGC) is needed in most wireless transceivers intended for communications under conditions of fading and distance variation, such as in IMDs to avoid voltage saturation at small $d$ or weak signals at large $d$ [39]. Although the PDM transceiver does not require AGC, because $V_R$ is amplified to create a square waveform, a similar mechanism can adaptively adjust $t_R$ in Fig. 6. Because similar to $t_d$, changes in the coils' coupling can vary $t_R$ and result in variations in $V_{INT}$. In this condition, $t_R$ values that are too small or too large will result in Rx-Data to be continuously "0" or "1", respectively. What is needed in this case is a local feedback mechanism that monitors a certain parameter in the Rx-Data, e.g. cyclic redundancy checking (CRC), and compensates for $t_R$ variations. In

TABLE III
BENCHMARKING OF RECENT INDUCTIVELY-POWERED DATA TELEMETRY LINKS

| Reference | Mod. Scheme | Comm. Link | # of Coils | Distance (mm) | Data Carrier Freq. (MHz) | Power Carrier Freq. (MHz) | Data Rate (Mbps) | Tx/Rx Power (pJ/bit) | CMOS Tech. (μm) | SIR (dB) | Die Area (mm$^2$) (Data Tx/Rx) | Supply Vol. (V) | BER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2004, [17] | pcFSK | Down | 2 | 5 | 5/10 | 5/10 | 2.5 | -/152 | 1.5 | - | -/0.29 | 5 | $10^{-5}$ |
| 2005, [20] | BPSK | Down | 4 | 15 | 10 | 10 | 1.12 | -/625 | 0.18 | - | -/0.2 | 1.8 | $10^{-5}$ |
| 2008, [21] | LSK$^{+}$ | Up | 2 | 20 | 25 | 25 | 2.8 | 35.7/1250 | 0.5 | - | 2.2/2.2$^{**}$ | 2.8 | $10^{-6}$ |
| 2012, [22] | FSK | Down | 4 | 20 | -/5 | 5 | 1.25 | - | 0.8 | - | - | 2.7 | - |
| 2012, [22] | BPSK | Up | 4 | 20 | 48 | 5 | 3 | 1962/- | 0.8 | - | 2.3$^{**}$ | 2.7 | $2\times10^{-4}$ |
| 2010, [23] | QPSK | Down | 4 | 5 | 13.56 | 1 | 4.16 | - | - | - | - | - | $2\times10^{-6}$ |
| 2008, [24] | BPSK | Down | 4 | 10~15 | 20 | 2 | 2 | -/3100 | 0.35 | -12$^{*}$ | -/4.4 | 4.5 | $10^{-7}$ |
| 2013, [29]$^{++}$ | DPSK | Down | 4 | - | 20 | 2 | 2 | - | 0.18 | - | - | 1.8 | $10^{-7}$ |
| **This Work** | **PDM** | **Down** | **4** | **10** | **50** | **13.56** | **13.56** | **960/162** | **0.35** | **-18.5** | **0.34/0.37** | **1.8** | **$4.3\times10^{-7}$** |

$^{*}$ A first order off-chip filter was used to improve SIR to $-6$ dB.
$^{**}$ including pads.
$^{+}$ LSK is only used for uplink.
$^{++}$ second-order filter was used to improve SIR.

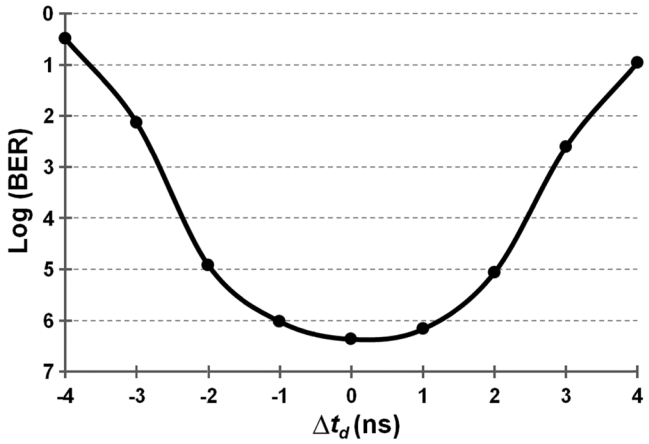


Fig. 15. Measured BER vs. $\Delta t_d$ for $\pm 4$ ns around its optimal value of $t_d = 28$ ns at $d = 10$ mm and $DR = 13.56$ Mbps while 42 mW was delivered to the Rx via $L_1 - L_2$ link. Jitter in crystal-based oscillators is in sub-nanoseconds and would not affect the BER significantly.

this scheme, which is under development, we plan to dynamically control the input to the delay block in Fig. 6.

Maximum data rate in this PDM transceiver is the same as $f_p$ because each data bit "1" modulates two zero-crossings of one power carrier cycle, $T_p$. In order to increase the PDM data rate, each data bit "1" or "0" could modulate only one of the zero crossings during each $T_p$. Therefore, each $T_p$ will include two bits, doubling the data rate to reach $2f_p$.

The PHM-based transceivers in [33] and [34] also achieved high data rate, low-power consumption, and small die size. However, due to the on-off keying (OOK) nature of the PHM, the signal amplitude should be considerably larger than the power carrier interference at the Rx input for proper data recovery (e.g. SIR > 10 dB). Although reducing $f_p$ and utilizing off-chip filters help to reduce the interference, the SIR would still be too low when a large PDL is required [24]. Therefore, the main advantage of the PDM over PHM is its robustness against large power carrier interference. According to our measurements, PDM offers reliable data communication in the presence of power interference that is one order of magnitude larger than the received data pulses. This is key in high performance IMDs, such as retinal prostheses that demand high PDL. The PHM, on the other hand, is suitable for low power IMDs that are equipped with rechargeable batteries and do not need to be continuously powered.

## VI. CONCLUSION

We have presented the first ASIC implementation of a low-power PDM-based transceiver in a standard CMOS process. The PDM technique, which concept was introduced in [35], has enabled us to achieve low-power, wideband, and robust telemetry along with power transmission, which is necessary in advanced inductively-powered IMDs. The PDM Tx is composed of a new LC driver circuit that can generate sharp pulses across a high-Q LC tank with large amplitudes in the order of $4 \times V_{DD}$. The PDM Rx operates as a pulse delay detector and enjoys lower power consumption compared to other methods due to less complexity. The presented PDM transceiver prototype also includes an on-chip class-D PA and power management circuits, operating at 13.56 MHz. The PDM transceiver achieved a high data rate of 13.56 Mbps with a BER of $4.3 \times 10^{-7}$ across a 10 mm dual-band inductive link, while delivering 42 mW of regulated power to the load. To the best of our knowledge, this is the best overall performance for near-field simultaneous data and power telemetry. Our future goal is to add mechanisms to adaptively adjust delays to increase the PDM robustness against the coils' distance variation and misalignments.

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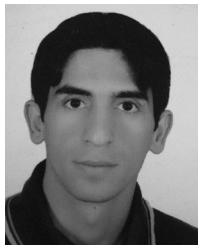

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