# VideoCore IV Typed Assembly Language Version 0.1

El Pin Al

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# 1. Syntax

To define the syntax, there are some primitive terms:

- *i* denotes an integer.
- i4 denotes a 4-bit integer in range [0,15].
- $i4^*$  denotes a 4-bit integer in range [1,16].
- $i7^*$  denotes a 7-bit integer in range [1,128].
- f denotes a floating-point number.

- *l* denotes a label.
- nat denotes an integer which is greater than or equal to 0.
- In general,  $\varepsilon$  denotes an empty construct.
- $\alpha$  denotes a variable.

The syntax is given below.

```
\nu ::= n \mid r
                                                                          operands
n \; ::= \qquad i \mid f
                                                                          numbers
r ::= rr \mid wr
                                                                          registers
rr ::= rwr \mid uniform \mid element\_number \mid vpmr
                                                                          readable registers
urr ::= a \mid element\_number
                                                                          unconstrained readable registers
wr ::= rwr \mid uniforms\_address
                                                                          writable registers
          | tmu | broadcast | vpmw
rwr ::= ga \mid rf
                                                                          both readable and writable registers
a ::= ga \mid sa
                                                                          accumulators
ga ::= r0 \mid r1 \mid r2 \mid r3
                                                                          general-purpose accumulators
sa ::= r4 \mid r5
                                                                          special-purpose accumulators
rf ::= A \mid B
                                                                          register files
A ::= ra0 \mid \dots \mid ra31
                                                                          locations in register file A
B ::= rb0 \mid \dots \mid rb31
                                                                          locations in register file B
tmu ::= tmu0 \mid tmu1
                                                                          TMU
vpmq ::= \varepsilon \mid (Y,i) :: vpmq
                                                                          VPM read queues
Y ::= \qquad \mathbf{y}_0 \mid \ldots \mid \mathbf{y}_{63}
                                                                          VPM Y
        rotate(wr, rr, i4) \mid mov(wr, \nu)
\iota ::=
                                                                          instructions
          \mid \text{setup\_vpm\_read}(Y, i4^*)
          \mid setup_vpm_write(Y)
          \mid \, \operatorname{setup\_dma\_load} \big( Y, i4^* \big) \mid \, \operatorname{start\_dma\_load} (rr)
          | wait_dma_load
          | setup_dma_store(Y, i7^*) | start_dma_store(rr)
          | wait_dma_store
```

```
cc ::= Z \mid N \mid C
                                                                 condition classes
c ::= set(cc) \mid clear(cc)
                                                                 conditions
qc ::= all(c) \mid any(c)
                                                                 quantified conditions
s ::= \varepsilon \mid \operatorname{load}\langle tmu \rangle
                                                                 signals
ci ::= (\iota, \varepsilon) \mid (\iota, c)
                                                                 conditional instructions
csi ::= (ci, s)
                                                                 conditional instructions with signals
I ::= \operatorname{jmp}(l) ; csi ; csi ; csi
                                                                 instruction sequences
        |(ci, thread\_end); csi; csi
        | csi ; I
        | \text{ if } qc \text{ jmp}(l) ; csi ; csi ; csi ; I
R ::= \varepsilon \mid R[rr \mapsto arr]
                                                                 register contexts
arrays
U ::= \varepsilon \mid n \circ U
                                                                 uniforms
T ::= \varepsilon \mid arr \mid arr :: arr \mid arr :: arr :: arr
                                                                 TMU
        | arr :: arr :: arr :: arr
V ::= \varepsilon \mid V[Y \mapsto at]
                                                                 VPM states
P ::= \varepsilon \mid P[l \mapsto I]
                                                                 programs
M ::= (R, U, T, V, vpmq, P, I)
                                                                 machines
```

#### 2. Type system

The type syntax is defined as follows:

$\tau ::=$	$b\mid at\mid vt\mid \Psi$	types
p ::=	$nat \mid \alpha \mid p + p \mid nat \times p$	pointers
b ::=	$\operatorname{int}(i) \mid \operatorname{int}(?) \mid \operatorname{float} \mid \operatorname{ptr}(p) \mid \operatorname{code}(\Theta)$	basic types
at ::=	[b,b,b,b,b,b,b,b,b,b,b,b,b,b,b]	array types
vt ::=	$\mathrm{vec}(b,lpha)$	vector types
$\Gamma ::=$	$\varepsilon \mid \Gamma[rr \mapsto at]$	register context types
$\Psi ::=$	$arepsilon \mid b \circ \Psi$	uniforms types
$\Sigma ::=$	$\varepsilon \   \ at \   \ at :: at \   \ at :: at :: at \   \ at :: at :: at$	TMU types
$\Pi ::=$	$\varepsilon \mid \Pi[Y \mapsto at]$	VPM state types
$vpmw\_addr ::=$	$arepsilon \mid Y$	VPM write addresses
C ::=	$(vpmq,\Pi,vpmw\_addr)$	VPM compound types
u ::=	u0   u1   u2	uniform-access countdowns
$\Theta ::=$	$(\Gamma, \Psi, u, \Sigma, C, \Omega, wr)$	state types
$\Phi \ ::=$	$\varepsilon \mid \Phi[l \mapsto \Theta]$	program types
DLS ::=	$arepsilon \mid \left(Y, i4^* ight)$	DMA load setups
DSS ::=	$arepsilon \mid \left(Y, i7^* ight)$	DMA store setups
DL ::=	$arepsilon \mid \left(Y, i4^*,  au ight)$	DMA loads
DS ::=	$\varepsilon \mid \left(Y, i7^*, \tau\right) \mid \text{type\_preserving}$	DMA stores

## 2.1. Propositions

 $\boldsymbol{p}_1 \ldots \boldsymbol{p}_2$  represents a range  $[\boldsymbol{p}_1, \boldsymbol{p}_2).$ 

$$\varphi ::= p ... p \mid \varphi \lor \varphi$$

propositions

#### 2.2. Memory representaion

$$\Omega::=\left\{\Xi\mid\varphi\right\}$$
 memory subset types 
$$\Xi::=\varepsilon\mid\Xi[p\mapsto\tau]$$
 memory types

The evaluation rules of memory subset types and memory types are given below. The equality rules for p are not defined here. There are the abuses of notations of a form  $x[y\mapsto z]$ .

$$\frac{p \text{ is in } \varphi}{\{\Xi \mid \varphi\}(p) \to_{\Omega} \Xi(p)}$$

$$\frac{p = p_1}{\Xi \left[p_1 \mapsto \tau\right](p) \to_{\Xi} \tau}$$

$$\frac{p \neq p_1}{\Xi \left[p_1 \mapsto \tau\right](p) \to_{\Xi} \Xi(p)}$$

#### 2.3. Typing rules

Typing rules are defined as follows. Note that  $dom(\Gamma)$  represents the domain of a context  $\Gamma$ , a map from read / write registers to array types.

numbers:

$$\vdash i : int(i) \qquad \vdash f : float$$

subtype relations:

$$\begin{split} & \operatorname{int}(i) <: \operatorname{int}(?) & \operatorname{int}(?) <: \operatorname{int}(?) & \frac{\forall i \ . \ at_1[i] <: at_2[i]}{at_1 <: at_2} \text{(S-Array)} \\ & \frac{m \leq n}{\operatorname{vec}(b, m) <: \operatorname{vec}(b, n)} \text{(S-Vector)} \end{split}$$

$$\Gamma <: \Gamma$$

$$\frac{\Gamma_1 <: \Gamma_2 \qquad rr \not\in dom \left(\Gamma_1\right)}{\Gamma_1[rr \mapsto at] <: \Gamma_2} \text{(S-Ctx-Width)} \qquad \frac{\Gamma_1 <: \Gamma_2 \qquad at_1 <: at_2}{\Gamma_1[rr \mapsto at_1] <: \Gamma_2[rr \mapsto at_2]} \text{(S-Ctx-Depth)}$$

pointers:

$$\frac{p \in dom(\Xi)}{\Xi \vdash p : \Xi(p)}$$

well-formed memory subsets:

$$\frac{\forall p \in dom(\Xi) \cdot p \dots (p + size\_of(\Xi(p))) \text{ is in } \varphi}{\vdash \{\Xi \mid \varphi\}}$$

registers:

$$\begin{array}{l} rr \in dom(\Gamma) \\ \hline \Gamma \vdash rr : \Gamma(rr) \end{array} \qquad \begin{array}{l} \Psi_1 \equiv b \circ \Psi_2 \\ \hline \vdash \text{uniform} : b \mid \Psi_1 \rightarrow \Psi_2 \end{array}$$
 
$$\vdash \text{element\_number} : [\text{int}(0), \text{int}(1), ..., \text{int}(15)]$$

$$\frac{vpmq_1 \equiv \Big(vpmq_2 :: \big(Y,i\big)\Big) \qquad i \geq 2 \qquad \Pi \vdash Y : at}{\Pi \vdash \text{vpmr} : at \mid vpmq_1 \rightarrow vpmq_2 :: \Big(inc(Y),i-1\Big)}$$

$$\frac{vpmq_{_{1}} \equiv \Big(vpmq_{_{2}} :: (Y\!,\!1)\Big) \qquad \Pi \vdash Y \colon at}{\Pi \vdash \mathrm{vpmr} : at \mid vpmq_{_{1}} \to vpmq_{_{2}}}$$

VPM:

$$\begin{split} &\frac{Y \in dom(\Pi)}{\Pi \vdash Y \colon \Pi(Y)} \\ &\frac{\Pi \vdash Y \colon at \quad at <: vt}{\Pi \vdash (Y,1) \colon vt} \\ &\frac{\Pi \vdash Y \colon at \quad at <: vt_1 \quad n \leq 62 \quad i7^* \geq 2 \quad \Pi \vdash \left(\mathbf{y}_{n+1}, i7^* - 1\right) \colon vt_2}{\Pi \vdash \left(\mathbf{y}_n, i7^*\right) \colon concat(vt_1, vt_2)} \end{split}$$

instructions:

$$\frac{\vdash \text{ element\_number} : at}{\vdash \text{ rotate}(rwr, \text{ element\_number}, i4) : \Gamma \rightarrow \Gamma[rwr \mapsto rotate(at, i4)] \; ; \; rwr}$$

```
\frac{\Pi \vdash \text{vpmr} : at \mid \textit{vpmq}_1 \rightarrow \textit{vpmq}_2}{\Pi \vdash \text{rotate}(\textit{rwr}, \text{vpmr}, i4) : \textit{vpmq}_1 \rightarrow \textit{vpmq}_2 \mid \Gamma \rightarrow \Gamma[\textit{rwr} \mapsto \textit{rotate}(at, i4)] \; ; \; \textit{rwr}}
\frac{rr \not\equiv wr_{before} \quad \Gamma \vdash rr: at \quad fst\big(rotate(at, i4)\big) \equiv b}{\Gamma; wr_{before} \vdash \text{rotate}(\text{broadcast}, rr, i4): \Gamma \rightarrow \Gamma[\text{r5} \mapsto array(b)]}
\frac{ \quad \vdash \text{ uniform} : b \mid \Psi_1 \rightarrow \Psi_2}{\vdash \text{ rotate(broadcast, uniform}, i4)} : \Gamma \rightarrow \Gamma \big\lceil \text{r5} \mapsto array(b) \big\rceil \mid \Psi_1 \rightarrow \Psi_2
\frac{\vdash \text{ element\_number} : at \qquad b \equiv \textit{fst}\big(\textit{rotate}(at, i4)\big)}{\vdash \text{ rotate}\big(\text{broadcast}, \text{element\_number}, i4\big) : \Gamma \rightarrow \Gamma\big[\text{r5} \mapsto \textit{array}(b)\big]}
\frac{\Pi \vdash \text{vpmr} : at \mid \textit{vpmq}_1 \rightarrow \textit{vpmq}_2 \quad \textit{fst}\big(\textit{rotate}(at, i4)\big) \equiv b}{\Pi \vdash \text{rotate}\big(\text{broadcast}, \text{vpmr}, i4\big) : \Gamma \rightarrow \Gamma\big[\text{r5} \mapsto \textit{array}(b)\big] \mid \textit{vpmq}_1 \rightarrow \textit{vpmq}_2}
\frac{rr \not\equiv wr_{before} \qquad \Gamma \vdash rr: at \qquad fst\big(rotate(at, i4)\big) \equiv ptr(p) \qquad \Xi \vdash p: \Psi_2}{\Gamma; \Xi; wr_{before} \vdash rotate(uniforms\_address, rr, i4): \Psi_1 \rightarrow \Psi_2 \mid u \rightarrow u2}
\frac{ \vdash \text{ uniform : ptr}(p) \mid \Psi_1 \to \Psi_2 \qquad \Xi \vdash p : \Psi_3}{\Xi \vdash \text{rotate}(\text{uniforms\_address}, \text{uniform}, i4) : \Psi_1 \to \Psi_3 \mid \text{u}0 \to \text{u}2}
\frac{\Pi \vdash \text{vpmr} : at \mid vpmq_1 \rightarrow vpmq_2 \quad fst\big(rotate(at, i4)\big) \equiv \text{ptr}(p) \quad \Xi \vdash p : \Psi_2}{\Pi; \; \Xi \vdash \text{rotate}\big(\text{uniforms\_address}, \text{vpmr}, i4\big) : \Psi_1 \rightarrow \Psi_2 \mid vpmq_1 \rightarrow vpmq_2 \mid u \rightarrow u2\big)}
\frac{rr \not\equiv wr_{before} \quad \Gamma \vdash rr: at \quad notfull(\Sigma^{tmu})}{\Gamma; \; \Xi \; ; \; wr_{before} \vdash \text{rotate}(tmu, rr, i4) : \Sigma^{tmu} \rightarrow rotate(map(unwrap_{\Xi}, at), i4) :: \Sigma^{tmu}}
\frac{\vdash \text{uniform}: \text{ptr}(p) \mid \Psi_1 \to \Psi_2 \quad \Xi \vdash p: b \quad notfull\left(\Sigma^{tmu}\right)}{\text{u0}; \Xi \vdash \text{rotate}(tmu, \text{uniform}, i4): \Sigma^{tmu} \to array(b) :: \Sigma^{tmu} \mid \Psi_1 \to \Psi_2}
\frac{\Pi \vdash \text{vpmr} : at \mid vpmq_1 \rightarrow vpmq_2 \quad notfull(\Sigma^{tmu})}{\Pi; \Xi \vdash \text{rotate}(tmu, \text{vpmr}, i4) : \Sigma^{tmu} \rightarrow rotate(map(unwrap_{\Xi}, at), i4) :: \Sigma^{tmu}}
\frac{rr \not\equiv wr_{before} \qquad rr \in dom(\Gamma) \qquad at \equiv rotate\big(\Gamma(rr), i4\big)}{wr_{before} \vdash \text{rotate}(\text{vpmw}, rr, i4) : \Pi \rightarrow \Pi[Y \mapsto at] \mid Y \rightarrow inc(Y)}
```

 $\vdash$  setup\_vpm\_write $(Y) : vpmw\_addr \rightarrow Y$ 

$$\frac{i + i\boldsymbol{4}^* \leq 64}{\vdash \text{setup\_dma\_load}\left(\mathbf{y}_i, i\boldsymbol{4}^*\right) : DLS \to \left(\mathbf{y}_i, i\boldsymbol{4}^*\right)}$$

$$\frac{\Gamma \vdash rr : at \qquad fst(at) \equiv ptr(p) \qquad \Xi \vdash p : \tau \qquad i4^* \times 16 \times 4 \leq size\_of(\tau)}{\left(Y, i4^*\right); \; \Xi \vdash start\_dma\_load(rr) : \varepsilon \rightarrow \left(Y, i4^*, \tau\right)}$$

 $\vdash \text{ wait\_dma\_load}: \left(Y, i4^*, \tau\right) \rightarrow \varepsilon \ | \ \Pi \rightarrow \Pi \ dma\_load\left(Y, i4^*, \tau\right)$ 

$$\frac{i + i7^* \leq 64}{\vdash \text{setup\_dma\_store}(y_i, i7^*) : DSS \to (y_i, i7^*)}$$

$$\frac{\Gamma \vdash rr: at_1 \quad fst(at_1) \equiv \operatorname{ptr}(p) \quad \Omega \vdash p: \tau \quad \Pi \vdash \left(Y, i7^*\right): \tau_1 \quad \tau_1 <: \tau}{\left(Y, i7^*\right); \ \Omega \vdash \operatorname{start\_dma\_store}(rr): \varepsilon \to \operatorname{type\_preserving}}$$

$$\frac{\Gamma \vdash rr : at_1 \qquad fst(at_1) \equiv ptr(p) \qquad \Pi \vdash \left(Y, i7^*\right) : \tau \qquad p \notin dom(\Omega) \qquad \vdash \Omega[p \mapsto \tau]}{\left(Y, i7^*\right); \ \Omega \vdash start\_dma\_store(rr) : \varepsilon \to (p, \tau)}$$

 $\vdash$  wait\_dma\_store : type\_preserving  $\rightarrow \varepsilon$ 

 $\vdash$  wait\_dma\_store :  $(p,\tau) \to \varepsilon \mid \Omega \to \Omega[p \mapsto \tau]$ 

#### conditional instructions:

$$\begin{array}{c|c} \vdash \iota: \Gamma_1 \rightarrow \Gamma_2 \mid u_1 \rightarrow u_2 \mid \Psi_1 \rightarrow \Psi_2 \mid \Sigma_1^{tmu} \rightarrow \Sigma_2^{tmu} \mid C_1 \rightarrow C_2 \mid wr_1 \rightarrow wr_2 \\ & [rr \mapsto at_1] \in \Gamma_1 \qquad \Gamma_2 \equiv \Gamma_{21} [rr \mapsto at_2] \\ \hline & at_1 <: at_2 \\ \hline \vdash (\iota,c): \Gamma_1 \rightarrow \Gamma_2 \mid u_1 \rightarrow u_2 \mid \Psi_1 \rightarrow \Psi_2 \mid \Sigma_1^{tmu} \rightarrow \Sigma_2^{tmu} \mid C_1 \rightarrow C_2 \mid wr_1 \rightarrow wr_2 \\ \hline & \vdash \iota: \Theta_1 \rightarrow \Theta_2 \\ \hline \vdash (\iota,\varepsilon): \Theta_1 \rightarrow \Theta_2 \end{array}$$

signals:

$$\vdash \operatorname{load}\langle tmu\rangle : \Sigma^{tmu} :: at \to \Sigma^{tmu} \mid \Gamma \to \Gamma[r4 \mapsto at]$$

conditional instructions with signals:

$$\frac{\vdash ci:\Theta_1 \rightarrow \Theta_2}{\vdash \left(ci,\varepsilon\right):\Theta_1 \rightarrow \Theta_2}$$

$$\begin{array}{c|c} \vdash ci : \Gamma \rightarrow \Gamma \big[ rr_1 \mapsto at_1 \big] \mid u_1 \rightarrow u_2 \mid \Psi_1 \rightarrow \Psi_2 \mid C_1 \rightarrow C_2 \mid \Omega_1 \rightarrow \Omega_2 \mid wr_1 \rightarrow wr_2 \\ & \vdash s : \Gamma \rightarrow \Gamma \big[ r4 \mapsto at_2 \big] \mid \Sigma_1^{tmu} \rightarrow \Sigma_2^{tmu} \\ \hline & \vdash (ci,s) : \Gamma \rightarrow \Gamma \big[ rr_1 \mapsto at_1 \big] \big[ r4 \mapsto at_2 \big] \mid u_1 \rightarrow u_2 \mid \Psi_1 \rightarrow \Psi_2 \\ & \mid \Sigma_1^{tmu} \rightarrow \Sigma_2^{tmu} \mid C_1 \rightarrow C_2 \mid \Omega_1 \rightarrow \Omega_2 \mid wr_1 \rightarrow wr_2 \end{array}$$

labels:

$$\frac{l \in dom(\Phi)}{\Phi \vdash l : \Phi(l)}$$

instruction sequences:

$$\begin{array}{c} \vdash csi: \Theta_1 \rightarrow \Theta_2 \\ \hline \Phi \vdash I: \Theta_2 \\ \hline \Phi \vdash csi: I: \Theta_1 \end{array}$$

$$\begin{split} \vdash csi_1 : \Theta_1 \rightarrow \Theta_2 \\ \vdash csi_2 : \Theta_2 \rightarrow \Theta_3 \\ \vdash csi_3 : \Theta_3 \rightarrow \Theta_4 \\ \Phi \vdash l : \operatorname{code}(\Theta_5) \\ \hline \Theta_4 <: \Theta_5 \\ \hline \Phi \vdash \operatorname{jmp}(l) \; ; \; csi_1 \; ; \; csi_2 \; ; \; csi_3 : \Theta_1 \end{split}$$

$$\begin{array}{c} \vdash ci:\Theta_{11} \rightarrow \Theta_2 & \vdash csi_1:\Theta_2 \rightarrow \Theta_3 \\ & \vdash csi_2:\Theta_3 \rightarrow \Theta_4 \\ regctx(\Theta_2) \equiv regctx(\Theta_{11})[rwr \mapsto at] \\ rwr \not\equiv ran \\ rwr \not\equiv rbn & \Theta_1 \equiv \left(\Gamma_1, \Psi_1, u_1, \Sigma_1^{tmu}, C_1, \Omega_1, wr_1\right) \\ \Theta_{11} \equiv \left(\Gamma_1 \setminus \{ ra14, rb14 \}, \Psi_1, u_1, \Sigma_1^{tmu}, C_1, \Omega_1, wr_1\right) \\ \left\{ ra14, rb14 \} \not\in regctx(\Theta_2) \\ \left\{ ra14, rb14 \} \not\in regctx(\Theta_3) \\ \left\{ ra14, rb14 \right\} \not\in regctx(\Theta_4) \\ \hline + (ci, thread\_end) \; ; \; csi_1 \; ; \; csi_2 : \Theta_1 \\ \hline + csi_1:\Theta_1 \rightarrow \Theta_2 \qquad \vdash csi_2:\Theta_2 \rightarrow \Theta_3 \\ \vdash csi_3:\Theta_3 \rightarrow \Theta_4 \\ \Phi \vdash l : code(\Theta_4) \qquad \Phi \vdash l : \Theta_5 \\ \hline \Theta_4 <:\Theta_5 \\ \hline \Phi \vdash \text{if } qc \; \text{jmp}(l) \; ; \; csi_1 \; ; \; csi_2 \; ; \; csi_3 \; ; \; l : \Theta_1 \\ \hline \end{array}$$

programs:

$$\frac{\forall l \in dom(P) \cdot \Phi \vdash P(l) : \Theta_l}{\Phi \vdash P}$$

It is defined that when the elements of at all have the same basic type b, it is convertible with vec(b, 16).

#### 2.4. Auxiliary functions

Note that all free meta-variables are assumed to be fresh.

$$\begin{split} & notfull \left(\Sigma^{tmu}\right) \stackrel{\text{\tiny def}}{=} \left(\Sigma^{tmu} \not\equiv at_1 :: at_2 :: at_3 :: at_4\right) \\ & unwrap_\Xi \left(\text{ptr}(p)\right) \stackrel{\text{\tiny def}}{=} \Xi(p) \text{ if } p \in dom(\Xi) \\ & fst \left([b_0, b_1, ..., b_{15}]\right) \stackrel{\text{\tiny def}}{=} b_0 \\ & map \left(f, [b_0, b_1, ..., b_{15}]\right) \stackrel{\text{\tiny def}}{=} \left[f(b_0), f(b_1), ..., f(b_{15})\right] \end{split}$$

When an array type has the same 16 basic type, written array(b):

$$\begin{split} &array(b) \stackrel{\mathrm{def}}{=} [b,b,...,b] \\ &inc(\mathbf{y}_{63}) \stackrel{\mathrm{def}}{=} \mathbf{y}_{0} \\ &inc(\mathbf{y}_{n}) \stackrel{\mathrm{def}}{=} \mathbf{y}_{n+1} \text{ if } 0 \leq n \leq 62 \\ &regctx((\Gamma,\Psi,u,\Sigma,C,\Omega,wr)) \stackrel{\mathrm{def}}{=} \Gamma \\ &size\_of(\tau) \text{ represents the size of a value of } \tau \text{ in bytes.} \\ &size\_of(b) \stackrel{\mathrm{def}}{=} 4 \\ &size\_of(at) \stackrel{\mathrm{def}}{=} 16 \times 4 \\ &size\_of(b \circ \Psi) \stackrel{\mathrm{def}}{=} 4 + size\_of(\Psi) \\ &size\_of(\varepsilon) \stackrel{\mathrm{def}}{=} 0 \\ &size\_of(\mathrm{vec}(b,n)) \stackrel{\mathrm{def}}{=} size\_of(b) \times n \\ &dma\_load(Y,1,\tau) \stackrel{\mathrm{def}}{=} [Y \mapsto truncate(\tau)] \end{split}$$

 $dma\_load \left(Y,i4^*,at\right) \stackrel{\text{\tiny def}}{=} \left[Y \mapsto at\right] \text{ if } i4^* \geq 2$ 

 $concat(vec(b, m), vec(b, n)) \stackrel{\text{\tiny def}}{=} vec(b, m + n)$ 

## 3. Future

 $truncate(at) \stackrel{\text{\tiny def}}{=} at$ 

- Any properties are not proved.
- There are many implicitness.
- The current definition is so conservative that it cannot serve practical use.
- The current definition may be incorrect or inconsistent.