3.3.2 CLOCK ARCHITECTURE

Figure 3-2 illustrates the block diagram of the clock generation module. The clock source selects between an external crystal (XXTIpll) and external clock (XEXTCLK). The clock generator consists of three PLLs (Phase Locked Loop) which generate high frequency clock signals up to 1.6GHz.

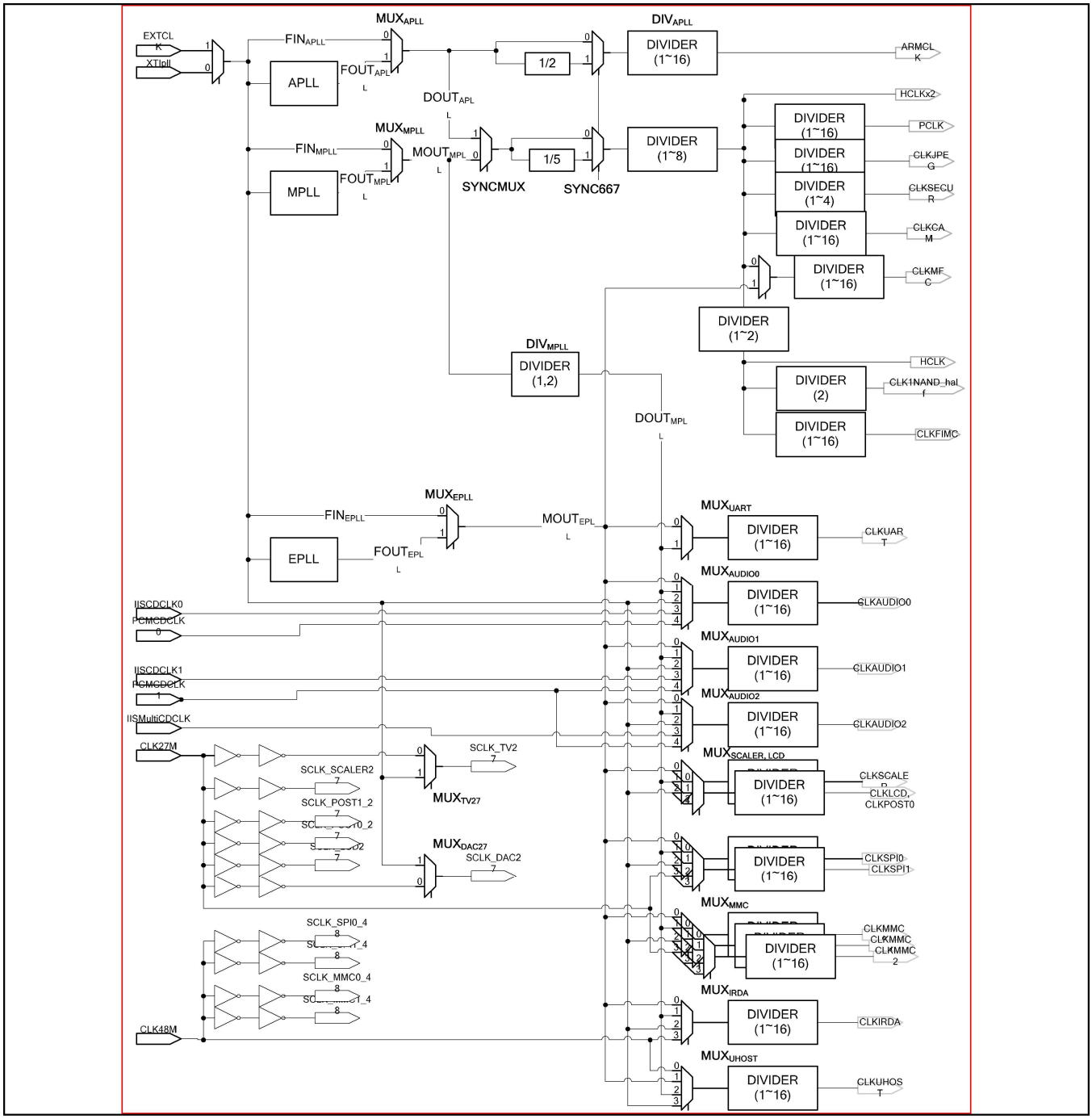

Figure 3-2. The block diagram of clock generator