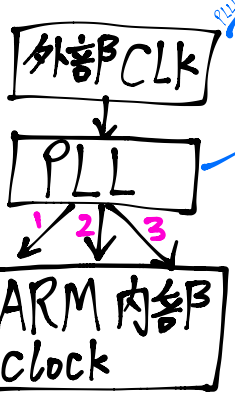
S3C6410

System clock Control

1. ARMPLL→ARMCLK
2. mainPLL
   ↓ ↘
   HCLK PCLK
3. extra PLL
   ↓
   外设



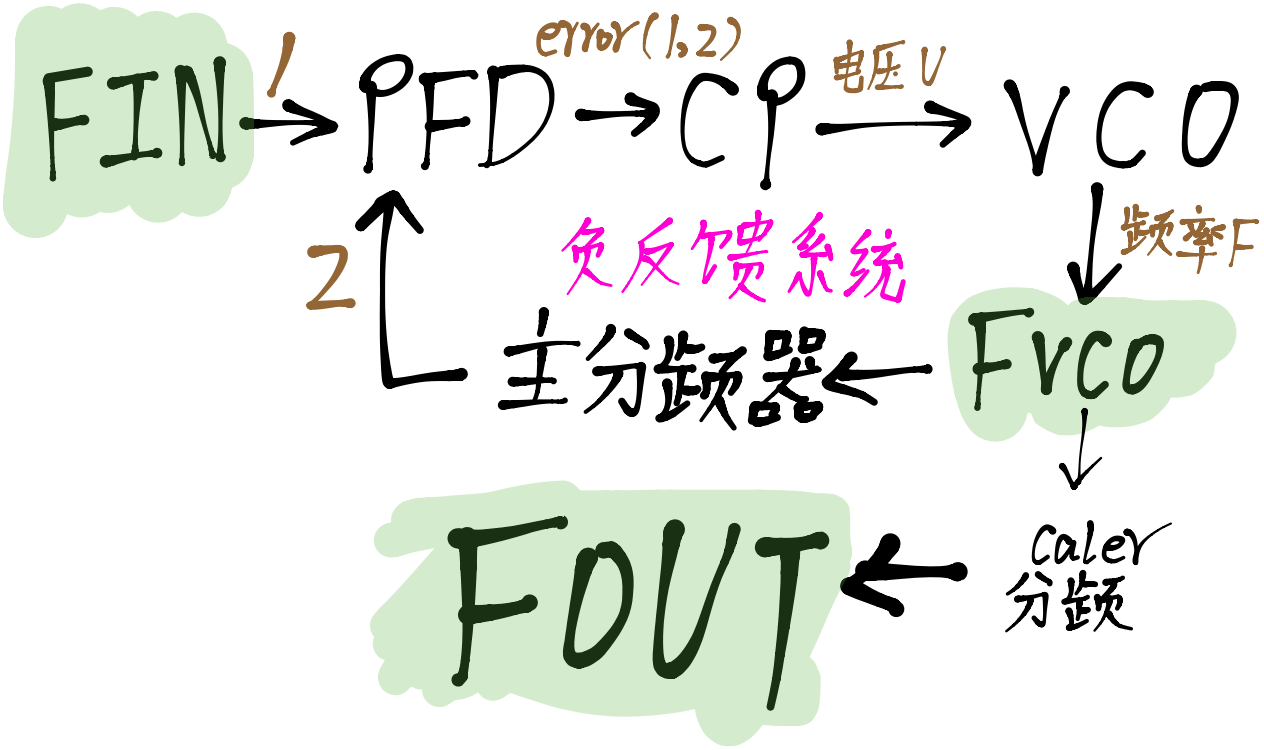
PLL原理 → 无法满足ARM系统内部多个倍频率

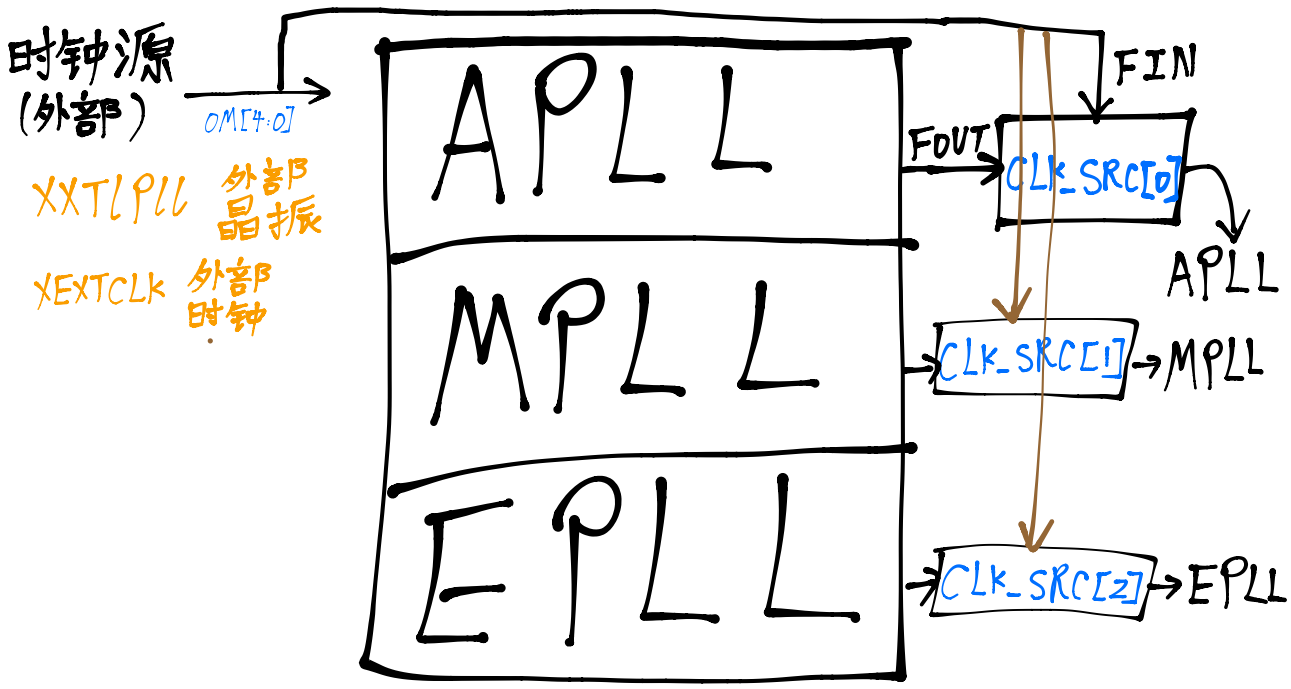
满足目标 ✓

分频/倍频
相位同步

1. ARM CLK → CPU 667M
2. HCLK ⇄ AXI bus / AHB bus 133M
3. PCLK → APB bus 66M
4. extra PLL clock → 外设
   UART
   I^2C

FIN → PLL → FOUT




时钟源
(外部)
OM[4:0]
XXTIPLL
外部晶振
XEXTCLK
外部时钟
APLL
MPLL
EPLL
FIN
FOUT
CLK_SRC[0]
APLL
CLK_SRC[1]
MPLL
CLK_SRC[2]
EPLL