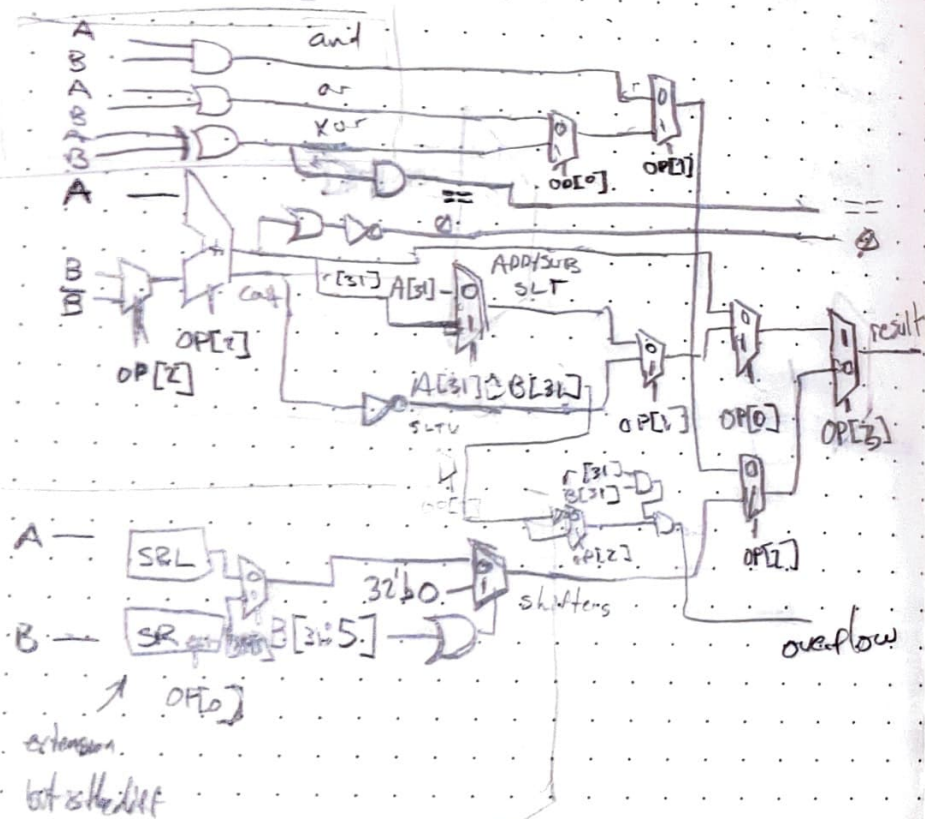


INSTRUCTION		(OP)
AND	0001	✓
OR	0010	✓
XOR	0011	✓
SLL	0101	✓
SRL	0110	✓
SRA	0111	✓
ADD	1000	✓
SUB	1001	✓
SLT	1010	✓
SLTU	1011	✓



I caught a few bugs testing and reflected here

$$\begin{array}{r}
 \text{SLTU} \\
 \begin{array}{r}
 42 \\
 111 \\
 + 101 \\
 \hline
 1100
 \end{array}
 \end{array}
 = 5$$

$$\begin{array}{r}
 421 \\
 111 \\
 + 111 \\
 \hline
 1110
 \end{array}
 = 7$$

$$\begin{array}{r}
 001 = 1 \\
 + 000 = 0 \\
 \hline
 1001
 \end{array}
 = 4$$

$$\begin{array}{r}
 111 \\
 + 010 \\
 \hline
 1001
 \end{array}
 = 5$$

$$\begin{array}{r}
 111 \\
 + 000 \\
 \hline
 111
 \end{array}
 = 7$$

$$\begin{array}{r}
 111 \\
 + 001 \\
 \hline
 1000
 \end{array}
 = 6$$

$$\Rightarrow \sim \text{cout}$$

- ✓ Equal  $A == B \Leftrightarrow (A \oplus B)$
- ✓ Zero  $A == 0 \Leftrightarrow \sim (1A)$
- ✓ Shift  $\geq 32$   $(\text{shift} > 32) != 0$
- Overflow

$$\sim (A[31] \wedge B[31]) \wedge (C[31])$$

$$\text{overflow} = \sim (A \oplus B) \& (C \oplus B)$$

A	B	C	expected sign
+	+	+	← risk
+	-	+	
-	+	-	← risk
-	-	-	

A	B	C
+	+	+
+	-	+
-	+	-
-	-	-