Fiona O'Connell, Kelly Deal, Danni Krauser

Senior Design Assignment #4

Part 1: User Stories

As a research scientist, I want to accelerate my machine learning model's inference time so that I can process large datasets more quickly.

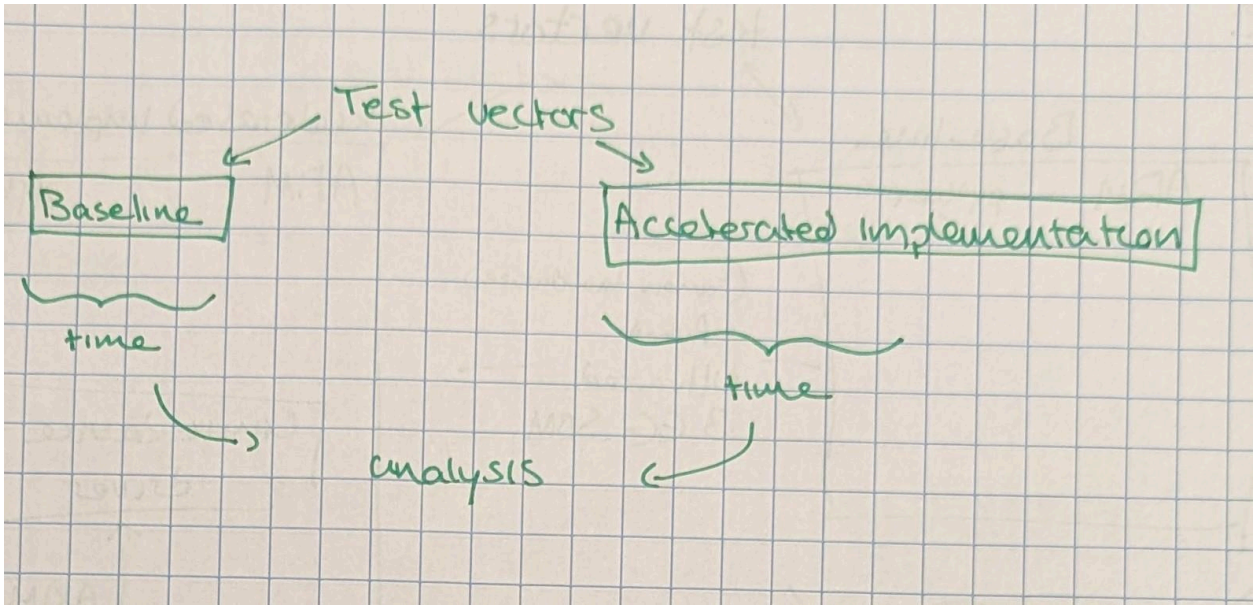
As a data analyst, I want to reduce the power consumption of a neural network so that I can deploy my model in an energy-constrained environment.

As a researcher, I want to measure the performance of a software algorithm on an FPGA so that I can prove the benefits of hardware acceleration.

Part 2: Design Diagram

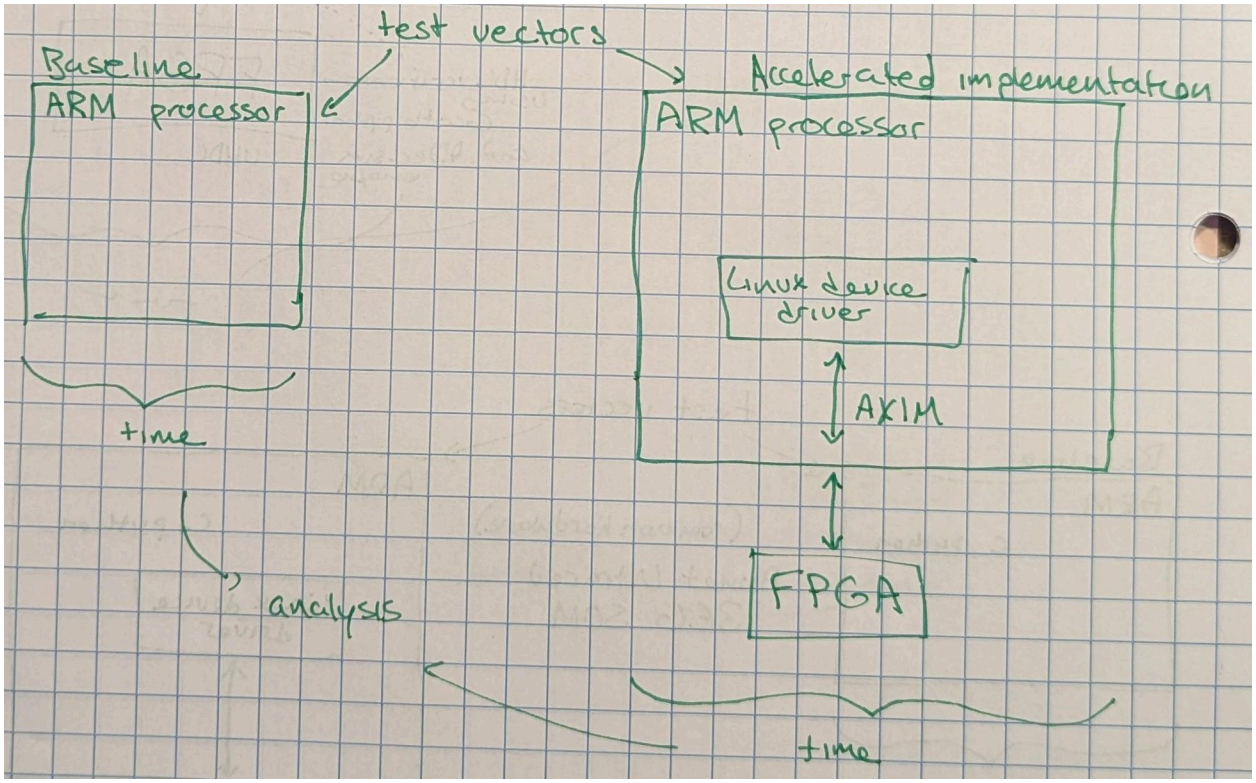
Design D0:

Input the test vectors into the baseline implementation and the accelerated implementation. Record the process time for analysis.



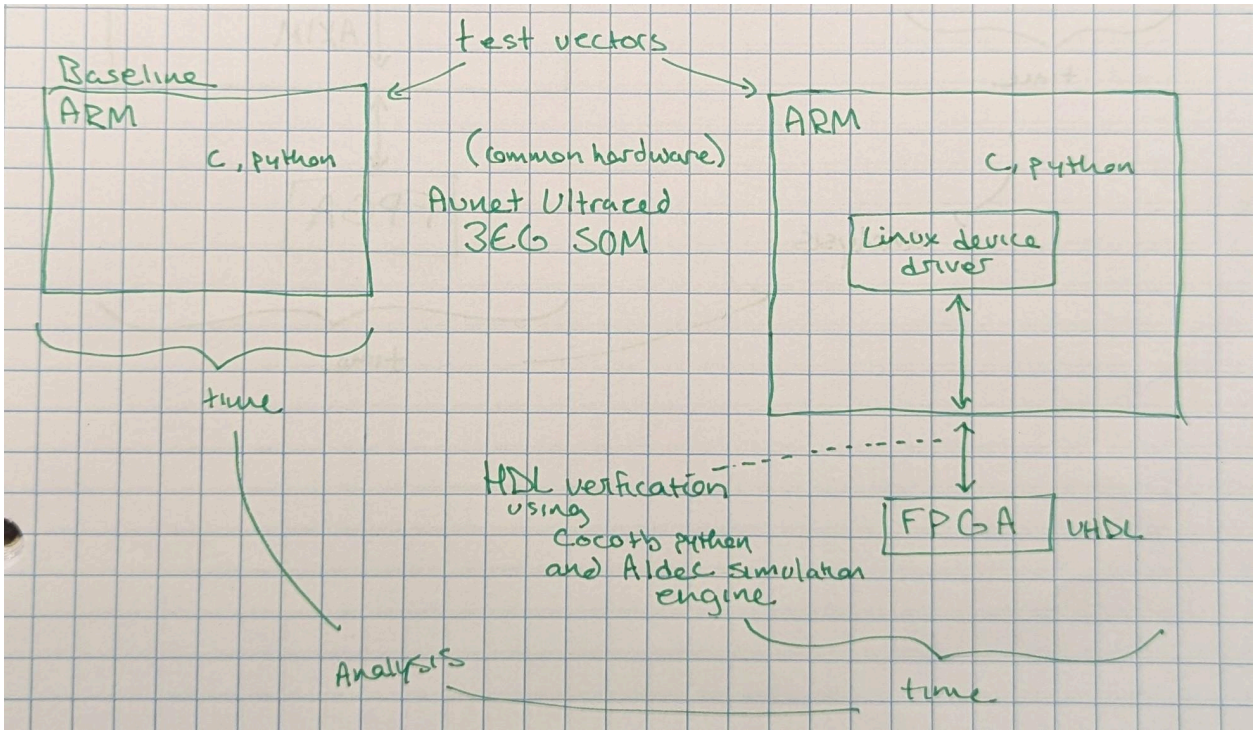
Design D1:

Input the test vectors into the baseline implementation and the accelerated implementation. The software baseline runs on the ARM processor; the accelerated implementation runs on the ARM processor, on which a Linux device driver communicates through an AXIM with the FPGA. Record the process time of each implementation for analysis.



Design D2:

Input the test vectors into the baseline implementation and the accelerated implementation. Each implementation runs on a common hardware: Avnet Ultrazed 3EG SOM. The software baseline runs on the ARM processor; the accelerated implementation runs on the ARM processor, on which a Linux device driver communicates through an AXIM with the FPGA. HDL verification using Cocotb and Aldec simulation engine will be used during the design and implementation of the accelerated version. Record the process time of each implementation for analysis.


test vectors
Baseline
ARM
C, Python
(common hardware)
Avnet Ultra96
3EG SOM
ARM
C, Python
Linux device driver
time
HDL verification
using
Cocotb python
and Aldec simulation
engine
FPGA
VHDL
Analysis
time