Signals and Circuits

ENGR 35500

Review

KENT STATE
UNIVERSITY

Final Exams

Date: Dec. 13, 2023 (Wednesday)

Time: 10:15 am-11:30 am

Closed book, closed note.
You only can have one A4 paper with two pages on which you can write anything. Of course, you can have some other blank papers for calculation.
Calculator is allowed. No cellphone or computer.

Final Exams

- Impedance and voltage about an AC circuit (15 points)
- Diode circuit problem (15 points)
- Transistor circuit problem (15 points)
- Number system problem(10 points)
- Boolean Algebra(15 points)
- Sequential circuit(10 points)
- Op-amp circuit (20 points)

Score

Requirement	Weight
Homework	20.0%
Quizzes	10.0%
Two Exams	63.0%
Attendance	7.0%
Total	100%

A	≥ 92%	C	≥ 71 and <74%
A-	≥ 88 and < 92%	C-	≥ 68 and <71%
B+	≥ 84 and < 88%	D+	≥ 64 and <68%
B	≥ 81 and < 84%	D	≥ 60 and <64%
B-	≥ 78 and < 81%	F	< 60.0
C+	≥ 74 and < 78%		

Note: students who have massive absences without excuse explanation (four times) will directly fail the class (-2 first time, -4 second time, -7 third time from the attendance points).

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Capacitor in AC

$$Xc = \frac{1}{2\pi f C}$$

Capacitive reactance for capacitors in series in AC

$$X_{CT} = X_{C_1} + X_{C_2} + \cdots + X_{C_n}$$

Capacitive reactance for capacitors in parallel in AC

$$\frac{1}{X_{CT}} = \frac{1}{X_{C_1}} + \frac{1}{X_{C_2}} + \frac{1}{X_{C_3}} + \cdots + \frac{1}{X_{C_n}}$$

Voltage divider in AC

$$V_x = \frac{X_{cx}}{X_{c1} + X_{c2} \cdots X_{cn}} V$$

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Inductor in AC

$$X_L = 2\pi f L$$

Inductive reactance for inductors in series in AC

$$X_{LT} = X_{L_1} + X_{L_2} + \cdots + X_{L_{1n}}$$

Inductive reactance for inductors in parallel in AC

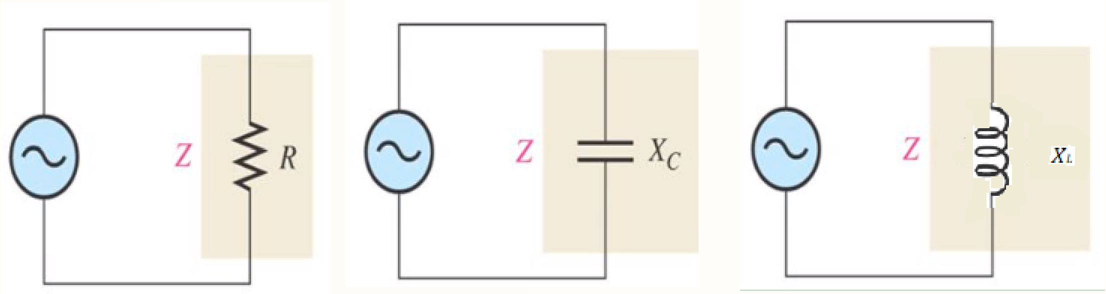
$$\frac{1}{X_{LT}} = \frac{1}{X_{L_1}} + \frac{1}{X_{L_2}} \cdots + \frac{1}{X_{Ln}}$$

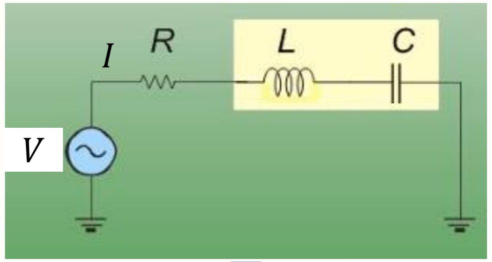
Voltage divider in AC

$$V_x = \frac{X_{L_1}}{X_{L_1} + X_{L_2} \cdots X_{L_n}} V$$

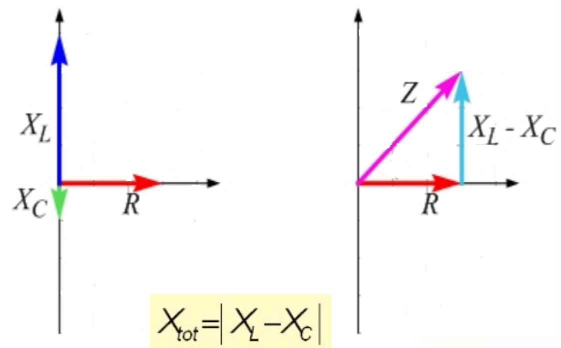
Impedance

Impedance and phase angle in RLC Series





Impedance triangle



$$X_{tot} = |X_L - X_C|$$

$$Z_{tot} = \sqrt{R^2 + X_{tot}^2}$$

$$\theta = \tan^{-1}\left(\frac{X_{tot}}{R}\right)$$

Purely resistor makes the phase angle between the source voltage and the total current zero degree;

Purely capacitor makes the voltage source voltage lags the current by 90 degree;

Purely inductor makes the voltage source voltage leads the current by 90 degree;

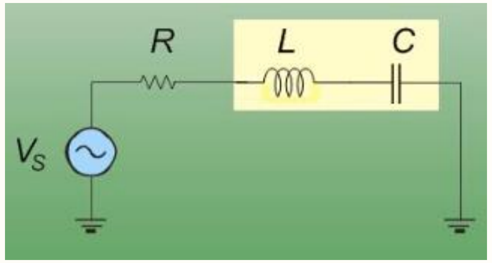
What will happen if resistor, inductor and capacitor are connected together in series?

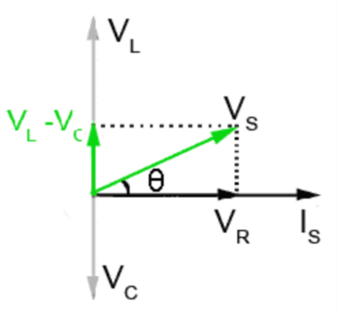
$voltage\ leads\ current\ by\ \theta\ if\ X_L > X_C$

$voltage\ lags\ current\ by\ \theta\ if\ X_L < X_C$

Figures: Text books; https://slideplayer.com/slide/6379082/

RCL voltage





$$V_R = \frac{RV_s}{\sqrt{R^2 + (X_L - X_C)^2}}$$

$$V_L = \frac{X_L V_s}{\sqrt{R^2 + (X_L - X_C)^2}}$$

$$V_C = \frac{X_C V_s}{\sqrt{R^2 + (X_L - X_C)^2}}$$

$$V_{LC} = \frac{|X_L - X_C| V_s}{\sqrt{R^2 + (X_L - X_C)^2}}$$

$Source\ voltage\ leads\ current\ by\ \theta\ if\ X_L > X_C$

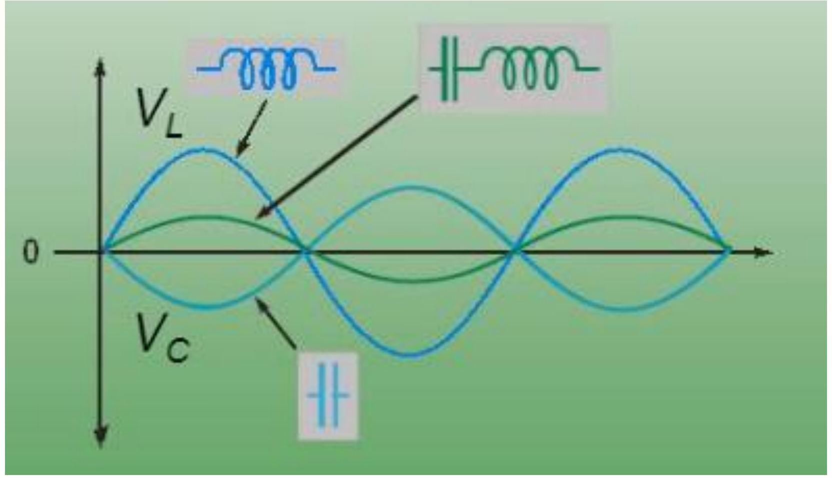
$Source\ voltage\ lags\ current\ by\ \theta\ if\ X_L < X_C$

Phase angel among I, V_R, V_L, V_C, and V_{LC}?

V_L and V_C always has 180 degree phase difference.

$E.G.$

$V_L > V_C$



Figures: https://slideplayer.com/slide/6379082/

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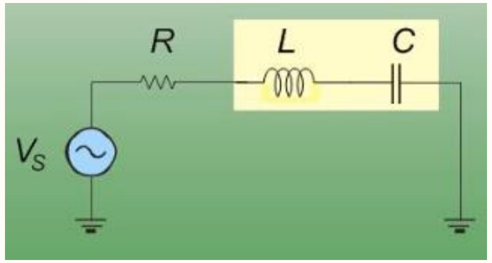
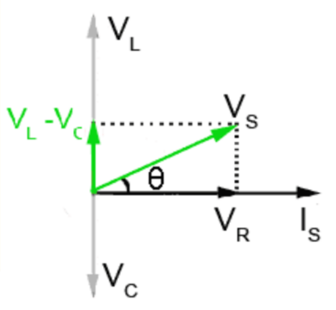
Resonance





V_C and V_L always has 180 degree phase angle

$$V_R = \frac{RV_s}{\sqrt{R^2 + (X_L - X_C)^2}}$$

$$V_L = \frac{X_L V_s}{\sqrt{R^2 + (X_L - X_C)^2}}$$

$$V_C = \frac{X_C V_s}{\sqrt{R^2 + (X_L - X_C)^2}}$$

$$V_{LC} = \frac{|X_L - X_C| V_s}{\sqrt{R^2 + (X_L - X_C)^2}}$$

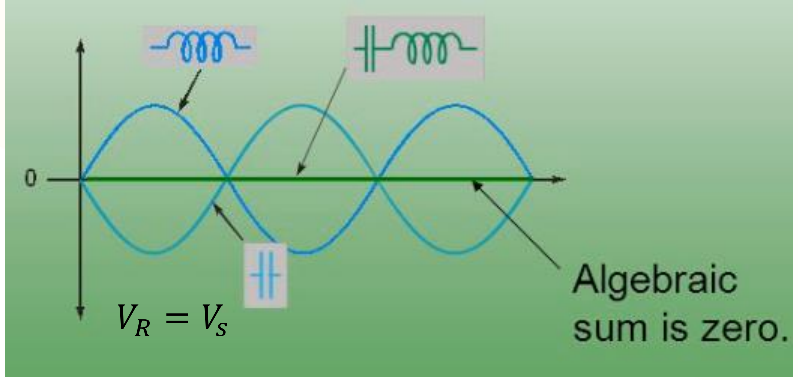
$Source\ voltage\ leads\ current\ by\ \theta\ if X_L > X_C$

$Source\ voltage\ lags\ current\ by\ \theta\ if X_L < X_C$

Phase angel among I, V_R, V_L, V_C, and V_{LC}?

$When\ X_L = X_C$?

Resonance



$$V_L = V_C = \frac{X_L V_s}{R}$$

$$V_{LC} = 0$$

$Source\ voltage\ leads\ current\ by\ 0\ degree$

$$Z = R$$

Figures: https://slideplayer.com/slide/6379082/

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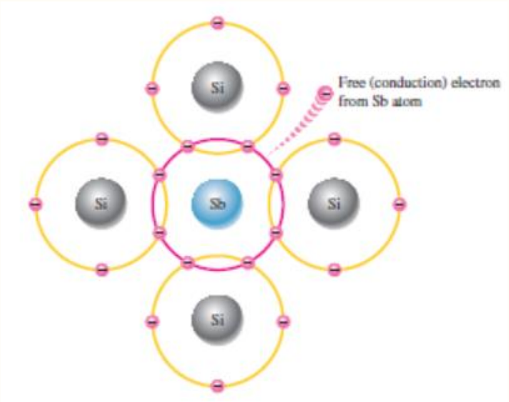
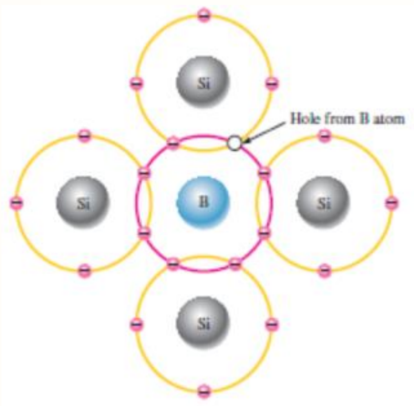
Diode



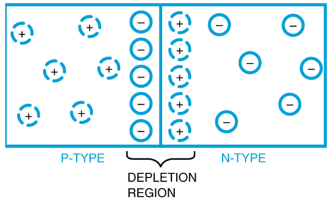
N-type semiconductor



P-type semiconductor

A semiconductor device with two terminals, typically allowing the flow of current in one direction only.

A junction diode is created by joining N- and P-type semiconductive materials together.



The depletion region is the area near the junction where electrons and holes are depleted; it extends only a short distance on either side of the junction.

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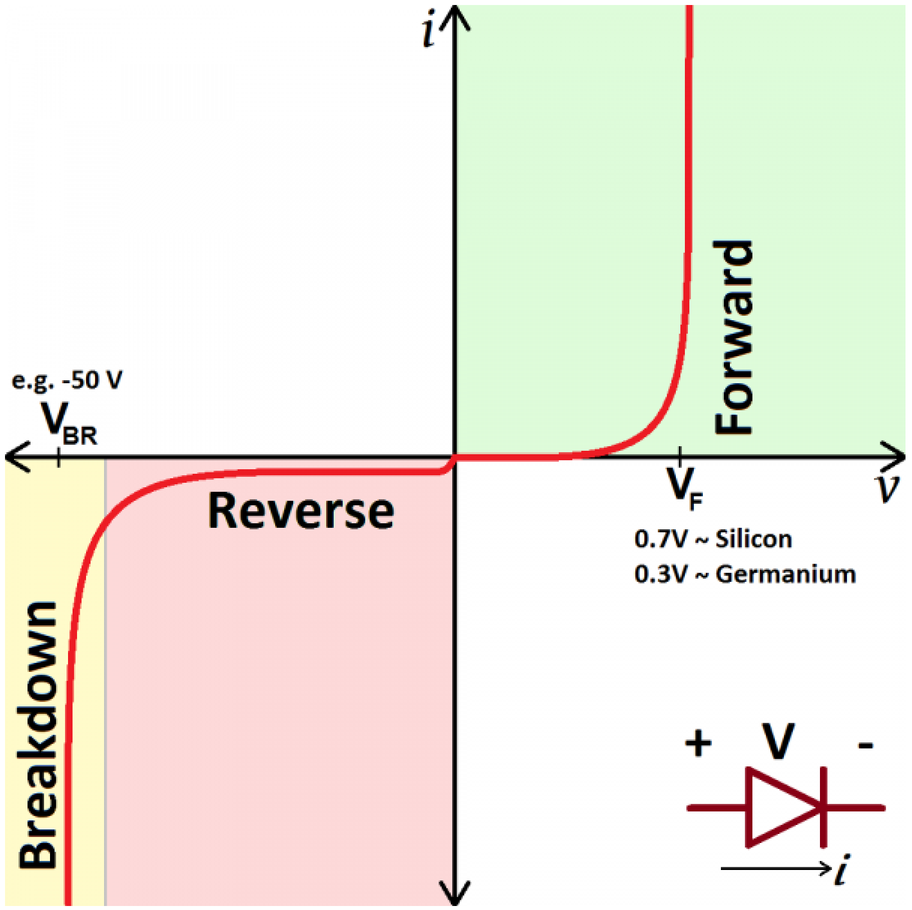
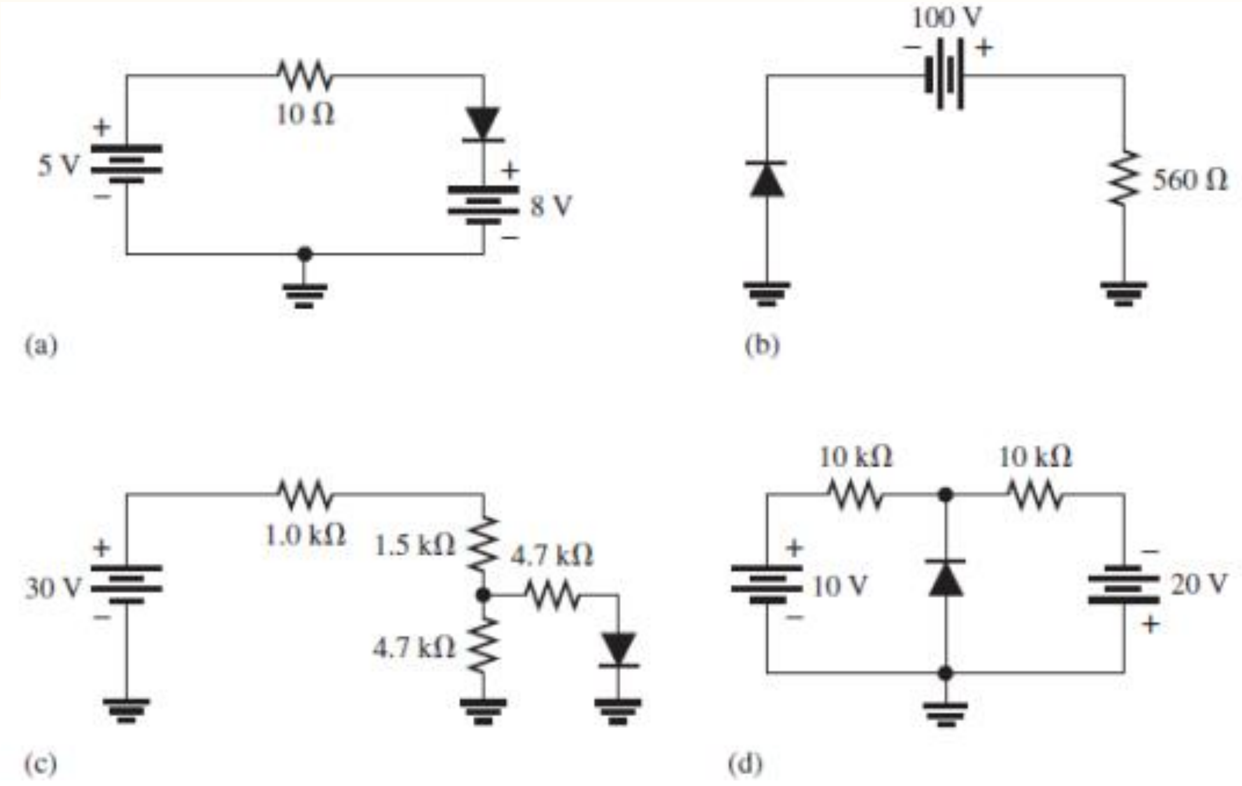
Diode characteristics



Diode

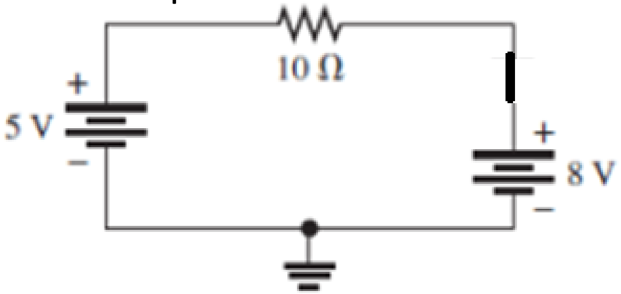
E.g.

Determine the voltage across each diode.



Step 1: Make assumption

Assume the diode is on forward bias, then there is a short on the diode part



Then the current

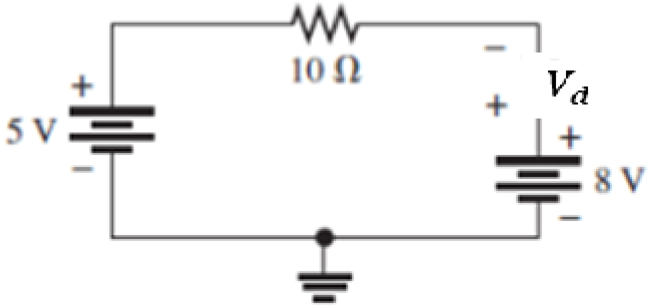
$$I = \frac{8-5}{10} = 0.3A$$

The assumed direction is counterclockwise

Step 2: Compare with the assumption

This is not consistent with the assumption, so the assumption is wrong.
Thus, the diode is on reverse bias.

Step 3: Calculate on the correct case



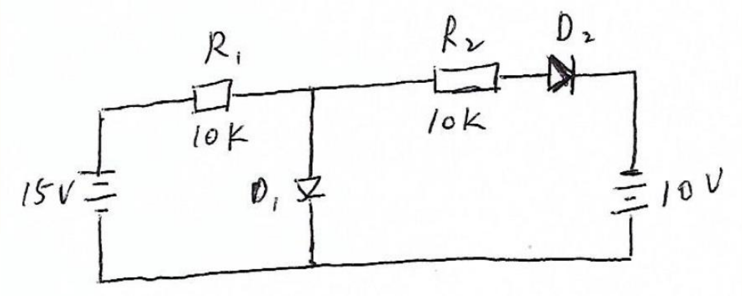
$$-5 - V_d + 8 = 0$$

$$V_d = 3\text{V}$$

Diode

E.g.

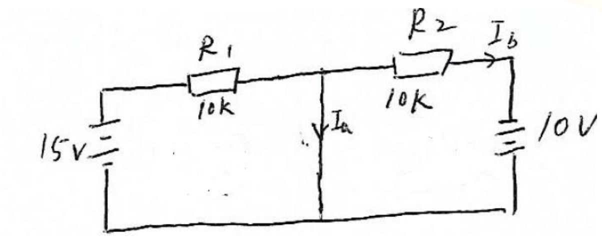
Determine the voltage across each diode



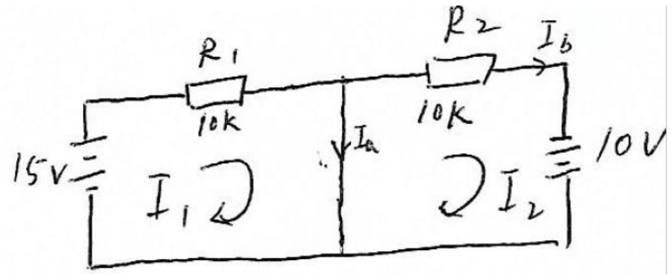
$$-15 + I_1 R_1 = 0$$
$$I_2 R_2 - 10V = 0$$
$$\Rightarrow I_1 = 1.5mA$$
$$I_2 = 1mA$$

Step 1: Make assumption

Assume the diodes are both on forward bias, then there is a short on the diode part



Mesh analysis



The current directions are both as drawn in the figure.

$$I_a = I_1 - I_2 = 0.5mA$$
$$I_b = I_2 = 1mA$$

Step 2: Compare with the assumption

This is consistent with the assumption, so the assumption is correct.

Thus, both of the diodes are on forward bias.

Step 3: Calculate on the correct case

$V_{d1} = 0V$ or 0.3v or 0.7v

$V_{d2} = 0V$ or 0.3v or 0.7v

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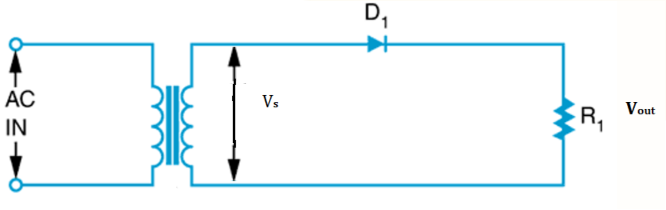
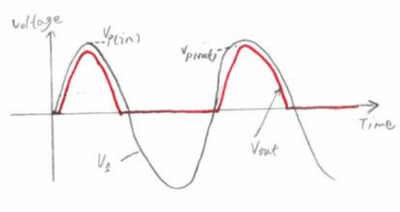
Rectifier Circuits

- The heart of the power supply.
- Converts incoming AC voltage to a DC voltage.
- Three basic types of rectifier circuits:

Half-wave rectifiers

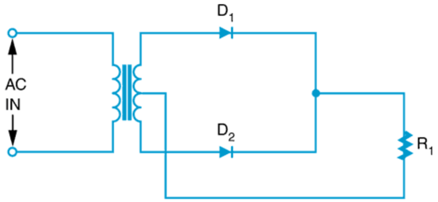


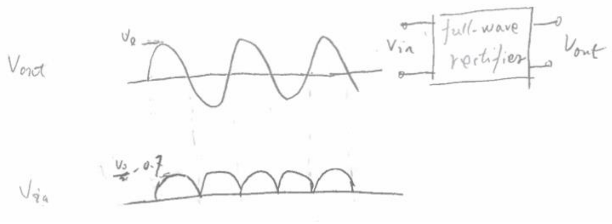


$$V_{avg} = \frac{V_{p(out)}}{\pi}$$

$V_{p(out)} = V_{p(in)}$-0.7V

Full-wave rectifiers

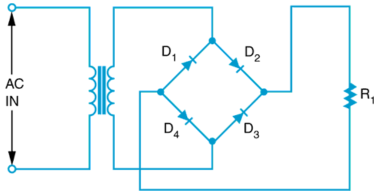


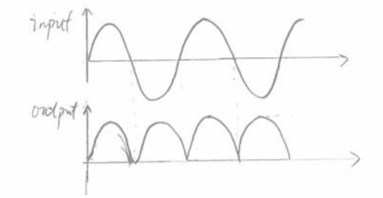


$$V_{avg} = \frac{2V_{p(out)}}{\pi}$$

$V_{p(out)} = \frac{V_{p(in)}}{2}$-0.7V

Bridge rectifiers

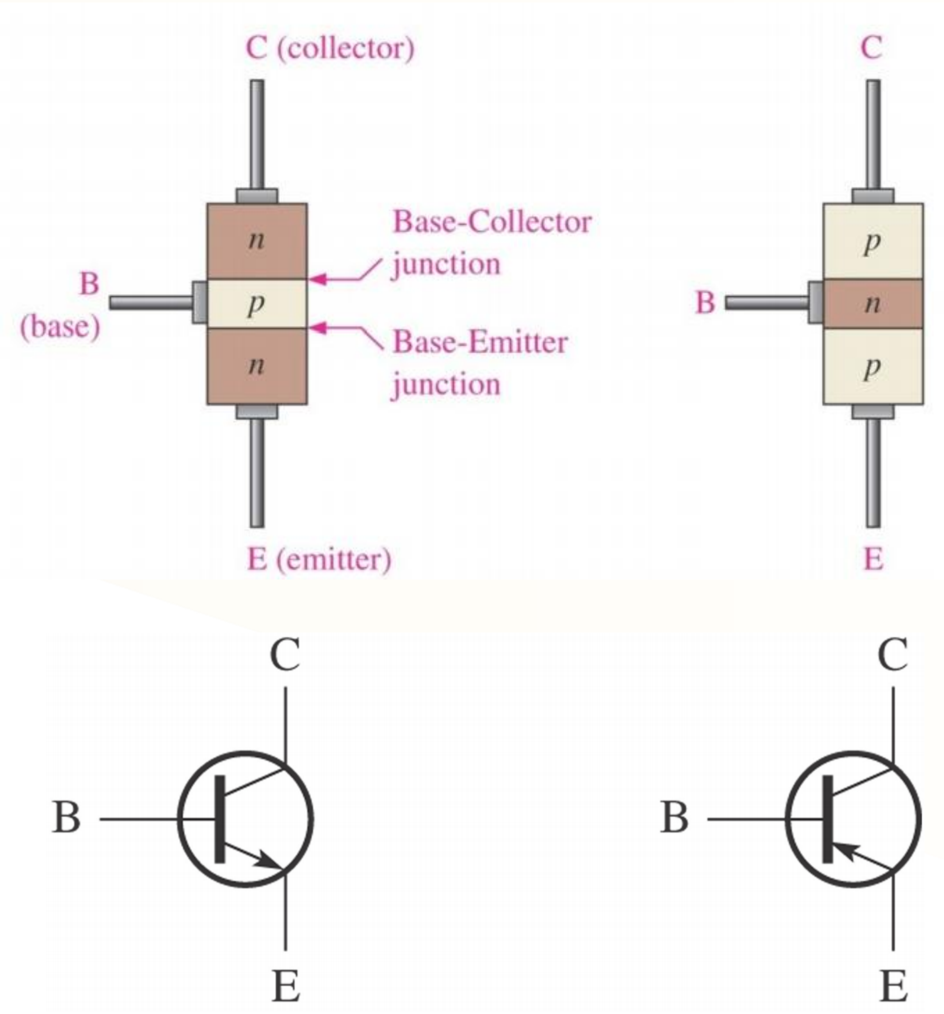




$$V_{avg} = \frac{2V_{p(out)}}{\pi}$$

$V_{p(out)} = V_{p(in)}$-0.7x2V

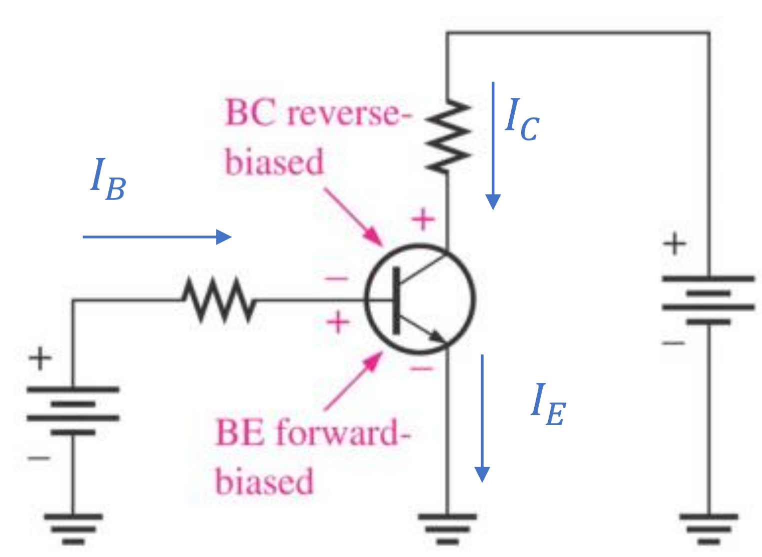
Transistor



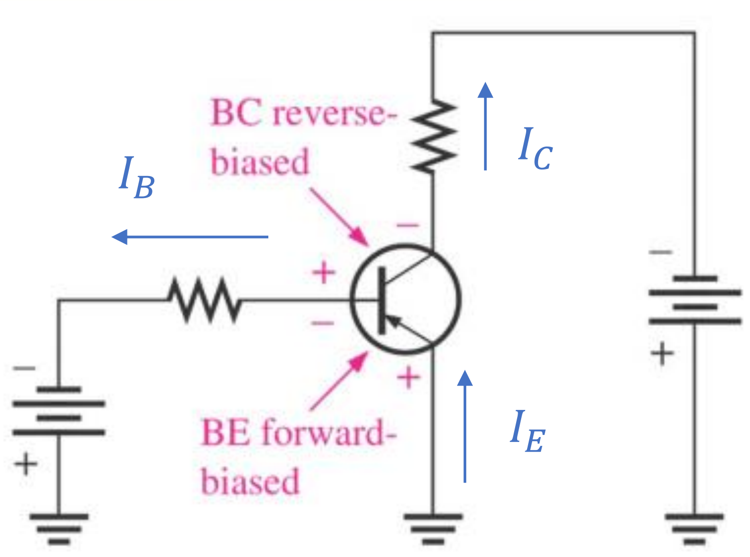
NPN

PNP

Transistor



NPN



PNP

If the transistor works in active region,

$$I_C = \beta I_B$$

$$I_E = I_C + I_B \qquad V_{CE} \geq 0$$

β~ 20 - 200 is determined by construction of the transistor

$$I_E \approx I_C$$

If the transistor works in saturation region,

$$I_C \leq \beta I_B$$

$$I_E = I_C + I_B$$

$$V_{CE} = 0$$

If the transistor works in cut-off case

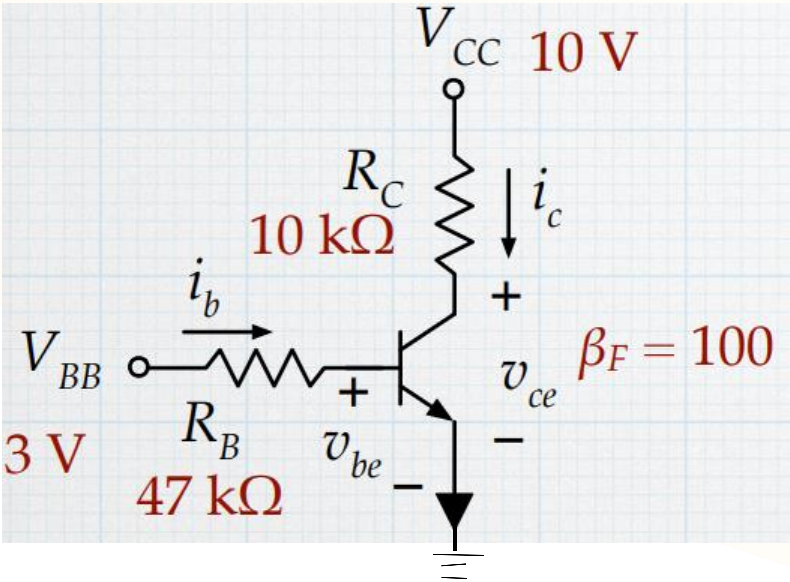
$$I_B = 0 \qquad I_C = 0$$

$$I_E = I_C + I_B = 0$$

$$V_{CE} = ?$$

Transistor in saturation

For example



$$i_B = \frac{V_{BB} - v_{BE}}{R_B} = \frac{3\text{ V} - 0.7\text{ V}}{47\text{ k}\Omega} = 48.9\,\mu\text{A}$$

$$i_C = \beta_F i_B = (100)\left(48.9\,\mu\text{A}\right) = 4.89\text{ mA}$$

$$\begin{aligned} v_{CE} &= V_{CC} - i_C R_C \\ &= 10\text{ V} - (4.89\text{ mA})\left(10\text{ k}\Omega\right) = -38.9\text{ V} \end{aligned}$$

???

Equations if in forward active region

Emitter voltage and Current

$$V_E = V_B - 0.7V$$

$$I_E = V_E / R_E$$

$$I_C = \beta I_B$$

$$I_E \approx I_C$$

$$I_B = I_C / \beta$$

Collector voltage: $V_C = V_{CC} - I_C R_C$

$$V_{CE} \approx V_C - V_E$$

$V_{CE} \geq 0$ (always)

Corrected solution:

$$i_B = \frac{V_{BB} - v_{BE}}{47k\Omega} = \frac{3v - 0.7}{47k\Omega} = 48.9\ uA$$

$$V_{CE} = 0$$

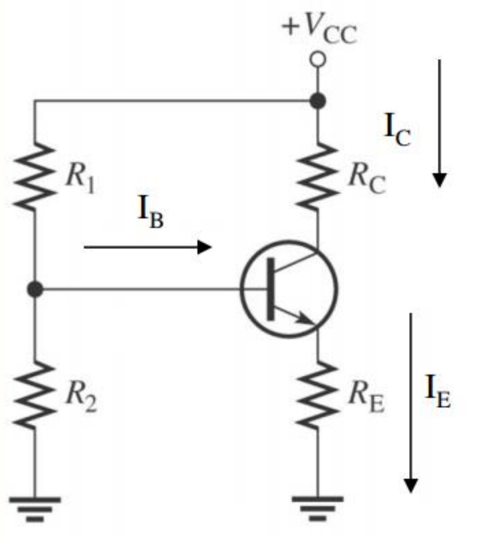
$$i_C = \frac{V_{CC} - v_{CE} - V_{EGroung}}{R_C} = \frac{10v}{10k\Omega} = 1000\ uA$$

$$i_E = i_B + i_C = 1048.9uA$$

DC Operation of BJTs

$E.g.$

$Determine\ V_B, V_E, V_C, I_B, I_E, I_C\ in\ the\ Figure, as\ \beta = 200,\ R_1 = 22k\Omega,\ R_2 = 10k\Omega,\ R_C = 1.0k\Omega,\ R_E = 1.0k\Omega,\ V_{CC} = 30V$



$$V_B = \frac{R_2}{R_1 + R_2} \times V_{cc} = \frac{10}{22 + 10} \times 30 = 9.375V$$

$$V_E = V_B - 0.7V = 8.675V$$

$$I_E = \frac{8.675V}{1kohm} = 8.675mA$$

$I_C \approx I_E$=8.675mA

$$I_B = I_C/\beta = \frac{8.675mA}{200} = 43.375\mu A$$

$$V_C = V_{CC} - I_C\, R_C = 30 - 8.675mA \times 1kohm = 21.325V$$

BJT Class A signal amplifiers

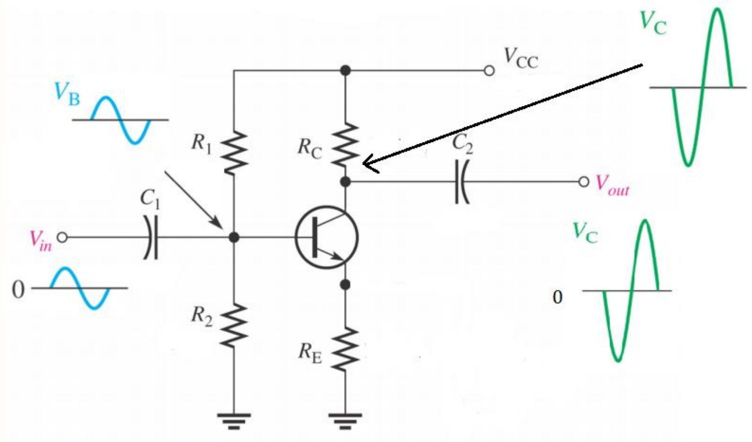
A **common-emitter** (CE) amplifier

– capacitors are used for coupling ac without disturbing dc levels

Signal Voltage Gain (A_V):

$$\frac{V_{out}}{V_{in}} \approx \frac{R_C}{R_E}$$

Actually the phase is shifted by 180 degree.



http://engineering.sdsu.edu/~johnston/ME204/Lecture_Notes/Transistors.pdf

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Numbering system

- Many numbering systems are in use in digital technology.

- The most common are the:

Decimal 537_{10}
Binary 101001_{2}
Octal 148_{8}
Hexadecimal $4BAF_{16}$

- To avoid confusion while using different numeral systems, the base of each individual number may be as specified by writing it as a subscript of the number.

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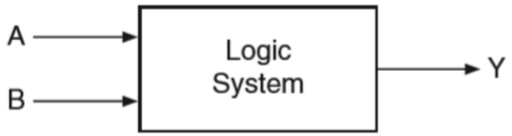
Logic Gates

- The most basic digital devices are called gates.
- A gate is called a combinational circuit.
- Three most important gates are: AND, OR, NOT.

- Other logic gates that are derived from these basic gates are the NAND gate, the NOR gate, the EXCLUSIVEOR gate and the EXCLUSIVE-NOR gate.



(a)

True table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(b)

Theorems of Boolean algebra

- Theorem 1

(Operations with '0' and '1')

$$\text{(a) } 0.X = 0 \quad \text{and} \quad \text{(b) } 1 + X = 1$$

- Theorem 2

(Operations with '0' and '1')

$$\text{(a) } 1.X = X \quad \text{and} \quad \text{(b) } 0 + X = X$$

- Theorem 3

(Idempotent or Identity Laws)

$$\text{(a) } X.X.X.\ldots.X = X \quad \text{and} \quad \text{(b)} X + X + X + \cdots + X = X$$

- Theorem 4

(Complementation Law)

$$\text{(a) } X.\overline{X} = 0 \quad \text{and} \quad \text{(b) } X + \overline{X} = 1$$

- Theorem 5

(Commutative Laws)

$$\text{(a) } X + Y = Y + X \quad \text{and} \quad \text{(b) } X.Y = Y.X$$

- Theorem 6

(Associative Laws)

$$\text{(a) } X + (Y + Z) = Y + (Z + X) = Z + (X + Y)$$

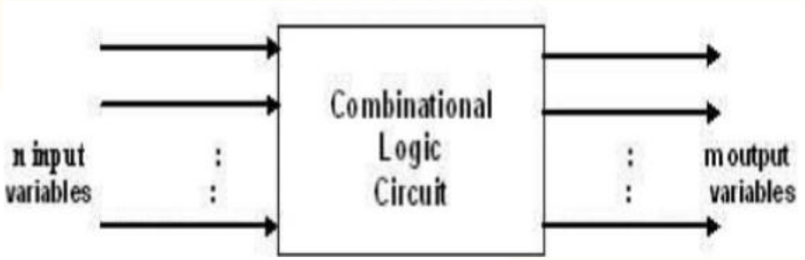
$$\text{(b) } X.(Y.Z) = Y.(Z.X) = Z.(X.Y)$$

- Theorem 7

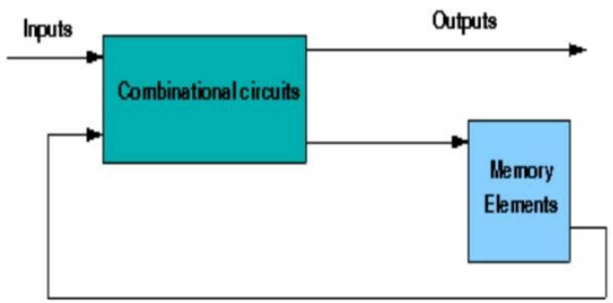
(Distributive Laws)

$$\text{(a) } X.(Y + Z) = X.Y + X.Z \quad \text{and} \quad \text{(b) } X + Y.Z = (X + Y).(X + Z)$$

Sequential Circuits



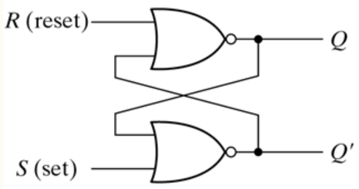
Combinational
circuit



sequential circuit

Asynchronous

SR Latch

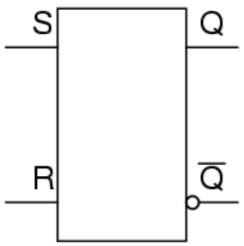


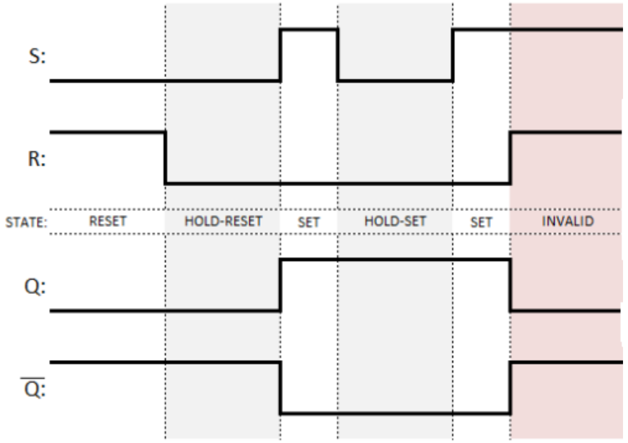
(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

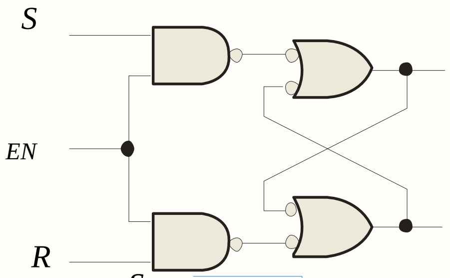
(b) Function table

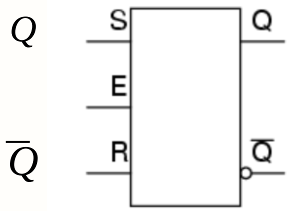
SR Latch with NOR Gates

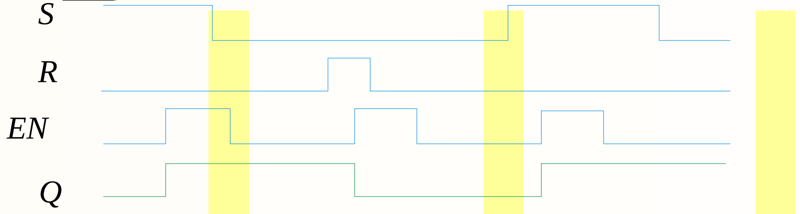




Gated SR Latch

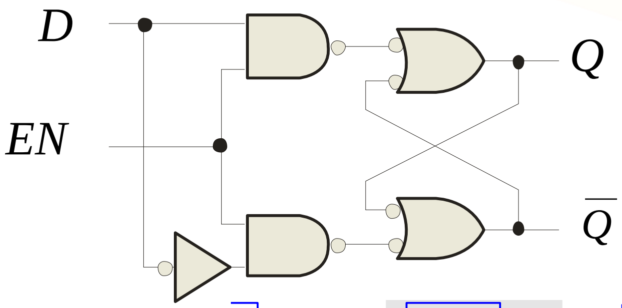


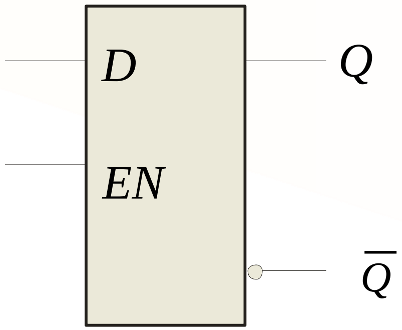


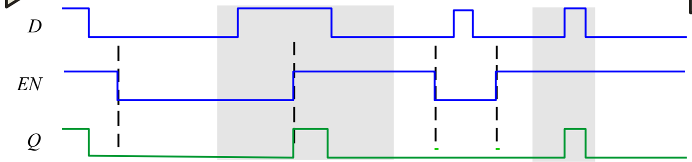


D Latch

The *D* latch is an variation of the *S*-*R* latch but combines the *S* and *R* inputs into a single *D* input as shown:



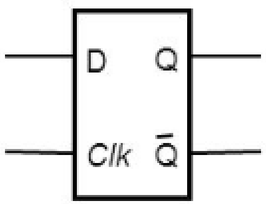




Synchronous

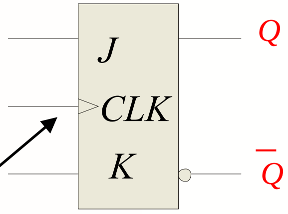
D Flip-Flops

A flip-flop differs from a latch in the manner it changes states. A flip-flop is a clocked device, in which only the clock edge determines when a new bit is entered.

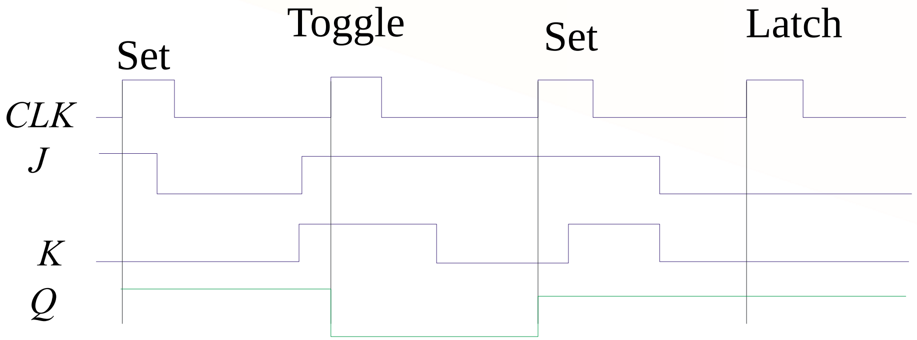


J-K Flip-Flops

Inputs			Outputs		Comments
J	K	CLK	Q	$\bar{Q}$	
0	0	↑	Q_0	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle



Notice that the outputs change on the leading edge of the clock.



What is an Operational Amplifier? (sum up)

An operational amplifier is a DC-coupled high gain electronic voltage amplifier with a differential input and usually, a single-end output. (Wikipedia)

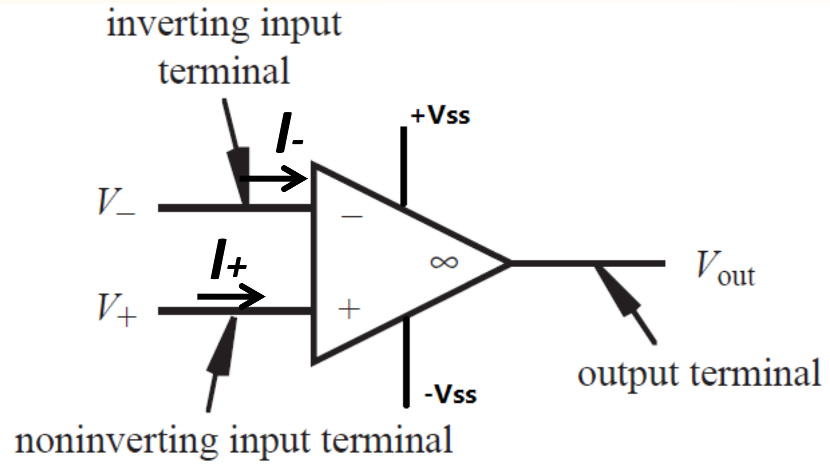


Fig.2. Op-amp schematic representation (open-loop)

VS

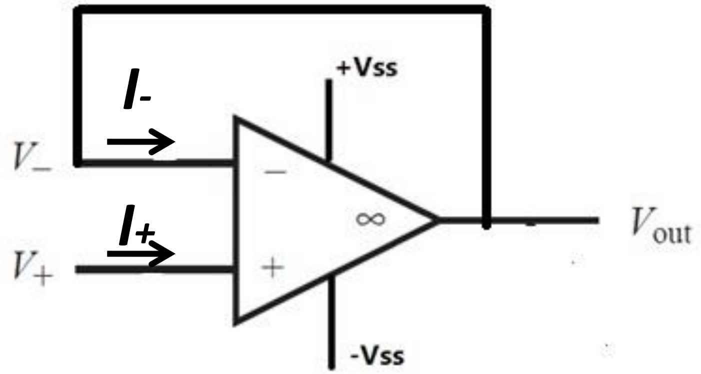


Fig.3. Op-amp schematic representation (closed-loop)

$$V_{out} = \begin{cases} +V_{ss} & V_+ > V_- \\ -V_{ss} & V_- > V_+ \end{cases}$$

Golden Rule 2:

$$I_+ = I_- = 0$$

Golden Rule 1:

$$V_+ = V_-$$

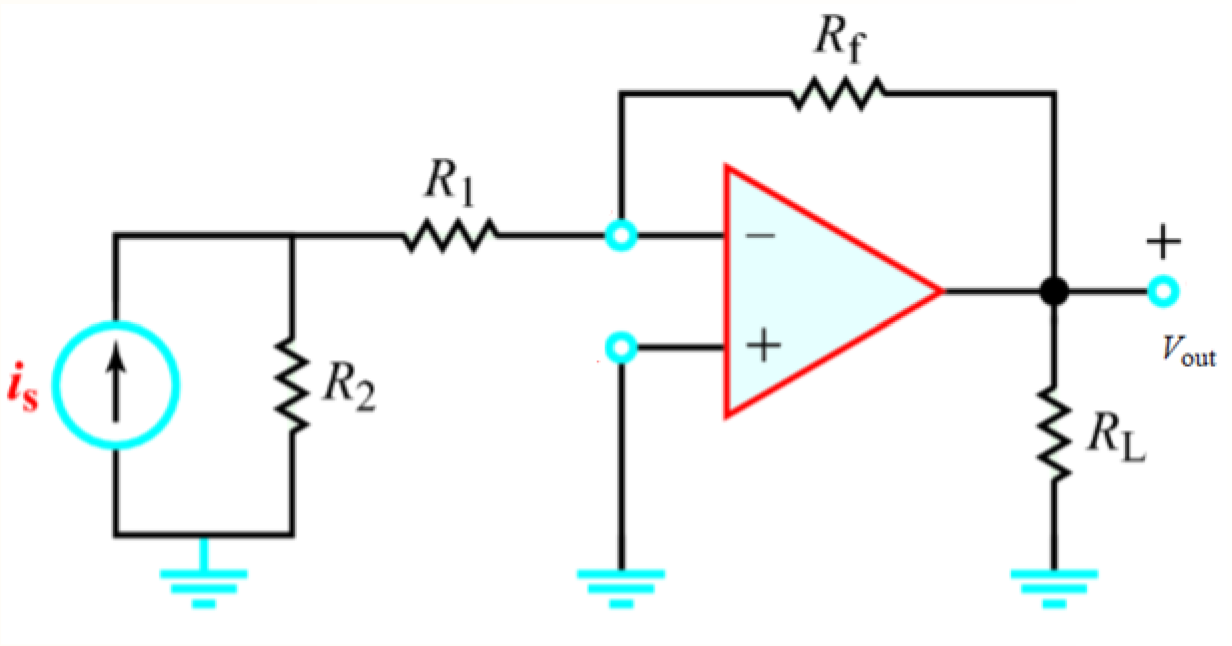
Golden Rule 2:

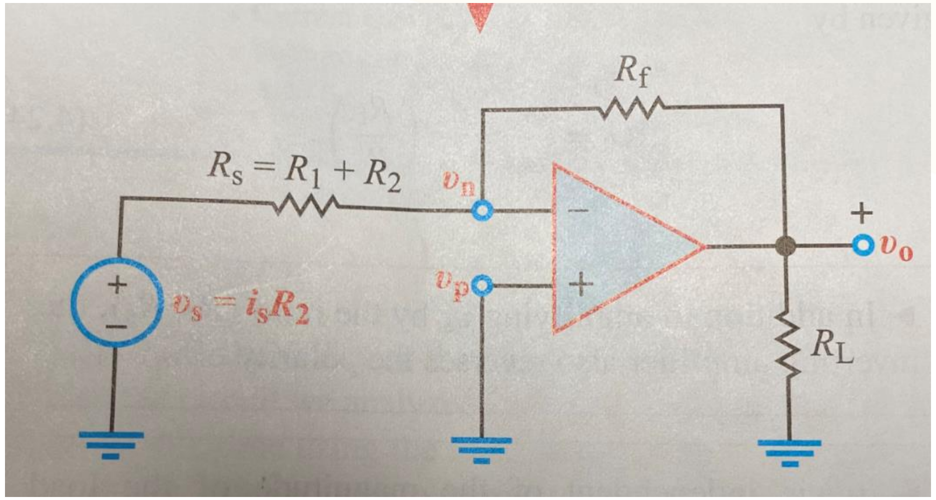
$$I_+ = I_- = 0$$

Op-Amp Application

Practice

Given i_s=1mA, R_1=1kΩ, R_2=2kΩ, R_f=30kΩ, R_L=10kΩ, determine V_{out}





$$v_o = -\left(\frac{R_f}{R_1 + R_2}\right) v_s = -\left(\frac{R_f}{R_1 + R_2}\right) R_2 i_s.$$

$$\frac{v_o}{i_s} = -\frac{R_f R_2}{R_1 + R_2}.$$