Design of an 64x12 SRAM Array in 65nm technology

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***Abstract*— The aim of this project is to build a 64-row by 12-bit SRAM memory array, using the 65nm CMOS technology. SRAM Peripherals as address decoder, column decoder, sense amplifier, precharge circuit and write drivers were implemented as well.**

I. Introduction

6T SRAM refers to a type of static random-access memory (SRAM) that uses six transistors per memory cell. This technology is widely used as Cache memory in microprocessors, embedded systems, and other digital devices due to its fast access time, low power consumption, and high-density storage capabilities. With 6T SRAM, each memory cell can store a single bit of data, and the six transistors act as an electronic switch that allows data to be written or read. This memory technology is critical for the operation of modern computing systems, and continues to be an essential component of many electronic devices.

II. System Overview

The 6T SRAM consists of 6 transistors that are ratioed hence the read and write operations are done properly, in this design a size ratio of 3-2-1 for PDN-Access-PUN respectively was used after careful considerations. The SRAM array consists of 64 rows each row consists of 12 bits hence each row consists of 12 6T SRAM cells with a total size of the array of 768 cells. Address decode (known as row decoder) was used to access the worldline for certain word (row) for a 64 words the address decoder is conventionally a 6 to 64 decoder but in this design a 16 to 64 address decoder was implemented which less power efficiency and more number of pins on chip, similarly for the column decoder since 12 columns won't give an integer number of address bits, in this design a 4 to 16 decoder was used with setting 4 of the 16 outputs to ground, hence it will reduce the number of pins on the chip from 12 to 4. Precharge circuit for the 12 bit lines and 12 bit line bars was implemented to charge the design to VDD before the read operation to avoid logic flipping. A Sense amplifier and write drivers for the 12 bit lines and 12 bit line bars were implemented, where the bit lines from the column decoder are connected to both write drivers and sense amplifiers and depending on the address input signal, the column selection circuit selects the required columns on which read or write operations are performed, a read operation is performed by sense amplifiers to speed up the read operation by amplifying the voltage difference between Bl and BL_B, and a write operation is performed by the write drivers.

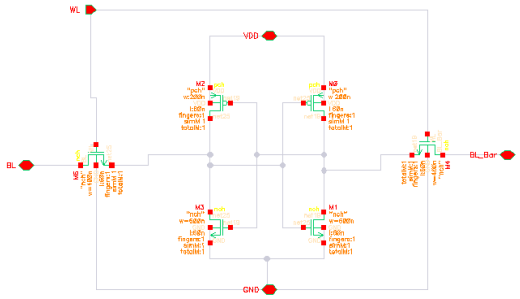

Figure 1. Schematic for one unit SRAM cell, the used ratio is 3-2-1.

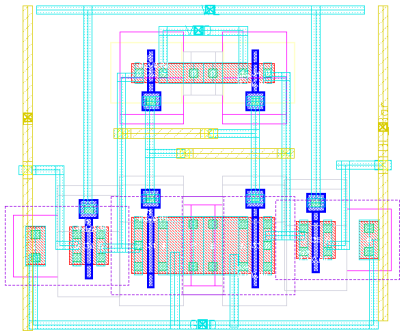

Figure 2. The 3-2-1 unit SRAM layout with layout area of 13.6 um^2.

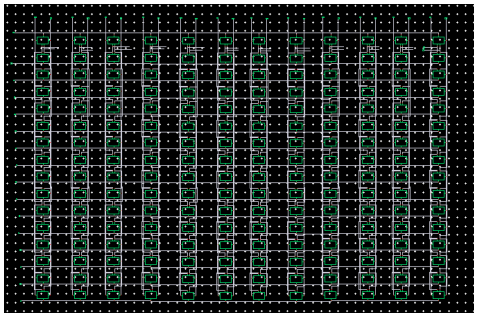

Figure 3. Schematic for the 16x12 SRAM array as a building block for the 64x12 SRAM array.

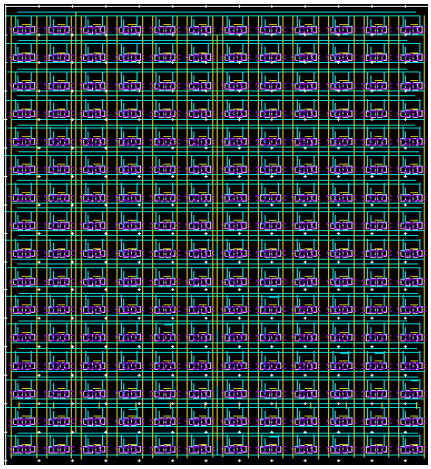

Figure 5. Layout for 16x12 SRAM array.

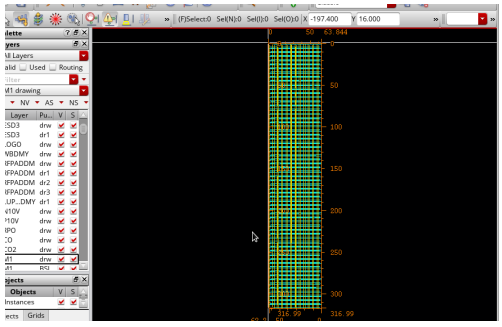

Figure 6. The full 64x12 SRAM array layout with layout area of 20k um^2.

III. SRAM Peripherals.

For proper accessing, sensing, and testing for the SRAM some peripherals are needed so the following peripherals were implemented, tested and layout for the whole 64x12 SRAM array: Bus of Precharge circuit, 64 output row decoder, 12 bit output column decoder, sense amplifier, and write drivers.

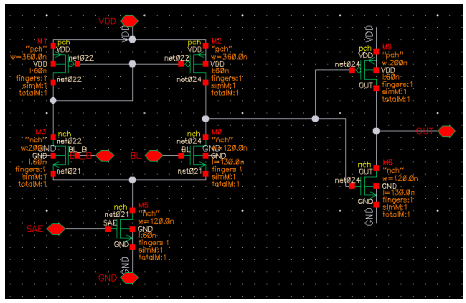

Figure 8. Sense amplifier for testing the voltage difference between BL and BL_B and amplifying it for overcoming the noises from parasitics on the lines then gives the output of the read operation.

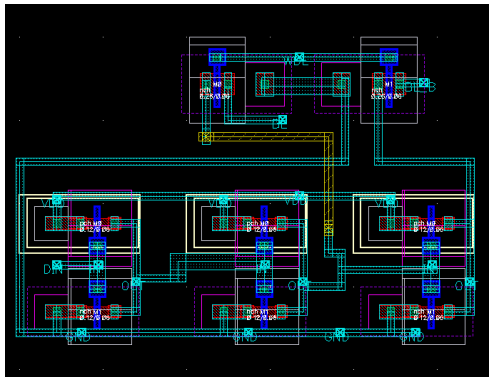

Figure 9. Write driver layout.

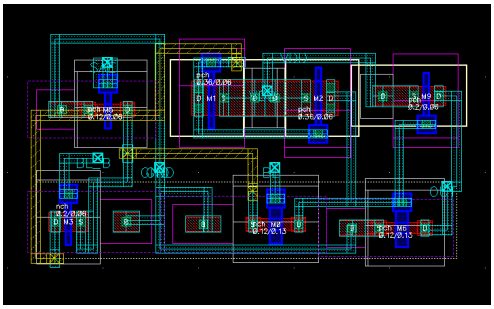

Figure 10. Layout for the sense Amplifier.

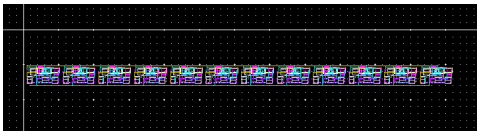

Figure 11. Layout for the sense amplifier bus for the 12 bit line and 12 bit line bars.

Figure 12. PEX for the 64x12 array.

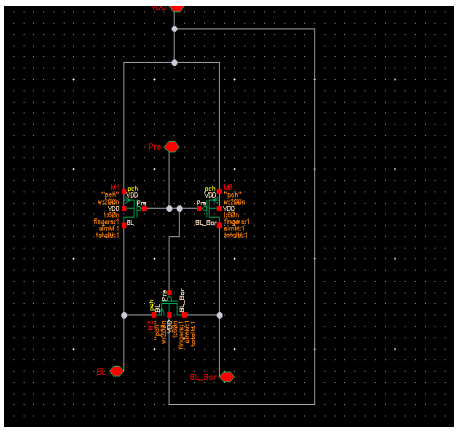

Figure 13. Precharge circuit for charging BL and BL_B to VDD before the read operation to avoid logic flipping.

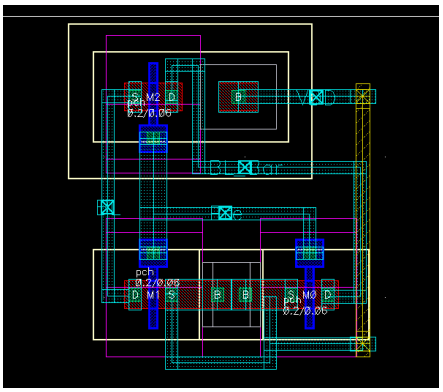

Figure 14. layout for the precharge circuit.

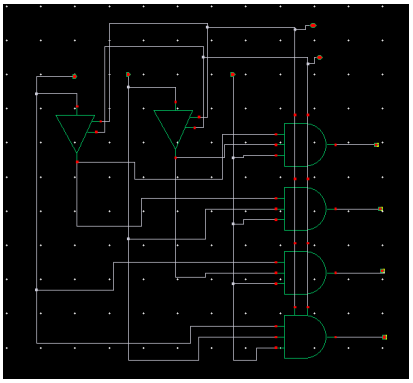

Figure 15. Schematic of the 2:4 decoder that is the building block for the hereditary address and column decoder.

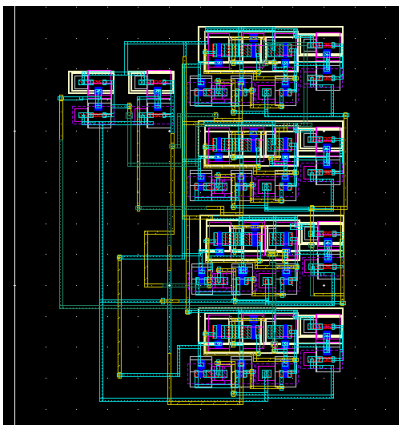

Figure 16. Layout for 2:4 decoder.

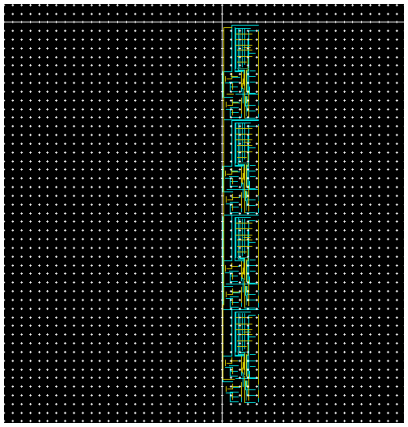

Figure 17. Layout for the Address decoder constructed from the lower 4:16 decoder that is constructed from the lower 2:4 decoder, the address decoder contains 64 outputs for the 64 word lines.

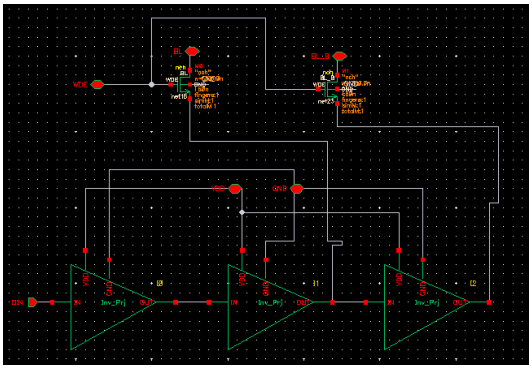

Figure 18. The schematic for the write driver.

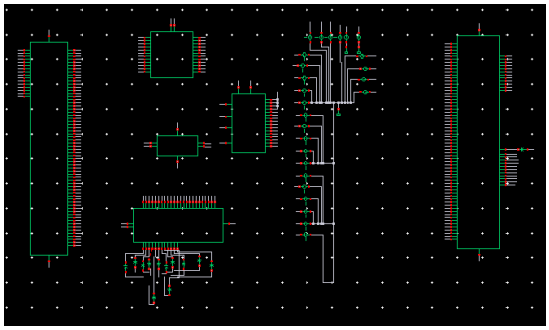

Figure 19. Test bench for the 64x12 SRAM

IV. Simulation Results

	Pre layout	Post layout
Write 1 delay	84.32p sec	93.72p sec
Write 0 delay	82.14p sec	102p sec
Read 1 delay	296.3p sec	577p sec
Read 0 delay	350.1p sec	601.35p sec
Average Write 0 power	1.563m watt	10.12m watt
Average Read 0 power	338.8u watt	25.11m watt
Average Write 1 power	1.906m watt	1.921m watt
Average Read 1 power	450.1m watt	645.2m watt
Average read delay	323.2p sec	589.175p sec
Average write delay	83.23p sec	97.86p sec
Average Read power	322.7694m watt	512.055m watt
Average write power	1.7345m watt	17.615m watt

Table 1. Simulation results.

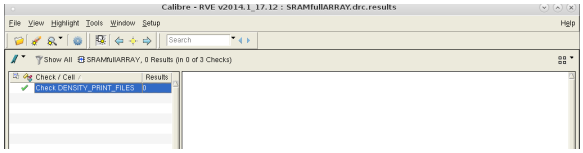

Figure 20. DRC clean

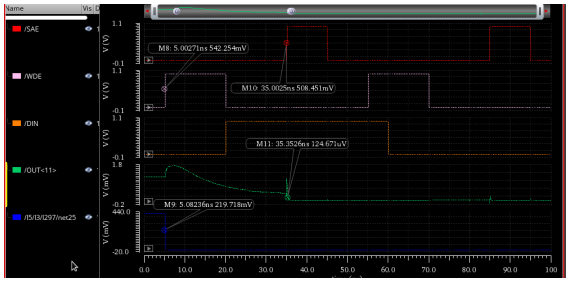

Figure 21. Delay in Reading and writing 0.

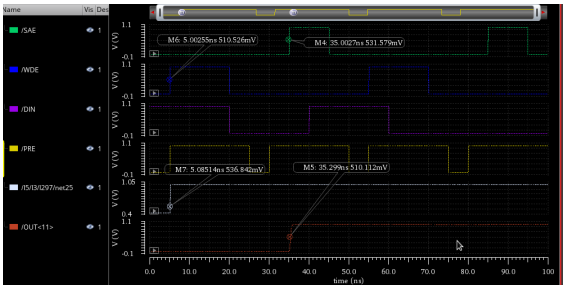

Figure 22. Delay Reading and Writing 1.

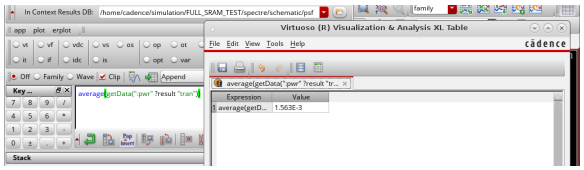

Figure 23. The used function for power calculations .

The figure of Merit $= P * delay^2 * Area$

FOM =

645.2*10^-3*(601.35*10^-12)^2*20000*10^-12

FOM = 4.66*10^-27 watt.sec.m^2

V. Conclusion

6T SRAM and its peripherals has many applications due to its speed and small power dissipations hence it has been extensively investigated and lots of modifications have been made to that initial design, even though the 6T SRAM essential design is still properly functioning as shown in the above report.

VI. Appendix

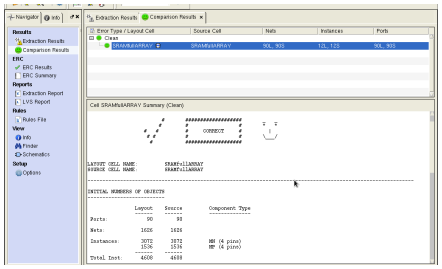

Figure 24. LVS is correct.