Analog Integrated Circuit Design - FALL2022-NANENG-421-LCTR-01.

Two stages Miller compensated OTA

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Introduction:

In this project we use the cadence virtuoso simulation tool to test the pre-layout and post-layout simulation for the two stages Miller compensated OTA with the first stage differential input and single ended output while the second stage is common source with active load, we are required to satisfy certain certain specifications regard the OP-Amp, this specifications is as shown in table 1.

V_{DD}	1.2V
GND	0V
Bias Circuit M12	90 μA
C_L	$0.2pF$
Nominal Input Common-mode (Input DC level)	0.7V
Nominal Output Common-mode (Output DC level)	0.7 ± 0.1V
Overall power consumption including the bias circuit	$\leq 2mWatt$
Output peak to peak swing	0.7V
Low frequency differential to single ended gain	$\geq 40dB$
Unity gain frequency	300MHz
Phase margin	$\geq 50°$
Slew rate	$\geq 9V/\mu s$
Maximum length of transistors	$5\times L_{min}$

Table 1. The design specifications.

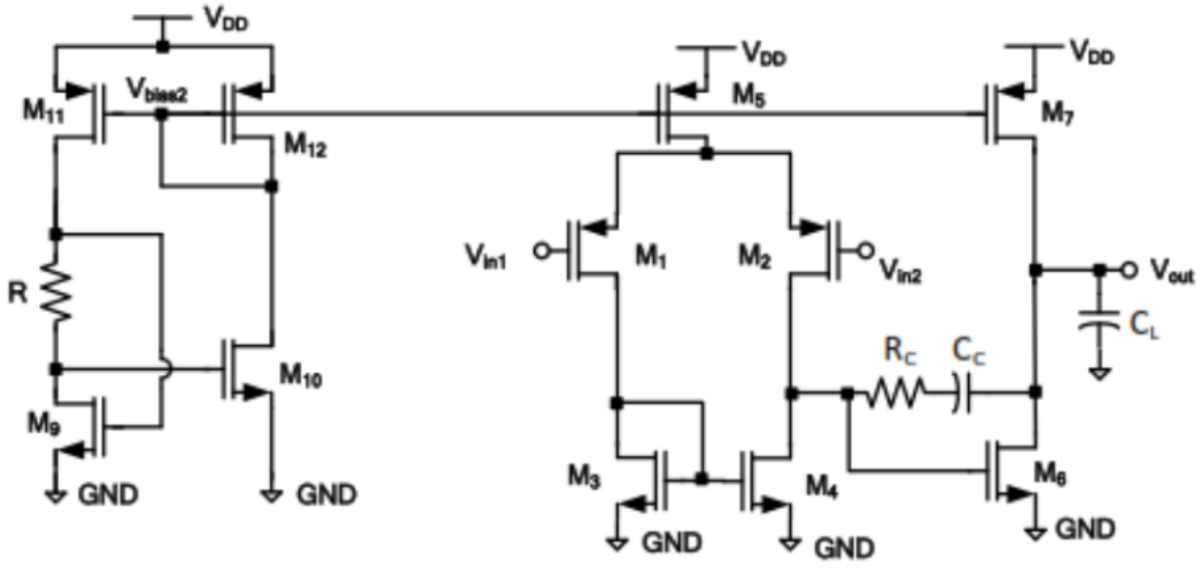


Figure 1. The OP-Amp design required.

The project flow went as follows:

Firstly we used the g_m/I_D design methodology as follows , we set theoretical equations for the circuit and put the specifications in table 1. In the equations to determine the g_{ds}/g_m and W/I_D for the transistors caring the input signal in both stages, after determining the g_m/I_D that would satisfy the specifications in both stages we used cadence library tsmc65 to sweep on the range of allowed length from 65 nm :325 nm , then get the graphs of g_{ds}/g_m and W/I_D Vs g_m/I_D and specify the length and width for the transistors caring the input signal in both stages (hence we perform the sweep on PMOS symbol for stage one and again on NMOS for stage 2), by now we have the length and width of the transistors caring the input signal and would fulfill the requirements.

Secondly we now build the circuit schematic on cadence and performing DC analysis to make sure all transistors are in saturation before performing the AC analysis and introducing the differential input signal, since we are forced to use VDD equal to 1.2V, the only remaining aspect that still has some degree of freedom is to change the length and width of the transistors till putting them in saturation. The strategy followed was as follows: since the whole branch is powered by 1.2V hence we need to divided this 1.2V in such a way that all the transistors in the branch have $V_{ds} \geq V_{gs} - V_{th}$,and we know that from the current saturation equation $V_{ds} \alpha \frac{L}{W}$, hence there are two cases : I. A transistor is not in saturation hence we increase its length and decrease its width, II. A transistor is not in saturation and carrying the input signal to the stage hence constrained to specific length and width for the gain, in this case we will change the length and width of the other transistors in the branch in reverse way to decrease the voltage drop on the other saturated transistors in that same branch hence increase the drop Vds on the transistor we need to put in saturation.

Thirdly we now are ready to perform AC analysis and satisfy all the requirements by sweeping on all the affecting parameters.

Part 1. The pre-layout simulation:

1. The theoretical Analysis:

Pmos "Stage one calculation of input transistors length and width"

- Satisfying the Bandwidth:

$F_u = 700MHz,\ SR = 500V/\mu s\ ,C_c = 0.5C_l$

$F_u = \frac{g_{m1}=g_{m2}}{2\pi C_c} \Rightarrow g_{m1} = 700 * 10^6 * \frac{44}{7} * 10^{-13} = 440\ \mu A/V$

$SR = \frac{I_B}{C_c} \Rightarrow I_B = 500 * 10^6 * 0.1 * 10^{-12} = 50\mu A$

$I_D = 0.5I_B = 25\ \mu A$

$\frac{g_{m1}}{I_D} = 17.6\ V^{-1}$

- satisfying the gain:

Solving for a total gain of 60dB.

Assuming that stage one gain is double the total gain.

Hence $A_1 \times \frac{A_1}{2} = 10^{60/20} \Rightarrow A_1 = 20\sqrt{5}$

Hence $\frac{g_{m1}}{g_{ds}} = 2 * A_1 = 40\sqrt{5}$

$\frac{g_{m1}}{g_{ds}} = 40\sqrt{5}$ $\frac{g_{m1}}{I_D} = 17.6\ V^{-1}$

NMOS "Stage two calculation for input transistors' length and width"

- Satisfying that current in second stage is 4 times current in first stage:

$\frac{G_{m2}}{C_c} = \frac{4G_{m1}}{C_l} \Rightarrow g_{m6} = 2g_{m1} = 880\ \mu A/V$

$I_{B2} = 4I_{B1} \Rightarrow I_{B2} = 4 * 50 * 10^{-6} = 200\ \mu A$

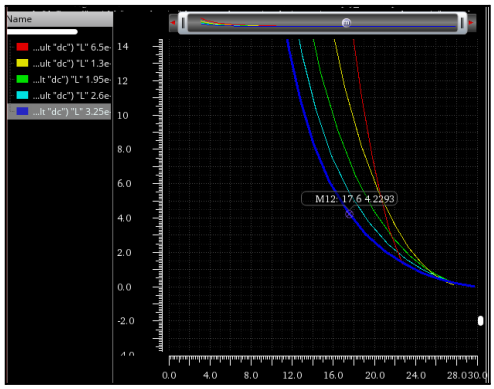
- satisfying the gain:

$A_2 = \frac{A_1}{2} = 10\sqrt{5}$

$\frac{g_{m6}}{g_{ds6}} = 20\sqrt{5}$

$\frac{g_{m6}}{g_{ds6}} = 20\sqrt{5}$ $\frac{g_{m6}}{I_D} = 4.4\ V^{-1}$

2. Sweeping on the length to determine the length and width that would satisfy our specifications using g_m/I_D design strategy.



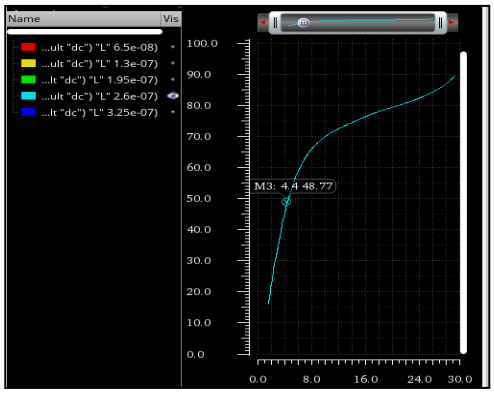
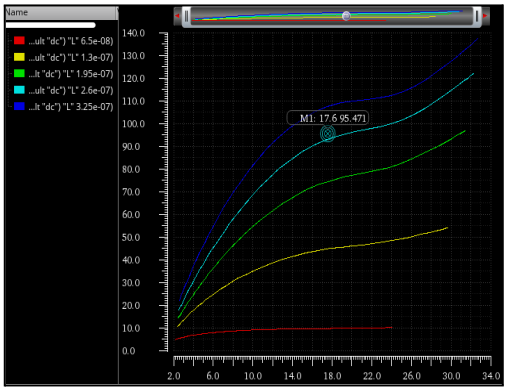


Figure 2 & 3. The I_D/W and g_{ds}/g_m respectively Vs g_m/I_D for NMOS , finding that the suitable length and width for the NMOS transistor carrying the input signal in stage two are 260 nm and 17.9 um respectively .



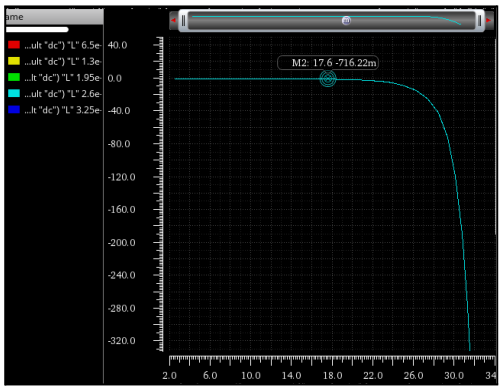


Figure 4 & 5. The I_D/W and g_{ds}/g_m respectively Vs g_m/I_D for PMOS , finding that the suitable length and width for the PMOS transistor carrying the input signal in stage one are 260 nm and 16.8 um respectively .

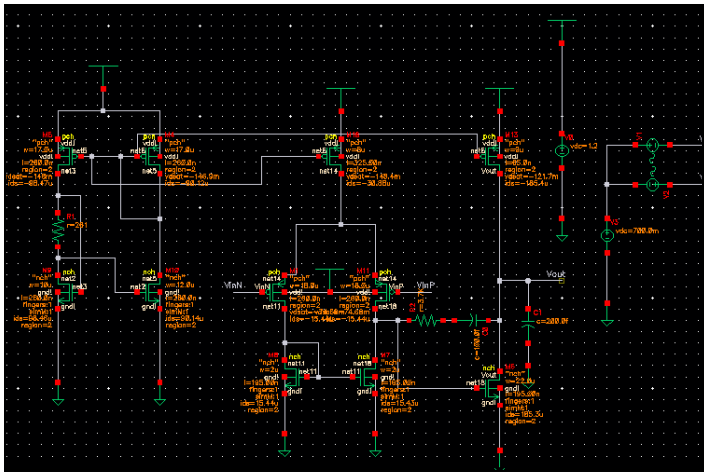
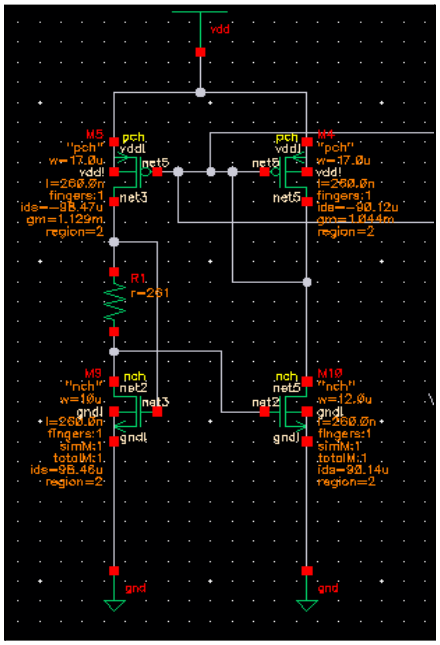


Figure 6. The DC analysis and all transistors are in saturation.

3. Fulfilling the pre-layout specifications:



1. The current in M4 in the bias circuit is required to be 90 uA, the current follows the following formula $I_{out} = \frac{1}{\mu_n C_{ox} R^2}\left[\sqrt{\left(\frac{L}{W}\right)_9} - \sqrt{\left(\frac{L}{W}\right)_{10}}\right]^2$, hence we swept on R and W(10) till achieving the required current value.

Figure 7. The current in the bias circuit is 90uA as required.

2. Fulfilling the requirement that the unity gain frequency should be more than or equal to 600MHz.

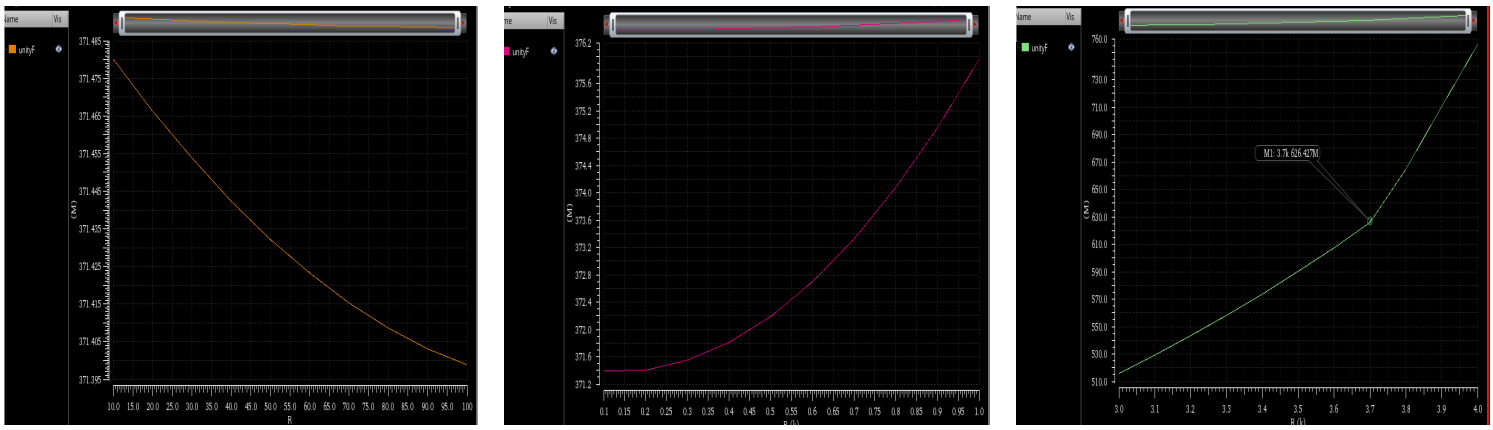


Figure 9,10 & 11. Sweeping on Rc till finding the suitable Rc that will fulfill a unity gain frequency of 600MHz, the chosen value is 3.7K Ω.

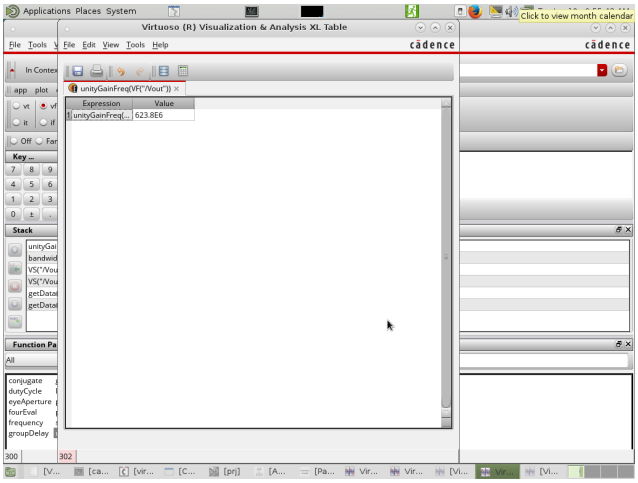


Figure 12. The unity gain frequency is 623.8MHz

3. Fulfilling that the gain in dB must be more than or equal to 40dB:

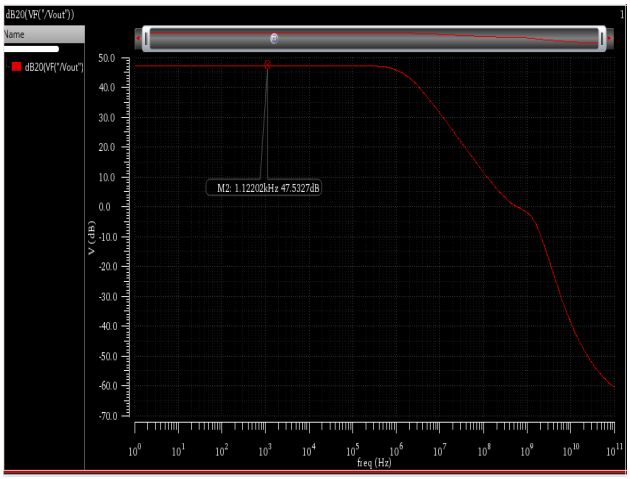


Figure 13. The gain is 47.5327 dB.

4. Fulfilling that the phase margin must be more than or equal to 50 degrees.

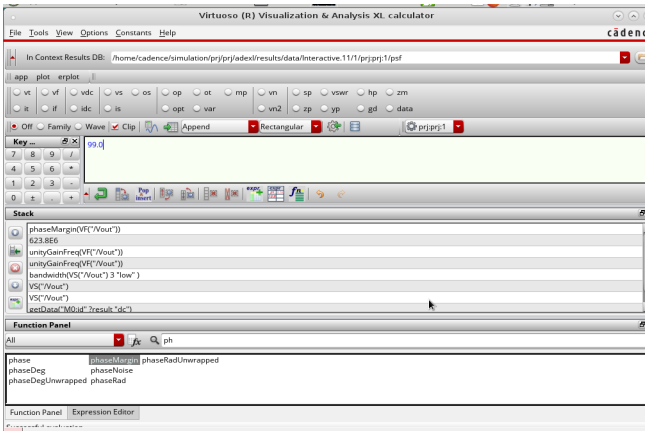


Figure 14. The phase margin is 99°.

5. Fulfilling the requirement that the slew rate is equal to or greater than 9V/us .

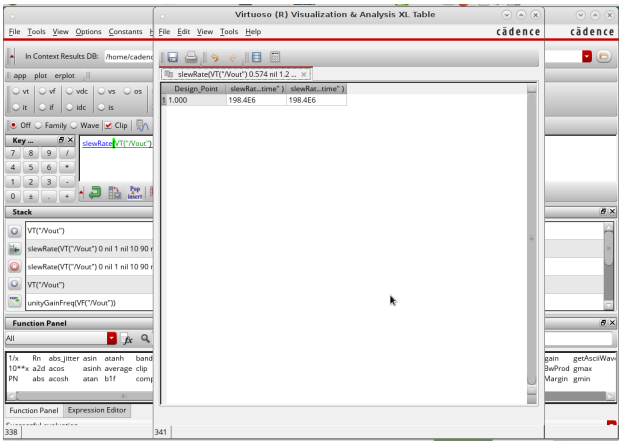


Figure 15. The slew rate is equal to 198 V/us.

6. Fulfilling the requirement that the peak to peak swing is equal to 0.7V.

The swing is calculated from the equation

$$swing = V_{DD} - |V_{sat(M13)}| - |V_{sat(M6)}|$$

$$swing = 1.2 - |0.1247| - |0.08895| = 0.98635V$$

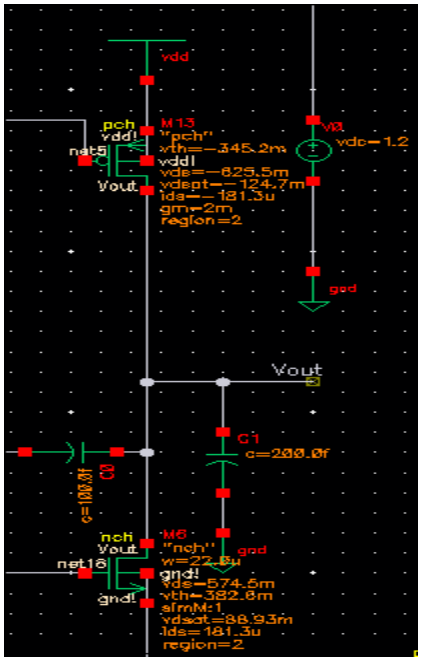


Figure 16. The DC analysis of stage 2, as it is the stage responsible for the swing.

7. Fulfilling the requirement that the power consumption should be less than or equal to 2 mW.

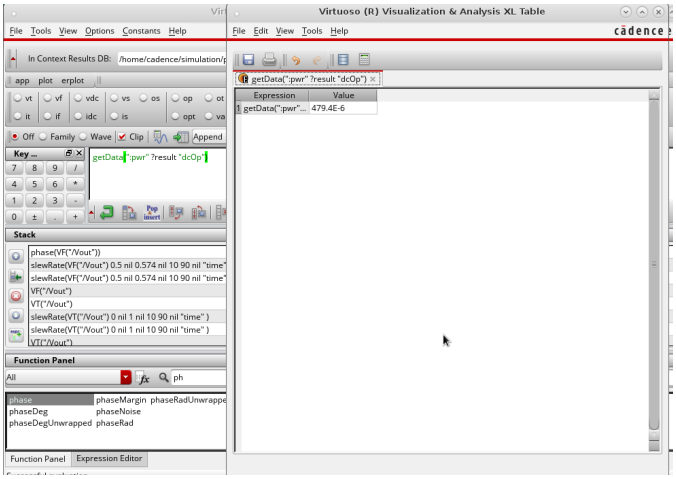


Figure 16. The power consumption was found to be 479.4 uWatt .

The power consumption analytically :

$$P = IV = 1.2 \times (90.12 + 98.464 + 30.88 + 185.44) \times 10^{-6} = 485.844\, uWatt\,.$$

8. Fulfilling the requirement that the output common mode is in range $0.6V \leq V_{out}(CM) \leq 0.8V$.

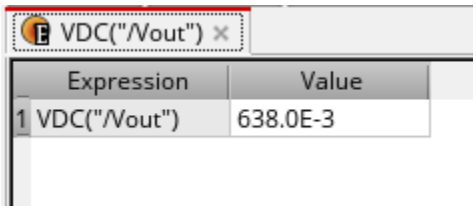


Figure 17. The output common mode is 0.638 V.

Summary of the Pre-layout outputs:

Requirement	Pre-layout Result
Bias Circuit M12 90 μA	$I_{out} = 90.12\ \mu A$
Nominal Output Common-mode (Output DC level) $0.7 \pm 0.1V$	$V_{out}(CM) = 0.638\ V$
Overall power consumption including the bias circuit $\leq 2mWatt$	$P = 0.479\ mWatt$
Output peak to peak swing 0.7V	$0.08895 \leq V_{out} \leq 1.0753$ peak -to- peak swing$= 0.98635\ V$
Low frequency differential to single ended gain $\geq 40dB$	$A_{overall} = 47.5327\ dB$
Unity gain frequency 300MHz	$F_u = 623.8\ MHz$
Phase margin $\geq 50°$	$PM = 99°$
Slew rate $\geq 9V/\mu s$	$SR = 198\ V/\mu s$

Table 2. Comparison between the requirements and the Pre-Layout results.

Part 2. Circuit Layout and Post layout simulation:

1. Complete layout for the circuit :

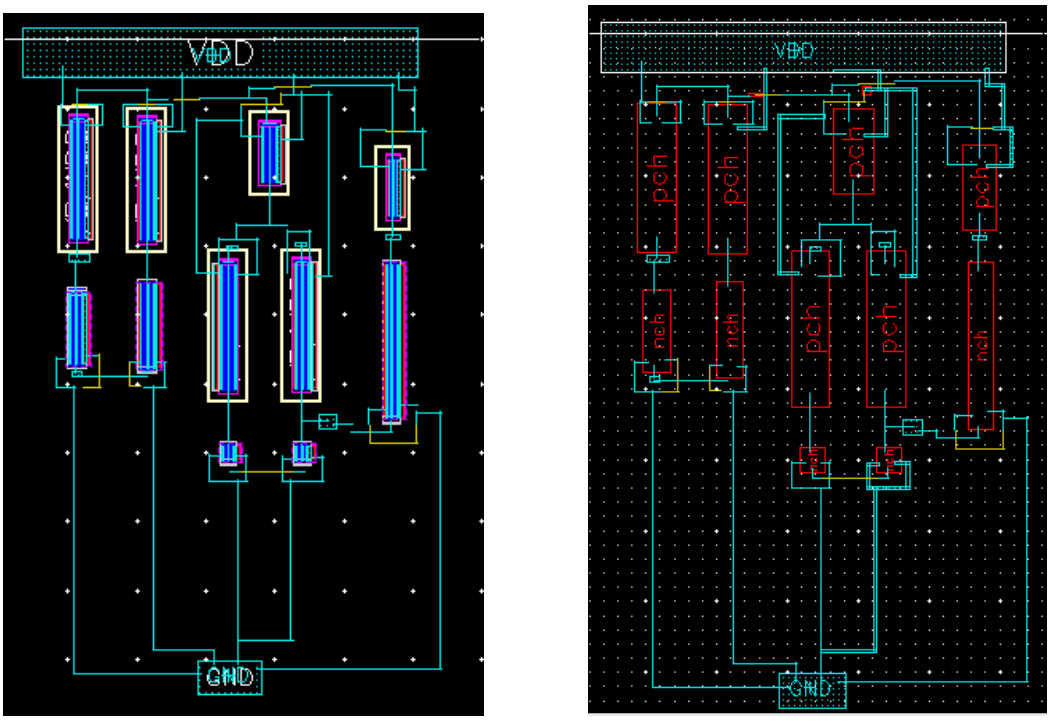


Figure 18. Complete layout for the circuit.

2. Running design rule check :

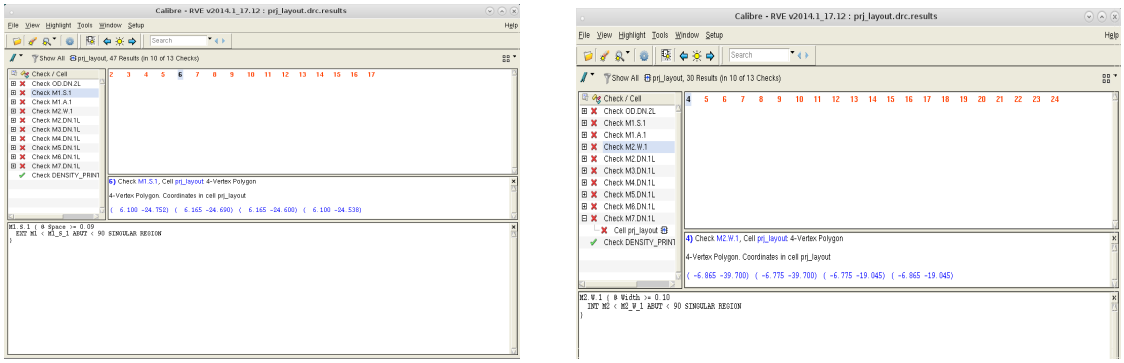


Figure 19. DRC errors.

This error says that Metal2 layer width should be at least 0.1um or more, and that the minimum distance between the poly routing on the gates and the Metal1 connection on the source next to it must be at least 0.09um, so I followed these rules and solved the errors.

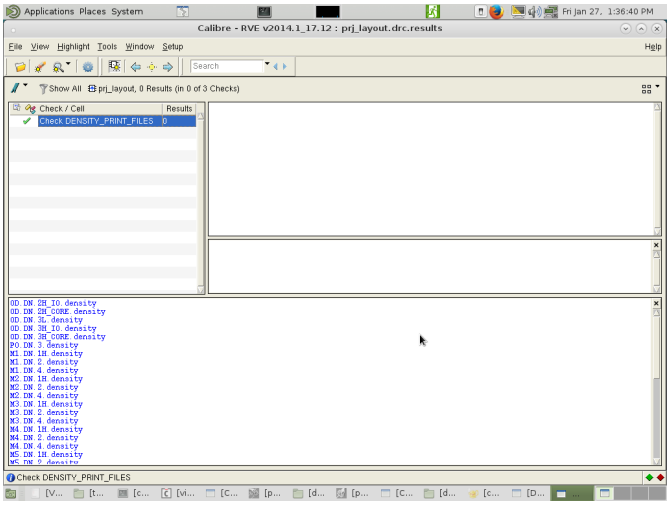


Figure 20. DRC clean.

2. Layout Versus Schematic (LVS) for the Op_Amp:

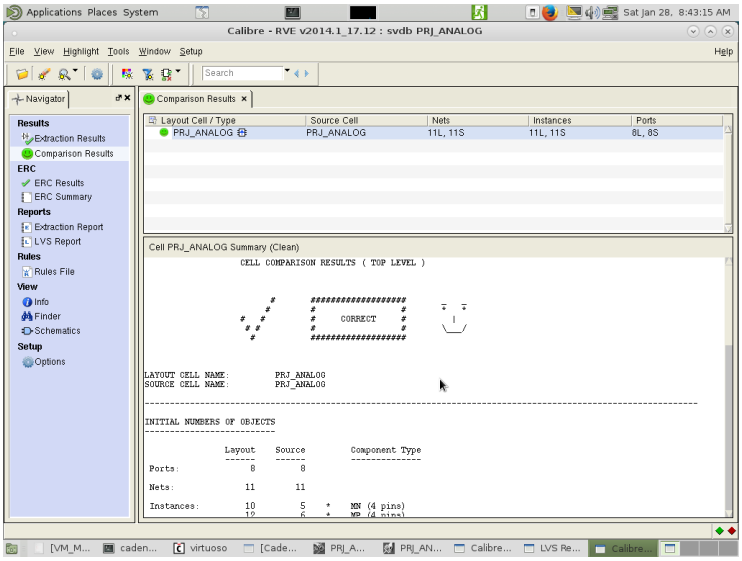


Figure 21. LVS clean.

3. Running the Parasitics Extraction (PEX) for the parasitics resistors and capacitors:

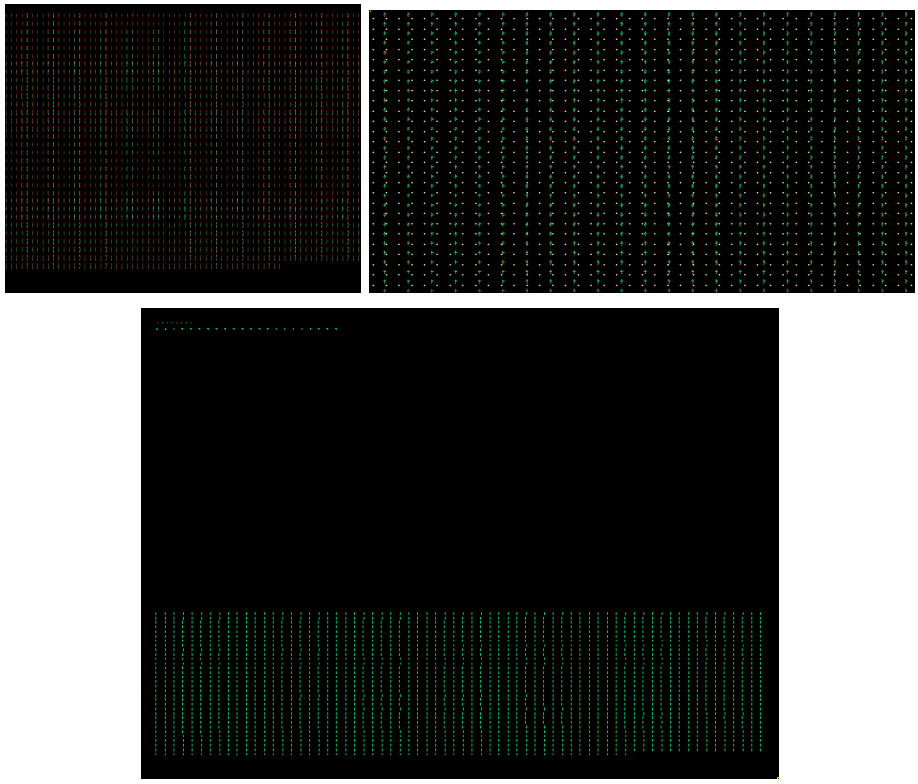


Figure 22. The parasitic capacitors and resistors for the Op_Amp.

The post layout simulation:

For starting the post layout simulation we had to build a symbol for the Op_Amp and perform a test bench for that symbol after the layout and PEX extractions.

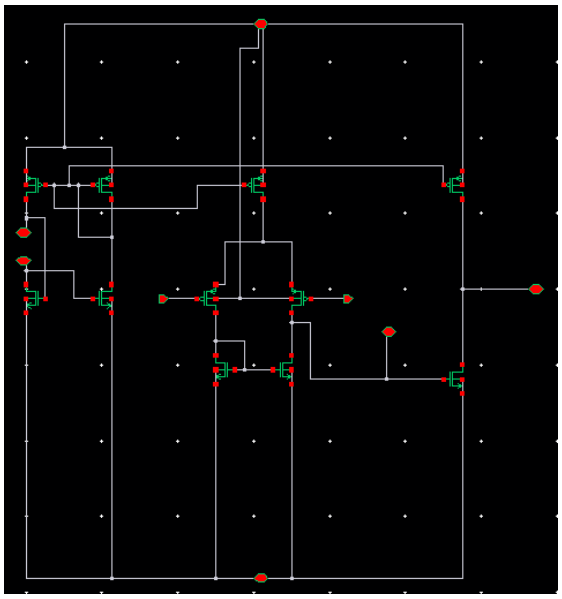


Figure 23. The schematic with Pins for the Layout and for the symbol.

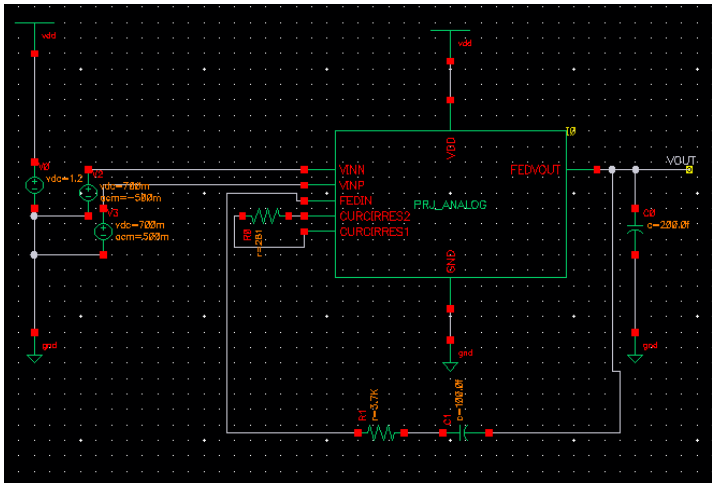


Figure 24. The symbol in the testbench .

Results after layout :

1. The gain post layout:

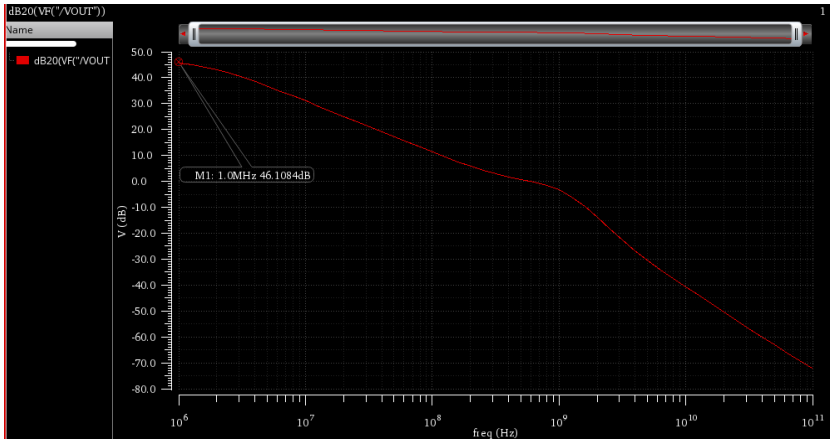


Figure 25. The gain after PEX has dropped from 47.5 db to 46.108 db.

2. The unity gain frequency:

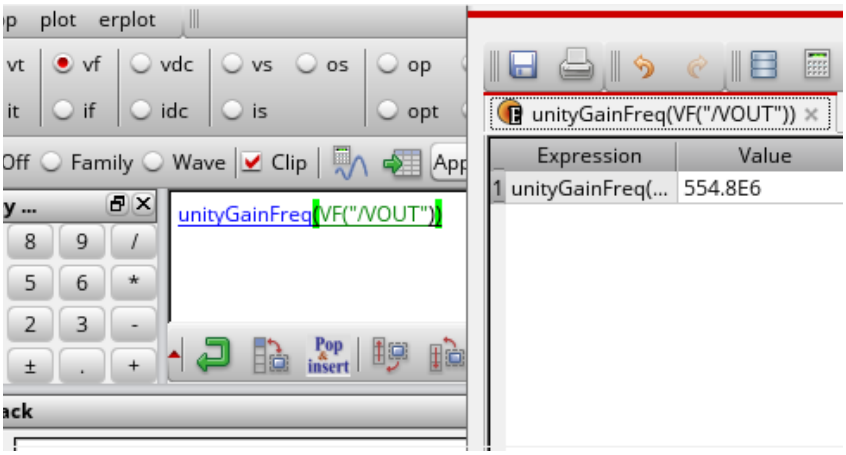


Figure 26. The unity gain frequency is about 554.8MHz.

3. The phase Margin:

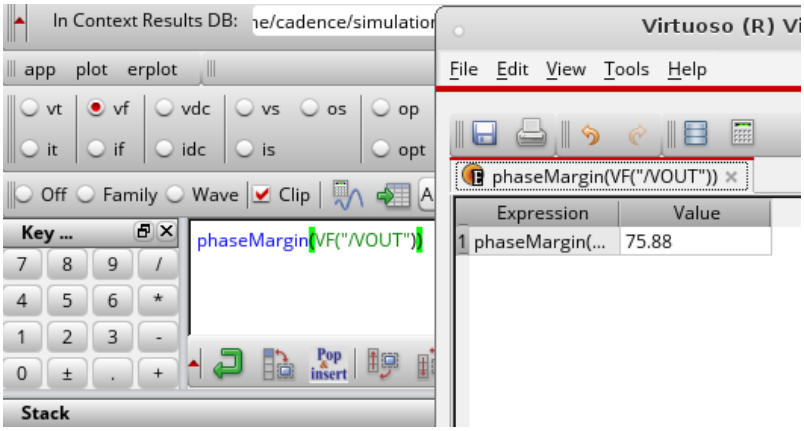


Figure 27. The phase margin dropped from 99° to 75.88° (still above the requirement of 50°).

4. The power consumption in the Op_Amp:

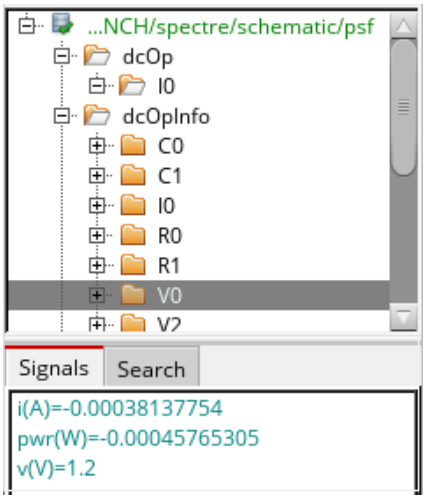


Figure 28. The power consumption for the Op_Amp post layout is 0.4576mWatt.

5. The peak to peak swing:

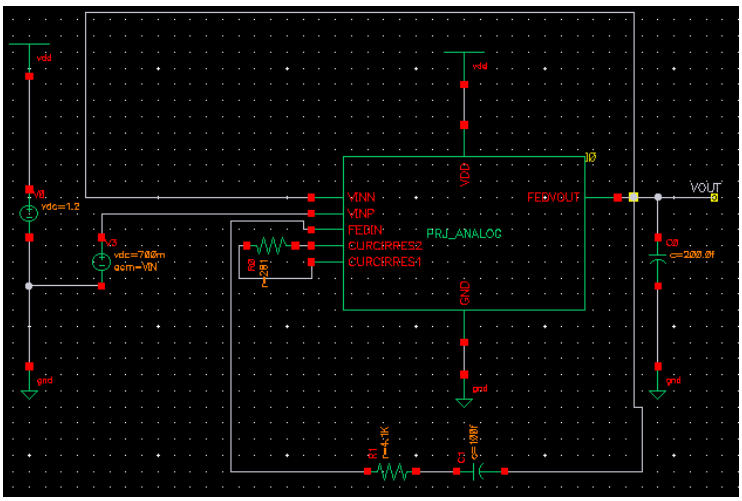


Figure 29. Connecting the negative input to the output (negative feedback) and swiping on the positive input from 0:VDD.

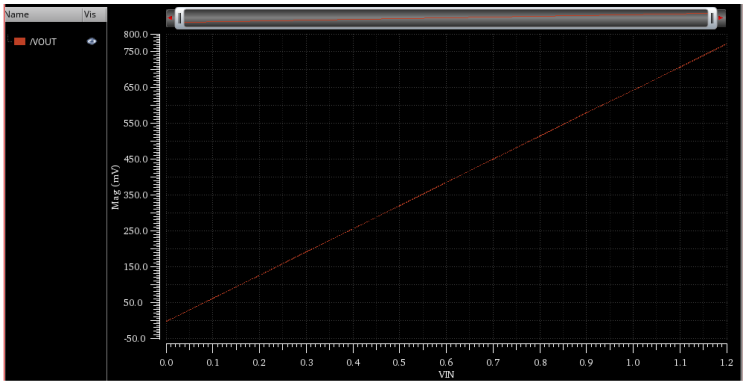


Figure 30. The VOUT vs VIN from 0:VDD, getting the peak-to-peak swing to be 0.797 V.

6. The output common mode :9

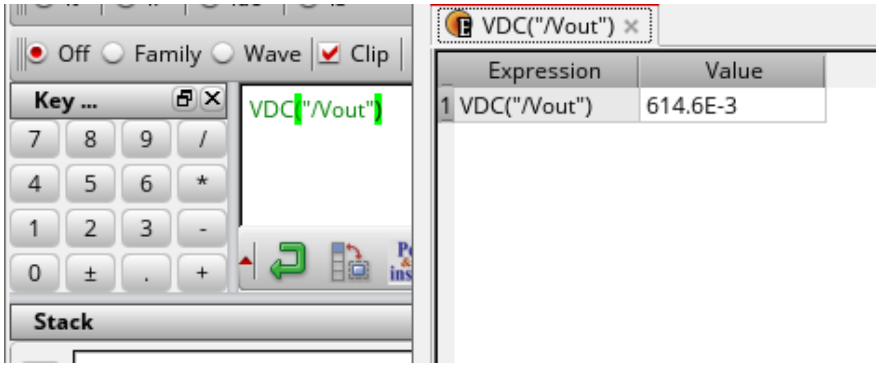


Figure 31. The output common mode is 0.6146 V.

7. The Slew Rate post the layout:

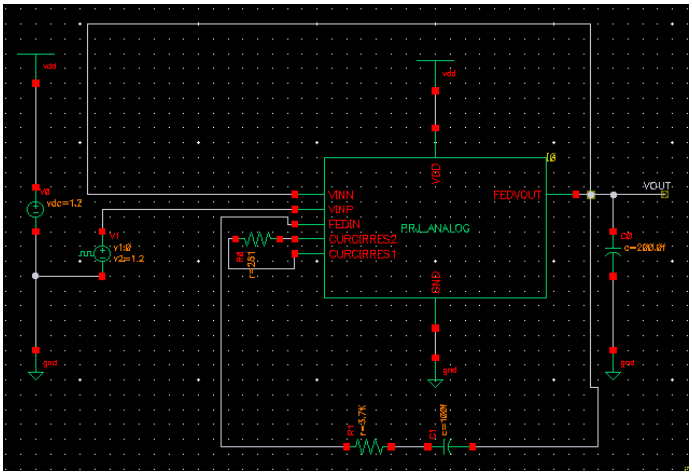


Figure 32. The symbol for calculating the Slew rate replaces only the VIN by a pulse (input square wave).

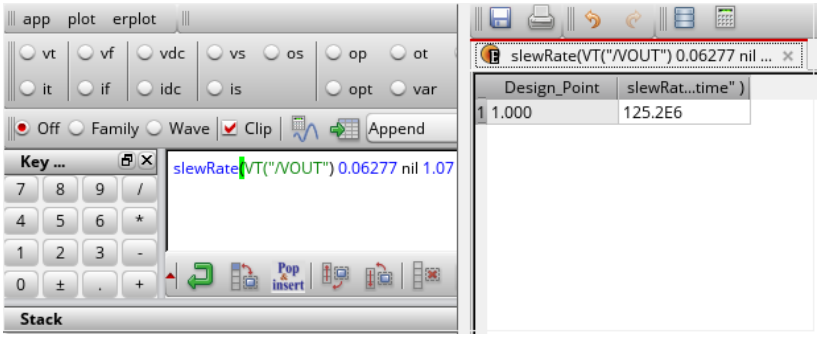


Figure 33. The Slew Rate post the layout is 125.2V/µsec .

8. The current in the bias circuit transistor:

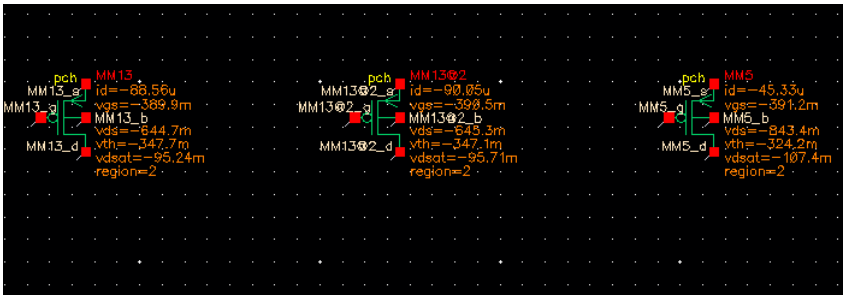


Figure 34. The current in the bias circuit transistor is 90.05uA.

Summary of the Post-layout outputs:

Requirement	Post-layout Result
Bias Circuit M12 90 μA	$I_{out} = 90.05\ \mu A$
Nominal Output Common-mode (Output DC level) $0.7 \pm 0.1V$	$V_{out}(CM) = 0.6146V$
Overall power consumption including the bias circuit $\leq 2mWatt$	$P = 0.4576mWatt$
Output peak to peak swing 0.7V	peak -to- peak swing$= 0.797\ V$
$A_{overall} = 47.5327\ dB$	$A_{overall} = 46.108\ dB$
Unity gain frequency 300MHz	$F_u = 554.8\ MHz$
$PM = 99°$	$PM = 75.88°$
Slew rate $\geq 9V/\mu s$	$SR = 125.2V/\mu s$

Table 3.Comparison between the requirements and the Post-Layout results.

Summary of the Pre-layout and Post-layout outputs:

Pre-layout Result	Post-layout Result
$I_{out} = 90.12\ \mu A$	$I_{out} = 90.05\ \mu A$
$V_{out}(CM) = 0.638\ V$	$V_{out}(CM) = 0.6146V$
$P = 0.409\ mWatt$	$P = 0.4576mWatt$
peak -to- peak swing $= 0.98635\ V$	peak -to- peak swing$= 0.797\ V$
$A_{overall} = 47.5\ dB$	$A_{overall} = 46.108\ dB$
$F_u = 623.8\ MHz$	$F_u = 554.8\ MHz$
PM$= 99°$	$PM = 75.88°$
$SR = 198V/\mu s$	$SR = 125.2V/\mu s$

Table 4.Comparison between the pre-layout and the Post-Layout results.

As expected the gain for the post layout simulation has decreased from pre layout simulation because the input current decreases due to the added effect of the parasitics as shown that the current of the bias circuit decreased in post layout simulation from pre layout, hence the output voltage decreases and accordingly the gain decreases as it represents vout/vin, the output voltage common mode decreased in the post layout simulation from pre layout simulation because it's simply the DC voltage and as the current in the branch decrease the voltage decreases as well because $V_{ds} \alpha\ I_d$, the phase margin decreased in the post layout simulation from the pre layout because of the increases in the parasitic resistance and capacitance hence the unity gain frequency decreases (as $F_u \alpha 1/CR$) and accordingly the gain goes to zero dB earlier and hence the phase margin decreases, the power consumption in the σta is increased due to the increase in the parasitic resistances and capacitors that would consume power, the slew rate decreased which means that the output would take more time to change (the maximum rate of change of an op amps output voltage decreased) and its as expected because adding parasitic elements would increase the capacitance value and the slew rate is defined as I(current)/C(capacitance) .