OVP Guide to Using Processor Models

Model specific information for ARM_MultiCluster

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

Contents

Chapter 1

Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

This model implements an ARM system containing clusters of MPCore processors communicating using a common GICv2 or GICv3 block.

By default, the system contains Cortex-A53MPx4 and Cortex-A57MPx4 clusters, but this can be changed using parameter "override_clusterVariants". This parameter is a comma-separated list of cluster components (e.g. "Cortex-A53MPx4,Cortex-A57MPx4"). Note that if a GICv2 is selected, the total number of PEs must not exceed 8.

1.2 Licensing

This document describes the interface to the MultiCluster only. Refer to documentation of individual clusters for information regarding implemented features, licensing and limitations.

1.3 Limitations

1.4 Features

By default, the model implements a GICv2. Parameter enableGICv3 can be used to select a GICv3 instead.

Chapter 2

Configuration

2.1 Location

This model's VLNV is arm.ovpworld.org/processor/arm/1.0.
The model source is usually at:
$IMPERAS_HOME/ImperasLib/source/arm.ovpworld.org/processor/arm/1.0
The model binary is usually at:
$IMPERAS_HOME/lib/$IMPERAS_ARCH/ImperasLib/arm.ovpworld.org/processor/arm/1.0

2.2 Asymmetric Multicore Processor

This processor contains more than one core of differing architectures

Chapter 3

All Variants in this model

This model has these variants

Variant	Description
ARMv4T	
ARMv4xM	
ARMv4	
ARMv4TxM	
ARMv5xM	
ARMv5	
ARMv5TxM	
ARMv5T	
ARMv5TExP	
ARMv5TE	
ARMv5TEJ	
ARMv6	
ARMv6K	
ARMv6T2	
ARMv6KZ	
ARMv7	
ARM7TDMI	
ARM7EJ-S	
ARM720T	
ARM920T	
ARM922T	
ARM926EJ-S	
ARM940T	
ARM946E	
ARM966E	
ARM968E-S	
ARM1020E	
ARM1022E	
ARM1026EJ-S	
ARM1136J-S	
ARM1156T2-S	

ARM1176JZ-S	
Cortex-R4	
Cortex-R4F	
Cortex-A5UP	
Cortex-A5MPx1	
Cortex-A5MPx2	
Cortex-A5MPx3	
Cortex-A5MPx4	
Cortex-A8	
Cortex-A9UP	
Cortex-A9MPx1	
Cortex-A9MPx2	
Cortex-A9MPx3	
Cortex-A9MPx4	
Cortex-A7UP	
Cortex-A7MPx1	
Cortex-A7MPx2	
Cortex-A7MPx3	
Cortex-A7MPx4	
Cortex-A15UP	
Cortex-A15MPx1	
Cortex-A15MPx2	
Cortex-A15MPx3	
Cortex-A15MPx4	
Cortex-A17MPx1	
Cortex-A17MPx2	
Cortex-A17MPx3	
Cortex-A17MPx4	
AArch32	
AArch64	
Cortex-A32MPx1	
Cortex-A32MPx2	
Cortex-A32MPx3	
Cortex-A32MPx4	
Cortex-A35MPx1	
Cortex-A35MPx2	
Cortex-A35MPx3	
Cortex-A35MPx4	
Cortex-A53MPx1	
Cortex-A53MPx2	
Cortex-A53MPx3	
Cortex-A53MPx4	
Cortex-A55MPx1	
Cortex-A55MPx2	
Cortex-A55MPx3	

Cortex-A55MPx4	
Cortex-A57MPx1	
Cortex-A57MPx2	
Cortex-A57MPx3	
Cortex-A57MPx4	
Cortex-A72MPx1	
Cortex-A72MPx2	
Cortex-A72MPx3	
Cortex-A72MPx4	
Cortex-A73MPx1	
Cortex-A73MPx2	
Cortex-A73MPx3	
Cortex-A73MPx4	
Cortex-A75MPx1	
Cortex-A75MPx2	
Cortex-A75MPx3	
Cortex-A75MPx4	
MultiCluster	(described in this document)

Table 3.1: All Variants in this model

Chapter 4

Bus Master Ports

This model has these bus master ports.

Name	min	max	Connect?	Description
INSTRUCTION	32	53	mandatory	
DATA	32	53	optional	
GICRegisters	32	32	optional	GIC memory-mapped register block

Table 4.1: Bus Master Ports

Chapter 5

Bus Slave Ports

This model has no bus slave ports.

Chapter 6

Net Ports

This model has these net ports.

Name	Type	Connect?	Description
SPI32	input	optional	Shared peripheral interrupt
SPI33	input	optional	Shared peripheral interrupt
SPI34	input	optional	Shared peripheral interrupt
SPI35	input	optional	Shared peripheral interrupt
SPI36	input	optional	Shared peripheral interrupt
SPI37	input	optional	Shared peripheral interrupt
SPI38	input	optional	Shared peripheral interrupt
SPI39	input	optional	Shared peripheral interrupt
SPI40	input	optional	Shared peripheral interrupt
SPI41	input	optional	Shared peripheral interrupt
SPI42	input	optional	Shared peripheral interrupt
SPI43	input	optional	Shared peripheral interrupt
SPI44	input	optional	Shared peripheral interrupt
SPI45	input	optional	Shared peripheral interrupt
SPI46	input	optional	Shared peripheral interrupt
SPI47	input	optional	Shared peripheral interrupt
SPI48	input	optional	Shared peripheral interrupt
SPI49	input	optional	Shared peripheral interrupt
SPI50	input	optional	Shared peripheral interrupt
SPI51	input	optional	Shared peripheral interrupt
SPI52	input	optional	Shared peripheral interrupt
SPI53	input	optional	Shared peripheral interrupt
SPI54	input	optional	Shared peripheral interrupt
SPI55	input	optional	Shared peripheral interrupt
SPI56	input	optional	Shared peripheral interrupt
SPI57	input	optional	Shared peripheral interrupt
SPI58	input	optional	Shared peripheral interrupt
SPI59	input	optional	Shared peripheral interrupt
SPI60	input	optional	Shared peripheral interrupt
SPI61	input	optional	Shared peripheral interrupt
SPI62	input	optional	Shared peripheral interrupt

SPI63	input	optional	Shared peripheral interrupt
SPI64	input	optional	Shared peripheral interrupt
SPI65	input	optional	Shared peripheral interrupt
SPI66	input	optional	Shared peripheral interrupt
SPI67	input	optional	Shared peripheral interrupt
SPI68	input	optional	Shared peripheral interrupt
SPI69	input	optional	Shared peripheral interrupt
SPI70	input	optional	Shared peripheral interrupt
SPI71	input	optional	Shared peripheral interrupt
SPI72	input	optional	Shared peripheral interrupt
SPI73	input	optional	Shared peripheral interrupt
SPI74	input	optional	Shared peripheral interrupt
SPI75	input	optional	Shared peripheral interrupt
SPI76	input	optional	Shared peripheral interrupt
SPI77	input	optional	Shared peripheral interrupt
SPI78	input	optional	Shared peripheral interrupt
SPI79	input	optional	Shared peripheral interrupt
SPI80	input	optional	Shared peripheral interrupt
SPI81	input	optional	Shared peripheral interrupt
SPI82	input	optional	Shared peripheral interrupt
SPI83	input	optional	Shared peripheral interrupt
SPI84	input	optional	Shared peripheral interrupt
SPI85	input	optional	Shared peripheral interrupt
SPI86	input	optional	Shared peripheral interrupt
SPI87	input	optional	Shared peripheral interrupt
SPI88	input	optional	Shared peripheral interrupt
SPI89	input	optional	Shared peripheral interrupt
SPI90	input	optional	Shared peripheral interrupt
SPI91	input	optional	Shared peripheral interrupt
SPI92	input	optional	Shared peripheral interrupt
SPI93	input	optional	Shared peripheral interrupt
SPI94	input	optional	Shared peripheral interrupt
SPI95	input	optional	Shared peripheral interrupt
SPIVector	input	optional	Shared peripheral interrupt vectorized input
periphReset	input	optional	Peripheral reset (active high)
CFGSDISABLE	input	optional	Secure configuration lockdown (active high)
GICCDISABLE	input	optional	GIC CPU interface logic disable (active high, sampled on rising edge of periphReset)
EVENTI	input	optional	Event input signal, active on rising edge
EVENTO	output	optional	Event output signal, active on rising edge
PPI16_C0_0	input	optional	Private peripheral interrupt
PPI17_C0_0	input	optional	Private peripheral interrupt

PPI18_C0_0	input	optional	Private peripheral interrupt
PPI19_C0_0	input	optional	Private peripheral interrupt
PPI20_C0_0	input	optional	Private peripheral interrupt
PPI21_C0_0	input	optional	Private peripheral interrupt
PPI22_C0_0	input	optional	Private peripheral interrupt
PPI23_C0_0	input	optional	Private peripheral interrupt
PPI24_C0_0	input	optional	Private peripheral interrupt
PPI25_C0_0	input	optional	Private peripheral interrupt
PPI26_C0_0	input	optional	Private peripheral interrupt
PPI27_C0_0	input	optional	Private peripheral interrupt
PPI28_C0_0	input	optional	Private peripheral interrupt
PPI29_C0_0	input	optional	Private peripheral interrupt
PPI30_C0_0	input	optional	Private peripheral interrupt
PPI31_C0_0	input	optional	Private peripheral interrupt
CNTVIRQ_C0_0	output	optional	Virtual timer event (active high)
CNTPSIRQ_C0_0	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C0_0	output	optional	Non-secure physical timer event (active high)
CNTPHPIRQ_C0_0	output	optional	Hypervisor physical timer event (active high)
IRQOUT_C0_0	output	optional	IRQ wakeup
FIQOUT_C0_0	output	optional	FIQ wakeup
CLUSTERIDAFF1_C0	input	optional	Configure MPIDR.Aff1
CLUSTERIDAFF2_C0	input	optional	Configure MPIDR.Aff2
CLUSTERIDAFF3_C0	input	optional	Configure MPIDR.Aff3
RVBARADDRx_C0_0	input	optional	Configure AArch64 Reset Vector Base Address at reset
AA64nAA32_C0_0	input	optional	Register width state at reset
VINITHI_C0_0	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_0	input	optional	Configure exception endianness (SCTLR.EE)
CFGTE_C0_0	input	optional	Configure exception state at reset (SCTLR.TE)
reset_C0_0	input	optional	Processor reset, active high
fiq_C0_0	input	optional	FIQ interrupt, active high (negation of nFIQ)
irq_C0_0	input	optional	IRQ interrupt, active high (negation of nIRQ)
sei_C0_0	input	optional	System error interrupt, active on rising edge (negation of nSEI)
vfiq_C0_0	input	optional	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C0_0	input	optional	Virtual IRQ interrupt, active high (negation of nVIRQ)

vsei_C0_0	input	optional	Virtual system error interrupt, active on rising edge (negation of nVSEI)
AXI_SLVERR_C0_0	input	optional	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C0_0	input	optional	CP15SDISABLE (active high)
PMUIRQ_C0_0	output	optional	Performance monitor event (active high)
SMPEN_C0_0	output	optional	CPUECTLR.SMPEN current value
PPI16_C0_1	input	optional	Private peripheral interrupt
PPI17_C0_1	input	optional	Private peripheral interrupt
PPI18_C0_1	input	optional	Private peripheral interrupt
PPI19_C0_1	input	optional	Private peripheral interrupt
PPI20_C0_1	input	optional	Private peripheral interrupt
PPI21_C0_1	input	optional	Private peripheral interrupt
PPI22_C0_1	input	optional	Private peripheral interrupt
PPI23_C0_1	input	optional	Private peripheral interrupt
PPI24_C0_1	input	optional	Private peripheral interrupt
PPI25_C0_1	input	optional	Private peripheral interrupt
PPI26_C0_1	input	optional	Private peripheral interrupt
PPI27_C0_1	input	optional	Private peripheral interrupt
PPI28_C0_1	input	optional	Private peripheral interrupt
PPI29_C0_1	input	optional	Private peripheral interrupt
PPI30_C0_1	input	optional	Private peripheral interrupt
PPI31_C0_1	input	optional	Private peripheral interrupt
CNTVIRQ_C0_1	output	optional	Virtual timer event (active high)
CNTPSIRQ_C0_1	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C0_1	output	optional	Non-secure physical timer event (active high)
CNTPHPIRQ_C0_1	output	optional	Hypervisor physical timer event (active high)
IRQOUT_C0_1	output	optional	IRQ wakeup
FIQOUT_C0_1	output	optional	FIQ wakeup
RVBARADDRx_C0_1	input	optional	Configure AArch64 Reset Vector Base Address at reset
AA64nAA32_C0_1	input	optional	Register width state at reset
VINITHI_C0_1	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_1	input	optional	Configure exception endianness (SCTLR.EE)
CFGTE_C0_1	input	optional	Configure exception state at reset (SCTLR.TE)
reset_C0_1	input	optional	Processor reset, active high
fiq_C0_1	input	optional	FIQ interrupt, active high (negation of nFIQ)
irq_C0_1	input	optional	IRQ interrupt, active high (negation of nIRQ)

sei_C0_1	input	optional	System error interrupt, active on rising edge (negation of nSEI)
vfiq_C0_1	input	optional	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C0_1	input	optional	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C0_1	input	optional	Virtual system error interrupt, active on rising edge (negation of nVSEI)
AXI_SLVERR_C0_1	input	optional	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C0_1	input	optional	CP15SDISABLE (active high)
PMUIRQ_C0_1	output	optional	Performance monitor event (active high)
SMPEN_C0_1	output	optional	CPUECTLR.SMPEN current value
PPI16_C0_2	input	optional	Private peripheral interrupt
PPI17_C0_2	input	optional	Private peripheral interrupt
PPI18_C0_2	input	optional	Private peripheral interrupt
PPI19_C0_2	input	optional	Private peripheral interrupt
PPI20_C0_2	input	optional	Private peripheral interrupt
PPI21_C0_2	input	optional	Private peripheral interrupt
PPI22_C0_2	input	optional	Private peripheral interrupt
PPI23_C0_2	input	optional	Private peripheral interrupt
PPI24_C0_2	input	optional	Private peripheral interrupt
PPI25_C0_2	input	optional	Private peripheral interrupt
PPI26_C0_2	input	optional	Private peripheral interrupt
PPI27_C0_2	input	optional	Private peripheral interrupt
PPI28_C0_2	input	optional	Private peripheral interrupt
PPI29_C0_2	input	optional	Private peripheral interrupt
PPI30_C0_2	input	optional	Private peripheral interrupt
PPI31_C0_2	input	optional	Private peripheral interrupt
CNTVIRQ_C0_2	output	optional	Virtual timer event (active high)
CNTPSIRQ_C0_2	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C0_2	output	optional	Non-secure physical timer event (active high)
CNTPHPIRQ_C0_2	output	optional	Hypervisor physical timer event (active high)
IRQOUT_C0_2	output	optional	IRQ wakeup
FIQOUT_C0_2	output	optional	FIQ wakeup
RVBARADDRx_C0_2	input	optional	Configure AArch64 Reset Vector Base Address at reset
AA64nAA32_C0_2	input	optional	Register width state at reset
VINITHI_C0_2	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_2	input	optional	Configure exception endianness (SCTLR.EE)
CFGTE_C0_2	input	optional	Configure exception state at reset (SCTLR.TE)

reset_C0_2	input	optional	Processor reset, active high
fiq_C0_2	input	optional	FIQ interrupt, active high (negation of nFIQ)
irq_C0_2	input	optional	IRQ interrupt, active high (negation of nIRQ)
sei_C0_2	input	optional	System error interrupt, active on rising edge (negation of nSEI)
vfiq_C0_2	input	optional	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C0_2	input	optional	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C0_2	input	optional	Virtual system error interrupt, active on rising edge (negation of nVSEI)
AXI_SLVERR_C0_2	input	optional	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C0_2	input	optional	CP15SDISABLE (active high)
PMUIRQ_C0_2	output	optional	Performance monitor event (active high)
SMPEN_C0_2	output	optional	CPUECTLR.SMPEN current value
PPI16_C0_3	input	optional	Private peripheral interrupt
PPI17_C0_3	input	optional	Private peripheral interrupt
PPI18_C0_3	input	optional	Private peripheral interrupt
PPI19_C0_3	input	optional	Private peripheral interrupt
PPI20_C0_3	input	optional	Private peripheral interrupt
PPI21_C0_3	input	optional	Private peripheral interrupt
PPI22_C0_3	input	optional	Private peripheral interrupt
PPI23_C0_3	input	optional	Private peripheral interrupt
PPI24_C0_3	input	optional	Private peripheral interrupt
PPI25_C0_3	input	optional	Private peripheral interrupt
PPI26_C0_3	input	optional	Private peripheral interrupt
PPI27_C0_3	input	optional	Private peripheral interrupt
PPI28_C0_3	input	optional	Private peripheral interrupt
PPI29_C0_3	input	optional	Private peripheral interrupt
PPI30_C0_3	input	optional	Private peripheral interrupt
PPI31_C0_3	input	optional	Private peripheral interrupt
CNTVIRQ_C0_3	output	optional	Virtual timer event (active high)
CNTPSIRQ_C0_3	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C0_3	output	optional	Non-secure physical timer event (active high)
CNTPHPIRQ_C0_3	output	optional	Hypervisor physical timer event (active high)
IRQOUT_C0_3	output	optional	IRQ wakeup
FIQOUT_C0_3	output	optional	FIQ wakeup
RVBARADDRx_C0_3	input	optional	Configure AArch64 Reset Vector Base Address at reset
AA64nAA32_C0_3	input	optional	Register width state at reset

VINITHI_C0_3	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_3	input	optional	Configure exception endianness (SCTLR.EE)
CFGTE_C0_3	input	optional	Configure exception state at reset (SCTLR.TE)
reset_C0_3	input	optional	Processor reset, active high
fiq_C0_3	input	optional	FIQ interrupt, active high (negation of nFIQ)
irq_C0_3	input	optional	IRQ interrupt, active high (negation of nIRQ)
sei_C0_3	input	optional	System error interrupt, active on rising edge (negation of nSEI)
vfiq_C0_3	input	optional	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C0_3	input	optional	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C0_3	input	optional	Virtual system error interrupt, active on rising edge (negation of nVSEI)
AXI_SLVERR_C0_3	input	optional	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C0_3	input	optional	CP15SDISABLE (active high)
PMUIRQ_C0_3	output	optional	Performance monitor event (active high)
SMPEN_C0_3	output	optional	CPUECTLR.SMPEN current value
PPI16_C1_0	input	optional	Private peripheral interrupt
PPI17_C1_0	input	optional	Private peripheral interrupt
PPI18_C1_0	input	optional	Private peripheral interrupt
PPI19_C1_0	input	optional	Private peripheral interrupt
PPI20_C1_0	input	optional	Private peripheral interrupt
PPI21_C1_0	input	optional	Private peripheral interrupt
PPI22_C1_0	input	optional	Private peripheral interrupt
PPI23_C1_0	input	optional	Private peripheral interrupt
PPI24_C1_0	input	optional	Private peripheral interrupt
PPI25_C1_0	input	optional	Private peripheral interrupt
PPI26_C1_0	input	optional	Private peripheral interrupt
PPI27_C1_0	input	optional	Private peripheral interrupt
PPI28_C1_0	input	optional	Private peripheral interrupt
PPI29_C1_0	input	optional	Private peripheral interrupt
PPI30_C1_0	input	optional	Private peripheral interrupt
PPI31_C1_0	input	optional	Private peripheral interrupt
CNTVIRQ_C1_0	output	optional	Virtual timer event (active high)
CNTPSIRQ_C1_0	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C1_0	output	optional	Non-secure physical timer event (active high)
CNTPHPIRQ_C1_0	output	optional	Hypervisor physical timer event (active high)

IRQOUT_C1_0	output	optional	IRQ wakeup
FIQOUT_C1_0	output	optional	FIQ wakeup
CLUSTERIDAFF1_C1	input	optional	Configure MPIDR.Aff1
CLUSTERIDAFF2_C1	input	optional	Configure MPIDR.Aff2
CLUSTERIDAFF3_C1	input	optional	Configure MPIDR.Aff3
RVBARADDRx_C1_0	input	optional	Configure AArch64 Reset Vector Base Address at reset
AA64nAA32_C1_0	input	optional	Register width state at reset
VINITHI_C1_0	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C1_0	input	optional	Configure exception endianness (SCTLR.EE)
CFGTE_C1_0	input	optional	Configure exception state at reset (SCTLR.TE)
reset_C1_0	input	optional	Processor reset, active high
fiq_C1_0	input	optional	FIQ interrupt, active high (negation of nFIQ)
irq_C1_0	input	optional	IRQ interrupt, active high (negation of nIRQ)
sei_C1_0	input	optional	System error interrupt, active on rising edge (negation of nSEI)
vfiq_C1_0	input	optional	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C1_0	input	optional	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C1_0	input	optional	Virtual system error interrupt, active on rising edge (negation of nVSEI)
AXI_SLVERR_C1_0	input	optional	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C1_0	input	optional	CP15SDISABLE (active high)
PMUIRQ_C1_0	output	optional	Performance monitor event (active high)
SMPEN_C1_0	output	optional	CPUECTLR.SMPEN current value
PPI16_C1_1	input	optional	Private peripheral interrupt
PPI17_C1_1	input	optional	Private peripheral interrupt
PPI18_C1_1	input	optional	Private peripheral interrupt
PPI19_C1_1	input	optional	Private peripheral interrupt
PPI20_C1_1	input	optional	Private peripheral interrupt
PPI21_C1_1	input	optional	Private peripheral interrupt
PPI22_C1_1	input	optional	Private peripheral interrupt
PPI23_C1_1	input	optional	Private peripheral interrupt
PPI24_C1_1	input	optional	Private peripheral interrupt
PPI25_C1_1	input	optional	Private peripheral interrupt
PPI26_C1_1	input	optional	Private peripheral interrupt
PPI27_C1_1	input	optional	Private peripheral interrupt
PPI28_C1_1	input	optional	Private peripheral interrupt
PPI29_C1_1	input	optional	Private peripheral interrupt

PPI30_C1_1	input	optional	Private peripheral interrupt
PPI31_C1_1	input	optional	Private peripheral interrupt
CNTVIRQ_C1_1	output	optional	Virtual timer event (active high)
CNTPSIRQ_C1_1	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C1_1	output	optional	Non-secure physical timer event (active high)
CNTPHPIRQ_C1_1	output	optional	Hypervisor physical timer event (active high)
IRQOUT_C1_1	output	optional	IRQ wakeup
FIQOUT_C1_1	output	optional	FIQ wakeup
RVBARADDRx_C1_1	input	optional	Configure AArch64 Reset Vector Base Address at reset
AA64nAA32_C1_1	input	optional	Register width state at reset
VINITHI_C1_1	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C1_1	input	optional	Configure exception endianness (SCTLR.EE)
CFGTE_C1_1	input	optional	Configure exception state at reset (SCTLR.TE)
reset_C1_1	input	optional	Processor reset, active high
fiq_C1_1	input	optional	FIQ interrupt, active high (negation of nFIQ)
irq_C1_1	input	optional	IRQ interrupt, active high (negation of nIRQ)
sei_C1_1	input	optional	System error interrupt, active on rising edge (negation of nSEI)
vfiq_C1_1	input	optional	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C1_1	input	optional	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C1_1	input	optional	Virtual system error interrupt, active on rising edge (negation of nVSEI)
AXI_SLVERR_C1_1	input	optional	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C1_1	input	optional	CP15SDISABLE (active high)
PMUIRQ_C1_1	output	optional	Performance monitor event (active high)
SMPEN_C1_1	output	optional	CPUECTLR.SMPEN current value
PPI16_C1_2	input	optional	Private peripheral interrupt
PPI17_C1_2	input	optional	Private peripheral interrupt
PPI18_C1_2	input	optional	Private peripheral interrupt
PPI19_C1_2	input	optional	Private peripheral interrupt
PPI20_C1_2	input	optional	Private peripheral interrupt
PPI21_C1_2	input	optional	Private peripheral interrupt
PPI22_C1_2	input	optional	Private peripheral interrupt
PPI23_C1_2	input	optional	Private peripheral interrupt
PPI24_C1_2	input	optional	Private peripheral interrupt
PPI25_C1_2	input	optional	Private peripheral interrupt

PPI26_C1_2	input	optional	Private peripheral interrupt
PPI27_C1_2	input	optional	Private peripheral interrupt
PPI28_C1_2	input	optional	Private peripheral interrupt
PPI29_C1_2	input	optional	Private peripheral interrupt
PPI30_C1_2	input	optional	Private peripheral interrupt
PPI31_C1_2	input	optional	Private peripheral interrupt
CNTVIRQ_C1_2	output	optional	Virtual timer event (active high)
CNTPSIRQ_C1_2	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C1_2	output	optional	Non-secure physical timer event (active high)
CNTPHPIRQ_C1_2	output	optional	Hypervisor physical timer event (active high)
IRQOUT_C1_2	output	optional	IRQ wakeup
FIQOUT_C1_2	output	optional	FIQ wakeup
RVBARADDRx_C1_2	input	optional	Configure AArch64 Reset Vector Base Address at reset
AA64nAA32_C1_2	input	optional	Register width state at reset
VINITHI_C1_2	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C1_2	input	optional	Configure exception endianness (SCTLR.EE)
CFGTE_C1_2	input	optional	Configure exception state at reset (SCTLR.TE)
reset_C1_2	input	optional	Processor reset, active high
fiq_C1_2	input	optional	FIQ interrupt, active high (negation of nFIQ)
irq_C1_2	input	optional	IRQ interrupt, active high (negation of nIRQ)
sei_C1_2	input	optional	System error interrupt, active on rising edge (negation of nSEI)
vfiq_C1_2	input	optional	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C1_2	input	optional	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C1_2	input	optional	Virtual system error interrupt, active on rising edge (negation of nVSEI)
AXI_SLVERR_C1_2	input	optional	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C1_2	input	optional	CP15SDISABLE (active high)
PMUIRQ_C1_2	output	optional	Performance monitor event (active high)
SMPEN_C1_2	output	optional	CPUECTLR.SMPEN current value
PPI16_C1_3	input	optional	Private peripheral interrupt
PPI17_C1_3	input	optional	Private peripheral interrupt
PPI18_C1_3	input	optional	Private peripheral interrupt
PPI19_C1_3	input	optional	Private peripheral interrupt
PPI20_C1_3	input	optional	Private peripheral interrupt
PPI21_C1_3	input	optional	Private peripheral interrupt

PPI22_C1_3	input	optional	Private peripheral interrupt
PPI23_C1_3	input	optional	Private peripheral interrupt
PPI24_C1_3	input	optional	Private peripheral interrupt
PPI25_C1_3	input	optional	Private peripheral interrupt
PPI26_C1_3	input	optional	Private peripheral interrupt
PPI27_C1_3	input	optional	Private peripheral interrupt
PPI28_C1_3	input	optional	Private peripheral interrupt
PPI29_C1_3	input	optional	Private peripheral interrupt
PPI30_C1_3	input	optional	Private peripheral interrupt
PPI31_C1_3	input	optional	Private peripheral interrupt
CNTVIRQ_C1_3	output	optional	Virtual timer event (active high)
CNTPSIRQ_C1_3	output	optional	Secure physical timer event (active high)
CNTPNSIRQ_C1_3	output	optional	Non-secure physical timer event (active high)
CNTPHPIRQ_C1_3	output	optional	Hypervisor physical timer event (active high)
IRQOUT_C1_3	output	optional	IRQ wakeup
FIQOUT_C1_3	output	optional	FIQ wakeup
RVBARADDRx_C1_3	input	optional	Configure AArch64 Reset Vector Base Address at reset
AA64nAA32_C1_3	input	optional	Register width state at reset
VINITHI_C1_3	input	optional	Configure HIVECS mode (SCTLR.V)
CFGEND_C1_3	input	optional	Configure exception endianness (SCTLR.EE)
CFGTE_C1_3	input	optional	Configure exception state at reset (SCTLR.TE)
reset_C1_3	input	optional	Processor reset, active high
fiq_C1_3	input	optional	FIQ interrupt, active high (negation of nFIQ)
irq_C1_3	input	optional	IRQ interrupt, active high (negation of nIRQ)
sei_C1_3	input	optional	System error interrupt, active on rising edge (negation of nSEI)
vfiq_C1_3	input	optional	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C1_3	input	optional	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C1_3	input	optional	Virtual system error interrupt, active on rising edge (negation of nVSEI)
AXI_SLVERR_C1_3	input	optional	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C1_3	input	optional	CP15SDISABLE (active high)
PMUIRQ_C1_3	output	optional	Performance monitor event (active high)
SMPEN_C1_3	output	optional	CPUECTLR.SMPEN current value

Table 6.1: Net Ports

Chapter 7

FIFO Ports

This model has no FIFO ports.

Chapter 8

Formal Parameters

Name	Type	Description
variant	Enumeration	Selects variant (either a generic ISA or a specific model)
disableGICModel	Boolean	Disable the internal GIC model entirely
enableGICv3	Boolean	Enable/disable GICv3 support
enableGICv2_64kB_Page	Boolean	Enable 64kB page size for GICv2 memory-mapped register groups (Xilinx Zynq Ultrascale support)
supportSTATUSR	Boolean	Enable/disable support for GICv3 GIC[CDV]_STATUSR registers
distinctMTCores	Boolean	For multi-threaded (MT) processors, simulate threads as separate cores (otherwise, simulate MT threads as a single entity)
override_clusterVariants	String	Specifies a comma-separated list of cluster variant names in this multicluster
override_timerScaleFactor	Uns32	Specifies the fraction of MIPS rate to use for MPCore timers (generic timers or global/local/watchdogs depending on implementation). Defaults to 20 for generic timers, 2 for others
override_GICD_NSACRPresent	Boolean	Specifies that optional GICD_NSACR distributor registers are present (GICv2 only)
override_GICD_PPISRPresent	Boolean	Specifies that implementation-specific GICD_PPISR distributor register is present (GICv1 ICDPPIS/ICPPISR, GICv1 and GICv2 only)
override_GICD_SPISRPresent	Boolean	Specifies that implementation-specific GICD_SPISR distributor registers are present (GICv1 ICDSPIS/ICSPISR)
override_GICv3_DistributorBase	Uns64	Specify distributor register block base address (GICv3 only)
override_GICv3_E1NWFPresent	Boolean	Specifies that GICR_CTLR.E1NWF is implemented (GICv3 only)
override_GIC_PPIMask	Uns32	Specify bitmask of implemented PPIs in the GIC (e.g. ID16 is 0x0001, ID31 is 0x8000)
override_GICCDISABLE	Boolean	Specify initial value of GICCDISABLE
override_GICC_IIDR	Uns32	Override GICC_IIDR register (GICv1 ICCIIDR)
override_GICD_TYPER	Uns32	Override GICD_TYPER register (GICv1 ICDICTR)
override_GICD_TYPER_ITLines	Uns32	Override ITLinesNumber field of GICD_TYPER register (GICv1 ICDICTR)
override_GICD_ICFGRN	Uns32	Override reset value of GICD_ICFGR2...GICD_ICFGRn (GICv1 ICDICFR2...ICDICFRn)
override_GICD_IIDR	Uns32	Override GICD_IIDR register (GICv1 ICDIIDR)
override_GICH_VTR	Uns32	Override GICH_VTR register
override_GICR_IIDR	Uns32	Override GICR_IIDR register (GICv3 and later)
override_GITS_IIDR	Uns32	Override GITS_IIDR register (GICv3 and later)
override_GITS_TYPER	Uns64	Override GITS_TYPER register (GICv3 and later)
override_ICCPMRBits	Uns32	Specify the number of writable bits in GICC_PMR (GICv1 ICCPMR)

override_minICCBPR	Uns32	Specify the minimum possible value for GICC_BPR (GICv1 ICCBPR)

Table 8.1: Parameters that can be set in: CLUSTER_GROUP

8.1 Parameter values

These are the current parameter values.

Name	Value
(Others)	
variant	MultiCluster
disableGICModel	F
enableGICv3	F
enableGICv2_64kB_Page	F
supportSTATUSR	F
distinctMTCores	F
override_clusterVariants	Cortex-A53MPx4,Cortex-A57MPx4
override_timerScaleFactor	2
override_GICD_NSACRPresent	F
override_GICD_PPISRPresent	F
override_GICD_SPISRPresent	F
override_GICv3_DistributorBase	0
override_GICv3_E1NWFPresent	F
override_GIC_PPIMask	0
override_GICCDISABLE	F
override_GICC_IIDR	0
override_GICD_TYPER	0
override_GICD_TYPER_ITLines	0
override_GICD_ICFGRN	0
override_GICD_IIDR	0
override_GICH_VTR	0
override_GICR_IIDR	0
override_GITS_IIDR	0
override_GITS_TYPER	0
override_ICCPMRBits	5
override_minICCBPR	0

Table 8.2: Parameter values

Chapter 9

Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

9.1 Level 1: CLUSTER_GROUP

9.1.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 9.1: isync command arguments

9.1.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-memory	String	show memory accesses by this instruction. Argument can be any combination of X (execute), L (load or store access) and S (system)
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-processorname	Boolean	Include processor name in all trace lines
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 9.2: itrace command arguments

Chapter 10

Registers

10.1 Level 1: CLUSTER_GROUP

No registers.