

### OVP Guide to Using Processor Models

# Model specific information for MIPS\_I6400

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Imperas OVP Fast Processor Model Documentation for MIPS_16400	

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### Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

### 1.1 Description

MIPS64 Configurable Processor Model

If you need other variants, these models can be obtained from www.OVPworld.org/ip-vendor-mips.

### 1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

### 1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/ip-vendor-mips.

Cache model does not implement coherency

### 1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

#### 1.5 Features

Only MIPS64 Instruction set implemented

MMU Type: Dual VTLB and FTLB

FPU implemented

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

Vectored interrupts implemented

## Configuration

### 2.1 Location

This model's VLNV is mips.ovpworld.org/processor/mips64/1.0.

The model source is usually at:

\$IMPERAS\_HOME/ImperasLib/source/mips.ovpworld.org/processor/mips64/1.0

The model binary is usually at:

\$IMPERAS\_HOME/lib/\$IMPERAS\_ARCH/ImperasLib/mips.ovpworld.org/processor/mips64/1.0

### 2.2 GDB Path

The default GDB for this model is: \$IMPERAS\_HOME/lib/\$IMPERAS\_ARCH/gdb/mips-sde-elf-gdb.

### 2.3 Semi-Host Library

The default semi-host library file is mips.ovpworld.org/semihosting/mips64Newlib/1.0

### 2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

### 2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

### 2.6 Processor ELF code

The ELF code supported by this model is: 0x8.

## All Variants in this model

This model has these variants

Variant	Description
P6600	
I6400	(described in this document)
MIPS64R6	
I6500	

Table 3.1: All Variants in this model

## **Bus Master Ports**

This model has these bus master ports.

Name	min	max	Connect?	Description
INSTRUCTION	INSTRUCTION 12 59 mandatory		mandatory	
DATA	12	59	optional	

Table 4.1: Bus Master Ports

# **Bus Slave Ports**

This model has no bus slave ports.

# Net Ports

This model has these net ports.

Name	Type	Connect?	Description
reset	input	optional	CMP reset
dint	input	optional	Debug external interrupt
int0	input	optional	GIC external interrupt
int1	input	optional	GIC external interrupt
int2	input	optional	GIC external interrupt
int3	input	optional	GIC external interrupt
int4	input	optional	GIC external interrupt
int5	input	optional	GIC external interrupt
int6	input	optional	GIC external interrupt
int7	input	optional	GIC external interrupt
int8	input	optional	GIC external interrupt
int9	input	optional	GIC external interrupt
int10	input	optional	GIC external interrupt
int11	input	optional	GIC external interrupt
int12	input	optional	GIC external interrupt
int13	input	optional	GIC external interrupt
int14	input	optional	GIC external interrupt
int15	input	optional	GIC external interrupt
int16	input	optional	GIC external interrupt
int17	input	optional	GIC external interrupt
int18	input	optional	GIC external interrupt
int19	input	optional	GIC external interrupt
int20	input	optional	GIC external interrupt
int21	input	optional	GIC external interrupt
int22	input	optional	GIC external interrupt
int23	input	optional	GIC external interrupt
int24	input	optional	GIC external interrupt
int25	input	optional	GIC external interrupt
int26	input	optional	GIC external interrupt
int27	input	optional	GIC external interrupt
int28	input	optional	GIC external interrupt

int29	input	optional	GIC external interrupt
int30	input	optional	GIC external interrupt
int31	input	optional	GIC external interrupt
int32	input	optional	GIC external interrupt
int33	input	optional	GIC external interrupt
int34	input	optional	GIC external interrupt
int35		optional	GIC external interrupt
int36	input		GIC external interrupt
	input	optional	-
int37	input	optional	GIC external interrupt GIC external interrupt
int38	input	optional	1
int39	input	optional	GIC external interrupt
int40	input	optional	GIC external interrupt
int41	input	optional	GIC external interrupt
int42	input	optional	GIC external interrupt
int43	input	optional	GIC external interrupt
int44	input	optional	GIC external interrupt
int45	input	optional	GIC external interrupt
int46	input	optional	GIC external interrupt
int47	input	optional	GIC external interrupt
int48	input	optional	GIC external interrupt
int49	input	optional	GIC external interrupt
int50	input	optional	GIC external interrupt
int51	input	optional	GIC external interrupt
int52	input	optional	GIC external interrupt
int53	input	optional	GIC external interrupt
int54	input	optional	GIC external interrupt
int55	input	optional	GIC external interrupt
int56	input	optional	GIC external interrupt
int57	input	optional	GIC external interrupt
int58	input	optional	GIC external interrupt
int59	input	optional	GIC external interrupt
int60	input	optional	GIC external interrupt
int61	input	optional	GIC external interrupt
int62	input	optional	GIC external interrupt
int63	input	optional	GIC external interrupt
int64	input	optional	GIC external interrupt
int65	input	optional	GIC external interrupt
int66	input	optional	GIC external interrupt
int67	input	optional	GIC external interrupt
int68	input	optional	GIC external interrupt
int69	input	optional	GIC external interrupt
int70	input	optional	GIC external interrupt
int71	input	optional	GIC external interrupt
int72	input	optional	GIC external interrupt
int73	input	optional	GIC external interrupt

int74	input	optional	GIC external interrupt
int75	input	optional	GIC external interrupt
int76	input	optional	GIC external interrupt
int77	input	optional	GIC external interrupt
int78	input	optional	GIC external interrupt
int79	input	optional	GIC external interrupt
int80	input	optional	GIC external interrupt
int81	input	optional	GIC external interrupt
int82	input	optional	GIC external interrupt
int83	input	optional	GIC external interrupt
int84	input	optional	GIC external interrupt
int85	input	optional	GIC external interrupt
int86	input	optional	GIC external interrupt
int87	input	optional	GIC external interrupt
int88	input	optional	GIC external interrupt
int89	input	optional	GIC external interrupt
int90	input	optional	GIC external interrupt
int91	input	optional	GIC external interrupt
int92	input	optional	GIC external interrupt
int93	input	optional	GIC external interrupt
int94	input	optional	GIC external interrupt
int95	input	optional	GIC external interrupt
int96	input	optional	GIC external interrupt
int97	input	optional	GIC external interrupt
int98	input	optional	GIC external interrupt
int99	input	optional	GIC external interrupt
int100	input	optional	GIC external interrupt
int101	input	optional	GIC external interrupt
int102	input	optional	GIC external interrupt
int103	input	optional	GIC external interrupt
int104	input	optional	GIC external interrupt
int105	input	optional	GIC external interrupt
int106	input	optional	GIC external interrupt
int107	input	optional	GIC external interrupt
int108	input	optional	GIC external interrupt
int109	input	optional	GIC external interrupt
int110	input	optional	GIC external interrupt
int111	input	optional	GIC external interrupt
int112	input	optional	GIC external interrupt
int113	input	optional	GIC external interrupt
int114	input	optional	GIC external interrupt
int115	input	optional	GIC external interrupt
int116	input	optional	GIC external interrupt
int117	input	optional	GIC external interrupt
int118	input	optional	GIC external interrupt
			<u>*</u>

[440	T.		
int119	input	optional	GIC external interrupt
int120	input	optional	GIC external interrupt
int121	input	optional	GIC external interrupt
int122	input	optional	GIC external interrupt
int 123	input	optional	GIC external interrupt
int 124	input	optional	GIC external interrupt
int125	input	optional	GIC external interrupt
int126	input	optional	GIC external interrupt
int127	input	optional	GIC external interrupt
ej_disable_probe_debug	input	optional	GIC ej_disable_probe_debug
ejtagbrk_override	input	optional	GIC ejtagbrk_override
ej_dint_in	input	optional	GIC ej_dint_in
GCR_CUSTOM_BASE	output	optional	Provides the least significant 32-bits of the value written to the GCR_CUSTOM_BASE register. Second half of GCR_CUSTOM_BASE_HI and GCR_CUSTOM_BASE output.
GCR_CUSTOM_BASE_UPPER	output	optional	Provides the most significant 32-bits of value written to the the GCR_CUSTOM_BASE register. First half of GCR_CUSTOM_BASE_HI and GCR_CUSTOM_BASE output.
dint_CPU0_VP0	input	optional	Debug external interrupt
hwint0_CPU0_VP0	input	optional	External interrupt
hwint1_CPU0_VP0	input	optional	External interrupt
hwint2_CPU0_VP0	input	optional	External interrupt
hwint3_CPU0_VP0	input	optional	External interrupt
hwint4_CPU0_VP0	input	optional	External interrupt
hwint5_CPU0_VP0	input	optional	External interrupt
nmi_CPU0_VP0	input	optional	Non-maskable external interrupt
EICPresent_CPU0_VP0	input	optional	Input signal SLEICPresent per VPE
EIC_RIPL_CPU0_VP0	input	optional	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VP0	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU0_VP0	input	optional	External interrupt controller vector number
EIC_VectorOffset_CPU0_VP0	input	optional	External interrupt controller vector offset
EIC_GID_CPU0_VP0	input	optional	External interrupt controller guest ID
intISS_CPU0_VP0	output	optional	True when interrupt request is serviced
causeTI_CPU0_VP0	output	optional	True when timer interrupt expires
causeIP0_CPU0_VP0	output	optional	Raised for software interrupt request IP0
causeIP1_CPU0_VP0	output	optional	Raised for software interrupt request IP1
si_sleep_CPU0_VP0	output	optional	True when the VPE is in WAIT state
hwint0	input	optional	External interrupt for compatibility
IIW IIIUU	րութա	obnonai	External interrupt for companionity

vc_run_CPU0_VP0	input	optional	Set to force stop of execution on processor
VC_1dii_C1 CO_V1 O	прис	optional	VPE (simulation control only)
Guest.EIC_RIPL_CPU0_VP0	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VP0	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VP0	input	optional	Guest External interrupt controller vector
Guest.EIC_vectorNum_CFU0_vFU	Input	орионаг	number
Guest.EIC_VectorOffset_CPU0_VP0	input	optional	Guest External interrupt controller vector
Guest.EIC_vectorOffset_CFO0_vF0	Input	орионаг	offset
Guest.EIC_GID_CPU0_VP0	input	optional	Guest External interrupt controller guest
Guest.EIC_GID_CI UU_VI U	Input	optionar	ID
Guest.intISS_CPU0_VP0	output	optional	True when Guest interrupt request is ser-
Guest.minss_C1 00_v1 0	Output	optionar	viced
Guest.causeTI_CPU0_VP0	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VP0	output	optional	Raised for Guest software interrupt re-
Guest.causem 0_Cr 00_vr 0	Output	optionar	quest IP0
Guest.causeIP1_CPU0_VP0	output	optional	Raised for Guest software interrupt re-
Guest.causem 1_C1 C0_V1 0	Output	optionar	quest IP1
dint_CPU0_VP1	input	optional	Debug external interrupt
hwint0_CPU0_VP1	input	optional	External interrupt
hwint1_CPU0_VP1	input	optional	External interrupt
hwint2_CPU0_VP1	input	optional	External interrupt
hwint3_CPU0_VP1	input	optional	External interrupt
hwint4_CPU0_VP1	input	optional	External interrupt
hwint5_CPU0_VP1	input	optional	External interrupt
nmi_CPU0_VP1		optional	Non-maskable external interrupt
EICPresent_CPU0_VP1	input	optional	Input signal SI_EICPresent per VPE
EIC-RIPL_CPU0_VP1	input	optional	External interrupt controller RIPL (alias
	input	optionar	of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VP1	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU0_VP1	input	optional	External interrupt controller vector num-
EIC_vectorivani_Cr Co_vr r	Input	optionar	ber
EIC_VectorOffset_CPU0_VP1	input	optional	External interrupt controller vector offset
EIC_GID_CPU0_VP1	input	optional	External interrupt controller guest ID
intISS_CPU0_VP1	output	optional	True when interrupt request is serviced
causeTI_CPU0_VP1	output	optional	True when timer interrupt expires
causeIP0_CPU0_VP1	output	optional	Raised for software interrupt request IP0
causeIP1_CPU0_VP1	output	optional	Raised for software interrupt request IP1
si_sleep_CPU0_VP1	output	optional	True when the VPE is in WAIT state
vc_run_CPU0_VP1	input	optional	Set to force stop of execution on processor
VO_1411_01 00_V1 1	Input	opuonar	VPE (simulation control only)
Guest.EIC_RIPL_CPU0_VP1	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VP1	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VP1	input	optional	Guest External interrupt controller vector
Gassillio Foctori Amilio Col VI I	Imput	optional	number
Guest.EIC_VectorOffset_CPU0_VP1	input	optional	Guest External interrupt controller vector
Gassillio_vectoronioco_or ou_vr	Imput	optional	offset
			offset

Guest.EIC_GID_CPU0_VP1	input	optional	Guest External interrupt controller guest ID
Guest.intISS_CPU0_VP1	output	optional	True when Guest interrupt request is ser-
	o strip str	- F	viced
Guest.causeTI_CPU0_VP1	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VP1	output	optional	Raised for Guest software interrupt re-
	_	-	quest IP0
Guest.causeIP1_CPU0_VP1	output	optional	Raised for Guest software interrupt re-
			quest IP1
dint_CPU1_VP0	input	optional	Debug external interrupt
hwint0_CPU1_VP0	input	optional	External interrupt
hwint1_CPU1_VP0	input	optional	External interrupt
hwint2_CPU1_VP0	input	optional	External interrupt
hwint3_CPU1_VP0	input	optional	External interrupt
hwint4_CPU1_VP0	input	optional	External interrupt
hwint5_CPU1_VP0	input	optional	External interrupt
nmi_CPU1_VP0	input	optional	Non-maskable external interrupt
EICPresent_CPU1_VP0	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VP0	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VP0	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU1_VP0	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU1_VP0	input	optional	External interrupt controller vector offset
EIC_GID_CPU1_VP0	input	optional	External interrupt controller guest ID
intISS_CPU1_VP0	output	optional	True when interrupt request is serviced
causeTI_CPU1_VP0	output	optional	True when timer interrupt expires
causeIP0_CPU1_VP0	output	optional	Raised for software interrupt request IP0
causeIP1_CPU1_VP0	output	optional	Raised for software interrupt request IP1
si_sleep_CPU1_VP0	output	optional	True when the VPE is in WAIT state
vc_run_CPU1_VP0	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU1_VP0	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VP0	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VP0	input	optional	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU1_VP0	input	optional	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU1_VP0	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU1_VP0	output	optional	True when Guest interrupt request is serviced
Guest.causeTI_CPU1_VP0	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VP0	output	optional	Raised for Guest software interrupt request IP0

C + ID1 CDII1 VD0		. 1	
Guest.causeIP1_CPU1_VP0	output	optional	Raised for Guest software interrupt re-
1: CDIII VD1	. ,	. 1	quest IP1
dint_CPU1_VP1	input	optional	Debug external interrupt
hwint0_CPU1_VP1	input	optional	External interrupt
hwint1_CPU1_VP1	input	optional	External interrupt
hwint2_CPU1_VP1	input	optional	External interrupt
hwint3_CPU1_VP1	input	optional	External interrupt
hwint4_CPU1_VP1	input	optional	External interrupt
hwint5_CPU1_VP1	input	optional	External interrupt
nmi_CPU1_VP1	input	optional	Non-maskable external interrupt
EICPresent_CPU1_VP1	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VP1	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VP1	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU1_VP1	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU1_VP1	input	optional	External interrupt controller vector offset
EIC_GID_CPU1_VP1	input	optional	External interrupt controller guest ID
intISS_CPU1_VP1	output	optional	True when interrupt request is serviced
causeTI_CPU1_VP1	output	optional	True when timer interrupt expires
causeIP0_CPU1_VP1	output	optional	Raised for software interrupt request IP0
causeIP1_CPU1_VP1	output	optional	Raised for software interrupt request IP1
si_sleep_CPU1_VP1	output	optional	True when the VPE is in WAIT state
vc_run_CPU1_VP1	input	optional	Set to force stop of execution on processor
	T	1	VPE (simulation control only)
Guest.EIC_RIPL_CPU1_VP1	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VP1	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VP1	input	optional	Guest External interrupt controller vector
	III par	optional	number
Guest.EIC_VectorOffset_CPU1_VP1	input	optional	Guest External interrupt controller vector
Guest. Lie-vector offiset-er er er	Inpat	optionar	offset
Guest.EIC_GID_CPU1_VP1	input	optional	Guest External interrupt controller guest
Guest. E101011 011 11	inpat	optional	ID
Guest.intISS_CPU1_VP1	output	optional	True when Guest interrupt request is ser-
Guest.intiss_cr Gr_vr1	Output	optionar	viced
Guest.causeTI_CPU1_VP1	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VP1	output	optional	Raised for Guest software interrupt re-
Guest.causem 0_C1 U1_V1 1	Սաւթա	optional	quest IP0
Guest.causeIP1_CPU1_VP1	output	optional	Raised for Guest software interrupt re-
Guest.causem 1_C1 U1_V1 1	Սաւթա	optional	quest IP1
dist CDII VD0	innut	ontional	=
dint_CPU2_VP0	input	optional	Debug external interrupt
hwint1_CPU2_VP0	input	optional	External interrupt
hwint1_CPU2_VP0	input	optional	External interrupt
hwint2_CPU2_VP0	input	optional	External interrupt
hwint3_CPU2_VP0	input	optional	External interrupt

hwint4_CPU2_VP0	input	optional	External interrupt
hwint5_CPU2_VP0	input	optional	External interrupt
nmi_CPU2_VP0	input	optional	Non-maskable external interrupt
EICPresent_CPU2_VP0	input	optional	Input signal SLEICPresent per VPE
EIC_RIPL_CPU2_VP0	input	optional	External interrupt controller RIPL (alias
	1	•	of hwint0 - 5 or 7)
EIC_EICSS_CPU2_VP0	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU2_VP0	input	optional	External interrupt controller vector num-
	_	-	ber
EIC_VectorOffset_CPU2_VP0	input	optional	External interrupt controller vector offset
EIC_GID_CPU2_VP0	input	optional	External interrupt controller guest ID
intISS_CPU2_VP0	output	optional	True when interrupt request is serviced
causeTI_CPU2_VP0	output	optional	True when timer interrupt expires
causeIP0_CPU2_VP0	output	optional	Raised for software interrupt request IP0
causeIP1_CPU2_VP0	output	optional	Raised for software interrupt request IP1
si_sleep_CPU2_VP0	output	optional	True when the VPE is in WAIT state
vc_run_CPU2_VP0	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU2_VP0	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU2_VP0	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU2_VP0	input	optional	Guest External interrupt controller vector
			number
Guest.EIC_VectorOffset_CPU2_VP0	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU2_VP0	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU2_VP0	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU2_VP0	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU2_VP0	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU2_VP0	output	optional	Raised for Guest software interrupt re-
1: + CDUO VD1	. ,	1	quest IP1
dint_CPU2_VP1	input	optional	Debug external interrupt
hwint0_CPU2_VP1	input	optional	External interrupt
hwint1_CPU2_VP1	input	optional	External interrupt
hwint2_CPU2_VP1 hwint3_CPU2_VP1	input	optional	External interrupt
	input	optional	External interrupt
hwint4_CPU2_VP1 hwint5_CPU2_VP1	input	optional	External interrupt
	input	optional	External interrupt
nmi_CPU2_VP1 EICPresent_CPU2_VP1	input	optional	Non-maskable external interrupt
	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU2_VP1	input	optional	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU2_VP1	innut	ontional	External interrupt controller EICSS
EIO_EIOSS_OFU2_VF1	input	optional	External interrupt controller EIC55

EIC_VectorNum_CPU2_VP1	innut	optional	External interrupt controller vector num-
EIC_vectorNum_CF U2_vF1	input	орионаг	_
EIC_VectorOffset_CPU2_VP1	innut	ontional	ber External interrupt controller vector offset
EIC_VectorOffset_CF U2_VF1	input input	optional optional	External interrupt controller guest ID
intISS_CPU2_VP1	_		True when interrupt request is serviced
causeTI_CPU2_VP1	output	optional	True when timer interrupt expires
causeIP0_CPU2_VP1	output	optional	Raised for software interrupt request IP0
causeIP1_CPU2_VP1	output	optional optional	Raised for software interrupt request IP1
	output		True when the VPE is in WAIT state
si_sleep_CPU2_VP1 vc_run_CPU2_VP1	output input	optional optional	Set to force stop of execution on processor
verun er ez vi i	mput	optional	VPE (simulation control only)
Guest.EIC_RIPL_CPU2_VP1	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU2_VP1	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU2_VP1	input	optional	Guest External interrupt controller vector
			number
Guest.EIC_VectorOffset_CPU2_VP1	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU2_VP1	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU2_VP1	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU2_VP1	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU2_VP1	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU2_VP1	output	optional	Raised for Guest software interrupt re-
			quest IP1
dint_CPU3_VP0	input	optional	Debug external interrupt
hwint0_CPU3_VP0	input	optional	External interrupt
hwint1_CPU3_VP0	input	optional	External interrupt
hwint2_CPU3_VP0	input	optional	External interrupt
hwint3_CPU3_VP0	input	optional	External interrupt
hwint4_CPU3_VP0	input	optional	External interrupt
hwint5_CPU3_VP0	input	optional	External interrupt
nmi_CPU3_VP0	input	optional	Non-maskable external interrupt
EICPresent_CPU3_VP0	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU3_VP0	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU3_VP0	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU3_VP0	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU3_VP0	input	optional	External interrupt controller vector offset
EIC_GID_CPU3_VP0	input	optional	External interrupt controller guest ID
intISS_CPU3_VP0	output	optional	True when interrupt request is serviced
causeTI_CPU3_VP0	output	optional	True when timer interrupt expires
causeIP0_CPU3_VP0	output	optional	Raised for software interrupt request IP0

causeIP1_CPU3_VP0	output	optional	Raised for software interrupt request IP1
si_sleep_CPU3_VP0	output	optional	True when the VPE is in WAIT state
vc_run_CPU3_VP0	input	optional	Set to force stop of execution on processor
	_	•	VPE (simulation control only)
Guest.EIC_RIPL_CPU3_VP0	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU3_VP0	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU3_VP0	input	optional	Guest External interrupt controller vector
	1	•	number
Guest.EIC_VectorOffset_CPU3_VP0	input	optional	Guest External interrupt controller vector
	1	-	offset
Guest.EIC_GID_CPU3_VP0	input	optional	Guest External interrupt controller guest
	1	•	ID
Guest.intISS_CPU3_VP0	output	optional	True when Guest interrupt request is ser-
		_	viced
Guest.causeTI_CPU3_VP0	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU3_VP0	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU3_VP0	output	optional	Raised for Guest software interrupt re-
			quest IP1
dint_CPU3_VP1	input	optional	Debug external interrupt
hwint0_CPU3_VP1	input	optional	External interrupt
hwint1_CPU3_VP1	input	optional	External interrupt
hwint2_CPU3_VP1	input	optional	External interrupt
hwint3_CPU3_VP1	input	optional	External interrupt
hwint4_CPU3_VP1	input	optional	External interrupt
hwint5_CPU3_VP1	input	optional	External interrupt
nmi_CPU3_VP1	input	optional	Non-maskable external interrupt
EICPresent_CPU3_VP1	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU3_VP1	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU3_VP1	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU3_VP1	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU3_VP1	input	optional	External interrupt controller vector offset
EIC_GID_CPU3_VP1	input	optional	External interrupt controller guest ID
intISS_CPU3_VP1	output	optional	True when interrupt request is serviced
causeTI_CPU3_VP1	output	optional	True when timer interrupt expires
causeIP0_CPU3_VP1	output	optional	Raised for software interrupt request IP0
causeIP1_CPU3_VP1	output	optional	Raised for software interrupt request IP1
si_sleep_CPU3_VP1	output	optional	True when the VPE is in WAIT state
vc_run_CPU3_VP1	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU3_VP1	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU3_VP1	input	optional	Guest External interrupt controller EICSS

Guest.EIC_VectorNum_CPU3_VP1	input	optional	Guest External interrupt controller vector
			number
Guest.EIC_VectorOffset_CPU3_VP1	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU3_VP1	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU3_VP1	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU3_VP1	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU3_VP1	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU3_VP1	output	optional	Raised for Guest software interrupt re-
			quest IP1

Table 6.1: Net Ports

# FIFO Ports

This model has no FIFO ports.

## Formal Parameters

Name	Type	Description
variant	Enumeration	Processor variant
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info struc-
		ture
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB
•		exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
gprNames	Boolean	Disassemble the register names from the default
		ABI instead of register numbers for MIPS-format
		trace output
supervisorMode	Boolean	Override whether processor implements supervisor
		mode
busErrors	Boolean	Override bus error exception behavior. When true,
		accesses of memory not defined by platform will
		cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when
		true (sets Config.MT=3, Config.KU/K23=2 and
		Config1.MMUSizeM1=0)
fixedDbgRegSize	Boolean	Enable applications to debug on P5600 with GDB
		version 2015.06-05 and prior
removeDSP	Boolean	Override the DSP-present configuration when true
		(sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true
		(sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true
		(sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true
		(disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from
		ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to
		maximum value to improve performance
perfCounters	Uns32	Performance Counters
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores
		only)

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ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC
IMODINOD	TT 00	implementation (MT cores only)
ITCFIFODepth	Uns32	Specify ITC FIFO cell depth. By default supports
		4.
ITCEmptyOnReset	Boolean	Specify ITC E/F cells reset to a known empty state.
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior,
		2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal
		operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0. Ig-
		nored if less than two VPEs configured.
VPE1MaxTC	Uns32	Specifies the maximum TCs initially on VPE1. Ig-
		nored if less than three VPEs configured.
segBits	Uns32	Override the number of address bits implemented
508210	011002	for 64 bit segments (MIPS64 Only)
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentCon-
		trol_0 register
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentCon-
		trol_0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentCon-
		trol_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentCon-
		trol_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentCon-
		trol_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentCon-
		trol_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentCon-
		trol_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentCon-
•		trol_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentCon-
		trol_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentCon-
inp ac eginenee	011302	trol_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentCon-
inpusegment to	0.11502	trol_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentCon-
inpusegment11	011852	trol_2 register
mpuSegment12	IIma 20	Attributes for segment 12 in MPU2 SegmentCon-
mpusegment12	Uns32	
	TT 00	trol-3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentCon-
9 114	77 00	trol_3 register
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentCon-
~		trol_3 register
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentCon-
		trol_3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
tcDisable	Uns32	Number of disabled TCs
vpeDisable	Uns32	Number of disabled VPEs
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
		<u> </u>

mvpconf1c1f	Boolean	Override MVPConf.C1F
mvpcontrolPolicyMode	Boolean	Override MVPControl.POLICY_MODE
hasFDC	Uns32	Specify the size of Fast Debug Channel register
		block
licenseWarningDays	Uns32	Specify the number of days before a license expires
		to start issuing a warning. 0 disables warnings.
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string separated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
TRU_PRESENT	Boolean	Disable or Enable based on TRU presence to control certain fields (e.x.perfCtl.PCTD
ucLLwordsLocked	Uns32	Numbers of words (4 byte) an uncached LL is lock-
		ing. Maximum: 4K
FUSA	Boolean	Enable Functional Safety
CPC_FAULT_SUPPORTED	Uns32	Specify the value for Functional Safety Supported register
CPC_FAULT_ENABLE	Uns32	Specify the value for Functional Safety Enable register
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object
		(.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll) defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller
		(sets Config3 VEIC)
config3VEIC_VPE0	Boolean	Enables an external interrupt controller on VPE0 (sets Config3 VEIC)
config3VEIC_VPE1	Boolean	Enables an external interrupt controller on VPE1 (sets Config3 VEIC)
config3VEIC_VPE2	Boolean	Enables an external interrupt controller on VPE2 (sets Config3 VEIC)
config3VEIC_VPE3	Boolean	Enables an external interrupt controller on VPE3 (sets Config3 VEIC)
${\bf rootFixedMMU}$	Boolean	Override the root MMU type to fixed mapping when true (sets Config.MT=3 and Config.KU/K23=2)
${\bf rootMMUSizeM1}$	Uns32	Override the root MMUSizeM1 field in Config1 register (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
usePreciseFpu	Uns32	Use the precise Floating Point emulation
simulateLite	Enumeration	Run Simulation with optimization. There are
		several optimizations which coule be combined (NONE, FS, MA or FSMA)
pridCompanyOptions	Uns32	Override the Company Options field in PRId register
pridRevision	Uns32	Override the Revision field in PRId register
*		

globalClusterNum	Uns32	Override the ClusterNum field in GlobalNumber register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intctlIPFDC	Uns32	Override the IPFDC field in IntCtl register
intctlIPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
maxVP	Uns32	Specify maximum number of Virtual Processors present in a core
numVP	Uns32	Specify number of Virtual Processors to be present
numVPtoStart	Uns32	Specify number of Virtual Processors to be started
sharedTLBindex	Uns32	Specify first shared TLB Index between Virtual Cores
xconfigSpecified	Boolean	True if the configuration comes from a valid xconfig file
intctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
intctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
intctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
intctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
intctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
intctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
intctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
intctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
intctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
intctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
intctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
intctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
intctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
intctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
intctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
intctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
intctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
intctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
intctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
intctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
intctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0

intctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
intctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
intctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
intctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
intctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
intctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
intctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
intctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
intctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
intctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
intctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
intctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
intctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
intctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
intctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
intctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
intctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
intctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
intctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
intctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
intctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
intctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
intctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
intctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
intctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
intctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
intctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
intctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0

intctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
intctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
intctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
intctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
intctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
intctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
intctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
intctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
intctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
intctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
intctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
intctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
intctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
intctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
intctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
intctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
intctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
intctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
intctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
intctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
intctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
intctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
intctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
intctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
intctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
intctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
intctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
intctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0

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intctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
intctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
intctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
intctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
intctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
intctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU4_VP3	Uns32	CPU4/VP2 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU5_VP0	Uns32	CPU4/VP3 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU5_VP1	Uns32	CPU5/VP0 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU5_VP2	Uns32	CPU5/VP1 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU5_VP3	Uns32	CPU5/VP2 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU6_VP0	Uns32	CPU5/VP3 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU6_VP1	Uns32	CPU6/VP0 Override the IPPCI field in IntCtl register for
intctlIPPCI_CPU6_VP2	Uns32	CPU6/VP1 Override the IPPCI field in IntCtl register for
		CPU6/VP2
intctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
intctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
intctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
intctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
intctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
segcfg0PA	Uns32	Set CFG0.PA field of SegCtl0 register
segcfg1PA	Uns32	Set CFG1.PA field of SegCtl0 register
segcfg2PA	Uns32	Set CFG2.PA field of SegCtl1 register
segcfg3PA	Uns32	Set CFG3.PA field of SegCtl1 register
segcfg4PA	Uns32	Set CFG4.PA field of SegCtl2 register
segcfg5PA	Uns32	Set CFG5.PA field of SegCtl2 register
segcfg0AM	Uns32	Set CFG0.AM field of SegCtl0 register
segcfg1AM	Uns32	Set CFG1.AM field of SegCtl0 register
segcfg2AM	Uns32	Set CFG2.AM field of SegCtl1 register
segcfg3AM	Uns32	Set CFG3.AM field of SegCtl1 register
segcfg4AM	Uns32	Set CFG4.AM field of SegCtl2 register
segcig4AW segcfg5AM	Uns32	Set CFG5.AM field of SegCtl2 register
segcfg0EU	Uns32	Set CFG0.EU field of SegCtl2 register
segcfg1EU	Uns32	Set CFG0.EU field of SegCtl0 register  Set CFG1.EU field of SegCtl0 register
segcfg2EU	Uns32	Set CFG1.EU field of SegCtl1 register
segcfg3EU	Uns32	Set CFG3.EU field of SegCtl1 register
segcfg4EU	Uns32	Set CFG3.EU field of SegCtl1 register  Set CFG4.EU field of SegCtl2 register
segcfg5EU	Uns32	Set CFG4.EU field of SegCtl2 register  Set CFG5.EU field of SegCtl2 register
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segcfg0C	Uns32	Set CFG0.C field of SegCtl0 register
segcfg1C	Uns32	Set CFG1.C field of SegCtl0 register
segcfg2C	Uns32	Set CFG2.C field of SegCtl1 register
segcfg3C	Uns32	Set CFG3.C field of SegCtl1 register
segcfg4C	Uns32	Set CFG4.C field of SegCtl2 register
segcfg5C	Uns32	Set CFG5.C field of SegCtl2 register
cdmmSize	Uns32	Override the cdmmsize reset value
configAR	Uns32	Enables R6 support
configBM	Uns32	Override the BM field in Config register (burst
ConngDW	Ulis52	mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM
ConngDSP	Doolean	_ ` ` `
configISP	Boolean	present) Override Config.ISP (instruction scratchpad RAM
conngisP	Boolean	
C IZO	II 90	present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0
C TITT	11 00	cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg
0.7722	***	cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23
		cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide
		unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
configBCP	Boolean	Override Config.BCP (Buffer Cache Present)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Dcache associativity)
config1DL	Uns32	Override Config1.DL (Dcache line size)
config1DS	Uns32	Override Config1.DS (Dcache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU
		entries-1)
config1MMUSizeM1_VPE1	Uns32	Override Config1.MMUSizeM1 for VPE1
config1MMUSizeM1_VPE2	Uns32	Override Config1.MMUSizeM1 for VPE2
config1MMUSizeM1_VPE3	Uns32	Override Config1.MMUSizeM1 for VPE3
config1WR	Boolean	Override Config1.WR (watchpoint registers
		present)
config1PC	Boolean	Override Config1.PC (Performance Counters
001111811 0	Booloan	present)
config1C2	Boolean	Override Config1.C2 (Coprocessor 2 present)
config2SU	Uns32	Override Comignes (Coprocessor 2 present)  Override the SU field in Config2 register
config2SS	Uns32	Override the SS field in Config2 register
config2SL	Uns32	Override the SL field in Config2 register
config2SA	Uns32	Override the SA field in Config2 register
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA

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	config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3MMAR         Uns32         Override Config3.MMAR           config3RX1         Boolean         Override Config3.RXI           config3UR1         Boolean         Override Config3.RXI           config3UR1         Boolean         Override Config3.RXI           config3UR1         Boolean         Override Config3.WZ           config3MSAP         Boolean         Override the Config3.WSAP           config3SP         Boolean         Override the EM Gid in Config3 register           config3PW         Boolean         Override the EM field in Config3 register           config4AE         Boolean         Override the Pfi field in Config3 register           config4MUConfig         Uns32         Override Config4.ME           config4MWUConfig         Uns32         Override Config4.MUConfig field (interpretation depends on MMUExtDef value)           config4MWUExtDef         Uns32         Override Config4.MMUExtDef           config4MWUExtDef         Uns32         Override Config5.MMWUExtDef           config5MRP         Boolean         Override Config5.MEAMMUExtDef           config5MRP         Boolean         Override Config5.MEAMMUExtDef           config5MRP         Boolean         Override Config5.MEAMMUExtDef           config5MRP         Boolean         Override Config5.MEAMMUExtDef			
config3MMAR         Uns22         Override Config3.RXI           config3RXI         Boolean         Override Config3.RXI           config3ULRI         Boolean         Override Config3.RXI           config3VZ         Boolean         Override Config3.VZI           config3MSAP         Boolean         Override Config4.WZ           config3SMGCR         Boolean         Override the CMGCR field in Config3 register           config3TL         Uns32         Override the TL field in Config3 register           config3PW         Boolean         Override the PW field in Config3 register           config4AE         Boolean         Override Config4.In Config3 register           config4HE         Uns32         Override Config4.In Config3 register           config4HMUConfig         Uns32         Override Config4.MMUConfig field (interpretation depends on MMUExtDef           config4MMUExtDef         Uns32         Override Config4.MMUConfig field (interpretation depends on MMUExtDef           config4MTLBSizeExt         Uns32         Override Config4.WTLBSizeExt           config4MUExtDef         Uns32         Override Config4.WTLBSizeExt           config5EVA         Boolean         Override Config4.WTLBSizeExt           config5MRP         Boolean         Override Config5.MEX           config5MExists         B			
config3RNI			
config3URI         Boolean         Override Config3.SC           config3URI         Boolean         Override Config3.URI           config3MSAP         Boolean         Override Config3.MSAP           nonfig3GMGCR         Boolean         Override to Config3.MSAP           config3SP         Boolean         Override the CMGCR field in Config3 register           config3TL         Uns32         Override the PB field in Config3 register           config4AE         Boolean         Override the PW field in Config3 register           config4IE         Uns32         Override Config4.AE           config4MMUConfig         Uns32         Override Config4.BI           config4MMUExtDef         Uns32         Override Config4.MMUConfig field (interpretation depends on MMUExtDef value)           config4MSEExts         Uns32         Override Config4.WTLB5izeExt           config4SEVA         Boolean         Override Config4.WTLB5izeExt           config5EVA         Boolean         Override Config5.EVA           config5MRP         Boolean         Override Config5.SEX           config5MRP         Boolean         Override Config5.MFExists           config5MSAEn         Boolean         Override Config5.MSEx           config5MSAEn         Boolean         Override Config5.MYII (enable MTHCO and MFHCO instruct			
config3ULRI         Boolean         Override Config3.URI           config3WS         Boolean         Override Config3.VZ           config3CMGCR         Boolean         Override Config3.WSAP           config3SP         Boolean         Override the CMGCR field in Config3 register           config3TL         Uns32         Override the SP field in Config3 register           config4TE         Boolean         Override Config4.IF           config4ME         Boolean         Override Config4.IF           config4MMUConfig         Uns32         Override Config4.MIMUConfig field (interpretation depends on MMUExtDef config4.IF           config4MMUExtDef         Uns32         Override Config4.MMUExtDef           config4MMUExtDef         Uns32         Override Config4.MMUExtDef           config4FXLBSizeExt         Uns32         Override Config4.MScrExis           config4FXCEXist         Uns32         Override Config5.MSCrExist           config5DEVA         Boolean         Override Config5.SLB (LLAddr supports LLbit)           config5MRP         Boolean         Override Config5.MRP (MaaR Present)           config5MSAEn         Boolean         Override Config5.MSAEn           config5MSAEn         Boolean         Override Config5.MSAEn           config5DEC         Boolean         Override Config5.M			
config3VX			
Boolean   Override Config3MSAP   Config3CMGCR   Boolean   Override the CMGCR field in Config3 register			
config3CMGCR         Boolean         Override the CMGCR field in Config3 register           config3PP         Boolean         Override the SP field in Config3 register           config3PW         Boolean         Override the TL field in Config3 register           config4AE         Boolean         Override Config4. ME           config4IE         Uns32         Override Config4. ME (config4. ME)           config4MUExtDef         Uns32         Override Config4. MMUCanfig field (interpretation depends on MMUExtDef value)           config4VTLBsizeExt         Uns32         Override Config4. MMUExtDef           config4VTLBsizeExt         Uns32         Override Config4. MMUExtDef           config4VTLBsizeExt         Uns32         Override Config4. MSerExist           config4VTLBsizeExt         Uns32         Override Config5. WA           config5EVA         Boolean         Override Config5. EVA           config5MP         Boolean         Override Config5. MRP (MaaR Present)           config5MRP         Boolean         Override Config5. MRP (MaaR Present)           config5MSAEn         Boolean         Override Config5. MRP (MaaR Present)           config5MWH         Boolean         Override Config5. MRP (MaaR Present)           config5MSAEn         Boolean         Override Config5. MWH (enable MTHC0 and MFHC0 instructions) </td <td></td> <td></td> <td></td>			
Boolean   Override the SP field in Config3 register			
config3TW         Boolean Override the PW field in Config3 register           config4AE         Boolean Override Config4.AE           config4HE         Uns32 Override Config4.AE           config4MUConfig         Uns32 Override Config4.MMUConfig field (interpretation depends on MMUExtDef value)           config4MMUExtDef         Uns32 Override Config4.MMUExtDef           config4YTLBSizeExt         Uns32 Override Config4.MMUExtDef           config4SEVA         Boolean Override Config5.EVA           config5EVA         Boolean Override Config5.ELB (LLAddr supports LLbit)           config5MRP         Boolean Override Config5.MRP (MaaR Present)           config5MRP         Boolean Override Config5.MRP (MaaR Present)           config5Mscor         Boolean Override Config5.MRP (MaaR Present)           config5MsAEn         Boolean Override Config5.MSAEn           config5MVH         Boolean Override Config5.MSAEn           config5DEC         Boolean Override Config5.MVH (enable MTHC0 and MFHC0 instructions)           config5GI         Uns32 Override Config5.GI (enable GINV)           config5GI         Uns32 Override Config5.GI (enable GINV)           config5TRB         Boolean Override Config5.TGC (frecap Present)           config7TR         Boolean Override Config5.TGC (frecap Present)           config7TRR         Boolean Override Config7.TGC (Hardware Cache Initializati		Boolean	1
Boolean   Override Config3 register		Boolean	
config4AE	config3TL	Uns32	Override the TL field in Config3 register
Config4MMUExtDef	config3PW	Boolean	Override the PW field in Config3 register
config4MMUConfig  Uns32 Override Config4.MMUConfig field (interpretation depends on MMUExtDef value)  config4WTLBSizeExt  Uns32 Override Config4.MWLExtDef  config4WTLBSizeExt  Uns32 Override Config4.MTLBSizeExt  config4KScrExist  Uns32 Override Config4.WTLBSizeExt  config5WA Boolean  Override Config5.EVA  config5LLB Boolean  Override Config5.ELB (LLAddr supports LLbit)  config5MRP Boolean  Override Config5.MRP (MaaR Present)  config5MRP Boolean  Override Config5.MRP (MaaR Present)  config5MSExists  mips32Macro  Boolean  Boolean  Override Config5.MRP (MaaR Present)  config5MSAEn  Boolean  Override Config5.MSAEn  config5MVH Boolean  Override Config5.MSAEn  config5MVH Boolean  Override Config5.MVH (enable MTHC0 and MFHC0 instructions)  config5GCC  Boolean  Override Config5.GC (to test Dual Endian Capability)  config5GT  Uns32 Override Config5.DC (to test Dual Endian Capability)  config5TLBEn  config5TLBEn  Boolean  Override Config5.TCP (CRCP Present)  config6FTLBEn  Boolean  Override Config5.TCP  Boolean  Override Config5.TCP  config6FTLBEn  Boolean  Override Config5.TCP  Config6FTLBEn  Boolean  Override Config7.AC (Alias removed Data cache)  config7TOCIDX.MODE  Uns32  Override Config7.AC (Alias removed Instruction cache)  Config7HCI  Boolean  Override Config7.AC (Alias removed Instruction cache)  Override Config7.AC (Alias removed Instruction cache)  Override Config7.AC (Alias removed Instruction cache)  Override Config7.AC (Maternative implementation of Watch registers)  config7TOCIDX.MODE  Uns32  Override Config7.BI (Alternative implementation of Watch registers)  config7BEN  Boolean  Override Config7.BI bit (Alternative implementation of Watch registers)  Override Config7.BI bit (Alternative implementation of Watch register	config4AE	Boolean	Override Config4.AE
config4MMUConfig  Uns32 Override Config4.MMUConfig field (interpretation depends on MMUExtDef value)  config4WTLBSizeExt  Uns32 Override Config4.MWLExtDef  config4WTLBSizeExt  Uns32 Override Config4.MTLBSizeExt  config4KScrExist  Uns32 Override Config4.WTLBSizeExt  config5WA Boolean  Override Config5.EVA  config5LLB Boolean  Override Config5.ELB (LLAddr supports LLbit)  config5MRP Boolean  Override Config5.MRP (MaaR Present)  config5MRP Boolean  Override Config5.MRP (MaaR Present)  config5MSExists  mips32Macro  Boolean  Boolean  Override Config5.MRP (MaaR Present)  config5MSAEn  Boolean  Override Config5.MSAEn  config5MVH Boolean  Override Config5.MSAEn  config5MVH Boolean  Override Config5.MVH (enable MTHC0 and MFHC0 instructions)  config5GCC  Boolean  Override Config5.GC (to test Dual Endian Capability)  config5GT  Uns32 Override Config5.DC (to test Dual Endian Capability)  config5TLBEn  config5TLBEn  Boolean  Override Config5.TCP (CRCP Present)  config6FTLBEn  Boolean  Override Config5.TCP  Boolean  Override Config5.TCP  config6FTLBEn  Boolean  Override Config5.TCP  Config6FTLBEn  Boolean  Override Config7.AC (Alias removed Data cache)  config7TOCIDX.MODE  Uns32  Override Config7.AC (Alias removed Instruction cache)  Config7HCI  Boolean  Override Config7.AC (Alias removed Instruction cache)  Override Config7.AC (Alias removed Instruction cache)  Override Config7.AC (Alias removed Instruction cache)  Override Config7.AC (Maternative implementation of Watch registers)  config7TOCIDX.MODE  Uns32  Override Config7.BI (Alternative implementation of Watch registers)  config7BEN  Boolean  Override Config7.BI bit (Alternative implementation of Watch registers)  Override Config7.BI bit (Alternative implementation of Watch register		Uns32	
depends on MMUExtDef value		Uns32	
config4MMUExtDef         Uns32         Override Config4.MMUExtDef           config4VTLBSizeExt         Uns32         Override Config4.MMUExtDef           config4KScrExist         Uns32         Override Config4.MScrExist           config5EVA         Boolean         Override Config5.EVA           config5DLB         Boolean         Override Config5.LLB (LLAddr supports LLbit)           config5MRP         Boolean         Override Config5.MFE (MaaR Present)           config5MFExists         Boolean         Override Config5.MFExists           mips32Macro         Boolean         Doverride Config5.MSAEn           config5MSAEn         Boolean         Override Config5.MSAEn           config5MVH         Boolean         Override Config5.MVH (enable MTHC0 and MFHC0 instructions)           config5DEC         Boolean         Override Config5.DEC (to test Dual Endian Capability)           config5GI         Uns32         Override Config5.DEC (to test Dual Endian Capability)           config5CRCP         Boolean         Override Config5.CRCP (CRCP Present)           config5VP         Boolean         Override Config5.VP           config6FTLBEn         Boolean         Override Config7.AR (Alias removed Data cache)           config7HCI         Boolean         Override Config7.HCI (Hardware Cache Initialization)           <			
config4VTLBSizeExt         Uns32         Override Config4.VTLBSizeExt           config4KScrExist         Uns32         Override Config4.KScrExist           config5LLB         Boolean         Override Config5.LLB (LLAddr supports LLbit)           config5MRP         Boolean         Override Config5.MRP (MaaR Present)           config5NFExists         Boolean         Override Config5.MRP (MaaR Present)           config5MSAEro         Boolean         Override Config5.MSAE and RESTORE macro instructions. Ignored if Config5.CA2 is not set)           config5MSAEn         Boolean         Override Config5.MSAEn           config5MVH         Boolean         Override Config5.MSAEn           config5DEC         Boolean         Override Config5.MSAEn           config5DEC         Boolean         Override Config5.DEC (to test Dual Endian Capability)           config5DEC         Boolean         Override Config5.GI (enable GINV)           config5GRCP         Boolean         Override Config5.GRCP (CRCP Present)           config6FTLBEn         Boolean         Override Config5.NP           config7AR         Boolean         Override Config7.AR (Alias removed Data cache)           config7HCI         Boolean         Override Config7.TAI (Marware Cache Initialization)           config7IAR         Boolean         Override Config7.TAI (Mait IE/IXMT ig	config4MMUExtDef	Uns32	/
config5EVA         Boolean         Override Config5.LB (LIAddr supports LIbit)           config5LLB         Boolean         Override Config5.LB (LIAddr supports LIbit)           config5MRP         Boolean         Override Config5.LB (LIAddr supports LIbit)           config5MRP         Boolean         Override Config5.LB (LIAddr supports LIbit)           config5MRP         Boolean         Override Config5.MRP (MaaR Present)           config5MSEsits         Boolean         Override Config5.MSAEs           config5MSAEn         Boolean         Override Config5.MSAEn           config5MVH         Boolean         Override Config5.MSAEn           config5DEC         Boolean         Override Config5.MVH (enable MTHC0 and MFHC0 instructions)           config5GI         Uns32         Override Config5.GI (enable GINV)           config5GRCP         Boolean         Override Config5.GI (enable GINV)           config5VP         Boolean         Override Config5.VP           config7AR         Boolean         Override Config5.VP           config7AR         Boolean         Override Config7.AR (Alias removed Data cache)           config7HCI         Boolean         Override Config7.HCI (Hardware Cache Initialization)           config7HAR         Boolean         Override Config7.HCI (Hardware Cache Initialization)           <			
config5EVA         Boolean         Override Config5.EVA           config5MRP         Boolean         Override Config5.LLB (LLAddr supports LLbit)           config5MRP         Boolean         Override Config5.MRP (MaaR Present)           config5MFExists         Boolean         Override Config5.NFExists           mips32Macro         Boolean         Enables the MIPS32 SAVE and RESTORE macro instructions. Ignored if Config5.CA2 is not set)           config5MSAEn         Boolean         Override Config5.MSAEn           config5MVH         Boolean         Override Config5.MVH (enable MTHC0 and MFHC0 instructions)           config5DEC         Boolean         Override Config5.DEC (to test Dual Endian Capability)           config5GI         Uns32         Override Config5.GRP (cRCP Present)           config5CRCP         Boolean         Override Config5.CRP (CRCP Present)           config6FTLBEn         Boolean         Override Config5.VP           config6FTLBEn         Boolean         Override Config7.EAR (Alias removed Data cache)           config7DCIDX.MODE         Uns32         Override Config7.AR (Alias removed Instruction cache)           config7HCI         Boolean         Override Config7.HAR (Alias removed Instruction cache)           config7WR         Boolean         Override Config7.HAR (Alias removed Instruction cache)           config7WR <td></td> <td></td> <td></td>			
config5LLB         Boolean         Override Config5.LLB (LLAddr supports LLbit)           config5MRP         Boolean         Override Config5.MRP (MaaR Present)           config5NFExists         Boolean         Override Config5.NFExists           mips32Macro         Boolean         Enables the MIPS32 SAVE and RESTORE macro instructions. Ignored if Config5.CA2 is not set)           config5MSAEn         Boolean         Override Config5.MVH (enable MTHC0 and MFHC0 instructions)           config5MVH         Boolean         Override Config5.DEC (to test Dual Endian Capability)           config5DEC         Boolean         Override Config5.DEC (to test Dual Endian Capability)           config5GI         Uns32         Override Config5.GI (enable GINV)           config5CRCP         Boolean         Override Config5.VP (CRCP Present)           config5VP         Boolean         Override Config5.VP (CRCP Present)           config7AR         Boolean         Override Config7.AR (Alias removed Data cache)           config7HCI         Boolean         Override Config7.DCIDX.MODE           config7HCI         Boolean         Override Config7.BCIDX.MODE           config7HAR         Boolean         Override Config7.HA (Alias removed Instruction cache)           config7BWI         Boolean         Override Config7.WI (wait IE/IXMT ignore)           config7WR			
config5MRP         Boolean         Override Config5.MRP (MaaR Present)           config5NFExists         Boolean         Override Config5.NFExists           mips32Macro         Boolean         Enables the MIPS32 SAVE and RESTORE macro instructions. Ignored if Config5.CA2 is not set)           config5MSAEn         Boolean         Override Config5.MSAEn           config5MVH         Boolean         Override Config5.MVH (enable MTHC0 and MFHC0 instructions)           config5DEC         Boolean         Override Config5.DEC (to test Dual Endian Capability)           config5GI         Uns32         Override Config5.GR (enable GINV)           config5CRCP         Boolean         Override Config5.CRCP (CRCP Present)           config5VP         Boolean         Override Config5.CRCP (CRCP Present)           config6FTLBEn         Boolean         Override Config7.CRCP (CRCP Present)           config7AR         Boolean         Override Config7.AR (Alias removed Data cache)           config7AR         Boolean         Override Config7.DCIDX.MODE           config7HCI         Boolean         Override Config7.HCI (Hardware Cache Initialization)           config7IAR         Boolean         Override Config7.HR (Alias removed Instruction cache)           config7WR         Boolean         Override Config7.SIR (Alias removed Instruction cache)           config7WR <td></td> <td></td> <td></td>			
Boolean   Override Config5.NFExists			
mips32Macro  Boolean  Config5MSAEn  Config5MSAEn  Boolean  Config5MVH  Boolean  Config5MVH  Boolean  Config5MVH  Boolean  Config5MVH  Boolean  Config5MVH  Boolean  Config5MVH  Config5MR  Config7MR  Config7MNDDE  Config7MR  Config7MI  Config7MI  Config7MI  Config7MR  Config7MR  Config7MR  Config7MR  Config7MVH  Config7MR  Config7			
instructions. Ignored if Config5.CA2 is not set)  config5MSAEn  Boolean  Override Config5.MSAEn  Override Config5.MSAEn  Override Config5.MVH (enable MTHC0 and MFHC0 instructions)  config5DEC  Boolean  Override Config5.DEC (to test Dual Endian Capability)  config5CRCP  Boolean  Override Config5.GI (enable GINV)  config5VP  Boolean  Override Config5.CRCP (CRCP Present)  config5VP  config6FTLBEn  Boolean  Override Config5.VP  config6FTLBEn  config7AR  Boolean  Override Config7.AR (Alias removed Data cache)  config7DCIDX_MODE  config7HCI  Boolean  Override Config7.HCI (Hardware Cache Initialization)  config7IAR  Boolean  Override Config7.IAR (Alias removed Instruction cache)  config7ES  Uns32  Override Config7.WII (wait IE/IXMT ignore)  config7ES  Uns32  Override Config7.BI ibit (Alternative implementation of Watch registers)  config7FPR  Boolean  Override Config7.FFR (one-half FPU clock ratio)  config7BTLM  Boolean  Override Config7.BILM bit  config7BUAD  Boolean  Override Config7.BILM bit  config7IAR. Boolean  Override Config7.BILM bit  config7IND  Boolean  Override Config7.BILM bit  config7INAD  Boolean  Override Config7.IAR bit for CPU0/VPE1			
config5MSAEn  config5MVH  Boolean  Override Config5.MSAEn  Override Config5.MYH (enable MTHC0 and MFHC0 instructions)  config5DEC  Boolean  Override Config5.DEC (to test Dual Endian Capability)  config5GI  Uns32  Override Config5.GI (enable GINV)  config5CRCP  Boolean  Override Config5.CRCP (CRCP Present)  config5VP  config5VP  Boolean  Override Config5.CRCP (CRCP Present)  config7AR  Boolean  Override Config7.AR (Alias removed Data cache)  config7DCIDX.MODE  Uns32  Override Config7.DCIDX.MODE  config7HCI  Boolean  Override Config7.HCI (Hardware Cache Initialization)  config7IAR  Boolean  Override Config7.WII (wait IE/IXMT ignore)  config7ES  Uns32  Override Config7.WII (wait IE/IXMT ignore)  override the ES field in Config7 register (Externalize sync)  config7FPR  Boolean  Override Config7.USP (one-half FPU clock ratio)  config7BTLM  Boolean  Override Config7.BTLM bit  config7BUSD  config7BTLM  Boolean  Override Config7.BTLM bit  config7INAD  Boolean  Override Config7.AR to (one-half FPU clock ratio)  config7BTLM  Boolean  Override Config7.BTLM bit  config7BTLM  Boolean  Override Config7.BTLM bit  config7INAD  Boolean  Override Config7.AR bit for CPU0/VPE0  config7IAR.CPU0.VPE1  Boolean  Override Config7.IAR bit for CPU0/VPE1	mips32Macro	Boolean	
config5MVH  Config5DEC  Boolean  Override Config5.MVH (enable MTHC0 and MFHC0 instructions)  Override Config5.DEC (to test Dual Endian Capability)  config5GI  Uns32  Override Config5.GI (enable GINV)  config5CRCP  Boolean  Override Config5.CRCP (CRCP Present)  config5VP  Config6FTLBEn  Boolean  Override Config5.VP  config6FTLBEn  Boolean  Override Config7.NR (Alias removed Data cache)  config7DCIDX.MODE  Uns32  Override Config7.DCIDX.MODE  config7HCI  Boolean  Override Config7.DCIDX.MODE  config7HCI  Boolean  Override Config7.HCI (Hardware Cache Initialization)  config7HAR  Boolean  Override Config7.HAR (Alias removed Instruction cache)  config7WII  Boolean  Override Config7.WII (wait IE/IXMT ignore)  config7ES  Uns32  Override Config7[31] bit (Alternative implementation of Watch registers)  config7BPR  Boolean  Override Config7.FPR (one-half FPU clock ratio)  config7BTLM  Boolean  Override Config7.BTLM bit  config7BS  Override Config7.BTLM bit  config7INAD  Boolean  Override Config7.BTLM bit  config7INAD  Boolean  Override Config7.IVAD bit  config7IAR.CPU0.VPE0  config7IAR.CPU0.VPE1  Boolean  Override Config7.IAR bit for CPU0/VPE1	0.5150.4.7	<u> </u>	
config5DEC  Boolean  Override Config5.DEC (to test Dual Endian Capability)  config5GI  Uns32  Override Config5.GI (enable GINV)  config5CRCP  Boolean  Override Config5.CRCP (CRCP Present)  config5VP  Boolean  Override Config5.VP  config6FTLBEn  Boolean  Override power on value of Config6.FTLBEn  config7AR  Boolean  Override Config7.AR (Alias removed Data cache)  config7DCIDX_MODE  Uns32  Override Config7.HCI (Hardware Cache Initialization)  config7HCI  Boolean  Override Config7.IAR (Alias removed Instruction cache)  config7WII  Boolean  Override Config7.WII (wait IE/IXMT ignore)  config7ES  Uns32  Override Config7.WII (wait IE/IXMT ignore)  Override Config7.II bit (Alternative implementation of Watch registers)  config7USP  Uns32  Override Config7.USP (UspRAM enable)  config7BTLM  Boolean  Override Config7.BTLM bit  config7BUNAD  Boolean  Override Config7.BusSlp bit  config7IRAC.CPU0.VPE0  Boolean  Override Config7.IAR bit for CPU0/VPE0  config7IAR.CPU0.VPE1  Boolean  Override Config7.IAR bit for CPU0/VPE1			
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config7WII  config7ES  Uns32  Override Config7.WII (wait IE/IXMT ignore)  Override the ES field in Config7 register (Externalize sync)  config7WR  Boolean  Override Config7[31] bit (Alternative implementation of Watch registers)  config7FPR  Boolean  Override Config7.FPR (one-half FPU clock ratio)  config7USP  Uns32  Override Config7.USP (USPRAM enable)  config7BTLM  config7BTLM  Boolean  Override Config7.BTLM bit  config7BusSlp  Boolean  Override Config7.BusSlp bit  config7IVAD  Boolean  Override Config7.IVAD bit  config7IRPS  Boolean  Override Config7.RPS bit  config7IAR_CPU0_VPE0  Boolean  Override Config7.IAR bit for CPU0/VPE0  config7IAR_CPU0_VPE1  Boolean  Override Config7.IAR bit for CPU0/VPE1			tion)
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config7IAR_CPU0_VPE1 Boolean Override Config7.IAR bit for CPU0/VPE1	config7USP config7BTLM config7BusSlp config7IVAD	Boolean Boolean	Override Config7.BTLM bit Override Config7.BusSlp bit Override Config7.IVAD bit
config7IAR_CPU0_VPE1  Boolean Override Config7.IAR bit for CPU0/VPE1  config7IAR_CPU0_VPE2  Boolean Override Config7_IAR bit for CPU0/VPE2	config7USP config7BTLM config7BusSlp config7IVAD config7RPS	Boolean Boolean Boolean Boolean	Override Config7.BTLM bit Override Config7.BusSlp bit Override Config7.IVAD bit Override Config7.RPS bit
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config7IAR_CPU0_VPE3	Boolean	Override Config7.IAR bit for CPU0/VPE3
config7IAR_CPU1_VPE0	Boolean	Override Config7.IAR bit for CPU1/VPE0
config7IAR_CPU1_VPE1	Boolean	Override Config7.IAR bit for CPU1/VPE1
config7IAR_CPU1_VPE2	Boolean	Override Config7.IAR bit for CPU1/VPE2
config7IAR_CPU1_VPE3	Boolean	Override Config7.IAR bit for CPU1/VPE3
config7IAR_CPU2_VPE0	Boolean	Override Config7.IAR bit for CPU2/VPE0
config7IAR_CPU2_VPE1	Boolean	Override Config7.IAR bit for CPU2/VPE1
config7IAR_CPU2_VPE2	Boolean	Override Config7.IAR bit for CPU2/VPE2
config7IAR_CPU2_VPE3	Boolean	Override Config7.IAR bit for CPU2/VPE3
config7IAR_CPU3_VPE0	Boolean	Override Config7.IAR bit for CPU3/VPE0
config7IAR_CPU3_VPE1	Boolean	Override Config7.IAR bit for CPU3/VPE1
config7IAR_CPU3_VPE2	Boolean	Override Config7.IAR bit for CPU3/VPE2
config7IAR_CPU3_VPE3	Boolean	Override Config7.IAR bit for CPU3/VPE3
config7IAR_CPU4_VPE0	Boolean	Override Config7.IAR bit for CPU4/VPE0
config7IAR_CPU4_VPE1	Boolean	Override Config7.IAR bit for CPU4/VPE1
config7IAR_CPU4_VPE2	Boolean	Override Config7.IAR bit for CPU4/VPE2
config7IAR_CPU4_VPE3	Boolean	Override Config7.IAR bit for CPU4/VPE3
config7IAR_CPU5_VPE0	Boolean	Override Config7.IAR bit for CPU5/VPE0
config7IAR_CPU5_VPE1	Boolean	Override Config7.IAR bit for CPU5/VPE1
config7IAR_CPU5_VPE2	Boolean	Override Config7.IAR bit for CPU5/VPE2
config7IAR_CPU5_VPE3	Boolean	Override Config7.IAR bit for CPU5/VPE3
config7IAR_CPU6_VPE0	Boolean	Override Config7.IAR bit for CPU6/VPE0
config7IAR_CPU6_VPE1	Boolean	Override Config7.IAR bit for CPU6/VPE1
config7IAR_CPU6_VPE2	Boolean	Override Config7.IAR bit for CPU6/VPE2
config7IAR_CPU6_VPE3	Boolean	Override Config7.IAR bit for CPU6/VPE3
config7IAR_CPU7_VPE0	Boolean	Override Config7.IAR bit for CPU7/VPE0
config7IAR_CPU7_VPE1	Boolean	Override Config7.IAR bit for CPU7/VPE1
config7IAR_CPU7_VPE2	Boolean	Override Config7.IAR bit for CPU7/VPE2
config7IAR_CPU7_VPE3	Boolean	Override Config7.IAR bit for CPU7/VPE3
config7IVAD_CPU0_VPE0	Boolean	Override Config7.IVAD bit for CPU0/VPE0
config7IVAD_CPU0_VPE1	Boolean	Override Config7.IVAD bit for CPU0/VPE1
config7IVAD_CPU0_VPE2	Boolean	Override Config7.IVAD bit for CPU0/VPE2
config7IVAD_CPU0_VPE3	Boolean	Override Config7.IVAD bit for CPU0/VPE3
config7IVAD_CPU1_VPE0	Boolean	Override Config7.IVAD bit for CPU1/VPE0
config7IVAD_CPU1_VPE1	Boolean	Override Config7.IVAD bit for CPU1/VPE1
config7IVAD_CPU1_VPE2	Boolean	Override Config7.IVAD bit for CPU1/VPE2
config7IVAD_CPU1_VPE3	Boolean	Override Config7.IVAD bit for CPU1/VPE3
config7IVAD_CPU2_VPE0	Boolean	Override Config7.IVAD bit for CPU2/VPE0
config7IVAD_CPU2_VPE1	Boolean	Override Config7.IVAD bit for CPU2/VPE1
config7IVAD_CPU2_VPE2	Boolean	Override Config7.IVAD bit for CPU2/VPE2
config7IVAD_CPU2_VPE3	Boolean	Override Config7.IVAD bit for CPU2/VPE3
config7IVAD_CPU3_VPE0	Boolean	Override Config7.IVAD bit for CPU3/VPE0
config7IVAD_CPU3_VPE1	Boolean	Override Config7.IVAD bit for CPU3/VPE1
config7IVAD_CPU3_VPE2	Boolean	Override Config7.IVAD bit for CPU3/VPE2
config7IVAD_CPU3_VPE3	Boolean	Override Config7.IVAD bit for CPU3/VPE3
config7IVAD_CPU4_VPE0	Boolean	Override Config7.IVAD bit for CPU4/VPE0
config7IVAD_CPU4_VPE1	Boolean	Override Config7.IVAD bit for CPU4/VPE1
config7IVAD_CPU4_VPE2	Boolean	Override Config7.IVAD bit for CPU4/VPE2
config7IVAD_CPU4_VPE3	Boolean	Override Config7.IVAD bit for CPU4/VPE3
config7IVAD_CPU5_VPE0	Boolean	Override Config7.IVAD bit for CPU5/VPE0
config7IVAD_CPU5_VPE1	Boolean	Override Config7.IVAD bit for CPU5/VPE1
config7IVAD_CPU5_VPE2	Boolean	Override Config7.IVAD bit for CPU5/VPE2
config7IVAD_CPU5_VPE3	Boolean	Override Config7.IVAD bit for CPU5/VPE3
config7IVAD_CPU6_VPE0	Boolean	Override Config7.IVAD bit for CPU6/VPE0
config7IVAD_CPU6_VPE1	Boolean	Override Config7.IVAD bit for CPU6/VPE1
config7IVAD_CPU6_VPE2	Boolean	Override Config7.IVAD bit for CPU6/VPE2
		1 .

	Daalaaa	Oil- C67 IVAD 1:4 f CDUC/VDE2
config7IVAD_CPU6_VPE3	Boolean	Override Config7.IVAD bit for CPU6/VPE3
config7IVAD_CPU7_VPE0	Boolean	Override Config7.IVAD bit for CPU7/VPE0
config7IVAD_CPU7_VPE1	Boolean	Override Config7.IVAD bit for CPU7/VPE1
config7IVAD_CPU7_VPE2	Boolean	Override Config7.IVAD bit for CPU7/VPE2
config7IVAD_CPU7_VPE3	Boolean	Override Config7.IVAD bit for CPU7/VPE3
config7RPS_CPU0_VPE0	Boolean	Override Config7.RPS bit for CPU0/VPE0
config7RPS_CPU0_VPE1	Boolean	Override Config7.RPS bit for CPU0/VPE1
config7RPS_CPU0_VPE2	Boolean	Override Config7.RPS bit for CPU0/VPE2
config7RPS_CPU0_VPE3	Boolean	Override Config7.RPS bit for CPU0/VPE3
config7RPS_CPU1_VPE0	Boolean	Override Config7.RPS bit for CPU1/VPE0
config7RPS_CPU1_VPE1	Boolean	Override Config7.RPS bit for CPU1/VPE1
config7RPS_CPU1_VPE2	Boolean	Override Config7.RPS bit for CPU1/VPE2
config7RPS_CPU1_VPE3	Boolean	Override Config7.RPS bit for CPU1/VPE3
config7RPS_CPU2_VPE0	Boolean	Override Config7.RPS bit for CPU2/VPE0
config7RPS_CPU2_VPE1	Boolean	Override Config7.RPS bit for CPU2/VPE1
config7RPS_CPU2_VPE2	Boolean	Override Config7.RPS bit for CPU2/VPE2
config7RPS_CPU2_VPE3	Boolean	Override Config7.RPS bit for CPU2/VPE3
config7RPS_CPU3_VPE0	Boolean	Override Config7.RPS bit for CPU3/VPE0
config7RPS_CPU3_VPE1	Boolean	Override Config7.RPS bit for CPU3/VPE1
config7RPS_CPU3_VPE2	Boolean	Override Config7.RPS bit for CPU3/VPE2
config7RPS_CPU3_VPE3	Boolean	Override Config7.RPS bit for CPU3/VPE3
config7RPS_CPU4_VPE0	Boolean	Override Config7.RPS bit for CPU4/VPE0
config7RPS_CPU4_VPE1	Boolean	Override Config7.RPS bit for CPU4/VPE1
config7RPS_CPU4_VPE2	Boolean	Override Config7.RPS bit for CPU4/VPE2
config7RPS_CPU4_VPE3	Boolean	Override Config7.RPS bit for CPU4/VPE3
config7RPS_CPU5_VPE0	Boolean	Override Config7.RPS bit for CPU5/VPE0
config7RPS_CPU5_VPE1	Boolean	Override Config7.RPS bit for CPU5/VPE1
config7RPS_CPU5_VPE2	Boolean	Override Config7.RPS bit for CPU5/VPE2
config7RPS_CPU5_VPE3	Boolean	Override Config7.RPS bit for CPU5/VPE3
config7RPS_CPU6_VPE0	Boolean	Override Config7.RPS bit for CPU6/VPE0
config7RPS_CPU6_VPE1	Boolean	Override Config7.RPS bit for CPU6/VPE1
config7RPS_CPU6_VPE2	Boolean	Override Config7.RPS bit for CPU6/VPE2
config7RPS_CPU6_VPE3	Boolean	Override Config7.RPS bit for CPU6/VPE3
config7RPS_CPU7_VPE0	Boolean	Override Config7.RPS bit for CPU7/VPE0
config7RPS_CPU7_VPE1	Boolean	Override Config7.RPS bit for CPU7/VPE1
config7RPS_CPU7_VPE2	Boolean	Override Config7.RPS bit for CPU7/VPE2
config7RPS_CPU7_VPE3	Boolean	Override Config7.RPS bit for CPU7/VPE3
statusFR	Boolean	Override coming that is the of Ci of Vi Es  Override power on value in Status.FR (Floating
Statusi It	Doolean	point register mode)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant
ICSI AD 52006	Doolean	with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings
ICSTNAIN2006	Doolean	match IEEE 754-2008 recommendation)
MD	II20	
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
srsconf0SRS1	Uns32	Override the SRS1 field in SRSConf0 register
srsconf0SRS2	Uns32	Override the SRS2 field in SRSConf0 register
srsconf0SRS3	Uns32	Override the SRS3 field in SRSConf0 register
wiredLimit	Uns32	Override Limit field of the Wired register
wiredLimitBits	Uns32	Override width of Limit field of the Wired register
wiredWiredBits	Uns32	Override width of Wired field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
parityEnable	Uns32	Specify error detection support: 0 - none; 1 - parity; 2 - ECC
useMpTb	Boolean	Override Use of multi-processor test bench
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use
		GCR_Cx_RESET_BASE on CMP processors)

UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the cor-
		responding BEV address bits
l1BufferCache	Boolean	L1 Buffer Cache
GCU_EX	Boolean	CMP system only: GCR custom block present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable
		within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable
		within cluster
PERFCNT_ROUTABLE	Boolean	CMP system only: performance counter interrupt
		routable within cluster
FDC_ROUTABLE	Boolean	CMP system only: fast debug channel interrupt
		routable within cluster
GCR_PCORES	Uns32	CMP system only: override
0.0202	0 0 -	GCR_CONFIG.PCORES (number of cores-1)
GCR_ADDR_REGIONS	Uns32	CMP system only: override
	011002	GCR_CONFIG.ADDR_REGIONS (number of
		MMIO address regions)
GCR_NUMAUX	Uns32	CMP system only: override
	011302	GCR_CONFIG.NUMAUX (number of auxil-
		iary memory ports)
GCR_BASE	Uns64	CMP system only: override
GCR_DASE	011804	GCR_BASE.GCR_BASE (default GCR regis-
		ter address)
GCR_MINOR_REV	Uns32	/
GUR_WIINUR_REV	Ulis52	CMP system only: override GCR_REV.MINOR_REV
CCD MAJOR REIL	TT 00	
GCR_MAJOR_REV	Uns32	CMP system only: override
CCD CACHE MINOD DEV	TT 90	GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override
CCD CACHE MAJOR REV	TT 00	GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override
CCD to ACCOC	TT 90	GCR_CACHE_REV.MAJOR_REV
GCR_L2_ASSOC	Uns32	CMP system only: override
COD to OPE CITE	TT 00	GCR_L2_CONFIG.ASSOC
GCR_L2_SET_SIZE	Uns32	CMP system only: override
GGD GVG GGAVERGG ALLAY AVD VVVD GVV	** **	GCR_L2_CONFIG.SET_SIZE
GCR_SYS_CONFIG2_MAX_VP_WIDTH	Uns32	CMP system only: override
		GCR_SYS_CONFIG2.MAX_VP_WIDTH
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override
		GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override
		GCR_IOCU1_REV.MAJOR_REV
GCR_BEV_BASE	Uns32	CMP system only: override GCR_BEV_BASE
GCR_KX_BASE_MODE	Boolean	CMP system only: override BEV_BASE_MODE &
		RESET_BASE_MODE
GCR_MMIO_REQ_LIMIT	Uns32	CMP system only: override
		GCR_MMIO_REQ_LIMIT.MMIO_REQ_LIMIT
		value
GCR_MMIO0_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO0_BOTTOM register value
GCR_MMIO0_TOP_ADDR	Uns32	CMP system only: override
-	•	GCR_MMIO0_TOP.TOP_ADDR value
	TT 04	CMP system only: override
GCR_MMIO1_BOTTOM	Uns64	CMF System only: Override
GCR_MMIO1_BOTTOM	Uns64	į
GCR_MMIO1_BOTTOM GCR_MMIO1_TOP_ADDR	Uns64 Uns32	GCR_MMIO1_BOTTOM register value  CMP system only: override

GCR_MMIO2_BOTTOM	Uns64	CMP system only: override GCR_MMIO2_BOTTOM register value
GCR_MMIO2_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO2_TOP.TOP_ADDR value
GCR_MMIO3_BOTTOM	Uns64	CMP system only: override GCR_MMIO3_BOTTOM register value
GCR_MMIO3_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO3_TOP.TOP_ADDR value
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override GIC_SH_DBG_CONFIG.NUM_TEAMS
GIC_TRIG_RESET	Uns32	CMP system only: Zero value of GIC_SH_TRIG_[31_0, 63_32]
GIC-PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
gicVirtualVPNum_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
gicVirtualVPNum_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
gicVirtualVPNum_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
gicVirtualVPNum_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3

gicVirtualVPNum_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
gicVirtualVPNum_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
gicVirtualVPNum_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
gicVirtualVPNum_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
gicVirtualVPNum_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
gicVirtualVPNum_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
gicVirtualVPNum_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
gicVirtualVPNum_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
gicVirtualVPNum_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
gicVirtualVPNum_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
gicVirtualVPNum_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
gicVirtualVPNum_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
gicVirtualVPNum_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
gicVirtualVPNum_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
gicVirtualVPNum_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
gicVirtualVPNum_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
gicVirtualVPNum_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
gicVirtualVPNum_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
gicVirtualVPNum_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
gicVirtualVPNum_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
gicVirtualVPNum_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
gicVirtualVPNum_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
gicVirtualVPNum_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
gicVirtualVPNum_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
gicVirtualVPNum_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
gicVirtualVPNum_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
gicVirtualVPNum_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
$gicVirtualVPNum\_CPU7\_VP3$	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3

COD CO DEGET DAGE	11 00	CALD I GOD OF DECEMBER 1
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GCR_C1_RESET_BASE	II 20	core 0  CMP system only: GCR_CL_RESET_BASE for
GCR_CT_RESET_BASE	Uns32	core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GCR_C2_RESET_DASE	Ulisaz	core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GOIL-COLILEBET -DASE	011802	core 3
GCR_C4_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GOILE THE BET BRIDE	011302	core 4
GCR_C5_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
	0.550	core 5
GCR_C6_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
		core 6
GCR_C7_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
		core 7
GCR_C8_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
		core 8
GCR_C9_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
		core 9
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
CCD Co DECEMBER DATE	77 00	for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
CCD C4 PEGET EVE DAGE	11 00	for core 3
GCR_C4_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GCR_C5_RESET_EXT_BASE	Uns32	for core 4  CMP system only: GCR_CL_RESET_EXT_BASE
GCR_CS_RESET_EXT_DASE	Ulisaz	for core 5
GCR_C6_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GOIL-CO-I(ESET-EXT-DASE	011852	for core 6
GCR_C7_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
	011502	for core 7
GCR_C8_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
0.0100000000000000000000000000000000000	0.550	for core 8
GCR_C9_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 9
CPC_C0_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 0
CPC_C1_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 1
CPC_C2_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 2
CPC_C3_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 3
CPC_C4_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 4
CPC_C5_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 5
CPC_C6_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 6
CPC_C7_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 7
CPC_C8_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 8
CPC_C9_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 9
EIC_OPTION	Uns32	Override the external interrupt controller
		EIC_OPTION
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register

guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest II TI held in IntCtl register  Override the Guest IPFDC field in IntCtl register
guestintetIIPPCI	Uns32	Override the Guest IPFDC field in IntCtl register  Override the Guest IPPCI field in IntCtl register
guestintctIFFCI guestintctIPTI_CPU0_VP0	Uns32	
		Override the IPTI field in IntCtl register for CPU0/VP0
guestintctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
guestintctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
guestintctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
guestintctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
guestintctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
guestintctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
guestintctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
guestintctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
guestintctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
guestintctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
guestintctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
guestintctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
guestintctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
guestintctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
guestintctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
guestintctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
guestintctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
guestintctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
guestintctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
guestintctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
guestintctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1

guestintctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
guestintctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
guestintctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
guestintctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
guestintctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
guestintctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
guestintctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
guestintctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
guestintctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
guestintctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
guestintctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
guestintctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
guestintctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
guestintctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
guestintctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
guestintctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
guestintctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
guestintctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
guestintctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
guestintctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
guestintctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
guestintctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
guestintctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
guestintctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
guestintctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
guestintctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
guestintctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
guestintctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1

$guest intctlIPFDC\_CPU4\_VP2$	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
guestintctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
guestintctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
guestintctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
guestintctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
guestintctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
guestintctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
guestintctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
$guestintctlIPFDC\_CPU6\_VP2$	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
guestintctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
guestintctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
guestintctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
guestintctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
guestintctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
guestintctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
guestintctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
guestintctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
guestintctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
guestintctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
guestintctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
$guest intct IIPPCI\_CPU1\_VP2$	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
guestintctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
guestintctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
guestintctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
guestintctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
guestintctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
guestintctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
guestintctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1

guestintctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
guestintctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
guestintctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
guestintctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
guestintctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
guestintctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
guestintctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
guestintctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
guestintctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
guestintctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
guestintctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
guestintctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
guestintctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
guestintctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
guestintctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
guestintctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
guestintctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
guestintctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2( <ispram bytes="" in="" size="">) - 11)</ispram>
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior
INT WHILL IIII	During	to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2( <dspram bytes="" in="" size="">) - 11)</dspram>
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag (used to enable the DSPRAM region prior to reset)
DSPRAM_PRESENT	Boolean	DSPRAM is present with SAAR
USPRAM_SIZE	Uns32	Encoded size of the USPRAM region (log2( <uspram bytes="" in="" size="">) - 11)</uspram>
USPRAM_BASE	Uns64	Starting physical address of the USPRAM region
USPRAM_ENABLE	Boolean	Set the enable bit of the USPRAM region's tag
		(used to enable the USPRAM region prior to reset)

String	Load a MIPS hex file into the USPRAM region
	prior to reset
Enumeration	Select misaligned data access exception signaling: never, checkCCA or always (never, checkCCA or always)
Boolean	Commit TLBWI/TLBRI on ECC; in MIPS_DV_MODE only
	Enumeration

Table 8.1: Parameters that can be set in: CMP

## 8.1 Parameter values

These are the current parameter values.

Name	Value
(Others)	
variant	I6400
endian	none
cacheenable	default
cachedebug	0
cacheextbiuinfo	0x0
mipsHexFile	
IMPERAS_MIPS_AVP_OPCODES	F
cacheIndexBypassTLB	F
MIPS_TRACE	F
gprNames	F
supervisorMode	F
busErrors	Т
fixedMMU	F
fixedDbgRegSize	F
removeDSP	F
removeCMP	F
removeFP	F
removeFTLB	F
isISA	F
hiddenTLBentries	F
perfCounters	0
ITCNumEntries	0
ITCNumFIFO	0
ITCFIFODepth	0
ITCEmptyOnReset	F
MTFPU	0
supportDenormals	F
VPE0MaxTC	0
VPE1MaxTC	0
segBits	0
mpuRegions	0
mpuType	0

mpuEnable	F
mpuSegment0	0
mpuSegment1	0
mpuSegment2	0
mpuSegment3	0
mpuSegment4	0
mpuSegment5	0
mpuSegment6	0
mpuSegment7	0
mpuSegment8	0
mpuSegment9	0
mpuSegment10	0
	0
mpuSegment11	0
mpuSegment12	
mpuSegment13	0
mpuSegment14	0
mpuSegment15	0
mvpconf0vpe	0
tcDisable	0
vpeDisable	0
mvpconf0tc	0
mvpconf0pcp	F
mvpconf0tcp	F
mvpconf1c1f	F
mvpcontrolPolicyMode	F
hasFDC	0
licenseWarningDays	15
MIPS_UHI	F
mipsUhiArgs	
mipsUhiJail	
MIPS_DV_MODE	F
MIPS_MAGIC_OPCODES	F
enableTrickbox	F
fpuexcdisable	F
TRU_PRESENT	F
ucLLwordsLocked	0
FUSA	F
CPC_FAULT_SUPPORTED	0
CPC_FAULT_ENABLE	0
cop2Bits	32
cop2FileName	
udiConfig	0
udiFileName	
vectoredinterrupt	F
externalinterrupt	F

config3VEIC_VPE0	F
config3VEIC_VPE1	F
config3VEIC_VPE2	F
config3VEIC_VPE3	F
rootFixedMMU	F
rootMMUSizeM1	0
srsctlHSS	0
firPS	0
firHas2008	0
usePreciseFpu	0
simulateLite	NONE
pridCompanyOptions	0
pridRevision	0
globalClusterNum	0
intctlIPTI	0
intctlIPFDC	0
intctlIPPCI	0
numWatch	0
maxVP	0
numVP	0
numVPtoStart	0
sharedTLBindex	0
xconfigSpecified	F
intctlIPTI_CPU0_VP0	0
intctlIPTI_CPU0_VP1	0
intctlIPTI_CPU0_VP2	0
intctlIPTI_CPU0_VP3	0
intctlIPTI_CPU1_VP0	0
intctlIPTI_CPU1_VP1	0
intctlIPTI_CPU1_VP2	0
intctlIPTI_CPU1_VP3	0
intctlIPTI_CPU2_VP0	0
intctlIPTI_CPU2_VP1	0
intctllPTI_CPU2_VP2	0
intctllPTI_CPU2_VP3	0
intetlIPTI_CPU3_VP0	0
intctllPTI_CPU3_VP1	0
intctllPTI_CPU3_VP2	0
intetllPTI_CPU3_VP3	0
intetlIPTI_CPU4_VP0	0
intetlIPTI_CPU4_VP1	0
intctllPTI_CPU4_VP2	0
intctllPTI_CPU4_VP3	0
intctllPTI_CPU5_VP0	0
intctllPTI_CPU5_VP1	0
111000111 11_01 00_V1 1	U

intctlIPTI_CPU5_VP2	0
intctlIPTI_CPU5_VP3	0
intctlIPTI_CPU6_VP0	0
intctlIPTI_CPU6_VP1	0
intctlIPTI_CPU6_VP2	0
intctlIPTI_CPU6_VP3	0
intctlIPTI_CPU7_VP0	0
intctlIPTI_CPU7_VP1	0
intctlIPTI_CPU7_VP2	0
intctlIPTI_CPU7_VP3	0
intctlIPFDC_CPU0_VP0	0
intctlIPFDC_CPU0_VP1	0
intctlIPFDC_CPU0_VP2	0
intctlIPFDC_CPU0_VP3	0
intctlIPFDC_CPU1_VP0	0
intctlIPFDC_CPU1_VP1	0
intctlIPFDC_CPU1_VP2	0
intctlIPFDC_CPU1_VP3	0
intctlIPFDC_CPU2_VP0	0
intctlIPFDC_CPU2_VP1	0
intctlIPFDC_CPU2_VP2	0
intctlIPFDC_CPU2_VP3	0
intctlIPFDC_CPU3_VP0	0
intctlIPFDC_CPU3_VP1	0
intctlIPFDC_CPU3_VP2	0
intctlIPFDC_CPU3_VP3	0
intctlIPFDC_CPU4_VP0	0
intctlIPFDC_CPU4_VP1	0
intctlIPFDC_CPU4_VP2	0
intctlIPFDC_CPU4_VP3	0
intctlIPFDC_CPU5_VP0	0
intctlIPFDC_CPU5_VP1	0
intctlIPFDC_CPU5_VP2	0
intctlIPFDC_CPU5_VP3	0
intctlIPFDC_CPU6_VP0	0
intctlIPFDC_CPU6_VP1	0
intctlIPFDC_CPU6_VP2	0
intctlIPFDC_CPU6_VP3	0
intctlIPFDC_CPU7_VP0	0
intctlIPFDC_CPU7_VP1	0
intctlIPFDC_CPU7_VP2	0
intctlIPFDC_CPU7_VP3	0
intctlIPPCI_CPU0_VP0	0
intctlIPPCI_CPU0_VP1	0
intctlIPPCI_CPU0_VP2	0
	<del></del>

intetlIPPCI_CPU0_VP3 intetlIPPCI_CPU1_VP0 intetlIPPCI_CPU1_VP1 intetlIPPCI_CPU1_VP2 intetlIPPCI_CPU1_VP3 intetlIPPCI_CPU2_VP0 intetlIPPCI_CPU2_VP0 intetlIPPCI_CPU2_VP1 intetlIPPCI_CPU2_VP2 intetlIPPCI_CPU2_VP3 intetlIPPCI_CPU3_VP0 intetlIPPCI_CPU3_VP0 intetlIPPCI_CPU3_VP1 intetlIPPCI_CPU3_VP1 intetlIPPCI_CPU3_VP2 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU4_VP0 intetlIPPCI_CPU4_VP0 intetlIPPCI_CPU4_VP1 intetlIPPCI_CPU4_VP2 intetlIPPCI_CPU4_VP3 intetlIPPCI_CPU5_VP0 intetlIPPCI_CPU5_VP0 intetlIPPCI_CPU5_VP1 intetlIPPCI_CPU5_VP3 intetlIPPCI_CPU5_VP3 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP1 intetlIPPCI_CPU6_VP1 intetlIPPCI_CPU6_VP2 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP1 intetlIPPCI_CPU7_VP2 intetlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA segcfg3PA segcfg3PA segcfg3PA segcfg3PA segcfg5PA
intctIIPPCI_CPU1_VP1 intctIIPPCI_CPU1_VP3 intctIIPPCI_CPU1_VP3 intctIIPPCI_CPU2_VP0 intctIIPPCI_CPU2_VP0 intctIIPPCI_CPU2_VP1 intctIIPPCI_CPU2_VP2 intctIIPPCI_CPU2_VP3 intctIIPPCI_CPU3_VP0 intctIIPPCI_CPU3_VP1 intctIIPPCI_CPU3_VP1 intctIIPPCI_CPU3_VP2 intctIIPPCI_CPU3_VP3 intctIIPPCI_CPU3_VP3 intctIIPPCI_CPU4_VP0 intctIIPPCI_CPU4_VP0 intctIIPPCI_CPU4_VP1 intctIIPPCI_CPU4_VP3 intctIIPPCI_CPU4_VP3 intctIIPPCI_CPU4_VP3 intctIIPPCI_CPU5_VP0 intctIIPPCI_CPU5_VP0 intctIIPPCI_CPU5_VP1 intctIIPPCI_CPU5_VP2 intctIIPPCI_CPU6_VP2 intctIIPPCI_CPU6_VP0 intctIIPPCI_CPU6_VP1 intctIIPPCI_CPU6_VP2 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU7_VP0 intctIIPPCI_CPU7_VP0 intctIIPPCI_CPU7_VP1 ontctIIPPCI_CPU7_VP3 segcfg0PA segcfg1PA segcfg2PA segcfg3PA segcfg3PA segcfg3PA segcfg3PA segcfg3PA
intctIIPPCI_CPU1_VP2 intctIIPPCI_CPU1_VP3 intctIIPPCI_CPU2_VP0 intctIIPPCI_CPU2_VP1 intctIIPPCI_CPU2_VP1 intctIIPPCI_CPU2_VP2 intctIIPPCI_CPU2_VP3 intctIIPPCI_CPU3_VP0 intctIIPPCI_CPU3_VP1 intctIIPPCI_CPU3_VP2 intctIIPPCI_CPU3_VP3 intctIIPPCI_CPU3_VP3 intctIIPPCI_CPU3_VP3 intctIIPPCI_CPU4_VP0 intctIIPPCI_CPU4_VP0 intctIIPPCI_CPU4_VP1 intctIIPPCI_CPU4_VP2 intctIIPPCI_CPU4_VP3 intctIIPPCI_CPU5_VP0 intctIIPPCI_CPU5_VP0 intctIIPPCI_CPU5_VP1 intctIIPPCI_CPU5_VP2 intctIIPPCI_CPU5_VP3 intctIIPPCI_CPU6_VP0 intctIIPPCI_CPU6_VP0 intctIIPPCI_CPU6_VP0 intctIIPPCI_CPU6_VP1 intctIIPPCI_CPU6_VP2 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU6_VP3 intctIIPPCI_CPU7_VP0 intctIIPPCI_CPU7_VP0 intctIIPPCI_CPU7_VP1 intctIIPPCI_CPU7_VP2 intctIIPPCI_CPU7_VP3 segcfg0PA segcfg1PA segcfg3PA segcfg3PA segcfg3PA segcfg3PA segcfg3PA
intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA segcfg3PA segcfg3PA segcfg3PA segcfg4PA
intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA segcfg1PA segcfg3PA segcfg3PA segcfg4PA
intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA segcfg1PA segcfg3PA segcfg3PA segcfg3PA segcfg4PA
intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA segcfg1PA segcfg3PA segcfg3PA segcfg3PA segcfg4PA
intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA segcfg2PA segcfg3PA segcfg3PA segcfg3PA segcfg4PA
intetlIPPCI_CPU3_VP1 intetlIPPCI_CPU3_VP2 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU4_VP0 intetlIPPCI_CPU4_VP1 intetlIPPCI_CPU4_VP2 intetlIPPCI_CPU4_VP3 intetlIPPCI_CPU5_VP0 intetlIPPCI_CPU5_VP0 intetlIPPCI_CPU5_VP1 intetlIPPCI_CPU5_VP2 intetlIPPCI_CPU5_VP3 intetlIPPCI_CPU5_VP3 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP1 intetlIPPCI_CPU6_VP2 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP1 intetlIPPCI_CPU7_VP2 intetlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA segcfg2PA segcfg3PA segcfg3PA segcfg4PA
intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg3PA         0           segcfg4PA         0           segcfg4PA         0
intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg3PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
segcfg2PA         0           segcfg3PA         0           segcfg4PA         0
segcfg3PA 0 segcfg4PA 0
segcfg4PA 0
segcfg5PA 0
segcfg0AM 0
segcfg1AM 0
segcfg2AM 0
segcfg3AM 0
segcfg4AM 0
segcfg5AM 0
segcfg0EU 0
segcfg1EU 0
segcfg2EU 0
segcfg3EU 0

segcfg5EU         0           segcfg0C         0           segcfg1C         0           segcfg2C         0           segcfg3C         0           segcfg5C         0           cdmmSize         0           configAR         0           configBM         0           configBP         F           configK0         0           configKU         0           configMDU         F           configMDU         F           configBSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1B         0           config1IL         0           config1IM         0           config1IM         0           config1IM         0           config1IM         0           config1IN         0           config1IN         0           config1IMUSizeM1         0           config1MMUSizeM1         0           config1VR         F           config2S         0           config		
segcfg1C         0           segcfg2C         0           segcfg3C         0           segcfg4C         0           segcfg5C         0           cdmmSize         0           configAR         0           configBM         0           configBP         F           configK0         0           configKU         0           configK23         0           configMDU         F           configMM         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DB         0           config1DB         0           config1IA         0           config1IB         0           config1IMMUSizeM1         0           config1MMUSizeM1.VPE1         0           config1WR         F           config1V2         F           config2SU         0           config2SL         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CDMM         F	segcfg4EU	0
segcfg1C         0           segcfg2C         0           segcfg3C         0           segcfg5C         0           configAR         0           configBM         0           configBN         0           configBNP         F           configK0         0           configKU         0           configMDU         F           configMM         F           configBP         F           configBP         F           configBP         F           configBD         F           configBD         F           config1DA         0           config1DA         0           config1DS         0           config1IA         0           config1IB         0           config1IMOUSizeM1         0           config1MMUSizeM1.VPE1         0           config1PC         F           config2SV         0           config2SS         0           config3BI         F           config3BI         F           config3BD         F           config3CDMM         F           c		
segcfg2C         0           segcfg3C         0           segcfg4C         0           configAR         0           configBM         0           configBN         0           configBSP         F           configK0         0           configKU         0           configMDU         F           configMM         F           configBBP         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1DS         0           config1IA         0           config1IB         0           config1IMOUSizeM1         0           config1MMUSizeM1-VPE1         0           config1WR         F           config1VR         F           config2SV         0           config2SS         0           config3BI         F           config3BP         F           config3CDMM         F           config3CDMM         F		
segcfg3C         0           segcfg4C         0           configAR         0           configBM         0           configBM         0           configBSP         F           configK0         0           configKU         0           configMDU         F           configMM         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1DS         0           config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1-VPE1         0           config1WR         F           config1PC         F           config2SV         0           config2SV         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CDMM         F	0 0	
segcfg4C         0           segcfg5C         0           configAR         0           configBM         0           configBSP         F           configISP         F           configK0         0           configKU         0           configMDU         F           configMM         F           configBSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1DS         0           config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1-VPE1         0           config1PC         F           config2SV         0           config2SV         0           config2SA         0           config3BP         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	0 0	
segcfg5C         0           cdmmSize         0           configAR         0           configBM         0           configBSP         F           configK0         0           configKU         0           configMDU         F           configMM         F           configMT         0           configBCP         F           MIPS16eASE         F           config1DA         0           config1DA         0           config1DS         0           config1B         0           config1IA         0           config1IB         0           config1MMUSizeM1         0           config1MMUSizeM1.VPE1         0           config1WR         F           config1VR         F           config2SV         0           config2SS         0           config2SA         0           config3BP         F           config3CDMM         F           config3CTXTC         F		
cdmmSize         0           configAR         0           configBM         0           configBSP         F           configK0         0           configKU         0           configK23         0           configMDU         F           configMM         F           configMT         0           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1IA         0           config1IA         0           config1IL         0           config1MMUSizeM1         0           config1MMUSizeM1-VPE1         0           config1MMUSizeM1-VPE3         0           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F		
configBM         0           configDSP         F           configISP         F           configK0         0           configKU         0           configK23         0           configMDU         F           configMM         F           configMT         0           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1IA         0           config1II         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MWR         F           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F		
configBM         0           configDSP         F           configISP         F           configK0         0           configKU         0           configK23         0           configMDU         F           configMM         F           configMM         F           configMT         0           configBSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DA         0           config1DS         0           config1DS         0           config1EP         F           config1IA         0           config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1WR         F           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F		
configDSP         F           configISP         F           configK0         0           configKU         0           configK23         0           configMDU         F           configMM         F           configMT         0           configBSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DA         0           config1DS         0           config1B         0           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1WR         F           config1PC         F           config2SU         0           config2SL         0           config2SA         0           config3BP         F           config3CDMM         F           config3CDMM         F		
configISP         F           configK0         0           configKU         0           configK23         0           configMDU         F           configMM         F           configMT         0           configBSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1DS         0           config1IA         0           config1IL         0           config1IN         0           config1MMUSizeM1         0           config1MMUSizeM1-VPE1         0           config1WR         F           config1PC         F           config1PC         F           config2SU         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F		
configK0         0           configK23         0           configMDU         F           configMM         F           configMT         0           configBB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1PC         F           config1PC         F           config2SU         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F		
configKU         0           configMDU         F           configMM         F           configMT         0           configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1DS         0           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1 VPE1         0           config1MMUSizeM1-VPE3         0           config1VR         F           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F		F
configMDU         F           configMM         F           configMT         0           configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DB         0           config1DS         0           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1-VPE1         0           config1MMUSizeM1-VPE3         0           config1VR         F           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	_	0
configMDU         F           configMM         F           configMT         0           configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1IA         0           config1IL         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1VR         F           config1VR         F           config1C2         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	configKU	0
configMM         F           configMT         0           configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IB         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE3         0           config1VR         F           config1C2         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	configK23	0
configMT         0           configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE3         0           config1PC         F           config1PC         F           config2SU         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	configMDU	F
configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IB         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	configMM	F
configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IL         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SL         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	configMT	0
MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE3         0           config1VR         F           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	configSB	F
config1DA         0           config1DS         0           config1EP         F           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CTXTC         F	configBCP	F
config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	MIPS16eASE	F
config1DS         0           config1EP         F           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1VR         F           config1PC         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F	config1DA	0
config1EP         F           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SL         0           config2SA         0           config3BI         F           config3CDMM         F           config3CTXTC         F	config1DL	0
config1IA         0           config1IIL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F	config1DS	0
config1IL         0           config1IS         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F	config1EP	F
config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1VR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F	config1IA	0
config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1VR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F	config1IL	0
config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F	config1IS	0
config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1MMUSizeM1	0
config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1MMUSizeM1_VPE1	0
config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config2SA         0           config3BI         F           config3CDMM         F           config3CTXTC         F	config1MMUSizeM1_VPE2	0
config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	$config1MMUSizeM1\_VPE3$	0
config1C2         F           config2SU         0           config2SS         0           config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1WR	F
config2SU         0           config2SS         0           config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1PC	F
config2SS         0           config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1C2	F
config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config2SU	0
config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F		0
config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config2SL	0
config3BP F config3CDMM F config3CTXTC F		0
config3CDMM F config3CTXTC F		F
config3CTXTC F	config3BP	F
9		
config3DSPP F		
	config3DSPP	F

config3DSP2P	F
config3IPLW	0
config3ISA	0
config3ISAOnExc	F
config3ITL	F
config3LPA	F
config3MCU	F
config3MMAR	0
config3RXI	F
config3SC	F
config3ULRI	F
config3VZ	F
config3MSAP	F
config3CMGCR	F
config3SP	F
config3TL	0
config3PW	F
config4AE	F
config4IE	0
config4MMUConfig	0
config4MMUExtDef	0
config4VTLBSizeExt	0
config4KScrExist	0
config5EVA	F
config5LLB	F
config5MRP	F
config5NFExists	F
mips32Macro	F
config5MSAEn	F
config5MVH	F
config5DEC	F
config5GI	0
config5CRCP	F
config5VP	F
config6FTLBEn	F
config7AR	F
config7DCIDX_MODE	0
config7HCI	F
config7IAR	F
config7WII	F
config7ES	0
config7WR	F
	F
config7FPR	
config7USP	0 F
config7BTLM	r

config7BusSlp	F
config7IVAD	F
config7RPS	F
config7IAR_CPU0_VPE0	F
config7IAR_CPU0_VPE1	F
config7IAR_CPU0_VPE2	F
config7IAR_CPU0_VPE3	F
config7IAR_CPU1_VPE0	F
config7IAR_CPU1_VPE1	F
config7IAR_CPU1_VPE2	F
config7IAR_CPU1_VPE3	F
config7IAR_CPU2_VPE0	F
config7IAR_CPU2_VPE1	F
config7IAR_CPU2_VPE2	F
config7IAR_CPU2_VPE3	F
config7IAR_CPU3_VPE0	F
config7IAR_CPU3_VPE1	F
config7IAR_CPU3_VPE2	F
config7IAR_CPU3_VPE3	F
config7IAR_CPU4_VPE0	F
config7IAR_CPU4_VPE1	F
config7IAR_CPU4_VPE2	F
config7IAR_CPU4_VPE3	F
config7IAR_CPU5_VPE0	F
config7IAR_CPU5_VPE1	F
config7IAR_CPU5_VPE2	F
config7IAR_CPU5_VPE3	F
config7IAR_CPU6_VPE0	F
config7IAR_CPU6_VPE1	F
config7IAR_CPU6_VPE2	F
config7IAR_CPU6_VPE3	F
config7IAR_CPU7_VPE0	F
config7IAR_CPU7_VPE1	F
config7IAR_CPU7_VPE2	F
config7IAR_CPU7_VPE3	F
config7IVAD_CPU0_VPE0	F
config7IVAD_CPU0_VPE1	F
config7IVAD_CPU0_VPE2	F
config7IVAD_CPU0_VPE3	F
config7IVAD_CPU1_VPE0	F
config7IVAD_CPU1_VPE1	F
config7IVAD_CPU1_VPE2	F
config7IVAD_CPU1_VPE3	F
config7IVAD_CPU2_VPE0	F F
config7IVAD_CPU2_VPE1	r

config7IVAD_CPU2_VPE2	F
config7IVAD_CPU2_VPE3	F
config7IVAD_CPU3_VPE0	F
config7IVAD_CPU3_VPE1	F
config7IVAD_CPU3_VPE2	F
config7IVAD_CPU3_VPE3	F
config7IVAD_CPU4_VPE0	F
config7IVAD_CPU4_VPE1	F
config7IVAD_CPU4_VPE2	F
config7IVAD_CPU4_VPE3	F
config7IVAD_CPU5_VPE0	F
config7IVAD_CPU5_VPE1	F
config7IVAD_CPU5_VPE2	F
config7IVAD_CPU5_VPE3	F
config7IVAD_CPU6_VPE0	F
config7IVAD_CPU6_VPE1	F
config7IVAD_CPU6_VPE2	F
config7IVAD_CPU6_VPE3	F
config7IVAD_CPU7_VPE0	F
config7IVAD_CPU7_VPE1	F
config7IVAD_CPU7_VPE2	F
config7IVAD_CPU7_VPE3	F
config7RPS_CPU0_VPE0	F
config7RPS_CPU0_VPE1	F
config7RPS_CPU0_VPE2	F
config7RPS_CPU0_VPE3	F
config7RPS_CPU1_VPE0	F
config7RPS_CPU1_VPE1	F
config7RPS_CPU1_VPE2	F
config7RPS_CPU1_VPE3	F
config7RPS_CPU2_VPE0	F
config7RPS_CPU2_VPE1	F
config7RPS_CPU2_VPE2	F
config7RPS_CPU2_VPE3	F
config7RPS_CPU3_VPE0	F
config7RPS_CPU3_VPE1	F
config7RPS_CPU3_VPE2	F
config7RPS_CPU3_VPE3	F
config7RPS_CPU4_VPE0	F
config7RPS_CPU4_VPE1	F
${\rm config7RPS\_CPU4\_VPE2}$	F
config7RPS_CPU4_VPE3	F
config7RPS_CPU5_VPE0	F
config7RPS_CPU5_VPE1	F
config7RPS_CPU5_VPE2	F

config7RPS_CPU5_VPE3	F
config7RPS_CPU6_VPE0	F
config7RPS_CPU6_VPE1	F
config7RPS_CPU6_VPE2	F
config7RPS_CPU6_VPE3	F
config7RPS_CPU7_VPE0	F
config7RPS_CPU7_VPE1	F
config7RPS_CPU7_VPE2	F
config7RPS_CPU7_VPE3	F
statusFR	F
fcsrABS2008	F
fcsrNAN2008	F
numMaarRegs	6
srsconf0SRS1	0
srsconf0SRS2	0
srsconf0SRS3	0
wiredLimit	0
wiredLimitBits	0
wiredWiredBits	0
cdmmBaseCI	F
parityEnable	1
useMpTb	Т
ExceptionBase	0
UseExceptionBase	F
l1BufferCache	F
GCU_EX	F
GIC_EX	F
CPC_EX	F
TIMER_ROUTABLE	F
SWINT_ROUTABLE	F
PERFCNT_ROUTABLE	F
FDC_ROUTABLE	F
GCR_PCORES	0
GCR_ADDR_REGIONS	0
GCR_NUMAUX	0
GCR_BASE	0
GCR_MINOR_REV	0
GCR_MAJOR_REV	0
GCR_CACHE_MINOR_REV	0
GCR_CACHE_MAJOR_REV	0
GCR_L2_ASSOC	0
GCR_L2_SET_SIZE	0
GCR_SYS_CONFIG2_MAX_VP_WIDTH	0
GCR_IOCU1_MINOR_REV	0
GCR_IOCU1_MAJOR_REV	0

GCR_BEV_BASE	0
GCR_KX_BASE_MODE	F
GCR_MMIO_REQ_LIMIT	0
GCR_MMIO0_BOTTOM	0
GCR_MMIO0_TOP_ADDR	0
GCR_MMIO1_BOTTOM	0
GCR_MMIO1_TOP_ADDR	0
GCR_MMIO2_BOTTOM	0
GCR_MMIO2_TOP_ADDR	0
GCR_MMIO3_BOTTOM	0
GCR_MMIO3_TOP_ADDR	0
GIC_NUMINTERRUPTS	0
GIC_COUNTBITS	0
GIC_MINOR_REV	0
GIC_MAJOR_REV	0
GIC_NUM_TEAMS	7
GIC_TRIG_RESET	0
GIC_PVPES	0
CPC_MICROSTEP	0
CPC_RAILDELAY	0
CPC_RESETLEN	0
CPC_MINOR_REV	0
CPC_MAJOR_REV	0
GIC_SH_GID_CONFIG31_0	0
GIC_SH_GID_CONFIG63_32	0
GIC_SH_GID_CONFIG95_64	0
GIC_SH_GID_CONFIG127_96	0
GIC_SH_GID_CONFIG159_128	0
GIC_SH_GID_CONFIG191_160	0
GIC_SH_GID_CONFIG223_192	0
GIC_SH_GID_CONFIG255_224	0
gicVirtualVPNum_CPU0_VP0	0
gicVirtualVPNum_CPU0_VP1	0
gicVirtualVPNum_CPU0_VP2	0
gicVirtualVPNum_CPU0_VP3	0
gicVirtualVPNum_CPU1_VP0	0
gicVirtualVPNum_CPU1_VP1	0
gicVirtualVPNum_CPU1_VP2	0
gicVirtualVPNum_CPU1_VP3	0
gicVirtualVPNum_CPU2_VP0	0
gicVirtualVPNum_CPU2_VP1	0
gicVirtualVPNum_CPU2_VP2	0
gicVirtualVPNum_CPU2_VP3	0
gicVirtualVPNum_CPU3_VP0	0
gicVirtualVPNum_CPU3_VP1	0

gicVirtualVPNum_CPU3_VP2	0
gicVirtualVPNum_CPU3_VP3	0
gicVirtualVPNum_CPU4_VP0	0
gicVirtualVPNum_CPU4_VP1	0
gicVirtualVPNum_CPU4_VP2	0
gicVirtualVPNum_CPU4_VP3	0
gicVirtualVPNum_CPU5_VP0	0
gicVirtualVPNum_CPU5_VP1	0
gicVirtualVPNum_CPU5_VP2	0
gicVirtualVPNum_CPU5_VP3	0
gicVirtualVPNum_CPU6_VP0	0
gicVirtualVPNum_CPU6_VP1	0
gicVirtualVPNum_CPU6_VP2	0
gicVirtualVPNum_CPU6_VP3	0
gicVirtualVPNum_CPU7_VP0	0
gicVirtualVPNum_CPU7_VP1	0
gicVirtualVPNum_CPU7_VP2	0
gicVirtualVPNum_CPU7_VP3	0
GCR_C0_RESET_BASE	0
GCR_C1_RESET_BASE	0
GCR_C2_RESET_BASE	0
GCR_C3_RESET_BASE	0
GCR_C4_RESET_BASE	0
GCR_C5_RESET_BASE	0
GCR_C6_RESET_BASE	0
GCR_C7_RESET_BASE	0
GCR_C8_RESET_BASE	0
GCR_C9_RESET_BASE	0
GCR_C0_RESET_EXT_BASE	0
GCR_C1_RESET_EXT_BASE	0
GCR_C2_RESET_EXT_BASE	0
GCR_C3_RESET_EXT_BASE	0
GCR_C4_RESET_EXT_BASE	0
GCR_C5_RESET_EXT_BASE	0
GCR_C6_RESET_EXT_BASE	0
GCR_C7_RESET_EXT_BASE	0
GCR_C8_RESET_EXT_BASE	0
GCR_C9_RESET_EXT_BASE	0
CPC_CO_VP_EN	0
CPC_C1_VP_EN	0
CPC_C2_VP_EN	0
CPC_C3_VP_EN	0
CPC_C4_VP_EN	0
CPC_C5_VP_EN	0
CPC_C6_VP_EN	0

CPC_C7_VP_EN	0
CPC_C8_VP_EN	0
CPC_C9_VP_EN	0
EIC_OPTION	2
guestCtl0RI	0
guestCtl0MC	0
guestCtl0CP0	0
guestCtl0AT	0
guestCtl0GT	0
guestCtl0CG	0
guestCtl0CF	0
guestCtl0G1	0
guestCtl0RAD	0
guestCtl0DRG	0
hasImpl17	F
hasImpl16	F
guestintctlIPTI	0
guestintctlIPFDC	0
guestintctlIPPCI	0
guestintctlIPTI_CPU0_VP0	0
guestintctlIPTI_CPU0_VP1	0
guestintctlIPTI_CPU0_VP2	0
guestintctlIPTI_CPU0_VP3	0
guestintctlIPTI_CPU1_VP0	0
guestintctlIPTI_CPU1_VP1	0
guestintctlIPTI_CPU1_VP2	0
guestintctlIPTI_CPU1_VP3	0
guestintctlIPTI_CPU2_VP0	0
guestintctlIPTI_CPU2_VP1	0
guestintctlIPTI_CPU2_VP2	0
guestintctlIPTI_CPU2_VP3	0
guestintctlIPTI_CPU3_VP0	0
guestintctlIPTI_CPU3_VP1	0
guestintctlIPTI_CPU3_VP2	0
guestintctlIPTI_CPU3_VP3	0
guestintctlIPTI_CPU4_VP0	0
guestintctlIPTI_CPU4_VP1	0
guestintctlIPTI_CPU4_VP2	0
guestintctlIPTI_CPU4_VP3	0
guestintctllPTI_CPU5_VP0	0
guestintctlIPTI_CPU5_VP1	0
guestintctlIPTI_CPU5_VP2	0
guestintctlIPTI_CPU5_VP3	0
guestintctllPTI_CPU6_VP0	0
guestintctlIPTI_CPU6_VP1	0
0	

guestintctIIPTI.CPU6_VP3 guestintctIIPTI.CPU7_VP0 guestintctIIPTI.CPU7_VP1 guestintctIIPTI.CPU7_VP2 guestintctIIPTI.CPU7_VP3 guestintctIIPTI.CPU7_VP3 guestintctIIPTI.CPU7_VP3 guestintctIIPFDC_CPU0_VP0 guestintctIIPFDC_CPU0_VP1 guestintctIIPFDC_CPU0_VP2 guestintctIIPFDC_CPU0_VP3 guestintctIIPFDC_CPU1_VP3 guestintctIIPFDC_CPU1_VP0 guestintctIIPFDC_CPU1_VP1 guestintctIIPFDC_CPU1_VP2 guestintctIIPFDC_CPU1_VP2 guestintctIIPFDC_CPU1_VP3 guestintctIIPFDC_CPU1_VP3 guestintctIIPFDC_CPU2_VP0 guestintctIIPFDC_CPU2_VP0 guestintctIIPFDC_CPU2_VP1 guestintctIIPFDC_CPU2_VP2 guestintctIIPFDC_CPU2_VP3 guestintctIIPFDC_CPU3_VP3 guestintctIIPFDC_CPU3_VP0 guestintctIIPFDC_CPU3_VP1 guestintctIIPFDC_CPU3_VP1 guestintctIIPFDC_CPU3_VP2 guestintctIIPFDC_CPU4_VP0 guestintctIIPFDC_CPU4_VP0 guestintctIIPFDC_CPU4_VP1 guestintctIIPFDC_CPU4_VP1 guestintctIIPFDC_CPU4_VP2 guestintctIIPFDC_CPU5_VP0 guestintctIIPFDC_CPU5_VP1 guestintctIIPFDC_CPU5_VP1 guestintctIIPFDC_CPU5_VP2 guestintctIIPFDC_CPU5_VP3 guestintctIIPFDC_CPU5_VP3 guestintctIIPFDC_CPU5_VP4 guestintctIIPFDC_CPU5_VP4 guestintctIIPFDC_CPU5_VP4 guestintctIIPFDC_CPU5_VP4 guestintctIIPFDC_CPU5_VP4 guestintctIIPFDC_CPU6_VP0	guestintctlIPTI_CPU6_VP2	0
guestintctIIPTI_CPU7_VP0 guestintctIIPTI_CPU7_VP1 guestintctIIPTI_CPU7_VP2 guestintctIIPTI_CPU7_VP3 guestintctIIPTI_CPU7_VP3 guestintctIIPFDC_CPU0_VP0 guestintctIIPFDC_CPU0_VP1 guestintctIIPFDC_CPU0_VP1 guestintctIIPFDC_CPU0_VP2 guestintctIIPFDC_CPU0_VP3 guestintctIIPFDC_CPU1_VP0 guestintctIIPFDC_CPU1_VP0 guestintctIIPFDC_CPU1_VP1 guestintctIIPFDC_CPU1_VP2 guestintctIIPFDC_CPU1_VP3 guestintctIIPFDC_CPU1_VP3 guestintctIIPFDC_CPU1_VP3 guestintctIIPFDC_CPU2_VP0 guestintctIIPFDC_CPU2_VP0 guestintctIIPFDC_CPU2_VP1 guestintctIIPFDC_CPU2_VP2 guestintctIIPFDC_CPU3_VP0 guestintctIIPFDC_CPU3_VP0 guestintctIIPFDC_CPU3_VP1 guestintctIIPFDC_CPU3_VP1 guestintctIIPFDC_CPU3_VP2 guestintctIIPFDC_CPU4_VP0 guestintctIIPFDC_CPU4_VP0 guestintctIIPFDC_CPU4_VP1 guestintctIIPFDC_CPU4_VP2 guestintctIIPFDC_CPU4_VP2 guestintctIIPFDC_CPU4_VP3 guestintctIIPFDC_CPU5_VP1 guestintctIIPFDC_CPU5_VP2 guestintctIIPFDC_CPU6_VP0 guestintctIIPFDC_CPU6_VP0 guestintctIIPFDC_CPU6_VP1 guestintctIIPFDC_CPU6_VP2 guestintctIIPFDC_CPU6_VP3 guestintctIIPFDC_CPU6_VP3 guestintctIIPFDC_CPU6_VP4 guestintctIIPFDC_CPU6_V		
guestintctIIPTLCPU7.VP1 guestintctIIPTLCPU7.VP2 guestintctIIPTLCPU7.VP3 guestintctIIPFDC_CPU0.VP0 guestintctIIPFDC_CPU0.VP1 guestintctIIPFDC_CPU0.VP1 guestintctIIPFDC_CPU0.VP2 guestintctIIPFDC_CPU0.VP3 guestintctIIPFDC_CPU1.VP0 guestintctIIPFDC_CPU1.VP0 guestintctIIPFDC_CPU1.VP1 guestintctIIPFDC_CPU1.VP2 guestintctIIPFDC_CPU1.VP3 guestintctIIPFDC_CPU1.VP3 guestintctIIPFDC_CPU1.VP3 guestintctIIPFDC_CPU2.VP0 guestintctIIPFDC_CPU2.VP0 guestintctIIPFDC_CPU2.VP1 guestintctIIPFDC_CPU2.VP2 guestintctIIPFDC_CPU3.VP0 guestintctIIPFDC_CPU3.VP0 guestintctIIPFDC_CPU3.VP1 guestintctIIPFDC_CPU3.VP2 guestintctIIPFDC_CPU3.VP2 guestintctIIPFDC_CPU3.VP3 guestintctIIPFDC_CPU3.VP3 guestintctIIPFDC_CPU4.VP0 guestintctIIPFDC_CPU4.VP0 guestintctIIPFDC_CPU4.VP1 guestintctIIPFDC_CPU4.VP2 guestintctIIPFDC_CPU5.VP3 guestintctIIPFDC_CPU5.VP1 guestintctIIPFDC_CPU5.VP1 guestintctIIPFDC_CPU5.VP2 guestintctIIPFDC_CPU5.VP3 guestintctIIPFDC_CPU5.VP3 guestintctIIPFDC_CPU6.VP0 guestintctIIPFDC_CPU6.VP1 guestintctIIPFDC_CPU6.VP2 guestintctIIPFDC_CPU6.VP3 guestintctIIPFDC_CPU6.VP3 guestintctIIPFDC_CPU6.VP3 guestintctIIPFDC_CPU7.VP0 guestintctIIPFDC_CPU7.VP1 guestintctIIPFDC_CPU7.VP2 guestintctIIPFDC_CPU7.VP2 guestintctIIPFDC_CPU7.VP3 guestintctIIPFDC_CPU7.VP2 guestintctIIPFDC_CPU7.VP2 guestintctIIPFDC_CPU7.VP3 guestintctIIPFDC_CPU7.VP3 guestintctIIPFDC_CPU7.VP4		
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guestintctIIPPCI_CPU3_VP1         0           guestintctIIPPCI_CPU3_VP2         0           guestintctIIPPCI_CPU4_VP0         0           guestintctIIPPCI_CPU4_VP1         0           guestintctIIPPCI_CPU4_VP2         0           guestintctIIPPCI_CPU4_VP3         0           guestintctIIPPCI_CPU5_VP0         0           guestintctIIPPCI_CPU5_VP1         0           guestintctIIPPCI_CPU5_VP2         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU6_VP0         0           guestintctIIPPCI_CPU6_VP1         0           guestintctIIPPCI_CPU6_VP2         0           guestintctIIPPCI_CPU6_VP3         0           guestintctIIPPCI_CPU7_VP0         0           guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_ENABLE         F           ISPRAM_ENABLE         F           DSPRAM_ENABLE         F           DSPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USP	9	0
guestintctIIPPCI_CPU3_VP3         0           guestintctIIPPCI_CPU4_VP0         0           guestintctIIPPCI_CPU4_VP1         0           guestintctIIPPCI_CPU4_VP2         0           guestintctIIPPCI_CPU4_VP3         0           guestintctIIPPCI_CPU4_VP3         0           guestintctIIPPCI_CPU5_VP0         0           guestintctIIPPCI_CPU5_VP1         0           guestintctIIPPCI_CPU5_VP2         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU6_VP0         0           guestintctIIPPCI_CPU6_VP1         0           guestintctIIPPCI_CPU6_VP2         0           guestintctIIPPCI_CPU6_VP3         0           guestintctIIPPCI_CPU7_VP0         0           guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_ENABLE         F           ISPRAM_ENABLE         F           DSPRAM_ENABLE         F           DSPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE </td <td>guestintctlIPPCI_CPU3_VP0</td> <td>0</td>	guestintctlIPPCI_CPU3_VP0	0
guestintctIIPPCI_CPU3_VP3         0           guestintctIIPPCI_CPU4_VP0         0           guestintctIIPPCI_CPU4_VP1         0           guestintctIIPPCI_CPU4_VP2         0           guestintctIIPPCI_CPU5_VP0         0           guestintctIIPPCI_CPU5_VP1         0           guestintctIIPPCI_CPU5_VP2         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU6_VP0         0           guestintctIIPPCI_CPU6_VP1         0           guestintctIIPPCI_CPU6_VP2         0           guestintctIIPPCI_CPU6_VP3         0           guestintctIIPPCI_CPU7_VP0         0           guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_BASE         0           ISPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_BASE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F	guestintctlIPPCI_CPU3_VP1	0
guestintctIIPPCI_CPU4_VP1         0           guestintctIIPPCI_CPU4_VP2         0           guestintctIIPPCI_CPU4_VP3         0           guestintctIIPPCI_CPU5_VP0         0           guestintctIIPPCI_CPU5_VP1         0           guestintctIIPPCI_CPU5_VP2         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU6_VP0         0           guestintctIIPPCI_CPU6_VP1         0           guestintctIIPPCI_CPU6_VP2         0           guestintctIIPPCI_CPU6_VP3         0           guestintctIIPPCI_CPU7_VP0         0           guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_ENABLE         F           ISPRAM_ENABLE         F           DSPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE         F     <	guestintctlIPPCI_CPU3_VP2	0
guestintctIIPPCI_CPU4_VP1         0           guestintctIIPPCI_CPU4_VP3         0           guestintctIIPPCI_CPU5_VP0         0           guestintctIIPPCI_CPU5_VP1         0           guestintctIIPPCI_CPU5_VP1         0           guestintctIIPPCI_CPU5_VP2         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU6_VP0         0           guestintctIIPPCI_CPU6_VP1         0           guestintctIIPPCI_CPU6_VP2         0           guestintctIIPPCI_CPU6_VP3         0           guestintctIIPPCI_CPU7_VP0         0           guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_BASE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_BASE         0           USPRAM_BASE0           USPRAM_ENABLEF           USPRAM_ENABLEF           USPRAM_ENABLEF           USPRAM_FILE          misalignedDataException         never	guestintctlIPPCI_CPU3_VP3	0
guestintctIIPPCI_CPU4_VP3         0           guestintctIIPPCI_CPU4_VP3         0           guestintctIIPPCI_CPU5_VP0         0           guestintctIIPPCI_CPU5_VP1         0           guestintctIIPPCI_CPU5_VP2         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU6_VP0         0           guestintctIIPPCI_CPU6_VP1         0           guestintctIIPPCI_CPU6_VP2         0           guestintctIIPPCI_CPU6_VP3         0           guestintctIIPPCI_CPU7_VP0         0           guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_BASE         0           ISPRAM_BASE         0           ISPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_PRESENT         F           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         0           USPRAM_FILE         misalignedDataException         never	guestintctlIPPCI_CPU4_VP0	0
guestintctIIPPCI_CPU5_VP0         0           guestintctIIPPCI_CPU5_VP1         0           guestintctIIPPCI_CPU5_VP2         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU6_VP0         0           guestintctIIPPCI_CPU6_VP1         0           guestintctIIPPCI_CPU6_VP2         0           guestintctIIPPCI_CPU6_VP3         0           guestintctIIPPCI_CPU7_VP0         0           guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_PRESENT         F           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         misalignedDataException         never	9	0
guestintctIIPPCI_CPU5_VP1         0           guestintctIIPPCI_CPU5_VP2         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU5_VP3         0           guestintctIIPPCI_CPU6_VP0         0           guestintctIIPPCI_CPU6_VP1         0           guestintctIIPPCI_CPU6_VP2         0           guestintctIIPPCI_CPU6_VP3         0           guestintctIIPPCI_CPU7_VP0         0           guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_ENABLE         F           ISPRAM_FILE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	guestintctlIPPCI_CPU4_VP2	0
guestintctlIPPCI_CPU5_VP1         0           guestintctlIPPCI_CPU5_VP2         0           guestintctlIPPCI_CPU5_VP3         0           guestintctlIPPCI_CPU6_VP0         0           guestintctlIPPCI_CPU6_VP1         0           guestintctlIPPCI_CPU6_VP2         0           guestintctlIPPCI_CPU6_VP3         0           guestintctlIPPCI_CPU7_VP0         0           guestintctlIPPCI_CPU7_VP1         0           guestintctlIPPCI_CPU7_VP2         0           guestintctlIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_FILE         0           DSPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         misalignedDataException         never	guestintctlIPPCI_CPU4_VP3	0
guestintctlIPPCI_CPU5_VP3         0           guestintctlIPPCI_CPU5_VP3         0           guestintctlIPPCI_CPU6_VP0         0           guestintctlIPPCI_CPU6_VP1         0           guestintctlIPPCI_CPU6_VP2         0           guestintctlIPPCI_CPU6_VP3         0           guestintctlIPPCI_CPU7_VP0         0           guestintctlIPPCI_CPU7_VP1         0           guestintctlIPPCI_CPU7_VP2         0           guestintctlIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	guestintctlIPPCI_CPU5_VP0	0
guestintctlIPPCI_CPU5_VP3         0           guestintctlIPPCI_CPU6_VP0         0           guestintctlIPPCI_CPU6_VP1         0           guestintctlIPPCI_CPU6_VP2         0           guestintctlIPPCI_CPU6_VP3         0           guestintctlIPPCI_CPU7_VP0         0           guestintctlIPPCI_CPU7_VP1         0           guestintctlIPPCI_CPU7_VP2         0           guestintctlIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_SIZE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           DSPRAM_ENABLE         F           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	guestintctlIPPCI_CPU5_VP1	0
guestintctlIPPCI_CPU6_VP0         0           guestintctlIPPCI_CPU6_VP1         0           guestintctlIPPCI_CPU6_VP2         0           guestintctlIPPCI_CPU6_VP3         0           guestintctlIPPCI_CPU7_VP0         0           guestintctlIPPCI_CPU7_VP1         0           guestintctlIPPCI_CPU7_VP2         0           guestintctlIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_SIZE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           DSPRAM_PRESENT         F           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	guestintctlIPPCI_CPU5_VP2	0
guestintctIIPPCI_CPU6_VP1         0           guestintctIIPPCI_CPU6_VP2         0           guestintctIIPPCI_CPU6_VP3         0           guestintctIIPPCI_CPU7_VP0         0           guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_FILE         0           DSPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_BASE         0           DSPRAM_PRESENT         F           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	guestintctlIPPCI_CPU5_VP3	0
guestintctlIPPCI_CPU6_VP3         0           guestintctlIPPCI_CPU6_VP3         0           guestintctlIPPCI_CPU7_VP0         0           guestintctlIPPCI_CPU7_VP1         0           guestintctlIPPCI_CPU7_VP2         0           guestintctlIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_SIZE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           DSPRAM_ENABLE         F           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	guestintctlIPPCI_CPU6_VP0	0
guestintctIIPPCI_CPU6_VP3         0           guestintctIIPPCI_CPU7_VP0         0           guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_FILE         F           DSPRAM_SIZE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	guestintctlIPPCI_CPU6_VP1	0
guestintctIIPPCI_CPU7_VP1         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_FILE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           DSPRAM_PRESENT         F           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never		0
guestintctlIPPCI_CPU7_VP1         0           guestintctlIPPCI_CPU7_VP2         0           guestintctlIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_FILE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           DSPRAM_ENABLE         F           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	guestintctlIPPCI_CPU6_VP3	0
guestintctIIPPCI_CPU7_VP2         0           guestintctIIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_FILE         0           DSPRAM_SIZE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           USPRAM_SIZE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	9	0
guestintctIIPPCI_CPU7_VP3         0           ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_FILE         0           DSPRAM_SIZE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           USPRAM_SIZE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never		0
ISPRAM_SIZE         0           ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_FILE         0           DSPRAM_SIZE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           USPRAM_SIZE         0           USPRAM_BASE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	guestintctlIPPCI_CPU7_VP2	0
ISPRAM_BASE         0           ISPRAM_ENABLE         F           ISPRAM_FILE         0           DSPRAM_SIZE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           DSPRAM_PRESENT         F           USPRAM_SIZE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_FILE         F           misalignedDataException         never	guestintctlIPPCI_CPU7_VP3	0
ISPRAM_ENABLEFISPRAM_FILE0DSPRAM_SIZE0DSPRAM_BASE0DSPRAM_ENABLEFDSPRAM_PRESENTFUSPRAM_SIZE0USPRAM_BASE0USPRAM_ENABLEFUSPRAM_ENABLEFUSPRAM_FILEmisalignedDataExceptionnever	ISPRAM_SIZE	0
ISPRAM_FILE         0           DSPRAM_SIZE         0           DSPRAM_BASE         0           DSPRAM_ENABLE         F           DSPRAM_PRESENT         F           USPRAM_SIZE         0           USPRAM_BASE         0           USPRAM_ENABLE         F           USPRAM_FILE         r           misalignedDataException         never	ISPRAM_BASE	0
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DSPRAM_BASE 0 DSPRAM_ENABLE F DSPRAM_PRESENT F USPRAM_SIZE 0 USPRAM_BASE 0 USPRAM_ENABLE F USPRAM_FILE misalignedDataException never	ISPRAM_FILE	
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USPRAM_SIZE 0 USPRAM_BASE 0 USPRAM_ENABLE F USPRAM_FILE misalignedDataException never	DSPRAM_ENABLE	F
USPRAM_BASE 0 USPRAM_ENABLE F USPRAM_FILE misalignedDataException never	DSPRAM_PRESENT	F
USPRAM_ENABLE F USPRAM_FILE misalignedDataException never	USPRAM_SIZE	0
USPRAM_FILE misalignedDataException never	USPRAM_BASE	0
misalignedDataException never	USPRAM_ENABLE	F
	USPRAM_FILE	
commitTlbwErr F		never
	commitTlbwErr	F

Table 8.2: Parameter values

Name	Type	Description
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags

cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
${\it cache Index By pass TLB}$	Boolean	When set, cache index ops do not generate TLB
MIPS_TRACE	Boolean	exceptions  Enable MIPS-format trace output
gprNames	Boolean	Disassemble the register names from the default
gprivames	Doolean	ABI instead of register numbers for MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
${\it fixedDbgRegSize}$	Boolean	Enable applications to debug on P5600 with GDB version 2015.06-05 and prior
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true (disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
perfCounters	Uns32	Performance Counters
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC implementation (MT cores only)
ITCFIFODepth	Uns32	Specify ITC FIFO cell depth. By default supports 4.
ITCEmptyOnReset	Boolean	Specify ITC E/F cells reset to a known empty state.
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0. Ignored if less than two VPEs configured.
VPE1MaxTC	Uns32	Specifies the maximum TCs initially on VPE1. Ignored if less than three VPEs configured.
segBits	Uns32	Override the number of address bits implemented for 64 bit segments (MIPS64 Only)
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentControl_0 register

mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentCon-
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentControl.0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentCon-
mpusegment2	Ulis52	trol_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentCon-
mpubegmenta	011302	trol_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentCon-
mpasesment i	011502	trol_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentCon-
F and a 9		trol_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentCon-
•		trol_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentCon-
		trol_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentCon-
		trol_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentCon-
		trol_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentCon-
		trol_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentCon-
		trol_2 register
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentCon-
~		trol_3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentCon-
0 114	11 00	trol_3 register
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentCon-
manus Commont 15	Uns32	trol_3 register Attributes for segment 15 in MPU2 SegmentCon-
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentControl.3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
tcDisable	Uns32	Number of disabled TCs
vpeDisable	Uns32	Number of disabled VPEs
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
mvpconf1c1f	Boolean	Override MVPConf.C1F
mvpcontrolPolicyMode	Boolean	Override MVPControl.POLICY_MODE
hasFDC	Uns32	Specify the size of Fast Debug Channel register
		block
licenseWarningDays	Uns32	Specify the number of days before a license expires
		to start issuing a warning. 0 disables warnings.
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string separated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
TRU_PRESENT	Boolean	Disable or Enable based on TRU presence to con-
		trol certain fields (e.x.perfCtl.PCTD
ucLLwordsLocked	Uns32	Numbers of words (4 byte) an uncached LL is lock-
		ing. Maximum: 4K
FUSA	Boolean	Enable Functional Safety
CPC_FAULT_SUPPORTED	Uns32	Specify the value for Functional Safety Supported
		register

CPC_FAULT_ENABLE	Uns32	Specify the value for Functional Safety Enable register
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object
•		(.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll)
		defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller
-		(sets Config3 VEIC)
config3VEIC_VPE0	Boolean	Enables an external interrupt controller on VPE0
config3VEIC_VPE1	Boolean	(sets Config3 VEIC) Enables an external interrupt controller on VPE1
conng3vEiC_vPEi	Boolean	(sets Config3 VEIC)
config3VEIC_VPE2	Boolean	Enables an external interrupt controller on VPE2
		(sets Config3 VEIC)
config3VEIC_VPE3	Boolean	Enables an external interrupt controller on VPE3
		(sets Config3 VEIC)
rootFixedMMU	Boolean	Override the root MMU type to fixed map-
		ping when true (sets Config.MT=3 and Con-
		fig.KU/K23=2)
rootMMUSizeM1	Uns32	Override the root MMUSizeM1 field in Config1 reg-
		ister (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number
		of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
usePreciseFpu	Uns32	Use the precise Floating Point emulation
simulateLite	Enumeration	Run Simulation with optimization. There are
		several optimizations which coule be combined
		(NONE, FS, MA or FSMA)
pridCompanyOptions	Uns32	Override the Company Options field in PRId reg-
: 4D:-:	Uns32	ister
pridRevision globalClusterNum		Override the Revision field in PRId register  Override the ClusterNum field in GlobalNumber
globalClusterNum	Uns32	
intctlIPTI	Uns32	register Override the IPTI field in IntCtl register
intctlIPFDC	Uns32	Override the IPT1 field in IntCt1 register  Override the IPFDC field in IntCt1 register
intctllPPCl	Uns32	Override the IPPCI field in IntCtl register  Specify number of Watch I o / Watch Hi register pairs
numWatch maxVP	Uns32 Uns32	Specify number of WatchLo/WatchHi register pairs Specify maximum number of Virtual Processors
maxvF	Ulisoz	
numVP	Uns32	present in a core Specify number of Virtual Processors to be present
numVPtoStart	Uns32	Specify number of Virtual Processors to be present Specify number of Virtual Processors to be started
sharedTLBindex	Uns32	Specify first shared TLB Index between Virtual
Shared I LDindex	Ulis52	Cores
xconfigSpecified	Boolean	True if the configuration comes from a valid xconfig file
intctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for
IIIIUUIIF II_OF OU_VFU	Ulisəz	
intctlIPTI_CPU0_VP1	Uns32	CPU0/VP0 Override the IPTI field in IntCtl register for
		CPU0/VP1
intctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2

intctlIPTI_CPU0_VP3	II 00	
	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
intctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
intctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
intctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
intctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
intctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
intetlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
intctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
intetlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
intctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
intctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
intctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
intctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
intctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
intctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
intctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
intctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
intctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
intctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
intctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
intctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
intctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
intctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
intctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
intctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
intctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
intctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
intctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2

intetlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
intctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
intctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
intctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
intctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
intctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
intctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
intctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
intctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
intctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
intctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
intctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
intctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
intctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
intctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
intctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
intctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
intctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
intctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
intctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
intctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
intctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
intctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
intctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
intctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
intctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
intctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
intctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2

intctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
intctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
intctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
intctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
intctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
intctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
intctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
intctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
intctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
intctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
intctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
intctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
intctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
intctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
intctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
intctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
intctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
intctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
intctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
intctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
intctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
intctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
intctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
intctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
intctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
intctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
intctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
intctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2

intctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
intctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
intctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
intctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
intctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
intctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
intctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
intctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
intctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
segcfg0PA	Uns32	Set CFG0.PA field of SegCtl0 register
segcfg1PA	Uns32	Set CFG1.PA field of SegCtl0 register
segcfg2PA	Uns32	Set CFG2.PA field of SegCtl1 register
segcfg3PA	Uns32	Set CFG3.PA field of SegCtl1 register
segcfg4PA	Uns32	Set CFG4.PA field of SegCtl2 register
segcfg5PA	Uns32	Set CFG5.PA field of SegCtl2 register
segcfg0AM	Uns32	Set CFG0.AM field of SegCtl0 register
segcfg1AM	Uns32	Set CFG1.AM field of SegCtl0 register
segcfg2AM	Uns32	Set CFG2.AM field of SegCtl1 register
segcfg3AM	Uns32	Set CFG3.AM field of SegCtl1 register
segcfg4AM	Uns32	Set CFG4.AM field of SegCtl2 register
segcfg5AM	Uns32	Set CFG5.AM field of SegCtl2 register
segcfg0EU	Uns32	Set CFG0.EU field of SegCtl0 register
segcfg1EU	Uns32	Set CFG1.EU field of SegCtl0 register
segcfg2EU	Uns32	Set CFG2.EU field of SegCtl1 register
segcfg3EU	Uns32	Set CFG3.EU field of SegCtl1 register
segcfg4EU	Uns32	Set CFG4.EU field of SegCtl2 register
segcfg5EU	Uns32	Set CFG5.EU field of SegCtl2 register
segcfg0C	Uns32	Set CFG0.C field of SegCtl0 register
segcfg1C	Uns32	Set CFG1.C field of SegCtl0 register
segcfg2C	Uns32	Set CFG2.C field of SegCtl1 register
segcfg3C	Uns32	Set CFG3.C field of SegCtl1 register
segcfg4C	Uns32	Set CFG4.C field of SegCtl2 register
segcfg5C	Uns32	Set CFG5.C field of SegCtl2 register
cdmmSize	Uns32	Override the cdmmsize reset value
configAR	Uns32	Enables R6 support
configBM	Uns32	Override the BM field in Config register (burst
configDSP	Boolean	mode) Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23 cacheability)

configMDU	Boolean	Override Config.MDU (iterative multiply/divide
C MM	D 1	unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
configBCP	Boolean	Override Config.BCP (Buffer Cache Present)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Deache associativity)
config1DL	Uns32	Override Config1.DL (Deache line size)
config1DS	Uns32	Override Config1.DS (Dcache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU
		entries-1)
config1MMUSizeM1_VPE1	Uns32	Override Config1.MMUSizeM1 for VPE1
config1MMUSizeM1_VPE2	Uns32	Override Config1.MMUSizeM1 for VPE2
config1MMUSizeM1_VPE3	Uns32	Override Config1.MMUSizeM1 for VPE3
config1WR	Boolean	Override Config1.WR (watchpoint registers
	Doolcan	present)
config1PC	Boolean	Override Config1.PC (Performance Counters
Comigii	Doolcan	present)
config1C2	Boolean	Override Config1.C2 (Coprocessor 2 present)
config2SU	Uns32	Override Collig1.C2 (Coplocessol 2 present)  Override the SU field in Config2 register
config2SS	Uns32	Override the SS field in Config2 register
config2SL	Uns32	Override the SL field in Config2 register
config2SA	Uns32	Override the SA field in Config2 register
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.LPA
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
config3VZ	Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3. VZ Override Config3. MSAP
config3CMGCR	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation
		depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt

C ARC D : A	11 90	O :1 C CARC E:4
config4KScrExist	Uns32	Override Config4.KScrExist
config5EVA	Boolean	Override Config5.EVA
config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
mips32Macro	Boolean	Enables the MIPS32 SAVE and RESTORE macro
C FACAT	D I	instructions. Ignored if Config5.CA2 is not set)
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and MFHC0 instructions)
config5DEC	D1	
conngoDEC	Boolean	Override Config5.DEC (to test Dual Endian Capa-
C C-I	II 20	bility)
config5GI	Uns32	Override Config5.GI (enable GINV)
config5CRCP	Boolean	Override Config5.CRCP (CRCP Present)
config5VP	Boolean	Override Config5.VP
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initializa-
CHAD	D I	tion)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction
C MILLI	D I	cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (External-
CAMD	D 1	ize sync)
config7WR	Boolean	Override Config7[31] bit (Alternative implementa-
C ZDDD	D 1	tion of Watch registers)
config7FPR	Boolean Uns32	Override Config7.FPR (one-half FPU clock ratio)
config7USP config7BTLM	Boolean	Override Config7.USP (USPRAM enable)
config7BusSlp	Boolean	Override Config7.BTLM bit Override Config7.BusSlp bit
config7IVAD	Boolean	Override Config7.IVAD bit
config7RPS	Boolean	Override Config7.IVAD bit Override Config7.RPS bit
config7IAR_CPU0_VPE0	Boolean	Override Config7.IAR bit for CPU0/VPE0
config7IAR_CPU0_VPE0	Boolean	Override Config7.IAR bit for CPU0/VPE0  Override Config7.IAR bit for CPU0/VPE1
config7IAR_CPU0_VPE1	Boolean	Override Config7.IAR bit for CPU0/VPE1  Override Config7.IAR bit for CPU0/VPE2
config7IAR_CPU0_VPE2	Boolean	Override Config7.IAR bit for CPU0/VPE2  Override Config7.IAR bit for CPU0/VPE3
_	Boolean	Override Config7.IAR bit for CPU1/VPE0
config7IAR_CPU1_VPE0 config7IAR_CPU1_VPE1	Boolean	Override Config7.IAR bit for CPU1/VPE1  Override Config7.IAR bit for CPU1/VPE1
config7IAR_CPU1_VPE2	Boolean	Override Config7.IAR bit for CPU1/VPE2  Override Config7.IAR bit for CPU1/VPE2
config7IAR_CPU1_VPE3	Boolean	Override Config7.IAR bit for CPU1/VPE3
config7IAR_CPU1_VPE3		
config7IAR_CPU2_VPE0 config7IAR_CPU2_VPE1	Boolean	Override Config7.IAR bit for CPU2/VPE0 Override Config7.IAR bit for CPU2/VPE1
	Boolean Boolean	
config7IAR_CPU2_VPE2		Override Config7.IAR bit for CPU2/VPE2 Override Config7.IAR bit for CPU2/VPE3
config7IAR_CPU2_VPE3	Boolean	1
config7IAR_CPU3_VPE0	Boolean	Override Config7.IAR bit for CPU3/VPE0 Override Config7.IAR bit for CPU3/VPE1
config7IAR_CPU3_VPE1	Boolean	
config7IAR_CPU3_VPE2	Boolean	Override Config7.IAR bit for CPU3/VPE2
config7IAR_CPU3_VPE3	Boolean	Override Config7.IAR bit for CPU3/VPE3
config7IAR_CPU4_VPE0	Boolean	Override Config7.IAR bit for CPU4/VPE0
config7IAR_CPU4_VPE1	Boolean	Override Config7.IAR bit for CPU4/VPE1
config7IAR_CPU4_VPE2	Boolean	Override Config7.IAR bit for CPU4/VPE2
config7IAR_CPU4_VPE3	Boolean	Override Config7.IAR bit for CPU4/VPE3
config7IAR_CPU5_VPE0	Boolean	Override Config7.IAR bit for CPU5/VPE0
config7IAR_CPU5_VPE1	Boolean	Override Config7.IAR bit for CPU5/VPE1
config7IAR_CPU5_VPE2	Boolean	Override Config7.IAR bit for CPU5/VPE2

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config7IAR_CPU5_VPE3	Boolean	Override Config7.IAR bit for CPU5/VPE3
config7IAR_CPU6_VPE0	Boolean	Override Config7.IAR bit for CPU6/VPE0
config7IAR_CPU6_VPE1	Boolean	Override Config7.IAR bit for CPU6/VPE1
config7IAR_CPU6_VPE2	Boolean	Override Config7.IAR bit for CPU6/VPE2
config7IAR_CPU6_VPE3	Boolean	Override Config7.IAR bit for CPU6/VPE3
config7IAR_CPU7_VPE0	Boolean	Override Config7.IAR bit for CPU7/VPE0
config7IAR_CPU7_VPE1	Boolean	Override Config7.IAR bit for CPU7/VPE1
config7IAR_CPU7_VPE2	Boolean	Override Config7.IAR bit for CPU7/VPE2
config7IAR_CPU7_VPE3	Boolean	Override Config7.IAR bit for CPU7/VPE3
config7IVAD_CPU0_VPE0	Boolean	Override Config7.IVAD bit for CPU0/VPE0
config7IVAD_CPU0_VPE1	Boolean	Override Config7.IVAD bit for CPU0/VPE1
config7IVAD_CPU0_VPE2	Boolean	Override Config7.IVAD bit for CPU0/VPE2
config7IVAD_CPU0_VPE3	Boolean	Override Config7.IVAD bit for CPU0/VPE3
config7IVAD_CPU1_VPE0	Boolean	Override Config7.IVAD bit for CPU1/VPE0
config7IVAD_CPU1_VPE1	Boolean	Override Config7.IVAD bit for CPU1/VPE1
config7IVAD_CPU1_VPE2	Boolean	Override Config7.IVAD bit for CPU1/VPE2
config7IVAD_CPU1_VPE3	Boolean	Override Config7.IVAD bit for CPU1/VPE3
config7IVAD_CPU2_VPE0	Boolean	Override Config7.IVAD bit for CPU2/VPE0
config7IVAD_CPU2_VPE1	Boolean	Override Config7.IVAD bit for CPU2/VPE1
config7IVAD_CPU2_VPE2	Boolean	Override Config7.IVAD bit for CPU2/VPE2
config7IVAD_CPU2_VPE3	Boolean	Override Config7.IVAD bit for CPU2/VPE3
config7IVAD_CPU3_VPE0	Boolean	Override Config7.IVAD bit for CPU3/VPE0
config7IVAD_CPU3_VPE1	Boolean	Override Config7.IVAD bit for CPU3/VPE1
config7IVAD_CPU3_VPE2	Boolean	Override Config7.IVAD bit for CPU3/VPE2
config7IVAD_CPU3_VPE3	Boolean	Override Config7.IVAD bit for CPU3/VPE3
config7IVAD_CPU4_VPE0	Boolean	Override Config7.IVAD bit for CPU4/VPE0
config7IVAD_CPU4_VPE1	Boolean	Override Config7.IVAD bit for CPU4/VPE1
config7IVAD_CPU4_VPE2	Boolean	Override Config7.IVAD bit for CPU4/VPE2
config7IVAD_CPU4_VPE3	Boolean	Override Config7.IVAD bit for CPU4/VPE3
config7IVAD_CPU5_VPE0	Boolean	Override Config7.IVAD bit for CPU5/VPE0  Override Config7.IVAD bit for CPU5/VPE0
config7IVAD_CPU5_VPE1	Boolean	Override Config7.IVAD bit for CPU5/VPE1
config7IVAD_CPU5_VPE2	Boolean	Override Config7.IVAD bit for CPU5/VPE2
config7IVAD_CPU5_VPE3	Boolean	Override Config7.IVAD bit for CPU5/VPE3
config7IVAD_CPU6_VPE0	Boolean	Override Config7.IVAD bit for CPU6/VPE0
config7IVAD_CPU6_VPE1	Boolean	Override Config7.IVAD bit for CPU6/VPE1
config7IVAD_CPU6_VPE2	Boolean	Override Config7.IVAD bit for CPU6/VPE2
config7IVAD_CPU6_VPE3	Boolean	Override Config7.IVAD bit for CPU6/VPE3
config7IVAD_CPU7_VPE0	Boolean	Override Config7.IVAD bit for CPU7/VPE0
config7IVAD_CPU7_VPE1	Boolean	Override Config7.IVAD bit for CPU7/VPE1
config7IVAD_CPU7_VPE2	Boolean	Override Config7.IVAD bit for CPU7/VPE2
config7IVAD_CPU7_VPE3	Boolean	Override Config7.IVAD bit for CPU7/VPE3
config7RPS_CPU0_VPE0	Boolean	Override Config7.RPS bit for CPU0/VPE0
config7RPS_CPU0_VPE1	Boolean	Override Config7.RPS bit for CPU0/VPE1
config7RPS_CPU0_VPE2	Boolean	Override Config7.RPS bit for CPU0/VPE2
config7RPS_CPU0_VPE3	Boolean	Override Config7.RPS bit for CPU0/VPE3
config7RPS_CPU1_VPE0	Boolean	Override Config7.RPS bit for CPU1/VPE0
config7RPS_CPU1_VPE1	Boolean	Override Config7.RPS bit for CPU1/VPE1
config7RPS_CPU1_VPE2	Boolean	Override Config7.RPS bit for CPU1/VPE2
config7RPS_CPU1_VPE3	Boolean	Override Config7.RPS bit for CPU1/VPE3
config7RPS_CPU2_VPE0	Boolean	Override Config7.RPS bit for CPU2/VPE0
config7RPS_CPU2_VPE1	Boolean	Override Config7.RPS bit for CPU2/VPE1
config7RPS_CPU2_VPE2	Boolean	Override Config7.RPS bit for CPU2/VPE2
config7RPS_CPU2_VPE3	Boolean	Override Config7.RPS bit for CPU2/VPE3
config7RPS_CPU3_VPE0	Boolean	Override Config7.RPS bit for CPU3/VPE0
config7RPS_CPU3_VPE1	Boolean	Override Config7.RPS bit for CPU3/VPE1
config7RPS_CPU3_VPE2	Boolean	Override Config7.RPS bit for CPU3/VPE2
		·

config7RPS_CPU3_VPE3	Boolean	Override Config7.RPS bit for CPU3/VPE3
config7RPS_CPU4_VPE0	Boolean	Override Config7.RPS bit for CPU4/VPE0
config7RPS_CPU4_VPE1	Boolean	Override Config7.RPS bit for CPU4/VPE1
config7RPS_CPU4_VPE2	Boolean	Override Config7.RPS bit for CPU4/VPE2
config7RPS_CPU4_VPE3	Boolean	Override Config7.RPS bit for CPU4/VPE3
config7RPS_CPU5_VPE0	Boolean	Override Config7.RPS bit for CPU5/VPE0
config7RPS_CPU5_VPE1	Boolean	Override Config7.RPS bit for CPU5/VPE1
config7RPS_CPU5_VPE2	Boolean	Override Config7.RPS bit for CPU5/VPE2
config7RPS_CPU5_VPE3	Boolean	Override Config7.RPS bit for CPU5/VPE3
config7RPS_CPU6_VPE0	Boolean	Override Config7.RPS bit for CPU6/VPE0
config7RPS_CPU6_VPE1	Boolean	Override Config7.RPS bit for CPU6/VPE1
config7RPS_CPU6_VPE2	Boolean	Override Config7.RPS bit for CPU6/VPE2
config7RPS_CPU6_VPE3	Boolean	Override Config7.RPS bit for CPU6/VPE3
config7RPS_CPU7_VPE0	Boolean	Override Config7.RPS bit for CPU7/VPE0
config7RPS_CPU7_VPE1	Boolean	Override Config7.RPS bit for CPU7/VPE1
config7RPS_CPU7_VPE2	Boolean	Override Config7.RPS bit for CPU7/VPE2
config7RPS_CPU7_VPE3	Boolean	Override Config7.RPS bit for CPU7/VPE3
statusFR	Boolean	Override power on value in Status.FR (Floating
		point register mode)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant
		with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings
		match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
srsconf0SRS1	Uns32	Override the SRS1 field in SRSConf0 register
srsconf0SRS2	Uns32	Override the SRS2 field in SRSConf0 register
srsconf0SRS3	Uns32	Override the SRS3 field in SRSConf0 register
wiredLimit	Uns32	Override Limit field of the Wired register
wiredLimitBits	Uns32	Override width of Limit field of the Wired register
wiredWiredBits	Uns32	Override width of Wired field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
parityEnable	Uns32	Specify error detection support: 0 - none; 1 - parity; 2 - ECC
useMpTb	Boolean	Override Use of multi-processor test bench
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use
_		GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the cor-
11D # C 1	D. I	responding BEV address bits
l1BufferCache	Boolean	L1 Buffer Cache
GCU_EX	Boolean	CMP system only: GCR custom block present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable
		within cluster
PERFCNT_ROUTABLE	Boolean	CMP system only: performance counter interrupt
EDG DOUBLD E	D 1	routable within cluster
FDC_ROUTABLE	Boolean	CMP system only: fast debug channel interrupt
GGD DGGDEG	TT 00	routable within cluster
GCR_PCORES	Uns32	CMP system only: override
CCP ADDD DECICES	TT 22	GCR_CONFIG.PCORES (number of cores-1)
GCR_ADDR_REGIONS	Uns32	CMP system only: override
		GCR_CONFIG.ADDR_REGIONS (number of
		MMIO address regions)

GCR_NUMAUX	Uns32	CMP system only: override GCR_CONFIG.NUMAUX (number of auxil-
		iary memory ports)
GCR_BASE	Uns64	CMP system only: override GCR_BASE.GCR_BASE (default GCR regis-
CCD MINOD DEV	11 00	ter address)
GCR_MINOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MAJOR_REV
GCR_L2_ASSOC	Uns32	CMP system only: override GCR_L2_CONFIG.ASSOC
GCR_L2_SET_SIZE	Uns32	CMP system only: override GCR_L2_CONFIG.SET_SIZE
GCR_SYS_CONFIG2_MAX_VP_WIDTH	Uns32	CMP system only: override GCR_SYS_CONFIG2.MAX_VP_WIDTH
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GCR_BEV_BASE	Uns32	CMP system only: override GCR_BEV_BASE
GCR_KX_BASE_MODE	Boolean	CMP system only: override BEV_BASE_MODE & RESET_BASE_MODE
GCR_MMIO_REQ_LIMIT	Uns32	CMP system only: override GCR_MMIO_REQ_LIMIT.MMIO_REQ_LIMIT value
GCR_MMIO0_BOTTOM	Uns64	CMP system only: override GCR_MMIO0_BOTTOM register value
GCR_MMIO0_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO0_TOP.TOP_ADDR value
GCR_MMIO1_BOTTOM	Uns64	CMP system only: override GCR_MMIO1_BOTTOM register value
GCR_MMIO1_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO1_TOP.TOP_ADDR value
GCR_MMIO2_BOTTOM	Uns64	CMP system only: override GCR_MMIO2_BOTTOM register value
GCR_MMIO2_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO2_TOP.TOP_ADDR value
GCR_MMIO3_BOTTOM	Uns64	CMP system only: override GCR_MMIO3_BOTTOM register value
GCR_MMIO3_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO3_TOP.TOP_ADDR value
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override GIC_SH_DBG_CONFIG.NUM_TEAMS

GIC_TRIG_RESET	Uns32	CMP system only: Zero value of GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255.224]
gicVirtualVPNum_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
gicVirtualVPNum_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
gicVirtualVPNum_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
gicVirtualVPNum_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
gicVirtualVPNum_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
gicVirtualVPNum_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
gicVirtualVPNum_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
gicVirtualVPNum_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
gicVirtualVPNum_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
gicVirtualVPNum_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
$gicVirtualVPNum\_CPU2\_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
gicVirtualVPNum_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
gicVirtualVPNum_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0

gicVirtualVPNum_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
gicVirtualVPNum_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
gicVirtualVPNum_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
gicVirtualVPNum_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
gicVirtualVPNum_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
gicVirtualVPNum_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
gicVirtualVPNum_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
gicVirtualVPNum_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
gicVirtualVPNum_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
gicVirtualVPNum_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
gicVirtualVPNum_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
gicVirtualVPNum_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
gicVirtualVPNum_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
gicVirtualVPNum_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
gicVirtualVPNum_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
gicVirtualVPNum_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
gicVirtualVPNum_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
gicVirtualVPNum_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
gicVirtualVPNum_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C4_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 4
GCR_C5_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 5
GCR_C6_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 6
GCR_C7_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 7
GCR_C8_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 8

GCR_C9_RESET_BASE	IIma22	CMP system only: GCR_CL_RESET_BASE for
GCR_C9_RESET_BASE	Uns32	· ·
GCR_C0_RESET_EXT_BASE	Uns32	core 9  CMP system only: GCR_CL_RESET_EXT_BASE
GCR_CU_RESET_EXT_BASE	Uns32	for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GCR_CT_RESET_EXT_BASE	Uns32	
CCD CO DECEM EVE DAGE	TT 90	for core 1  CMP system only: GCR_CL_RESET_EXT_BASE
GCR_C2_RESET_EXT_BASE	Uns32	
CCD Co DECEMENT DACE	TT 00	for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GGD G4 DEGER EVER DAGE	***	for core 3
GCR_C4_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 4
GCR_C5_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 5
GCR_C6_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 6
GCR_C7_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 7
GCR_C8_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 8
GCR_C9_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 9
CPC_C0_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 0
CPC_C1_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 1
CPC_C2_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 2
CPC_C3_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 3
CPC_C4_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 4
CPC_C5_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 5
CPC_C6_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 6
CPC_C7_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 7
CPC_C8_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 8
CPC_C9_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 9
EIC_OPTION	Uns32	Override the external interrupt controller
		EIC_OPTION
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register
guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest IPFDC field in IntCtl register
guestintctIIPPCI	Uns32	Override the Guest IPPCI field in IntCtl register
guestintctIIPTI_CPU0_VP0	Uns32	Override the Guest II Tel held in IntCtl register for
Successificant 11201 002410	011502	CPU0/VP0
guestintctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for
Successificant 11_Of OU_VII	011852	CPU0/VP1
guestintctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for
guestificult 11_OFUU_VFZ	Ulisaz	CPU0/VP2
		OF OU/ VF2

guestintctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
guestintctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
guestintctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
guestintctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
guestintctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
guestintctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
guestintctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
guestintctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
guestintctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
guestintctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
guestintctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
guestintctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
guestintctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
guestintctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
guestintctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
guestintctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
guestintctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
guestintctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
guestintctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
guestintctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
guestintctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
guestintctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
guestintctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
guestintctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
guestintctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
guestintctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
guestintctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
guestintctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2

guestintctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
guestintctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
guestintctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
guestintctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
guestintctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
guestintctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
guestintctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
guestintctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
guestintctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
guestintctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
guestintctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
guestintctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
guestintctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
guestintctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
guestintctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
guestintctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
guestintctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
guestintctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
guestintctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
guestintctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
guestintctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
guestintctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
guestintctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
guestintctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
guestintctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
guestintctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
guestintctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
guestintctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2

guestintctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
guestintctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
guestintctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
guestintctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
guestintctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
guestintctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
guestintctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
guestintctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
guestintctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
guestintctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
guestintctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
guestintctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
guestintctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
guestintctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
guestintctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
guestintctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
guestintctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
guestintctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
guestintctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
guestintctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
guestintctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
guestintctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
guestintctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
guestintctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
guestintctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
guestintctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
guestintctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
$guest int ctlIPPCI\_CPU5\_VP2$	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2

guestintctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
guestintctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
guestintctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
guestintctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
guestintctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
guestintctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
guestintctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
guestintctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
guestintctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2( <ispram bytes="" in="" size="">) - 11)</ispram>
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2( <dspram bytes="" in="" size="">) - 11)</dspram>
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag (used to enable the DSPRAM region prior to reset)
DSPRAM_PRESENT	Boolean	DSPRAM is present with SAAR
USPRAM_SIZE	Uns32	Encoded size of the USPRAM region (log2( <uspram bytes="" in="" size="">) - 11)</uspram>
USPRAM_BASE	Uns64	Starting physical address of the USPRAM region
USPRAM_ENABLE	Boolean	Set the enable bit of the USPRAM region's tag (used to enable the USPRAM region prior to reset)
USPRAM_FILE	String	Load a MIPS hex file into the USPRAM region prior to reset
misaligned Data Exception	Enumeration	Select misaligned data access exception signaling: never, checkCCA or always (never, checkCCA or always)
commitTlbwErr	Boolean	Commit TLBWI/TLBRI on ECC; in MIPS_DV_MODE only

Table 8.3: Parameters that can be set in: CPU

## 8.2 Parameter values

These are the current parameter values.

Name	Value
(Others)	
endian	none

cacheenable	default
cachedebug	0
cacheextbiuinfo	0x0
mipsHexFile	
IMPERAS_MIPS_AVP_OPCODES	F
cacheIndexBypassTLB	F
MIPS_TRACE	F
gprNames	F
supervisorMode	F
busErrors	T
fixedMMU	F
fixedDbgRegSize	F
removeDSP	F
removeCMP	F
removeFP	F
removeFTLB	F
isISA	F
hiddenTLBentries	F
perfCounters	0
ITCNumEntries	0
ITCNumFIFO	0
ITCFIFODepth	0
ITCEmptyOnReset	F
MTFPU	0
supportDenormals	F
VPE0MaxTC	0
VPE1MaxTC	0
segBits	0
mpuRegions	0
mpuType	0
mpuEnable	F
mpuSegment0	0
mpuSegment1	0
mpuSegment2	0
mpuSegment3	0
mpuSegment4	0
mpuSegment5	0
mpuSegment6	0
mpuSegment7	0
mpuSegment8	0
mpuSegment9	0
mpuSegment10	0
mpuSegment11	0
mpuSegment12	0
mpuSegment13	0

mpuSegment14	0
mpuSegment15	0
mvpconf0vpe	0
tcDisable	0
vpeDisable	0
mvpconf0tc	0
mvpconf0pcp	F
mvpconf0tcp	F
mvpconf1c1f	F
mvpcontrolPolicyMode	F
hasFDC	0
licenseWarningDays	15
MIPS_UHI	F
mipsUhiArgs	I I
mipsUhiJail	
MIPS_DV_MODE	F
MIPS_MAGIC_OPCODES	F
	F
enableTrickbox	
fpuexcdisable TRU_PRESENT	F F
ucLLwordsLocked	0
FUSA	F
CPC_FAULT_SUPPORTED	0
CPC_FAULT_ENABLE	0
cop2Bits	32
cop2FileName	
udiConfig	0
udiFileName	
vectoredinterrupt	F
externalinterrupt	F
config3VEIC_VPE0	F
config3VEIC_VPE1	F
config3VEIC_VPE2	F
config3VEIC_VPE3	F
rootFixedMMU	F
rootMMUSizeM1	0
srsctlHSS	0
firPS	0
firHas2008	0
usePreciseFpu	0
simulateLite	NONE
pridCompanyOptions	0
pridRevision	0
globalClusterNum	0
intctlIPTI	0

intctlIPPCI         0           mumWatch         0           maxVP         0           numVP         0           numVP         0           numVPtoStart         0           sharedTLBindex         0           xconfigSpecified         F           intctIIPTLCPU0_VP0         0           intctIIPTLCPU0_VP1         0           intctIIPTLCPU0_VP2         0           intctIIPTLCPU1_VP0         0           intctIIPTLCPU1_VP1         0           intctIIPTLCPU1_VP2         0           intctIIPTLCPU1_VP3         0           intctIIPTLCPU2_VP0         0           intctIIPTLCPU2_VP1         0           intctIIPTLCPU2_VP2         0           intctIIPTLCPU2_VP3         0           intctIIPTLCPU3_VP0         0           intctIIPTLCPU3_VP1         0           intctIIPTLCPU3_VP2         0           intctIIPTLCPU3_VP2         0           intctIIPTLCPU3_VP2         0           intctIIPTLCPU4_VP0         0           intctIIPTLCPU4_VP2         0           intctIIPTLCPU4_VP3         0           intctIIPTLCPU5_VP2         0           intctIIPTLCPU5_VP3<		
numWatch         0           maxVP         0           numVP         0           numVPtoStart         0           sharedTLBindex         0           xconfigSpecified         F           intctllPTI_CPU0_VP0         0           intctllPTI_CPU0_VP1         0           intctllPTI_CPU0_VP2         0           intctllPTI_CPU1_VP0         0           intctllPTI_CPU1_VP1         0           intctllPTI_CPU1_VP2         0           intctllPTI_CPU1_VP3         0           intctllPTI_CPU2_VP0         0           intctllPTI_CPU2_VP0         0           intctllPTI_CPU2_VP1         0           intctllPTI_CPU2_VP1         0           intctllPTI_CPU2_VP2         0           intctllPTI_CPU2_VP3         0           intctllPTI_CPU2_VP3         0           intctllPTI_CPU3_VP0         0           intctllPTI_CPU3_VP1         0           intctllPTI_CPU3_VP3         0           intctllPTI_CPU4_VP2         0           intctllPTI_CPU4_VP3         0           intctllPTI_CPU5_VP1         0           intctllPTI_CPU5_VP2         0           intctllPTI_CPU6_VP2         0 <td></td> <td>0</td>		0
maxVP         0           numVP         0           numVPtoStart         0           sharedTLBindex         0           xconfigSpecified         F           intctlIPTLCPU0_VP0         0           intctlIPTLCPU0_VP1         0           intctlIPTLCPU0_VP2         0           intctlIPTLCPU1_VP0         0           intctlIPTLCPU1_VP1         0           intctlIPTLCPU1_VP2         0           intctlIPTLCPU1_VP3         0           intctlIPTLCPU2_VP0         0           intctlIPTLCPU2_VP0         0           intctlIPTLCPU2_VP1         0           intctlIPTLCPU2_VP3         0           intctlIPTLCPU3_VP0         0           intctlIPTLCPU3_VP3         0           intctlIPTLCPU3_VP3         0           intctlIPTLCPU3_VP3         0           intctlIPTLCPU3_VP3         0           intctlIPTLCPU4_VP0         0           intctlIPTLCPU4_VP3         0           intctlIPTLCPU5_VP0         0           intctlIPTLCPU5_VP1         0           intctlIPTLCPU5_VP2         0           intctlIPTLCPU6_VP3         0           intctlIPTLCPU6_VP3         0		, v
numVP         0           sharedTLBindex         0           xconfigSpecified         F           intctlIPTLCPU0_VP0         0           intctlIPTLCPU0_VP1         0           intctlIPTLCPU0_VP2         0           intctlIPTLCPU0_VP3         0           intctlIPTLCPU1_VP0         0           intctlIPTLCPU1_VP1         0           intctlIPTLCPU1_VP2         0           intctlIPTLCPU1_VP3         0           intctlIPTLCPU2_VP0         0           intctlIPTLCPU2_VP0         0           intctlIPTLCPU2_VP1         0           intctlIPTLCPU2_VP2         0           intctlIPTLCPU2_VP3         0           intctlIPTLCPU2_VP3         0           intctlIPTLCPU3_VP3         0           intctlIPTLCPU3_VP3         0           intctlIPTLCPU3_VP3         0           intctlIPTLCPU4_VP3         0           intctlIPTLCPU4_VP3         0           intctlIPTLCPU5_VP0         0           intctlIPTLCPU5_VP2         0           intctlIPTLCPU6_VP1         0           intctlIPTLCPU6_VP2         0           intctlIPTLCPU6_VP3         0           intctlIPTLCPU7_VP0         0		_
numVPtoStart         0           sharedTLBindex         0           xconfigSpecified         F           intctlIPTI_CPU0_VP0         0           intctlIPTI_CPU0_VP1         0           intctlIPTI_CPU0_VP2         0           intctlIPTI_CPU1_VP0         0           intctlIPTI_CPU1_VP1         0           intctlIPTI_CPU1_VP2         0           intctlIPTI_CPU1_VP3         0           intctlIPTI_CPU2_VP0         0           intctlIPTI_CPU2_VP0         0           intctlIPTI_CPU2_VP1         0           intctlIPTI_CPU2_VP1         0           intctlIPTI_CPU2_VP2         0           intctlIPTI_CPU2_VP3         0           intctlIPTI_CPU2_VP3         0           intctlIPTI_CPU3_VP0         0           intctlIPTI_CPU3_VP2         0           intctlIPTI_CPU3_VP3         0           intctlIPTI_CPU4_VP2         0           intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CP		
sharedTLBindex xconfigSpecified intctIIPTI_CPU0_VP0 intctIIPTI_CPU0_VP1 intctIIPTI_CPU0_VP2 intctIIPTI_CPU0_VP3 intctIIPTI_CPU0_VP3 intctIIPTI_CPU1_VP0 intctIIPTI_CPU1_VP0 intctIIPTI_CPU1_VP1 intctIIPTI_CPU1_VP2 intctIIPTI_CPU1_VP3 intctIIPTI_CPU2_VP0 intctIIPTI_CPU2_VP0 intctIIPTI_CPU2_VP1 intctIIPTI_CPU2_VP2 intctIIPTI_CPU3_VP0 intctIIPTI_CPU3_VP0 intctIIPTI_CPU3_VP0 intctIIPTI_CPU3_VP1 intctIIPTI_CPU3_VP2 intctIIPTI_CPU3_VP3 intctIIPTI_CPU3_VP3 intctIIPTI_CPU3_VP3 intctIIPTI_CPU4_VP0 intctIIPTI_CPU4_VP0 intctIIPTI_CPU4_VP1 intctIIPTI_CPU4_VP2 intctIIPTI_CPU5_VP0 intctIIPTI_CPU5_VP0 intctIIPTI_CPU5_VP1 intctIIPTI_CPU5_VP2 intctIIPTI_CPU5_VP3 intctIIPTI_CPU6_VP0 intctIIPTI_CPU6_VP0 intctIIPTI_CPU6_VP0 intctIIPTI_CPU6_VP1 intctIIPTI_CPU6_VP2 intctIIPTI_CPU6_VP3 intctIIPTI_CPU6_VP3 intctIIPTI_CPU6_VP3 intctIIPTI_CPU6_VP3 intctIIPTI_CPU7_VP0 intctIIPTI_CPU7_VP0 intctIIPTI_CPU7_VP0 intctIIPTI_CPU7_VP1 intctIIPTI_CPU7_VP2 intctIIPTI_CPU7_VP3 intctIIPTI_CPU7_VP3 intctIIPTI_CPU7_VP3 intctIIPFDC_CPU0_VP0 intctIIPFDC_CPU0_VP0 intctIIPFDC_CPU0_VP0 intctIIPFDC_CPU0_VP0		
xconfigSpecified intctllPTI_CPU0_VP0 intctllPTI_CPU0_VP1 intctllPTI_CPU0_VP2 intctllPTI_CPU0_VP3 intctllPTI_CPU1_VP0 intctllPTI_CPU1_VP0 intctllPTI_CPU1_VP1 intctllPTI_CPU1_VP2 intctllPTI_CPU1_VP3 intctllPTI_CPU2_VP0 intctllPTI_CPU2_VP0 intctllPTI_CPU2_VP1 intctllPTI_CPU2_VP2 intctllPTI_CPU3_VP0 intctllPTI_CPU3_VP0 intctllPTI_CPU3_VP0 intctllPTI_CPU3_VP0 intctllPTI_CPU3_VP0 intctllPTI_CPU3_VP1 intctllPTI_CPU3_VP2 intctllPTI_CPU3_VP2 intctllPTI_CPU3_VP3 intctllPTI_CPU4_VP0 intctllPTI_CPU4_VP0 intctllPTI_CPU4_VP1 intctllPTI_CPU4_VP2 intctllPTI_CPU4_VP3 intctllPTI_CPU5_VP0 intctllPTI_CPU5_VP0 intctllPTI_CPU5_VP1 intctllPTI_CPU5_VP2 intctllPTI_CPU5_VP2 intctllPTI_CPU6_VP0 intctllPTI_CPU6_VP0 intctllPTI_CPU6_VP0 intctllPTI_CPU6_VP0 intctllPTI_CPU6_VP1 intctllPTI_CPU6_VP2 intctllPTI_CPU6_VP3 intctllPTI_CPU6_VP3 intctllPTI_CPU7_VP0 intctllPTI_CPU7_VP0 intctllPTI_CPU7_VP0 intctllPTI_CPU7_VP2 intctllPTI_CPU7_VP3 intctllPTI_CPU6_CPU0_VP0 intctllPFDC_CPU0_VP0 intctllPFDC_CPU0_VP0 intctllPFDC_CPU0_VP0 intctllPFDC_CPU0_VP2 intctllPFDC_CPU0_VP3 intctllPFDC_CPU0_VP3 intctllPFDC_CPU0_VP3 intctllPFDC_CPU0_VP3 intctllPFDC_CPU0_VP3		0
intctllPTI_CPU0_VP0 intctllPTI_CPU0_VP1 intctllPTI_CPU0_VP2 intctllPTI_CPU0_VP3 intctllPTI_CPU1_VP0 intctllPTI_CPU1_VP0 intctllPTI_CPU1_VP1 intctllPTI_CPU1_VP2 intctllPTI_CPU1_VP3 intctllPTI_CPU1_VP3 intctllPTI_CPU2_VP0 intctllPTI_CPU2_VP0 intctllPTI_CPU2_VP1 intctllPTI_CPU3_VP0 intctllPTI_CPU3_VP0 intctllPTI_CPU3_VP1 intctllPTI_CPU3_VP2 intctllPTI_CPU3_VP3 intctllPTI_CPU3_VP3 intctllPTI_CPU3_VP3 intctllPTI_CPU4_VP0 intctllPTI_CPU4_VP0 intctllPTI_CPU4_VP1 intctllPTI_CPU4_VP2 intctllPTI_CPU4_VP3 intctllPTI_CPU4_VP3 intctllPTI_CPU4_VP3 intctllPTI_CPU5_VP0 intctllPTI_CPU5_VP0 intctllPTI_CPU5_VP1 intctllPTI_CPU5_VP2 intctllPTI_CPU6_VP0 intctllPTI_CPU6_VP0 intctllPTI_CPU6_VP1 intctllPTI_CPU6_VP2 intctllPTI_CPU6_VP3 intctllPTI_CPU6_VP3 intctllPTI_CPU6_VP0 intctllPTI_CPU6_VP3 intctllPTI_CPU7_VP0 intctllPTI_CPU7_VP0 intctllPTI_CPU7_VP1 intctllPTI_CPU7_VP2 intctllPTI_CPU7_VP3 intctllPTI_CPU7_VP3 intctllPTI_CPU0_VP0 intctllPTI_CPU0_VP0 intctllPTI_CPU0_VP0 intctllPTI_CPU0_VP0 intctllPTI_CPU0_VP0 intctllPTD_CCPU0_VP0 intctllPFDC_CPU0_VP0 intctllPFDC_CPU0_VP0 intctllPFDC_CPU0_VP2 intctllPFDC_CPU0_VP3 intctllPFDC_CPU0_VP3 intctllPFDC_CPU0_VP3	sharedTLBindex	0
intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU0_VP3 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP2 intctlIPTI_CPU1_VP3 intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP1 intctlIPTI_CPU2_VP2 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP1 intctlIPTI_CPU3_VP2 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP1 intctlIPTI_CPU4_VP2 intctlIPTI_CPU4_VP3 intctlIPTI_CPU4_VP3 intctlIPTI_CPU4_VP3 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP1 intctlIPTI_CPU5_VP2 intctlIPTI_CPU5_VP3 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP1 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP1 intctlIPTI_CPU7_VP1 intctlIPTI_CPU7_VP2 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPFD_C_CPU0_VP0 intctlIPFD_C_CPU0_VP0 intctlIPFD_C_CPU0_VP2 intctlIPFD_C_CPU0_VP3 intctlIPFD_C_CPU0_VP3 intctlIPFD_C_CPU0_VP3		F
intctlIPTI_CPU0_VP2 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP2 intctlIPTI_CPU1_VP3 intctlIPTI_CPU1_VP3 intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP1 intctlIPTI_CPU2_VP1 intctlIPTI_CPU2_VP2 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP1 intctlIPTI_CPU3_VP2 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP1 intctlIPTI_CPU4_VP2 intctlIPTI_CPU4_VP3 intctlIPTI_CPU4_VP3 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP1 intctlIPTI_CPU5_VP2 intctlIPTI_CPU6_VP2 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP1 intctlIPTI_CPU7_VP2 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPFD_C_CPU0_VP0 intctlIPFD_C_CPU0_VP0 intctlIPFD_C_CPU0_VP2 intctlIPFD_C_CPU0_VP3 intctlIPFD_C_CPU0_VP3 intctlIPFD_C_CPU0_VP3 intctlIPFD_C_CPU0_VP3		0
intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP2 intctlIPTI_CPU1_VP3 intctlIPTI_CPU1_VP3 intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP1 intctlIPTI_CPU2_VP2 intctlIPTI_CPU2_VP3 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP1 intctlIPTI_CPU3_VP2 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP1 intctlIPTI_CPU4_VP2 intctlIPTI_CPU4_VP3 intctlIPTI_CPU4_VP3 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP1 intctlIPTI_CPU5_VP3 intctlIPTI_CPU5_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP1 intctlIPTI_CPU6_VP2 intctlIPTI_CPU6_VP2 intctlIPTI_CPU6_VP3 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP1 intctlIPTI_CPU7_VP2 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU0_VP0 intctlIPTD_CPU0_VP0 intctlIPFDC_CPU0_VP0 intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3	intctlIPTI_CPU0_VP1	0
intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP2 intctlIPTI_CPU1_VP3 intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP1 intctlIPTI_CPU2_VP2 intctlIPTI_CPU2_VP3 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP1 intctlIPTI_CPU3_VP2 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP2 intctlIPTI_CPU4_VP3 intctlIPTI_CPU4_VP3 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP1 intctlIPTI_CPU5_VP2 intctlIPTI_CPU5_VP3 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP1 intctlIPTI_CPU6_VP2 intctlIPTI_CPU6_VP3 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP1 intctlIPTI_CPU7_VP2 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP0 intctlIPTD_CPU0_VP1 intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3	intctlIPTI_CPU0_VP2	0
intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP2 intctlIPTI_CPU1_VP3 intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP1 intctlIPTI_CPU2_VP1 intctlIPTI_CPU2_VP2 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP1 intctlIPTI_CPU3_VP2 intctlIPTI_CPU3_VP2 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP1 intctlIPTI_CPU4_VP2 intctlIPTI_CPU4_VP3 intctlIPTI_CPU4_VP3 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP1 intctlIPTI_CPU5_VP2 intctlIPTI_CPU5_VP3 intctlIPTI_CPU5_VP3 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP1 intctlIPTI_CPU6_VP2 intctlIPTI_CPU6_VP3 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP1 intctlIPTI_CPU7_VP2 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU0_VP0 intctlIPFDC_CPU0_VP0 intctlIPFDC_CPU0_VP0 intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3	intctlIPTI_CPU0_VP3	0
intctlIPTI_CPU1_VP3 intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP1 intctlIPTI_CPU2_VP1 intctlIPTI_CPU2_VP2 intctlIPTI_CPU2_VP3 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP1 intctlIPTI_CPU3_VP2 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP1 intctlIPTI_CPU4_VP2 intctlIPTI_CPU4_VP3 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP1 intctlIPTI_CPU5_VP2 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP1 intctlIPTI_CPU6_VP2 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP1 intctlIPTI_CPU7_VP2 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTD_CPU0_VP0 intctlIPFDC_CPU0_VP1 intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3	intctlIPTI_CPU1_VP0	0
intctlIPTI_CPU1_VP3 intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP1 intctlIPTI_CPU2_VP2 intctlIPTI_CPU2_VP3 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP1 intctlIPTI_CPU3_VP2 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP1 intctlIPTI_CPU4_VP2 intctlIPTI_CPU4_VP3 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP1 intctlIPTI_CPU5_VP2 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP1 intctlIPTI_CPU6_VP2 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP1 intctlIPTI_CPU7_VP2 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP1 intctlIPTI_CPU7_VP3 intctlIPFDC_CPU0_VP0 intctlIPFDC_CPU0_VP1 intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3	intctlIPTI_CPU1_VP1	0
intctlIPTI_CPU2_VP0 intctlIPTI_CPU2_VP2 intctlIPTI_CPU2_VP3 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP0 intctlIPTI_CPU3_VP1 intctlIPTI_CPU3_VP2 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU3_VP3 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP0 intctlIPTI_CPU4_VP2 intctlIPTI_CPU4_VP3 intctlIPTI_CPU5_VP0 intctlIPTI_CPU5_VP1 intctlIPTI_CPU5_VP2 intctlIPTI_CPU5_VP3 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP0 intctlIPTI_CPU6_VP1 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU6_VP3 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP0 intctlIPTI_CPU7_VP1 intctlIPTI_CPU7_VP2 intctlIPTI_CPU7_VP3 intctlIPTI_CPU7_VP3 intctlIPTD_CPU0_VP0 intctlIPFDC_CPU0_VP0 intctlIPFDC_CPU0_VP1 intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3	intctlIPTI_CPU1_VP2	0
intctlIPTI_CPU2_VP2         0           intctlIPTI_CPU2_VP3         0           intctlIPTI_CPU3_VP0         0           intctlIPTI_CPU3_VP1         0           intctlIPTI_CPU3_VP2         0           intctlIPTI_CPU3_VP3         0           intctlIPTI_CPU4_VP0         0           intctlIPTI_CPU4_VP1         0           intctlIPTI_CPU4_VP2         0           intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU1_VP3	0
intctlIPTI_CPU2_VP3         0           intctlIPTI_CPU3_VP0         0           intctlIPTI_CPU3_VP1         0           intctlIPTI_CPU3_VP2         0           intctlIPTI_CPU3_VP3         0           intctlIPTI_CPU4_VP0         0           intctlIPTI_CPU4_VP1         0           intctlIPTI_CPU4_VP2         0           intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU2_VP0	0
intctlIPTI_CPU2_VP3         0           intctlIPTI_CPU3_VP0         0           intctlIPTI_CPU3_VP1         0           intctlIPTI_CPU3_VP2         0           intctlIPTI_CPU3_VP3         0           intctlIPTI_CPU4_VP0         0           intctlIPTI_CPU4_VP1         0           intctlIPTI_CPU4_VP2         0           intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU2_VP1	0
intctlIPTI_CPU3_VP1         0           intctlIPTI_CPU3_VP2         0           intctlIPTI_CPU3_VP3         0           intctlIPTI_CPU4_VP0         0           intctlIPTI_CPU4_VP1         0           intctlIPTI_CPU4_VP2         0           intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU2_VP2	0
intctlIPTLCPU3_VP2         0           intctlIPTLCPU3_VP3         0           intctlIPTLCPU4_VP0         0           intctlIPTLCPU4_VP1         0           intctlIPTLCPU4_VP2         0           intctlIPTLCPU4_VP3         0           intctlIPTLCPU5_VP0         0           intctlIPTLCPU5_VP1         0           intctlIPTLCPU5_VP2         0           intctlIPTLCPU5_VP3         0           intctlIPTLCPU6_VP0         0           intctlIPTLCPU6_VP1         0           intctlIPTLCPU6_VP2         0           intctlIPTLCPU6_VP3         0           intctlIPTLCPU7_VP0         0           intctlIPTLCPU7_VP1         0           intctlIPTLCPU7_VP2         0           intctlIPTLCPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU2_VP3	0
intctlIPTI_CPU3_VP3         0           intctlIPTI_CPU4_VP0         0           intctlIPTI_CPU4_VP1         0           intctlIPTI_CPU4_VP2         0           intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP3         0           intctlIPTD_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU3_VP0	0
intctlIPTI_CPU3_VP3         0           intctlIPTI_CPU4_VP0         0           intctlIPTI_CPU4_VP1         0           intctlIPTI_CPU4_VP2         0           intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU3_VP1	0
intctlIPTI_CPU4_VP1         0           intctlIPTI_CPU4_VP1         0           intctlIPTI_CPU4_VP2         0           intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPTDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU3_VP2	0
intctlIPTI_CPU4_VP2         0           intctlIPTI_CPU4_VP2         0           intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU3_VP3	0
intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU4_VP0	0
intctlIPTI_CPU4_VP3         0           intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU4_VP1	0
intctlIPTI_CPU5_VP0         0           intctlIPTI_CPU5_VP1         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU4_VP2	0
intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP2         0           intctlIPTI_CPU5_VP3         0           intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU4_VP3	0
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intctlIPTI_CPU6_VP0         0           intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0		0
intctlIPTI_CPU6_VP1         0           intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU5_VP3	0
intctlIPTI_CPU6_VP2         0           intctlIPTI_CPU6_VP3         0           intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU6_VP0	0
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intctlIPTI_CPU7_VP0         0           intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU6_VP2	0
intctlIPTI_CPU7_VP1         0           intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU6_VP3	0
intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU7_VP0	0
intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU7_VP1	0
intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0	intctlIPTI_CPU7_VP2	0
intctlIPFDC_CPU0_VP1 0 intctlIPFDC_CPU0_VP2 0 intctlIPFDC_CPU0_VP3 0		0
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intctlIPFDC_CPU0_VP3 0	intctlIPFDC_CPU0_VP1	0
	intctlIPFDC_CPU0_VP2	0
intctlIPFDC_CPU1_VP0 0	intctlIPFDC_CPU0_VP3	0
	intctlIPFDC_CPU1_VP0	0

intetlIPFDC_CPU1_VP2 intetlIPFDC_CPU1_VP3 intetlIPFDC_CPU2_VP0 intetlIPFDC_CPU2_VP1 intetlIPFDC_CPU2_VP2 intetlIPFDC_CPU2_VP2 intetlIPFDC_CPU2_VP3 intetlIPFDC_CPU3_VP0 intetlIPFDC_CPU3_VP0 intetlIPFDC_CPU3_VP1 intetlIPFDC_CPU3_VP2 intetlIPFDC_CPU3_VP2 intetlIPFDC_CPU3_VP3 intetlIPFDC_CPU3_VP3 intetlIPFDC_CPU4_VP0 intetlIPFDC_CPU4_VP0 intetlIPFDC_CPU4_VP1 intetlIPFDC_CPU4_VP2 intetlIPFDC_CPU4_VP3 intetlIPFDC_CPU4_VP3 intetlIPFDC_CPU5_VP0 intetlIPFDC_CPU5_VP1 intetlIPFDC_CPU5_VP2 intetlIPFDC_CPU5_VP2 intetlIPFDC_CPU5_VP3 intetlIPFDC_CPU5_VP3 intetlIPFDC_CPU6_VP0 intetlIPFDC_CPU6_VP0 intetlIPFDC_CPU6_VP1 intetlIPFDC_CPU6_VP2 intetlIPFDC_CPU6_VP2 intetlIPFDC_CPU6_VP3 intetlIPFDC_CPU6_VP3 intetlIPFDC_CPU7_VP0 intetlIPFDC_CPU7_VP0 intetlIPFDC_CPU7_VP1 intetlIPFDC_CPU7_VP3 intetlIPPCI_CPU0_VP3 intetlIPPCI_CPU0_VP3 intetlIPPCI_CPU0_VP3 intetlIPPCI_CPU0_VP3 intetlIPPCI_CPU1_VP0 intetlIPPCI_CPU0_VP3 intetlIPPCI_CPU1_VP0 intetlIPPCI_CPU1_VP0 intetlIPPCI_CPU1_VP0 intetlIPPCI_CPU1_VP1 intetlIPPCI_CPU1_VP2 intetlIPPCI_CPU1_VP3 intetlIPPCI_CPU1_VP3 intetlIPPCI_CPU2_VP3 intetlIPPCI_CPU2_VP1 intetlIPPCI_CPU3_VP1 intetlIPPCI_CPU3_VP2 intetlIPPCI_CPU3_VP1 intetlIPPCI_CPU3_VP2 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP4 intetlIPPCI_CPU4_VP0 intetlIPP	intctlIPFDC_CPU1_VP1	
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intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPPCL_CPU0_VP0 intctlIPPCL_CPU0_VP1 intctlIPPCL_CPU0_VP1 intctlIPPCL_CPU0_VP3 intctlIPPCL_CPU0_VP3 intctlIPPCL_CPU1_VP0 intctlIPPCL_CPU1_VP0 intctlIPPCL_CPU1_VP2 intctlIPPCL_CPU1_VP2 intctlIPPCL_CPU1_VP3 intctlIPPCL_CPU1_VP3 intctlIPPCL_CPU2_VP0 intctlIPPCL_CPU2_VP0 intctlIPPCL_CPU2_VP1 intctlIPPCL_CPU2_VP2 intctlIPPCL_CPU3_VP0 intctlIPPCL_CPU3_VP0 intctlIPPCL_CPU3_VP0 intctlIPPCL_CPU3_VP1 intctlIPPCL_CPU3_VP1 intctlIPPCL_CPU3_VP1 intctlIPPCL_CPU3_VP2 intctlIPPCL_CPU3_VP1 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU4_VP0 0	intctlIPFDC_CPU6_VP2	0
intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0           intctlIPPCI_CPU0_VP2         0           intctlIPPCI_CPU0_VP3         0           intctlIPPCI_CPU1_VP0         0           intctlIPPCI_CPU1_VP1         0           intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPFDC_CPU6_VP3	0
intctlIPFDC_CPU7_VP3         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0           intctlIPPCI_CPU0_VP2         0           intctlIPPCI_CPU0_VP3         0           intctlIPPCI_CPU1_VP0         0           intctlIPPCI_CPU1_VP1         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPFDC_CPU7_VP0	0
intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0           intctlIPPCI_CPU0_VP2         0           intctlIPPCI_CPU0_VP3         0           intctlIPPCI_CPU1_VP0         0           intctlIPPCI_CPU1_VP1         0           intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPFDC_CPU7_VP1	0
intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0           intctlIPPCI_CPU0_VP2         0           intctlIPPCI_CPU0_VP3         0           intctlIPPCI_CPU1_VP0         0           intctlIPPCI_CPU1_VP1         0           intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPFDC_CPU7_VP2	0
intctlIPPCI_CPU0_VP2         0           intctlIPPCI_CPU0_VP3         0           intctlIPPCI_CPU1_VP0         0           intctlIPPCI_CPU1_VP1         0           intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPFDC_CPU7_VP3	0
intctlIPPCI_CPU0_VP3         0           intctlIPPCI_CPU0_VP3         0           intctlIPPCI_CPU1_VP0         0           intctlIPPCI_CPU1_VP1         0           intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU0_VP0	0
intctlIPPCI_CPU0_VP3         0           intctlIPPCI_CPU1_VP0         0           intctlIPPCI_CPU1_VP1         0           intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU0_VP1	0
intctlIPPCI_CPU1_VP0         0           intctlIPPCI_CPU1_VP1         0           intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU0_VP2	0
intctlIPPCI_CPU1_VP1         0           intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU0_VP3	0
intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU1_VP0	0
intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU1_VP1	0
intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU1_VP2	0
intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU1_VP3	0
intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU2_VP0	0
intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU2_VP1	0
intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU2_VP2	0
intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU2_VP3	0
intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0	intctlIPPCI_CPU3_VP0	
intctlIPPCI_CPU3_VP2 0 intctlIPPCI_CPU3_VP3 0 intctlIPPCI_CPU4_VP0 0		
intctlIPPCI_CPU3_VP3 0 intctlIPPCI_CPU4_VP0 0		
intctlIPPCI_CPU4_VP0 0		

intctlIPPCI_CPU4_VP2	0
intctlIPPCI_CPU4_VP3	0
intctlIPPCI_CPU5_VP0	0
intctlIPPCI_CPU5_VP1	0
intctlIPPCI_CPU5_VP2	0
intctlIPPCI_CPU5_VP3	0
intctlIPPCI_CPU6_VP0	0
intctlIPPCI_CPU6_VP1	0
intctlIPPCI_CPU6_VP2	0
intctlIPPCI_CPU6_VP3	0
intctlIPPCI_CPU7_VP0	0
intctlIPPCI_CPU7_VP1	0
intctlIPPCI_CPU7_VP2	0
intctlIPPCI_CPU7_VP3	0
segcfg0PA	0
segcfg1PA	0
segcfg2PA	0
segcfg3PA	0
segcfg4PA	0
segcfg5PA	0
segcfg0AM	0
segcfg1AM	0
segcfg2AM	0
segcfg3AM	0
segcfg4AM	0
segcfg5AM	0
segcfg0EU	0
segcfg1EU	0
segcfg2EU	0
segcfg3EU	0
segcfg4EU	0
segcfg5EU	0
segcfg0C	0
segcfg1C	0
segcfg2C	0
segcfg3C	0
segcfg4C	0
segcfg5C	0
cdmmSize	0
configAR	0
configBM	0
configDSP	F
configISP	F
configK0	0
configKU	0
0**	J

C IZO2	
configK23	0
configMDU	F
configMM	F
configMT	0
configSB	F
configBCP	F
MIPS16eASE	F
config1DA	0
config1DL	0
config1DS	0
config1EP	F
config1IA	0
config1IL	0
config1IS	0
config1MMUSizeM1	0
config1MMUSizeM1_VPE1	0
config1MMUSizeM1_VPE2	0
config1MMUSizeM1_VPE3	0
config1WR	F
config1PC	F
config1C2	F
config2SU	0
config2SS	0
config2SL	0
config2SA	0
config3BI	F
config3BP	F
config3CDMM	F
config3CTXTC	F
config3DSPP	F
config3DSP2P	F
config3IPLW	0
config3ISA	0
config3ISAOnExc	F
config3ITL	F
config3LPA	F
config3MCU	F
config3MMAR	0
config3RXI	F
config3SC	F
config3ULRI	F
config3VZ	F
config3MSAP	F
config3CMGCR	F
config3SP	F
comigosi	Γ

config3TL	0
config3PW	F
config4AE	F
config4IE	0
config4MMUConfig	0
config4MMUExtDef	0
config4VTLBSizeExt	0
config4KScrExist	0
config5EVA	F
config5LLB	F
config5MRP	F
config5NFExists	F
mips32Macro	F
config5MSAEn	F
config5MVH	F
config5DEC	F
config5GI	0
config5CRCP	F
config5VP	F
config6FTLBEn	F
config7AR	F
config7DCIDX_MODE	0
config7HCI	F
config7IAR	F
config7WII	F
config7ES	0
config7WR	F
config7FPR	F
config7USP	0
config7BTLM	F
config7BusSlp	F
config7IVAD	F
config7RPS	F
config7IAR_CPU0_VPE0	F
config7IAR_CPU0_VPE1	F
config7IAR_CPU0_VPE2	F
config7IAR_CPU0_VPE3	F
config7IAR_CPU1_VPE0	F
config7IAR_CPU1_VPE1	F
config7IAR_CPU1_VPE2	F
config7IAR_CPU1_VPE3	F
config7IAR_CPU2_VPE0	F
config7IAR_CPU2_VPE1	F
config7IAR_CPU2_VPE2	F
config7IAR_CPU2_VPE3	F

config7IAR_CPU3_VPE0	F
config7IAR_CPU3_VPE1	F
config7IAR_CPU3_VPE2	F
config7IAR_CPU3_VPE3	F
config7IAR_CPU4_VPE0	F
config7IAR_CPU4_VPE1	F
config7IAR_CPU4_VPE2	F
config7IAR_CPU4_VPE3	F
config7IAR_CPU5_VPE0	F
config7IAR_CPU5_VPE1	F
config7IAR_CPU5_VPE2	F
config7IAR_CPU5_VPE3	F
config7IAR_CPU6_VPE0	F
config7IAR_CPU6_VPE1	F
config7IAR_CPU6_VPE2	F
config7IAR_CPU6_VPE3	F
config7IAR_CPU7_VPE0	F
config7IAR_CPU7_VPE1	F
config7IAR_CPU7_VPE2	F
config7IAR_CPU7_VPE3	F
config7IVAD_CPU0_VPE0	F
config7IVAD_CPU0_VPE1	F
config7IVAD_CPU0_VPE2	F
config7IVAD_CPU0_VPE3	F
config7IVAD_CPU1_VPE0	F
config7IVAD_CPU1_VPE1	F
config7IVAD_CPU1_VPE2	F
config7IVAD_CPU1_VPE3	F
config7IVAD_CPU2_VPE0	F
config7IVAD_CPU2_VPE1	F
config7IVAD_CPU2_VPE2	F
config7IVAD_CPU2_VPE3	F
config7IVAD_CPU3_VPE0	F
config7IVAD_CPU3_VPE1	F
config7IVAD_CPU3_VPE2	F
config7IVAD_CPU3_VPE3	F
config7IVAD_CPU4_VPE0	F
config7IVAD_CPU4_VPE1	F
config7IVAD_CPU4_VPE2	F
config7IVAD_CPU4_VPE3	F
config7IVAD_CPU5_VPE0	F
config7IVAD_CPU5_VPE1	F
config7IVAD_CPU5_VPE2	F
config7IVAD_CPU5_VPE3	F
config7IVAD_CPU6_VPE0	F

config7IVAD_CPU6_VPE2 config7IVAD_CPU6_VPE3 config7IVAD_CPU7_VPE0 config7IVAD_CPU7_VPE1 config7IVAD_CPU7_VPE2	F F F F F
config7IVAD_CPU6_VPE3 config7IVAD_CPU7_VPE0 config7IVAD_CPU7_VPE1 config7IVAD_CPU7_VPE2	F F
config7IVAD_CPU7_VPE0 config7IVAD_CPU7_VPE1 config7IVAD_CPU7_VPE2	F F
config7IVAD_CPU7_VPE1	F
config7IVAD_CPU7_VPE2	
9	Η.
6 HILLAD CIDILE LIDES	
8	F
0	F
0	F
0	F
0	F
0	F
8	F
0	F
0	F
0	F
8	F
9	F
0	F
config7RPS_CPU3_VPE0	F
config7RPS_CPU3_VPE1	F
config7RPS_CPU3_VPE2	F
config7RPS_CPU3_VPE3	F
config7RPS_CPU4_VPE0	F
8	F
config7RPS_CPU4_VPE2	F
config7RPS_CPU4_VPE3	F
0	F
config7RPS_CPU5_VPE1	F
0	F
0	F
config7RPS_CPU6_VPE0	F
config7RPS_CPU6_VPE1	F
0	F
config7RPS_CPU6_VPE3	F
config7RPS_CPU7_VPE0	F
config7RPS_CPU7_VPE1	F
config7RPS_CPU7_VPE2	F
config7RPS_CPU7_VPE3	F
	F
fcsrABS2008	F
fcsrNAN2008	F
numMaarRegs	6
srsconf0SRS1	0
srsconf0SRS2	0

srsconf0SRS3	0
wiredLimit	0
wiredLimitBits	0
wiredWiredBits	0
cdmmBaseCI	F
parityEnable	1
useMpTb	T
ExceptionBase	0
UseExceptionBase	F
11BufferCache	F
GCU_EX	F
GIC-EX	F
CPC_EX	F
TIMER_ROUTABLE	F
SWINT_ROUTABLE	F
PERFCNT_ROUTABLE	F
FDC_ROUTABLE	F
GCR_PCORES	0
GCR_ADDR_REGIONS	0
GCR_NUMAUX	0
GCR_BASE	0
GCR_MINOR_REV	, ,
GCR_MAJOR_REV	0
GCR_CACHE_MINOR_REV	0
GCR_CACHE_MAJOR_REV	0
GCR_L2_ASSOC	0
GCR_L2_SET_SIZE	0
GCR_SYS_CONFIG2_MAX_VP_WIDTH	0
GCR_IOCU1_MINOR_REV	0
GCR_IOCU1_MAJOR_REV	0
GCR_BEV_BASE	0
GCR_KX_BASE_MODE	F
GCR_MMIO_REQ_LIMIT	0
GCR_MMIO0_BOTTOM	0
GCR_MMIO0_BOTTOM  GCR_MMIO0_TOP_ADDR	0
GCR_MMIO1_BOTTOM	0
GCR_MMIO1_BO11OM  GCR_MMIO1_TOP_ADDR	0
GCR_MMIO2_BOTTOM	0
GCR_MMIO2_BOTTOM  GCR_MMIO2_TOP_ADDR	0
GCR_MMIO3_BOTTOM	0
GCR_MMIO3_BOT TOM GCR_MMIO3_TOP_ADDR	0
GIC_NUMINTERRUPTS	0
GIC_COUNTBITS	0
GIC_COUNTBITS GIC_MINOR_REV	0
GIC_MINOR_REV GIC_MAJOR_REV	0
GIO_IVIAJOR_RE V	U

GIC_NUM_TEAMS	7
GIC_TRIG_RESET	0
GIC_PVPES	0
CPC_MICROSTEP	0
CPC_RAILDELAY	0
CPC_RESETLEN	0
CPC_MINOR_REV	0
CPC_MAJOR_REV	0
GIC_SH_GID_CONFIG31_0	0
GIC_SH_GID_CONFIG63_32	0
GIC_SH_GID_CONFIG95_64	0
GIC_SH_GID_CONFIG127_96	0
GIC_SH_GID_CONFIG159_128	0
GIC_SH_GID_CONFIG191_160	0
GIC_SH_GID_CONFIG223_192	0
GIC_SH_GID_CONFIG255_224	0
gicVirtualVPNum_CPU0_VP0	0
gicVirtualVPNum_CPU0_VP1	0
gicVirtualVPNum_CPU0_VP2	0
gicVirtualVPNum_CPU0_VP3	0
gicVirtualVPNum_CPU1_VP0	0
gicVirtualVPNum_CPU1_VP1	0
gicVirtualVPNum_CPU1_VP2	0
gicVirtualVPNum_CPU1_VP3	0
gicVirtualVPNum_CPU2_VP0	0
gicVirtualVPNum_CPU2_VP1	0
gicVirtualVPNum_CPU2_VP2	0
gicVirtualVPNum_CPU2_VP3	0
gicVirtualVPNum_CPU3_VP0	0
gicVirtualVPNum_CPU3_VP1	0
gicVirtualVPNum_CPU3_VP2	0
gicVirtualVPNum_CPU3_VP3	0
gicVirtualVPNum_CPU4_VP0	0
gicVirtualVPNum_CPU4_VP1	0
gicVirtualVPNum_CPU4_VP2	0
gicVirtualVPNum_CPU4_VP3	0
gicVirtualVPNum_CPU5_VP0	0
gicVirtualVPNum_CPU5_VP1	0
gicVirtualVPNum_CPU5_VP2	0
gicVirtualVPNum_CPU5_VP3	0
gicVirtualVPNum_CPU6_VP0	0
gicVirtualVPNum_CPU6_VP1	0
gicVirtualVPNum_CPU6_VP2	0
gicVirtualVPNum_CPU6_VP3	0
gicVirtualVPNum_CPU7_VP0	0

gicVirtualVPNum_CPU7_VP1	0
gicVirtualVPNum_CPU7_VP2	0
gicVirtualVPNum_CPU7_VP3	0
GCR_C0_RESET_BASE	0
GCR_C1_RESET_BASE	0
GCR_C2_RESET_BASE	0
GCR_C3_RESET_BASE	0
GCR_C4_RESET_BASE	0
GCR_C5_RESET_BASE	0
GCR_C6_RESET_BASE	0
GCR_C7_RESET_BASE	0
GCR_C8_RESET_BASE	0
GCR_C9_RESET_BASE	0
GCR_C0_RESET_EXT_BASE	0
GCR_C1_RESET_EXT_BASE	0
GCR_C2_RESET_EXT_BASE	0
GCR_C3_RESET_EXT_BASE	0
GCR_C4_RESET_EXT_BASE	0
GCR_C5_RESET_EXT_BASE	0
GCR_C6_RESET_EXT_BASE	0
GCR_C7_RESET_EXT_BASE	0
GCR_C8_RESET_EXT_BASE	0
GCR_C9_RESET_EXT_BASE	0
CPC_C0_VP_EN	0
CPC_C1_VP_EN	0
CPC_C2_VP_EN	0
CPC_C3_VP_EN	0
CPC_C4_VP_EN	0
CPC_C5_VP_EN	0
CPC_C6_VP_EN	0
CPC_C7_VP_EN	0
CPC_C8_VP_EN	0
CPC_C9_VP_EN	0
EIC_OPTION	2
guestCtl0RI	0
guestCtl0MC	0
guestCtl0CP0	0
guestCtl0AT	0
guestCtl0GT	0
guestCtl0CG	0
guestCtl0CF	0
guestCtl0G1	0
guestCtl0RAD	0
guestCtl0DRG	0
hasImpl17	F

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guestintctIIPTI_CPU6_VP1 0 guestintctIIPTI_CPU6_VP2 0 guestintctIIPTI_CPU6_VP3 0 guestintctIIPTI_CPU7_VP0 0 guestintctIIPTI_CPU7_VP1 0 guestintctIIPTI_CPU7_VP2 0 guestintctIIPTI_CPU7_VP2 0 guestintctIIPTI_CPU7_VP3 0 guestintctIIPFDC_CPU0_VP0 0 guestintctIIPFDC_CPU0_VP1 0 guestintctIIPFDC_CPU0_VP2 0 guestintctIIPFDC_CPU0_VP2 0 guestintctIIPFDC_CPU0_VP3 0 guestintctIIPFDC_CPU1_VP0 0 guestintctIIPFDC_CPU1_VP0 0 guestintctIIPFDC_CPU1_VP1 0 guestintctIIPFDC_CPU1_VP1 0 guestintctIIPFDC_CPU1_VP2 0 guestintctIIPFDC_CPU1_VP3 0	guestintctlIPTI_CPU5_VP3	0
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guestintctIIPTI_CPU6_VP3         0           guestintctIIPTI_CPU7_VP0         0           guestintctIIPTI_CPU7_VP1         0           guestintctIIPTI_CPU7_VP2         0           guestintctIIPTI_CPU7_VP3         0           guestintctIIPFDC_CPU0_VP0         0           guestintctIIPFDC_CPU0_VP1         0           guestintctIIPFDC_CPU0_VP2         0           guestintctIIPFDC_CPU0_VP3         0           guestintctIIPFDC_CPU1_VP0         0           guestintctIIPFDC_CPU1_VP1         0           guestintctIIPFDC_CPU1_VP2         0           guestintctIIPFDC_CPU1_VP3         0		0
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guestintctIIPTI_CPU7_VP2 0 guestintctIIPTI_CPU7_VP3 0 guestintctIIPFDC_CPU0_VP0 0 guestintctIIPFDC_CPU0_VP1 0 guestintctIIPFDC_CPU0_VP2 0 guestintctIIPFDC_CPU0_VP3 0 guestintctIIPFDC_CPU1_VP0 0 guestintctIIPFDC_CPU1_VP0 0 guestintctIIPFDC_CPU1_VP1 0 guestintctIIPFDC_CPU1_VP1 0 guestintctIIPFDC_CPU1_VP2 0 guestintctIIPFDC_CPU1_VP3 0	guestintctlIPTI_CPU7_VP0	0
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guestintctlIPFDC_CPU1_VP1 0 guestintctlIPFDC_CPU1_VP2 0 guestintctlIPFDC_CPU1_VP3 0		0
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guestintctlIPFDC_CPU2_VP1	0
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guestintctlIPFDC_CPU2_VP3	0
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guestintctlIPFDC_CPU3_VP2	0
guestintctlIPFDC_CPU3_VP3	0
guestintctlIPFDC_CPU4_VP0	0
guestintctlIPFDC_CPU4_VP1	0
guestintctlIPFDC_CPU4_VP2	0
guestintctlIPFDC_CPU4_VP3	0
guestintctlIPFDC_CPU5_VP0	0
guestintctlIPFDC_CPU5_VP1	0
guestintctlIPFDC_CPU5_VP2	0
guestintctlIPFDC_CPU5_VP3	0
guestintctlIPFDC_CPU6_VP0	0
guestintctlIPFDC_CPU6_VP1	0
guestintctlIPFDC_CPU6_VP2	0
guestintctlIPFDC_CPU6_VP3	0
guestintctlIPFDC_CPU7_VP0	0
guestintctlIPFDC_CPU7_VP1	0
guestintctlIPFDC_CPU7_VP2	0
guestintctlIPFDC_CPU7_VP3	0
guestintctlIPPCI_CPU0_VP0	0
guestintctlIPPCI_CPU0_VP1	0
guestintctlIPPCI_CPU0_VP2	0
guestintctlIPPCI_CPU0_VP3	0
guestintctlIPPCI_CPU1_VP0	0
guestintctlIPPCI_CPU1_VP1	0
guestintctlIPPCI_CPU1_VP2	0
guestintctlIPPCI_CPU1_VP3	0
guestintctlIPPCI_CPU2_VP0	0
guestintctlIPPCI_CPU2_VP1	0
guestintctlIPPCI_CPU2_VP2	0
guestintctlIPPCI_CPU2_VP3	0
guestintctlIPPCI_CPU3_VP0	0
guestintctlIPPCI_CPU3_VP1	0
guestintctlIPPCI_CPU3_VP2	0
guestintctlIPPCI_CPU3_VP3	0
guestintctlIPPCI_CPU4_VP0	0
guestintctlIPPCI_CPU4_VP1	0
guestintctlIPPCI_CPU4_VP2	0
guestintctlIPPCI_CPU4_VP3	0
guestintctlIPPCI_CPU5_VP0	0
guestintctlIPPCI_CPU5_VP1	0
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guestintctlIPPCI_CPU5_VP2	0
guestintctlIPPCI_CPU5_VP3	0
guestintctlIPPCI_CPU6_VP0	0
guestintctlIPPCI_CPU6_VP1	0
guestintctlIPPCI_CPU6_VP2	0
guestintctlIPPCI_CPU6_VP3	0
guestintctlIPPCI_CPU7_VP0	0
guestintctlIPPCI_CPU7_VP1	0
guestintctlIPPCI_CPU7_VP2	0
guestintctlIPPCI_CPU7_VP3	0
ISPRAM_SIZE	0
ISPRAM_BASE	0
ISPRAM_ENABLE	F
ISPRAM_FILE	
DSPRAM_SIZE	0
DSPRAM_BASE	0
DSPRAM_ENABLE	F
DSPRAM_PRESENT	F
USPRAM_SIZE	0
USPRAM_BASE	0
USPRAM_ENABLE	F
USPRAM_FILE	
misalignedDataException	never
commitTlbwErr	F

Table 8.4: Parameter values

Name	Type	Description
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info struc-
		ture
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
		(specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB
		exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
gprNames	Boolean	Disassemble the register names from the default
		ABI instead of register numbers for MIPS-format
		trace output
supervisorMode	Boolean	Override whether processor implements supervisor
		mode
busErrors	Boolean	Override bus error exception behavior. When true,
		accesses of memory not defined by platform will
		cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when
		true (sets Config.MT=3, Config.KU/K23=2 and
		Config1.MMUSizeM1=0)

fixedDbgRegSize	Boolean	Enable applications to debug on P5600 with GDB
		version 2015.06-05 and prior
removeDSP	Boolean	Override the DSP-present configuration when true
		(sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true
		(sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true
		(sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true
		(disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from
		ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to
40	***	maximum value to improve performance
perfCounters	Uns32	Performance Counters
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores
IECNI DIEC	11 90	only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC
ITCFIFODepth	Uns32	implementation (MT cores only)  Specify ITC FIFO cell depth. By default supports
ПСтгорери	Ulis52	Specify 11C F1FO cell depth. By default supports 4.
ITCEmptyOnReset	Boolean	Specify ITC E/F cells reset to a known empty state.
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior,
WIIIO	011852	2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal
supportDenormals	Doolean	operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0. Ig-
VIEGWAXIO	0 11502	nored if less than two VPEs configured.
VPE1MaxTC	Uns32	Specifies the maximum TCs initially on VPE1. Ig-
V1 211110011 0	0111002	nored if less than three VPEs configured.
segBits	Uns32	Override the number of address bits implemented
		for 64 bit segments (MIPS64 Only)
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentCon-
		trol_0 register
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentCon-
		trol_0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentCon-
		trol_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentCon-
		trol_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentCon-
		trol_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentCon-
		trol_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentCon-
C	77 00	trol_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentCon-
g	*** ***	trol_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentCon-
2 10	77 00	trol_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentCon-
	TT 00	trol_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentCon-
		trol_2 register

Une32	Attributes for segment 11 in MPU2 SegmentCon-
011552	trol.2 register
Uns32	Attributes for segment 12 in MPU2 SegmentCon-
011392	trol.3 register
Uns32	Attributes for segment 13 in MPU2 SegmentCon-
0 11592	trol-3 register
Uns32	Attributes for segment 14 in MPU2 SegmentCon-
0 11502	trol.3 register
Uns32	Attributes for segment 15 in MPU2 SegmentCon-
011302	trol_3 register
Uns32	Override MVPConf0.PVPE
	Number of disabled TCs
	Number of disabled VPEs
	Override MVPConf0.PTC
	Override MVPConf0.PCP
	Override MVPConf0.TCP
	Override MVPConf.C1F
	Override MVPControl.POLICY_MODE
	Specify the size of Fast Debug Channel register
011302	block
Hng32	Specify the number of days before a license expires
011302	to start issuing a warning. 0 disables warnings.
Boolean	Enable MIPS-Unified Hosting interface
	Specifies UHI arguments string separated by spaces
	Specifies UHI jailroot
	Enable Design Verification mode
	Enable MIPS-specific magic Pass/Fail opcodes
	Enable trickbox addresses (specific for AVP)
	Disable FPU exceptions
	Disable or Enable based on TRU presence to con-
Doolean	trol certain fields (e.x.perfCtl.PCTD
Hng32	Numbers of words (4 byte) an uncached LL is lock-
Ulis52	ing. Maximum: 4K
Boolean	Enable Functional Safety
	Specify the value for Functional Safety Supported
Ulis52	register
Hng32	Specify the value for Functional Safety Enable reg-
011502	ister
Uns32	Specifies width in bits of COP2 registers (32 or 64)
	Specifies COP2 dynamically-loaded object
String	(.so/.dll) defining COP2 instructions
Int32	Specifies UDI configuration attribute
	Specifies UDI dynamically-loaded object (.so/.dll)
String	defining UDI instructions
Boolean	Enables vectored interrupts (sets Config3 VInt)
	Enables the use of an external interrupt controller
Boolean	(sets Config3 VEIC)
Boolean	Enables an external interrupt controller on VPE0
Doolcan	(sets Config3 VEIC)
	I LOUD COMIED VINCI
Roologn	
Boolean	Enables an external interrupt controller on VPE1
	Enables an external interrupt controller on VPE1 (sets Config3 VEIC)
Boolean  Boolean	Enables an external interrupt controller on VPE1 (sets Config3 VEIC)  Enables an external interrupt controller on VPE2
	Enables an external interrupt controller on VPE1 (sets Config3 VEIC)
	Uns32

rootFixedMMU	Boolean	Override the root MMU type to fixed map-
		ping when true (sets Config.MT=3 and Con-
		fig.KU/K23=2)
rootMMUSizeM1	Uns32	Override the root MMUSizeM1 field in Config1 reg-
		ister (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number
		of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
usePreciseFpu	Uns32	Use the precise Floating Point emulation
simulateLite	Enumeration	Run Simulation with optimization. There are
		several optimizations which coule be combined
		(NONE, FS, MA or FSMA)
pridCompanyOptions	Uns32	Override the Company Options field in PRId reg-
		ister
pridRevision	Uns32	Override the Revision field in PRId register
globalClusterNum	Uns32	Override the ClusterNum field in GlobalNumber
		register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intctlIPFDC	Uns32	Override the IPFDC field in IntCtl register
intctlIPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
maxVP	Uns32	Specify maximum number of Virtual Processors
		present in a core
numVP	Uns32	Specify number of Virtual Processors to be present
numVPtoStart	Uns32	Specify number of Virtual Processors to be started
$\operatorname{sharedTLBindex}$	Uns32	Specify first shared TLB Index between Virtual
		Cores
xconfigSpecified	Boolean	True if the configuration comes from a valid xconfig file
intctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
intctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for
	0 0	CPU0/VP1
intctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for
		CPU0/VP2
intctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for
		CPU0/VP3
intctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for
		CPU1/VP0
intctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for
		CPU1/VP1
intctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for
		CPU1/VP2
intctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for
		CPU1/VP3
intctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for
		CPU2/VP0
intctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
intctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for
		CPU2/VP2
intctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for
		CPU2/VP3
intctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for
		CPU3/VP0

intctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
intctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
intctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
intctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
intctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
intctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
intctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
intctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
intctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
intctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
intctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
intctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
intctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
intctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
intctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
intctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
intctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
intctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
intctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
intctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
intctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
intctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
intctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
intctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
intctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
intctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
intctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
intctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0

intctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
intctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
intctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
intctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
intctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
intctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
intctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
intctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
intctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
intctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
intctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
intctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
intctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
intctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
intctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
intctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
intctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
intctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
intctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
intctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
intctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
intctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
intctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
intctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
intctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
intctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
intctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
intctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0

intctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for
A DEPOS OF SERVICE	77. 00	CPU1/VP1
intctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
intctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
intctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
intctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
intctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
intctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
intctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
intctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
intctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
intctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
intctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
intctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
intctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
intctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
intctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
intctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
intctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
intctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
intctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
intctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
intctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
intctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
intctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
intctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
intctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
intctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
segcfg0PA	Uns32	Set CFG0.PA field of SegCtl0 register
segcfg1PA	Uns32	Set CFG1.PA field of SegCtl0 register
segcfg2PA	Uns32	Set CFG2.PA field of SegCtl1 register

C aDA	11 90	
segcfg3PA	Uns32	Set CFG3.PA field of SegCtl1 register
segcfg4PA	Uns32	Set CFG4.PA field of SegCtl2 register
segcfg5PA	Uns32	Set CFG5.PA field of SegCtl2 register
segcfg0AM	Uns32	Set CFG0.AM field of SegCtl0 register
segcfg1AM	Uns32	Set CFG1.AM field of SegCtl0 register
segcfg2AM	Uns32	Set CFG2.AM field of SegCtl1 register
segcfg3AM	Uns32	Set CFG3.AM field of SegCtl1 register
segcfg4AM	Uns32	Set CFG4.AM field of SegCtl2 register
segcfg5AM	Uns32	Set CFG5.AM field of SegCtl2 register
segcfg0EU	Uns32	Set CFG0.EU field of SegCtl0 register
segcfg1EU	Uns32	Set CFG1.EU field of SegCtl0 register
segcfg2EU	Uns32	Set CFG2.EU field of SegCtl1 register
segcfg3EU	Uns32	Set CFG3.EU field of SegCtl1 register
segcfg4EU	Uns32	Set CFG4.EU field of SegCtl2 register
segcfg5EU	Uns32	Set CFG5.EU field of SegCtl2 register
segcfg0C	Uns32	Set CFG0.C field of SegCtl0 register
segcfg1C	Uns32	Set CFG1.C field of SegCtl0 register
segcfg2C	Uns32	Set CFG2.C field of SegCtl1 register
segcfg3C	Uns32	Set CFG3.C field of SegCtl1 register
segcfg4C	Uns32	Set CFG4.C field of SegCtl2 register
segcig4C segcfg5C	Uns32	Set CFG5.C field of SegCtl2 register
cdmmSize	Uns32	Override the cdmmsize reset value
configAR	Uns32	Enables R6 support
		Override the BM field in Config register (burst
configBM	Uns32	mode)
configDSP	Dooloom	Override Config.DSP (data scratchpad RAM
CONTIGUESP	Boolean	, ,
C -ICD	D1	present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM
C 170	11 00	present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0
C TZII	11 00	cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg
0.7700	***	cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23
		cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide
		unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
configBCP	Boolean	Override Config.BCP (Buffer Cache Present)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Deache associativity)
config1DL	Uns32	Override Config1.DL (Dcache line size)
config1DS	Uns32	Override Config1.DS (Deache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU
		entries-1)
config1MMUSizeM1_VPE1	Uns32	Override Config1.MMUSizeM1 for VPE1
config1MMUSizeM1_VPE2	Uns32	Override Config1.MMUSizeM1 for VPE2
config1MMUSizeM1_VPE3	Uns32	Override Config1.MMUSizeM1 for VPE3
config1WR	Boolean	Override Config1.WR (watchpoint registers
Comigivit	Doolean	present)
		Property)

config1PC	Boolean	Override Config1.PC (Performance Counters present)
config1C2	Boolean	Override Config1.C2 (Coprocessor 2 present)
config2SU	Uns32	Override the SU field in Config2 register
config2SS	Uns32	Override the SS field in Config2 register
config2SL	Uns32	Override the SL field in Config2 register
config2SA	Uns32	Override the SA field in Config2 register
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.ITL Override Config3.LPA
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC		Override Configs.RAI Override Configs.SC
	Boolean	Override Configs.SC Override Configs.ULRI
config3ULRI config3VZ	Boolean Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3.VZ Override Config3.MSAP
config3CMGCR		
	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation
C AMMILE AD C	11 20	depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config4KScrExist	Uns32	Override Config4.KScrExist
config5EVA	Boolean	Override Config5.EVA
config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
mips32Macro	Boolean	Enables the MIPS32 SAVE and RESTORE macro
C MICAE	D 1	instructions. Ignored if Config5.CA2 is not set)
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and
a *DEG	D 1	MFHC0 instructions)
config5DEC	Boolean	Override Config5.DEC (to test Dual Endian Capability)
config5GI	Uns32	Override Config5.GI (enable GINV)
config5CRCP	Boolean	Override Config5.CRCP (CRCP Present)
config5VP	Boolean	Override Config5.VP
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initializa-
		tion)

config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (External-
		ize sync)
config7WR	Boolean	Override Config7[31] bit (Alternative implementa-
		tion of Watch registers)
config7FPR	Boolean	Override Config7.FPR (one-half FPU clock ratio)
config7USP	Uns32	Override Config7.USP (USPRAM enable)
config7BTLM	Boolean	Override Config7.BTLM bit
config7BusSlp	Boolean	Override Config7.BusSlp bit
config7IVAD	Boolean	Override Config7.IVAD bit
config7RPS	Boolean	Override Config7.RPS bit
config7IAR_CPU0_VPE0	Boolean	Override Config7.IAR bit for CPU0/VPE0
config7IAR_CPU0_VPE1	Boolean	Override Config7.IAR bit for CPU0/VPE1
config7IAR_CPU0_VPE2	Boolean	Override Config7.IAR bit for CPU0/VPE2
config7IAR_CPU0_VPE3	Boolean	Override Config7.IAR bit for CPU0/VPE3
config7IAR_CPU1_VPE0	Boolean	Override Config7.IAR bit for CPU1/VPE0
config7IAR_CPU1_VPE1 config7IAR_CPU1_VPE2	Boolean Boolean	Override Config7.IAR bit for CPU1/VPE1
config7IAR_CPU1_VPE2	Boolean	Override Config7.IAR bit for CPU1/VPE2 Override Config7.IAR bit for CPU1/VPE3
config7IAR_CPU1_VPE3	Boolean	Override Config7.IAR bit for CPU1/VPE3  Override Config7.IAR bit for CPU2/VPE0
config7IAR_CPU2_VPE1	Boolean	Override Config7.IAR bit for CPU2/VPE1
config7IAR_CPU2_VPE2	Boolean	Override Config7.IAR bit for CPU2/VPE2  Override Config7.IAR bit for CPU2/VPE2
config7IAR_CPU2_VPE3	Boolean	Override Config7.IAR bit for CPU2/VPE3
config7IAR_CPU3_VPE0	Boolean	Override Config7.IAR bit for CPU3/VPE0
config7IAR_CPU3_VPE1	Boolean	Override Config7.IAR bit for CPU3/VPE1
config7IAR_CPU3_VPE2	Boolean	Override Config7.IAR bit for CPU3/VPE2
config7IAR_CPU3_VPE3	Boolean	Override Config7.IAR bit for CPU3/VPE3
config7IAR_CPU4_VPE0	Boolean	Override Config7.IAR bit for CPU4/VPE0
config7IAR_CPU4_VPE1	Boolean	Override Config7.IAR bit for CPU4/VPE1
config7IAR_CPU4_VPE2	Boolean	Override Config7.IAR bit for CPU4/VPE2
config7IAR_CPU4_VPE3	Boolean	Override Config7.IAR bit for CPU4/VPE3
config7IAR_CPU5_VPE0	Boolean	Override Config7.IAR bit for CPU5/VPE0
config7IAR_CPU5_VPE1	Boolean	Override Config7.IAR bit for CPU5/VPE1
config7IAR_CPU5_VPE2	Boolean	Override Config7.IAR bit for CPU5/VPE2
config7IAR_CPU5_VPE3	Boolean	Override Config7.IAR bit for CPU5/VPE3
config7IAR_CPU6_VPE0	Boolean	Override Config7.IAR bit for CPU6/VPE0
config7IAR_CPU6_VPE1	Boolean	Override Config7.IAR bit for CPU6/VPE1
config7IAR_CPU6_VPE2	Boolean	Override Config7.IAR bit for CPU6/VPE2
config7IAR_CPU6_VPE3	Boolean	Override Config7.IAR bit for CPU6/VPE3
config7IAR_CPU7_VPE0	Boolean	Override Config7.IAR bit for CPU7/VPE0
config7IAR_CPU7_VPE1	Boolean	Override Config7.IAR bit for CPU7/VPE1
config7IAR_CPU7_VPE2	Boolean	Override Config7.IAR bit for CPU7/VPE2
config7IAR_CPU7_VPE3	Boolean	Override Config7.IAR bit for CPU7/VPE3
config7IVAD_CPU0_VPE0	Boolean	Override Config7.IVAD bit for CPU0/VPE0
config7IVAD_CPU0_VPE1	Boolean	Override Config7.IVAD bit for CPU0/VPE1
config7IVAD_CPU0_VPE2 config7IVAD_CPU0_VPE3	Boolean	Override Config7.IVAD bit for CPU0/VPE2 Override Config7.IVAD bit for CPU0/VPE3
config7IVAD_CPU1_VPE3	Boolean Boolean	Override Config7.IVAD bit for CPU0/VPE3  Override Config7.IVAD bit for CPU1/VPE0
config7IVAD_CPU1_VPE1	Boolean	Override Config7.IVAD bit for CPU1/VPE1  Override Config7.IVAD bit for CPU1/VPE1
config7IVAD_CPU1_VPE1	Boolean	Override Config7.IVAD bit for CPU1/VPE1 Override Config7.IVAD bit for CPU1/VPE2
config7IVAD_CPU1_VPE3	Boolean	Override Config7.IVAD bit for CPU1/VPE3  Override Config7.IVAD bit for CPU1/VPE3
config7IVAD_CPU2_VPE0	Boolean	Override Config7.IVAD bit for CPU2/VPE0
config7IVAD_CPU2_VPE1	Boolean	Override Config7.IVAD bit for CPU2/VPE1
config7IVAD_CPU2_VPE2	Boolean	Override Config7.IVAD bit for CPU2/VPE2

config7IVAD_CPU2_VPE3	Boolean	Override Config7.IVAD bit for CPU2/VPE3
config7IVAD_CPU3_VPE0	Boolean	Override Config7.IVAD bit for CPU3/VPE0
config7IVAD_CPU3_VPE1	Boolean	Override Config7.IVAD bit for CPU3/VPE1
config7IVAD_CPU3_VPE2	Boolean	Override Config7.IVAD bit for CPU3/VPE2
config7IVAD_CPU3_VPE3	Boolean	Override Config7.IVAD bit for CPU3/VPE3
config7IVAD_CPU4_VPE0	Boolean	Override Config7.IVAD bit for CPU4/VPE0
config7IVAD_CPU4_VPE1	Boolean	Override Config7.IVAD bit for CPU4/VPE1
config7IVAD_CPU4_VPE2	Boolean	Override Config7.IVAD bit for CPU4/VPE2
config7IVAD_CPU4_VPE3	Boolean	Override Config7.IVAD bit for CPU4/VPE3
config7IVAD_CPU5_VPE0	Boolean	Override Config7.IVAD bit for CPU5/VPE0
config7IVAD_CPU5_VPE1	Boolean	Override Config7.IVAD bit for CPU5/VPE1
config7IVAD_CPU5_VPE2	Boolean	Override Config7.IVAD bit for CPU5/VPE2
config7IVAD_CPU5_VPE3	Boolean	Override Config7.IVAD bit for CPU5/VPE3
config7IVAD_CPU6_VPE0	Boolean	Override Config7.IVAD bit for CPU6/VPE0
config7IVAD_CPU6_VPE1	Boolean	Override Config7.IVAD bit for CPU6/VPE1
config7IVAD_CPU6_VPE2	Boolean	Override Config7.IVAD bit for CPU6/VPE2
config7IVAD_CPU6_VPE3	Boolean	Override Config7.IVAD bit for CPU6/VPE3
config7IVAD_CPU7_VPE0	Boolean	Override Config7.IVAD bit for CPU7/VPE0
config7IVAD_CPU7_VPE1	Boolean	Override Config7.IVAD bit for CPU7/VPE1
config7IVAD_CPU7_VPE2	Boolean	Override Config7.IVAD bit for CPU7/VPE2
config7IVAD_CPU7_VPE3	Boolean	Override Config7.IVAD bit for CPU7/VPE3
config7RPS_CPU0_VPE0	Boolean	Override Config7.RPS bit for CPU0/VPE0
config7RPS_CPU0_VPE1	Boolean	Override Config7.RPS bit for CPU0/VPE1
config7RPS_CPU0_VPE2	Boolean	Override Config7.RPS bit for CPU0/VPE2
config7RPS_CPU0_VPE3	Boolean	Override Config7.RPS bit for CPU0/VPE3
config7RPS_CPU1_VPE0	Boolean	Override Config7.RPS bit for CPU1/VPE0
config7RPS_CPU1_VPE1	Boolean	Override Config7.RPS bit for CPU1/VPE1
config7RPS_CPU1_VPE2	Boolean	Override Config7.RPS bit for CPU1/VPE2
config7RPS_CPU1_VPE3	Boolean	Override Config7.RPS bit for CPU1/VPE3
config7RPS_CPU2_VPE0	Boolean	Override Config7.RPS bit for CPU2/VPE0
config7RPS_CPU2_VPE1	Boolean	Override Config7.RPS bit for CPU2/VPE1
config7RPS_CPU2_VPE2	Boolean	Override Config7.RPS bit for CPU2/VPE2
config7RPS_CPU2_VPE3	Boolean	Override Config7.RPS bit for CPU2/VPE3
config7RPS_CPU3_VPE0	Boolean	Override Config7.RPS bit for CPU3/VPE0
config7RPS_CPU3_VPE1	Boolean	Override Config7.RPS bit for CPU3/VPE1
_		
config7RPS_CPU3_VPE2 config7RPS_CPU3_VPE3	Boolean Boolean	Override Config7.RPS bit for CPU3/VPE2 Override Config7.RPS bit for CPU3/VPE3
config7RPS_CPU3_VPE3	Boolean	Override Config7.RPS bit for CPU4/VPE0
config7RPS_CPU4_VPE1	Boolean	Override Config7.RPS bit for CPU4/VPE1
config7RPS_CPU4_VPE2	Boolean	Override Config7.RPS bit for CPU4/VPE2
config7RPS_CPU4_VPE3	Boolean	Override Config7.RPS bit for CPU4/VPE3
config7RPS_CPU5_VPE0	Boolean	Override Config7.RPS bit for CPU5/VPE0
config7RPS_CPU5_VPE1	Boolean	Override Config7.RPS bit for CPU5/VPE1
config7RPS_CPU5_VPE2	Boolean	Override Config7.RPS bit for CPU5/VPE2
config7RPS_CPU5_VPE3	Boolean	Override Config7.RPS bit for CPU5/VPE3
config7RPS_CPU6_VPE0	Boolean	Override Config7.RPS bit for CPU6/VPE0
config7RPS_CPU6_VPE1	Boolean	Override Config7.RPS bit for CPU6/VPE1
config7RPS_CPU6_VPE2	Boolean	Override Config7.RPS bit for CPU6/VPE2
config7RPS_CPU6_VPE3	Boolean	Override Config7.RPS bit for CPU6/VPE3
config7RPS_CPU7_VPE0	Boolean	Override Config7.RPS bit for CPU7/VPE0
config7RPS_CPU7_VPE1	Boolean	Override Config7.RPS bit for CPU7/VPE1
config7RPS_CPU7_VPE2	Boolean	Override Config7.RPS bit for CPU7/VPE2
config7RPS_CPU7_VPE3	Boolean	Override Config7.RPS bit for CPU7/VPE3
statusFR	Boolean	Override power on value in Status.FR (Floating
		point register mode)

fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
srsconf0SRS1	Uns32	Override humber of MAAR registers (must be even)  Override the SRS1 field in SRSConf0 register
srsconf0SRS2	Uns32	Override the SRS2 field in SRSConf0 register
srsconf0SRS3	Uns32	
		Override the SRS3 field in SRSConf0 register
wiredLimit	Uns32	Override Limit field of the Wired register
wiredLimitBits	Uns32	Override width of Limit field of the Wired register
wiredWiredBits	Uns32	Override width of Wired field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
parityEnable	Uns32	Specify error detection support: 0 - none; 1 - parity; 2 - ECC
useMpTb	Boolean	Override Use of multi-processor test bench
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use
•		GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the cor-
r		responding BEV address bits
l1BufferCache	Boolean	L1 Buffer Cache
GCU_EX	Boolean	CMP system only: GCR custom block present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable
TIMER_ROOTABLE	Boolean	within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable
SWINT ROOTABLE	Boolean	within cluster
PERFCNT_ROUTABLE	Boolean	CMP system only: performance counter interrupt
		routable within cluster
FDC_ROUTABLE	Boolean	CMP system only: fast debug channel interrupt
		routable within cluster
GCR_PCORES	Uns32	CMP system only: override
		GCR_CONFIG.PCORES (number of cores-1)
GCR_ADDR_REGIONS	Uns32	CMP system only: override
		GCR_CONFIG.ADDR_REGIONS (number of
		MMIO address regions)
GCR_NUMAUX	Uns32	CMP system only: override
0.010_11.0111011	011502	GCR_CONFIG.NUMAUX (number of auxil-
		iary memory ports)
GCR_BASE	Uns64	CMP system only: override
O O I O D I		GCR_BASE.GCR_BASE (default GCR regis-
		ter address)
GCR_MINOR_REV	Uns32	CMP system only: override
GCR_MINOR_REV	Ulisoz	GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	
GCR_MAJOR_REV	Ulis52	CMP system only: override GCR_REV.MAJOR_REV
CCD CACHE MINOR DEV	II. 90	
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override
CCD CACHE MAJOR PRIV	11 00	GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override
GGD to LOGO G	**	GCR_CACHE_REV.MAJOR_REV
GCR_L2_ASSOC	Uns32	CMP system only: override
CICID TO COMP COMP		GCR_L2_CONFIG.ASSOC
GCR_L2_SET_SIZE	Uns32	CMP system only: override
	_	GCR_L2_CONFIG.SET_SIZE
GCR_SYS_CONFIG2_MAX_VP_WIDTH	Uns32	CMP system only: override
		GCR_SYS_CONFIG2.MAX_VP_WIDTH

GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override
		GCR_IOCU1_REV.MAJOR_REV
GCR_BEV_BASE	Uns32	CMP system only: override GCR_BEV_BASE
GCR_KX_BASE_MODE	Boolean	CMP system only: override BEV_BASE_MODE & RESET_BASE_MODE
GCR_MMIO_REQ_LIMIT	Uns32	CMP system only: override GCR_MMIO_REQ_LIMIT.MMIO_REQ_LIMIT
		value
GCR_MMIO0_BOTTOM	Uns64	CMP system only: override GCR_MMIO0_BOTTOM register value
GCR_MMIO0_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO0_TOP.TOP_ADDR value
GCR_MMIO1_BOTTOM	Uns64	CMP system only: override GCR_MMIO1_BOTTOM register value
GCR_MMIO1_TOP_ADDR	Uns32	CMP system only: override
CCD MMO2 DOTTOM	11 04	GCR_MMIO1_TOP.TOP_ADDR value
GCR_MMIO2_BOTTOM	Uns64	CMP system only: override GCR_MMIO2_BOTTOM register value
GCR_MMIO2_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO2_TOP.TOP_ADDR value
GCR_MMIO3_BOTTOM	Uns64	CMP system only: override GCR_MMIO3_BOTTOM register value
GCR_MMIO3_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO3_TOP.TOP_ADDR value
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override
		GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override
GIC_TRIG_RESET	Uns32	GIC_SH_DBG_CONFIG.NUM_TEAMS  CMP system only: Zero value of
	Ulis52	GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override
CPC_MINOR_REV	Uns32	CPC_RESETLEN.RESETLEN  CMP system only: override
		CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override
		GIC_SH_GID_CONFIG[95_64]

GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
gicVirtualVPNum_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
gicVirtualVPNum_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
gicVirtualVPNum_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
gicVirtualVPNum_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
gicVirtualVPNum_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
gicVirtualVPNum_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
gicVirtualVPNum_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
gicVirtualVPNum_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
gicVirtualVPNum_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
gicVirtualVPNum_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
gicVirtualVPNum_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
gicVirtualVPNum_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
gicVirtualVPNum_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
gicVirtualVPNum_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
gicVirtualVPNum_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
gicVirtualVPNum_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
gicVirtualVPNum_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
gicVirtualVPNum_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
gicVirtualVPNum_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
gicVirtualVPNum_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
gicVirtualVPNum_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
gicVirtualVPNum_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
gicVirtualVPNum_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2

$gicVirtual VPNum\_CPU5\_VP3$	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
gicVirtualVPNum_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
gicVirtualVPNum_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
gicVirtualVPNum_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
gicVirtualVPNum_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
gicVirtualVPNum_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
gicVirtualVPNum_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
gicVirtualVPNum_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
gicVirtualVPNum_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C4_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 4
GCR_C5_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 5
GCR_C6_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 6
GCR_C7_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 7
GCR_C8_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 8
GCR_C9_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 9
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 3
GCR_C4_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 4
GCR_C5_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 5
GCR_C6_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 6
GCR_C7_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 7
GCR_C8_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 8

GCR_C9_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 9
CPC_C0_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 0
CPC_C1_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 1
CPC_C2_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 2
CPC_C3_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 3
CPC_C4_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 4
CPC_C5_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 5
CPC_C6_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 6
CPC_C7_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 7
CPC_C8_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 8
CPC_C9_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 9
EIC_OPTION	Uns32	Override the external interrupt controller
		EIC_OPTION
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register
guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest IPFDC field in IntCtl register
guestintctlIPPCI	Uns32	Override the Guest IPPCI field in IntCtl register
guestintctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
guestintctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
$guestintct IIPTI\_CPU0\_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
guestintctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
guestintctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
guestintctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
$guestintct IIPTI\_CPU1\_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
guestintctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
guestintctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
guestintctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
guestintctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
guestintctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
guestintctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0

guestintctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
guestintctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
guestintctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
guestintctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
guestintctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
$guest int ctlIPTI\_CPU4\_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
$guestintct IIPTI\_CPU4\_VP3$	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
guestintctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
$guest int ctlIPTI\_CPU5\_VP1$	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
$guest int ctlIPTI\_CPU5\_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
$guest int ctlIPTI\_CPU5\_VP3$	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
$guest int ctlIPTI\_CPU6\_VP0$	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
guestintctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
$guest int ctlIPTI\_CPU6\_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
$guestintct IIPTI\_CPU6\_VP3$	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
guestintctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
guestintctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
guestintctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
guestintctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
guestintctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
guestintctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
guestintctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
guestintctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
guestintctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
guestintctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
$guest intctlIPFDC\_CPU1\_VP2$	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
guestintctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
guestintctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0

guestintctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
guestintctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
guestintctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
guestintctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
guestintctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
guestintctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
guestintctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
guestintctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
guestintctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
guestintctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
guestintctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
guestintctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
guestintctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
guestintctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
guestintctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
guestintctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
guestintctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
guestintctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
guestintctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
guestintctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
guestintctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
guestintctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
guestintctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
guestintctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
guestintctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
guestintctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
guestintctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
guestintctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0

guestintctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for
		CPU1/VP1
guestintctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
guestintctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
guestintctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
guestintctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
guestintctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
guestintctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
guestintctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
guestintctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
guestintctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
guestintctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
guestintctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
guestintctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
guestintctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
guestintctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
guestintctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
guestintctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
guestintctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
guestintctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
guestintctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
guestintctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
guestintctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
guestintctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
guestintctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
guestintctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
guestintctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
guestintctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2( <ispram bytes="" in="" size="">) - 11)</ispram>
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region

ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used
		to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior
		to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region
		$(\log 2(< DSPRAM \text{ size in bytes}) - 11)$
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag
		(used to enable the DSPRAM region prior to re-
		set)
DSPRAM_PRESENT	Boolean	DSPRAM is present with SAAR
USPRAM_SIZE	Uns32	Encoded size of the USPRAM region
		$(\log 2(\langle \text{USPRAM size in bytes} \rangle) - 11)$
USPRAM_BASE	Uns64	Starting physical address of the USPRAM region
USPRAM_ENABLE	Boolean	Set the enable bit of the USPRAM region's tag
		(used to enable the USPRAM region prior to re-
		set)
USPRAM_FILE	String	Load a MIPS hex file into the USPRAM region
		prior to reset
misalignedDataException	Enumeration	Select misaligned data access exception signaling:
		never, checkCCA or always (never, checkCCA or
		always)
commitTlbwErr	Boolean	Commit TLBWI/TLBRI on ECC; in
		MIPS_DV_MODE only

Table 8.5: Parameters that can be set in: VP

## 8.3 Parameter values

These are the current parameter values.

Name	Value
(Others)	
endian	none
cacheenable	default
cachedebug	0
cacheextbiuinfo	0x0
mipsHexFile	
IMPERAS_MIPS_AVP_OPCODES	F
cacheIndexBypassTLB	F
MIPS_TRACE	F
gprNames	F
supervisorMode	F
busErrors	Т
fixedMMU	F
fixedDbgRegSize	F
removeDSP	F
removeCMP	F
removeFP	F
removeFTLB	F
isISA	F

hiddenTLBentries perfCounters ITCNumEntries ITCNumFIFO ITCFIFODepth ITCEmptyOnReset MTFPU	F 0 0 0 0 F 0 F
ITCNumEntries ITCNumFIFO ITCFIFODepth ITCEmptyOnReset	0 0 0 F 0 F
ITCNumFIFO ITCFIFODepth ITCEmptyOnReset	0 0 F 0 F
ITCFIFODepth ITCEmptyOnReset	0 F 0 F
ITCEmptyOnReset	F 0 F
	0 F
	F
_	
supportDenormals	
VPE0MaxTC	0
VPE1MaxTC	0
segBits	0
mpuRegions	0
mpuType	0
mpuEnable	F
mpuSegment0	0
mpuSegment1	0
mpuSegment2	0
mpuSegment3	0
mpuSegment4	0
mpuSegment5	0
mpuSegment6	0
mpuSegment7	0
mpuSegment8	0
mpuSegment9	0
mpuSegment10	0
mpuSegment11	0
mpuSegment12	0
mpuSegment13	0
mpuSegment14	0
mpuSegment15	0
mvpconf0vpe	0
tcDisable	0
vpeDisable	0
mvpconf0tc	0
mvpconf0pcp	F
mvpconf0tcp	F
mvpconf1c1f	F
mvpcontrolPolicyMode	F
hasFDC	0
licenseWarningDays	15
MIPS_UHI	F
mipsUhiArgs	
mipsUhiJail	
MIPS_DV_MODE	F
MIPS_MAGIC_OPCODES	F

enableTrickbox	F
fpuexcdisable	F
TRU_PRESENT	F
ucLLwordsLocked	0
FUSA	F
CPC_FAULT_SUPPORTED	0
CPC_FAULT_ENABLE	0
cop2Bits	32
cop2FileName	
udiConfig	0
udiFileName	
vectoredinterrupt	F
externalinterrupt	F
config3VEIC_VPE0	F
config3VEIC_VPE1	F
config3VEIC_VPE2	F
config3VEIC_VPE3	F
rootFixedMMU	F
rootMMUSizeM1	0
srsctlHSS	0
firPS	0
firHas2008	0
usePreciseFpu	0
simulateLite	NTONTO
	NONE
pridCompanyOptions	NONE 0
pridCompanyOptions pridRevision	
pridCompanyOptions pridRevision globalClusterNum	0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI	0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC	0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI	0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch	0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP	0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP	0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart	0 0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVP sharedTLBindex	0 0 0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified	0 0 0 0 0 0 0 0 0 0 0 0 F
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0	0 0 0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1	0 0 0 0 0 0 0 0 0 0 0 F
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2	0 0 0 0 0 0 0 0 0 0 0 F 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU0_VP3	0 0 0 0 0 0 0 0 0 0 F 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU0_VP3 intctlIPTI_CPU1_VP0	0 0 0 0 0 0 0 0 0 0 0 F 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU0_VP3 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP1	0 0 0 0 0 0 0 0 0 0 0 F 0 0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP2	0 0 0 0 0 0 0 0 0 0 F 0 0 0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU0_VP3 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP1	0 0 0 0 0 0 0 0 0 0 0 F 0 0 0 0 0 0 0 0

·	0
intctlIPTI_CPU2_VP1	0
intctlIPTI_CPU2_VP2	0
intctlIPTI_CPU2_VP3	0
intctlIPTI_CPU3_VP0	0
intctlIPTI_CPU3_VP1	0
intctlIPTI_CPU3_VP2	0
intctlIPTI_CPU3_VP3	0
intctlIPTI_CPU4_VP0	0
intctlIPTI_CPU4_VP1	0
intctlIPTI_CPU4_VP2	0
intctlIPTI_CPU4_VP3	0
intctlIPTI_CPU5_VP0	0
intctlIPTI_CPU5_VP1	0
intctlIPTI_CPU5_VP2	0
intctlIPTI_CPU5_VP3	0
intctlIPTI_CPU6_VP0	0
intctlIPTI_CPU6_VP1	0
intctlIPTI_CPU6_VP2	0
intctlIPTI_CPU6_VP3	0
intctlIPTI_CPU7_VP0	0
intctlIPTI_CPU7_VP1	0
intctlIPTI_CPU7_VP2	0
intctlIPTI_CPU7_VP3	0
intctlIPFDC_CPU0_VP0	0
intctlIPFDC_CPU0_VP1	0
intctlIPFDC_CPU0_VP2	0
intctlIPFDC_CPU0_VP3	0
intctlIPFDC_CPU1_VP0	0
intctlIPFDC_CPU1_VP1	0
intctlIPFDC_CPU1_VP2	0
intctlIPFDC_CPU1_VP3	0
intctlIPFDC_CPU2_VP0	0
intctlIPFDC_CPU2_VP1	0
intctlIPFDC_CPU2_VP2	0
intctlIPFDC_CPU2_VP3	0
intctlIPFDC_CPU3_VP0	0
intctlIPFDC_CPU3_VP1	0
intetHFDC_CFU3_VF2	0
intctIIPFDC_CPU3_VP2	
	0
intctlIPFDC_CPU4_VP0	0
intctlIPFDC_CPU4_VP1	0
intctlIPFDC_CPU4_VP2	0
intctlIPFDC_CPU4_VP3	0
intctlIPFDC_CPU5_VP0	0
intctlIPFDC_CPU5_VP1	0

intetlIPFDC.CPU5.VP3         0           intetlIPFDC.CPU6.VP0         0           intetlIPFDC.CPU6.VP0         0           intetlIPFDC.CPU6.VP1         0           intetlIPFDC.CPU6.VP2         0           intetlIPFDC.CPU7.VP0         0           intetlIPFDC.CPU7.VP1         0           intetlIPFDC.CPU7.VP2         0           intetlIPFDC.CPU7.VP3         0           intetlIPFDC.CPU0.VP3         0           intetlIPPCI.CPU0.VP0         0           intetlIPPCI.CPU0.VP1         0           intetlIPPCI.CPU0.VP2         0           intetlIPPCI.CPU0.VP3         0           intetlIPPCI.CPU1.VP0         0           intetlIPPCI.CPU1.VP1         0           intetlIPPCI.CPU1.VP2         0           intetlIPPCI.CPU1.VP3         0           intetlIPPCI.CPU1.VP3         0           intetlIPPCI.CPU2.VP0         0           intetlIPPCI.CPU2.VP1         0           intetlIPPCI.CPU2.VP3         0           intetlIPPCI.CPU3.VP1         0           intetlIPPCI.CPU3.VP2         0           intetlIPPCI.CPU3.VP3         0           intetlIPPCI.CPU4.VP3         0           intetlIPPCI.CPU4.VP3         0		
intetlIPFDC_CPU6_VP1 intetlIPFDC_CPU6_VP2 intetlIPFDC_CPU6_VP3 intetlIPFDC_CPU6_VP3 intetlIPFDC_CPU6_VP3 intetlIPFDC_CPU7_VP0 intetlIPFDC_CPU7_VP1 intetlIPFDC_CPU7_VP1 intetlIPFDC_CPU7_VP2 intetlIPFDC_CPU7_VP3 intetlIPFDC_CPU7_VP3 intetlIPPCL_CPU0_VP0 intetlIPPCL_CPU0_VP0 intetlIPPCL_CPU0_VP1 intetlIPPCL_CPU0_VP2 intetlIPPCL_CPU0_VP3 intetlIPPCL_CPU0_VP3 intetlIPPCL_CPU1_VP0 intetlIPPCL_CPU1_VP0 intetlIPPCL_CPU1_VP1 intetlIPPCL_CPU1_VP2 intetlIPPCL_CPU1_VP2 intetlIPPCL_CPU1_VP3 intetlIPPCL_CPU1_VP3 intetlIPPCL_CPU2_VP0 intetlIPPCL_CPU2_VP0 intetlIPPCL_CPU2_VP1 intetlIPPCL_CPU2_VP2 intetlIPPCL_CPU3_VP1 intetlIPPCL_CPU3_VP1 intetlIPPCL_CPU3_VP2 intetlIPPCL_CPU3_VP3 intetlIPPCL_CPU3_VP3 intetlIPPCL_CPU4_VP0 intetlIPPCL_CPU4_VP0 intetlIPPCL_CPU4_VP0 intetlIPPCL_CPU4_VP1 intetlIPPCL_CPU4_VP1 intetlIPPCL_CPU5_VP0 intetlIPPCL_CPU5_VP0 intetlIPPCL_CPU5_VP1 intetlIPPCL_CPU5_VP1 intetlIPPCL_CPU5_VP2 intetlIPPCL_CPU5_VP1 intetlIPPCL_CPU5_VP2 intetlIPPCL_CPU5_VP3 intetlIPP	intctlIPFDC_CPU5_VP2	0
intctlIPFDC_CPU6_VP2 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP3 intctlIPPCL_CPU0_VP0 intctlIPPCL_CPU0_VP0 intctlIPPCL_CPU0_VP1 intctlIPPCL_CPU0_VP2 intctlIPPCL_CPU0_VP3 intctlIPPCL_CPU1_VP0 intctlIPPCL_CPU1_VP0 intctlIPPCL_CPU1_VP1 intctlIPPCL_CPU1_VP1 intctlIPPCL_CPU1_VP2 intctlIPPCL_CPU1_VP3 intctlIPPCL_CPU2_VP0 intctlIPPCL_CPU2_VP0 intctlIPPCL_CPU2_VP0 intctlIPPCL_CPU2_VP1 intctlIPPCL_CPU3_VP0 intctlIPPCL_CPU3_VP0 intctlIPPCL_CPU3_VP0 intctlIPPCL_CPU3_VP1 intctlIPPCL_CPU3_VP1 intctlIPPCL_CPU3_VP2 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU4_VP0 intctlIPPCL_CPU4_VP0 intctlIPPCL_CPU4_VP1 intctlIPPCL_CPU4_VP1 intctlIPPCL_CPU4_VP2 intctlIPPCL_CPU4_VP2 intctlIPPCL_CPU4_VP3 intctlIPPCL_CPU5_VP0 intctlIPPCL_CPU5_VP0 intctlIPPCL_CPU5_VP1 intctlIPPCL_CPU5_VP2 intctlIPPCL_CPU5_VP2 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP4 intctlIPP		0
intctlIPFDC_CPU6_VP2 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPPCL_CPU0_VP0 intctlIPPCL_CPU0_VP0 intctlIPPCL_CPU0_VP1 intctlIPPCL_CPU0_VP2 intctlIPPCL_CPU0_VP2 intctlIPPCL_CPU0_VP3 intctlIPPCL_CPU1_VP0 intctlIPPCL_CPU1_VP0 intctlIPPCL_CPU1_VP1 intctlIPPCL_CPU1_VP2 intctlIPPCL_CPU1_VP3 intctlIPPCL_CPU1_VP3 intctlIPPCL_CPU2_VP0 intctlIPPCL_CPU2_VP0 intctlIPPCL_CPU2_VP1 intctlIPPCL_CPU2_VP2 intctlIPPCL_CPU3_VP0 intctlIPPCL_CPU3_VP0 intctlIPPCL_CPU3_VP1 intctlIPPCL_CPU3_VP1 intctlIPPCL_CPU3_VP2 intctlIPPCL_CPU3_VP2 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU4_VP0 intctlIPPCL_CPU4_VP0 intctlIPPCL_CPU4_VP1 intctlIPPCL_CPU4_VP2 intctlIPPCL_CPU4_VP2 intctlIPPCL_CPU4_VP3 intctlIPPCL_CPU4_VP3 intctlIPPCL_CPU5_VP0 intctlIPPCL_CPU5_VP0 intctlIPPCL_CPU5_VP1 intctlIPPCL_CPU5_VP2 intctlIPPCL_CPU5_VP2 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP4 intctlIPP		0
intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP3 intctlIPPCI_CPU0_VP0 intctlIPPCI_CPU0_VP0 intctlIPPCI_CPU0_VP1 intctlIPPCI_CPU0_VP2 intctlIPPCI_CPU0_VP3 intctlIPPCI_CPU1_VP0 intctlIPPCI_CPU1_VP0 intctlIPPCI_CPU1_VP1 intctlIPPCI_CPU1_VP2 intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg1PA o	intctlIPFDC_CPU6_VP1	0
intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP3 intctlIPPCI_CPU0_VP0 intctlIPPCI_CPU0_VP0 intctlIPPCI_CPU0_VP1 intctlIPPCI_CPU0_VP2 intctlIPPCI_CPU0_VP3 intctlIPPCI_CPU1_VP0 intctlIPPCI_CPU1_VP1 intctlIPPCI_CPU1_VP1 intctlIPPCI_CPU1_VP2 intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg1PA o	intctlIPFDC_CPU6_VP2	0
intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPPCL_CPU0_VP0 intctlIPPCL_CPU0_VP1 intctlIPPCL_CPU0_VP1 intctlIPPCL_CPU0_VP2 intctlIPPCL_CPU0_VP3 intctlIPPCL_CPU1_VP0 intctlIPPCL_CPU1_VP0 intctlIPPCL_CPU1_VP1 intctlIPPCL_CPU1_VP2 intctlIPPCL_CPU1_VP3 intctlIPPCL_CPU1_VP3 intctlIPPCL_CPU2_VP0 intctlIPPCL_CPU2_VP1 intctlIPPCL_CPU2_VP2 intctlIPPCL_CPU3_VP2 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP0 intctlIPPCL_CPU3_VP1 intctlIPPCL_CPU3_VP2 intctlIPPCL_CPU3_VP2 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU3_VP3 intctlIPPCL_CPU4_VP0 intctlIPPCL_CPU4_VP0 intctlIPPCL_CPU4_VP1 intctlIPPCL_CPU5_VP1 intctlIPPCL_CPU5_VP1 intctlIPPCL_CPU5_VP1 intctlIPPCL_CPU5_VP1 intctlIPPCL_CPU5_VP1 intctlIPPCL_CPU5_VP2 intctlIPPCL_CPU5_VP2 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU5_VP3 intctlIPPCL_CPU6_VP0 intctlIPPCL_CPU6_VP0 intctlIPPCL_CPU6_VP1 intctlIPPCL_CPU6_VP2 intctlIPPCL_CPU6_VP3 intctlIPPCL_CPU7_VP0 intctlIPPCL_CPU7_VP0 intctlIPPCL_CPU7_VP1 intctlIPPCL_CPU7_VP2 intctlIPPCL_CPU7_VP3 segcfg1PA o	intctlIPFDC_CPU6_VP3	0
intetlIPFDC_CPU7_VP2 intetlIPFDC_CPU7_VP3 intetlIPPCI_CPU0_VP0 intetlIPPCI_CPU0_VP1 intetlIPPCI_CPU0_VP2 intetlIPPCI_CPU0_VP2 intetlIPPCI_CPU0_VP3 intetlIPPCI_CPU1_VP0 intetlIPPCI_CPU1_VP1 intetlIPPCI_CPU1_VP1 intetlIPPCI_CPU1_VP2 intetlIPPCI_CPU1_VP3 intetlIPPCI_CPU1_VP3 intetlIPPCI_CPU2_VP0 intetlIPPCI_CPU2_VP0 intetlIPPCI_CPU2_VP2 intetlIPPCI_CPU2_VP3 intetlIPPCI_CPU3_VP0 intetlIPPCI_CPU3_VP0 intetlIPPCI_CPU3_VP1 intetlIPPCI_CPU3_VP1 intetlIPPCI_CPU3_VP2 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU4_VP0 intetlIPPCI_CPU4_VP0 intetlIPPCI_CPU4_VP1 intetlIPPCI_CPU4_VP2 intetlIPPCI_CPU4_VP3 intetlIPPCI_CPU5_VP0 intetlIPPCI_CPU5_VP0 intetlIPPCI_CPU5_VP1 intetlIPPCI_CPU5_VP1 intetlIPPCI_CPU5_VP2 intetlIPPCI_CPU5_VP3 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP1 intetlIPPCI_CPU6_VP1 intetlIPPCI_CPU6_VP2 intetlIPPCI_CPU6_VP2 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP1 intetlIPPCI_CPU7_VP2 intetlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPFDC_CPU7_VP0	0
intctlIPFDC_CPU7_VP3 intctlIPPCI_CPU0_VP0 intctlIPPCI_CPU0_VP1 intctlIPPCI_CPU0_VP2 intctlIPPCI_CPU0_VP3 intctlIPPCI_CPU1_VP0 intctlIPPCI_CPU1_VP0 intctlIPPCI_CPU1_VP1 intctlIPPCI_CPU1_VP2 intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPFDC_CPU7_VP1	0
intetlIPPCI_CPU0_VP0 intetlIPPCI_CPU0_VP2 intetlIPPCI_CPU0_VP3 intetlIPPCI_CPU0_VP3 intetlIPPCI_CPU1_VP0 intetlIPPCI_CPU1_VP0 intetlIPPCI_CPU1_VP1 intetlIPPCI_CPU1_VP2 intetlIPPCI_CPU1_VP3 intetlIPPCI_CPU1_VP3 intetlIPPCI_CPU2_VP0 intetlIPPCI_CPU2_VP0 intetlIPPCI_CPU2_VP1 intetlIPPCI_CPU3_VP2 intetlIPPCI_CPU3_VP0 intetlIPPCI_CPU3_VP0 intetlIPPCI_CPU3_VP1 intetlIPPCI_CPU3_VP1 intetlIPPCI_CPU3_VP2 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU4_VP0 intetlIPPCI_CPU4_VP0 intetlIPPCI_CPU4_VP1 intetlIPPCI_CPU4_VP2 intetlIPPCI_CPU4_VP3 intetlIPPCI_CPU4_VP3 intetlIPPCI_CPU5_VP0 intetlIPPCI_CPU5_VP1 intetlIPPCI_CPU5_VP2 intetlIPPCI_CPU5_VP2 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP1 intetlIPPCI_CPU6_VP2 intetlIPPCI_CPU6_VP2 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP1 intetlIPPCI_CPU7_VP2 intetlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPFDC_CPU7_VP2	0
intctlIPPCI_CPU0_VP1 intctlIPPCI_CPU0_VP3 intctlIPPCI_CPU1_VP0 intctlIPPCI_CPU1_VP0 intctlIPPCI_CPU1_VP1 intctlIPPCI_CPU1_VP1 intctlIPPCI_CPU1_VP2 intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPFDC_CPU7_VP3	0
intctlIPPCI_CPU0_VP3 intctlIPPCI_CPU1_VP0 intctlIPPCI_CPU1_VP1 intctlIPPCI_CPU1_VP1 intctlIPPCI_CPU1_VP2 intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPPCI_CPU0_VP0	0
intctlIPPCI_CPU1_VP0 intctlIPPCI_CPU1_VP1 intctlIPPCI_CPU1_VP2 intctlIPPCI_CPU1_VP2 intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPPCI_CPU0_VP1	0
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intctlIPPCI_CPU1_VP1 intctlIPPCI_CPU1_VP2 intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPPCI_CPU0_VP3	0
intctlIPPCI_CPU1_VP2 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPPCI_CPU1_VP0	0
intctlIPPCI_CPU1_VP3 intctlIPPCI_CPU2_VP0 intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg0PA segcfg1PA	intctlIPPCI_CPU1_VP1	0
intctlIPPCI_CPU2_VP1 intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP1 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPPCI_CPU1_VP2	0
intctlIPPCI_CPU2_VP2 intctlIPPCI_CPU2_VP3 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP0 intctlIPPCI_CPU3_VP1 intctlIPPCI_CPU3_VP2 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU3_VP3 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP0 intctlIPPCI_CPU4_VP2 intctlIPPCI_CPU4_VP3 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP0 intctlIPPCI_CPU5_VP1 intctlIPPCI_CPU5_VP2 intctlIPPCI_CPU5_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP0 intctlIPPCI_CPU6_VP1 intctlIPPCI_CPU6_VP2 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU6_VP3 intctlIPPCI_CPU7_VP0 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP1 intctlIPPCI_CPU7_VP2 intctlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPPCI_CPU1_VP3	0
intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU2_VP0	0
intetlIPPCI_CPU2_VP3 intetlIPPCI_CPU3_VP0 intetlIPPCI_CPU3_VP1 intetlIPPCI_CPU3_VP2 intetlIPPCI_CPU3_VP3 intetlIPPCI_CPU4_VP0 intetlIPPCI_CPU4_VP0 intetlIPPCI_CPU4_VP2 intetlIPPCI_CPU4_VP3 intetlIPPCI_CPU4_VP3 intetlIPPCI_CPU5_VP0 intetlIPPCI_CPU5_VP1 intetlIPPCI_CPU5_VP2 intetlIPPCI_CPU5_VP3 intetlIPPCI_CPU5_VP3 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP0 intetlIPPCI_CPU6_VP1 intetlIPPCI_CPU6_VP2 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU6_VP3 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP0 intetlIPPCI_CPU7_VP1 intetlIPPCI_CPU7_VP2 intetlIPPCI_CPU7_VP2 intetlIPPCI_CPU7_VP3 segcfg0PA segcfg1PA	intctlIPPCI_CPU2_VP1	0
intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU2_VP2	0
intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU2_VP3	0
intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU3_VP0	0
intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU3_VP1	0
intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU3_VP2	0
intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU3_VP3	0
intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU4_VP0	0
intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU4_VP1	0
intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU4_VP2	0
intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU4_VP3	0
intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU5_VP0	0
intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU5_VP1	0
intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU5_VP2	0
intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU5_VP3	0
intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU6_VP0	0
intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU6_VP1	0
intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU6_VP2	0
intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU6_VP3	0
intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU7_VP0	0
intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0		0
segcfg0PA         0           segcfg1PA         0	intctlIPPCI_CPU7_VP2	0
segcfg1PA 0	intctlIPPCI_CPU7_VP3	0
	segcfg0PA	0
segcfg2PA 0		0
	segcfg2PA	0

segcfg3PA	0
segcfg4PA	0
segcfg5PA	0
segcfg0AM	0
segcfg1AM	0
segcfg2AM	0
segcfg3AM	0
segcfg4AM	0
segcfg5AM	0
segcfg0EU	0
segcfg1EU	0
segcfg2EU	0
segcfg3EU	0
segcfg4EU	0
segcfg5EU	0
segcfg0C	0
segcfg1C	0
segcfg2C	0
segcfg3C	0
segcfg4C	0
segcfg5C	0
cdmmSize	0
configAR	0
configBM	0
configDSP	F
configISP	F
configK0	0
configKU	0
configK23	0
configMDU	F
configMM	F
configMT	0
configSB	F
configBCP	F
MIPS16eASE	F
config1DA	0
config1DL	0
config1DS	0
config1EP	F
config1IA	0
config1IL	0
config1IS	0
config1MMUSizeM1	0
config1MMUSizeM1_VPE1	0
config1MMUSizeM1_VPE2	0

config1MMUSizeM1_VPE3	0
config1WR	F
config1PC	F
config1C2	F
config2SU	0
config2SS	0
config2SL	0
config2SA	0
config3BI	F
config3BP	F
config3CDMM	F
config3CTXTC	F
config3DSPP	F
config3DSP2P	F
config3IPLW	0
config3ISA	0
config3ISAOnExc	F
config3ITL	F
config3LPA	F
config3MCU	F
config3MMAR	0
config3RXI	F
config3SC	F
config3ULRI	F
config3VZ	F
config3MSAP	F
config3CMGCR	F
config3SP	F
config3TL	0
config3PW	F
config4AE	F
config4IE	0
config4MMUConfig	0
config4MMUExtDef	0
config4VTLBSizeExt	0
config4KScrExist	0
config5EVA	F
config5LLB	F
config5MRP	F
config5NFExists	F
mips32Macro	F
config5MSAEn	F
config5MVH	F
config5DEC	F
config5GI	0
0-0	

config5CRCP	F
config5VP	F
config6FTLBEn	F
config7AR	F
config7DCIDX_MODE	0
config7HCI	F
config7IAR	F
config7WII	F
config7ES	0
config7WR	F
config7FPR	F
config7USP	0
config7BTLM	F
config7BusSlp	F
config7IVAD	F
config7RPS	F
config7IAR_CPU0_VPE0	F
config7IAR_CPU0_VPE1	F
config7IAR_CPU0_VPE2	F
config7IAR_CPU0_VPE3	F
config7IAR_CPU1_VPE0	F
config7IAR_CPU1_VPE1	F
config7IAR_CPU1_VPE2	F
config7IAR_CPU1_VPE3	F
config7IAR_CPU2_VPE0	F
config7IAR_CPU2_VPE1	F
config7IAR_CPU2_VPE2	F
config7IAR_CPU2_VPE3	F
config7IAR_CPU3_VPE0	F
config7IAR_CPU3_VPE1	F
config7IAR_CPU3_VPE2	F
config7IAR_CPU3_VPE3	F
config7IAR_CPU4_VPE0	F
config7IAR_CPU4_VPE1	F
config7IAR_CPU4_VPE2	F
config7IAR_CPU4_VPE3	F
config7IAR_CPU5_VPE0	F
config7IAR_CPU5_VPE1	F
$config7IAR\_CPU5\_VPE2$	F
config7IAR_CPU5_VPE3	F
config7IAR_CPU6_VPE0	F
config7IAR_CPU6_VPE1	F
config7IAR_CPU6_VPE2	F
config7IAR_CPU6_VPE3	F
config7IAR_CPU7_VPE0	F

config7IAR_CPU7_VPE1	F
config7IAR_CPU7_VPE2	F
config7IAR_CPU7_VPE3	F
config7IVAD_CPU0_VPE0	F
config7IVAD_CPU0_VPE1	F
config7IVAD_CPU0_VPE2	F
config7IVAD_CPU0_VPE3	F
config7IVAD_CPU1_VPE0	F
config7IVAD_CPU1_VPE1	F
config7IVAD_CPU1_VPE2	F
config7IVAD_CPU1_VPE3	F
config7IVAD_CPU2_VPE0	F
config7IVAD_CPU2_VPE1	F
config7IVAD_CPU2_VPE2	F
config7IVAD_CPU2_VPE3	F
config7IVAD_CPU3_VPE0	F
config7IVAD_CPU3_VPE1	F
config7IVAD_CPU3_VPE2	F
config7IVAD_CPU3_VPE3	F
config7IVAD_CPU4_VPE0	F
config7IVAD_CPU4_VPE1	F
config7IVAD_CPU4_VPE2	F
config7IVAD_CPU4_VPE3	F
config7IVAD_CPU5_VPE0	F
config7IVAD_CPU5_VPE1	F
config7IVAD_CPU5_VPE2	F
config7IVAD_CPU5_VPE3	F
config7IVAD_CPU6_VPE0	F
config7IVAD_CPU6_VPE1	F
config7IVAD_CPU6_VPE2	F
config7IVAD_CPU6_VPE3	F
config7IVAD_CPU7_VPE0	F
config7IVAD_CPU7_VPE1	F
config7IVAD_CPU7_VPE2	F
config7IVAD_CPU7_VPE3	F
config7RPS_CPU0_VPE0	F
config7RPS_CPU0_VPE1	F
config7RPS_CPU0_VPE2	F
config7RPS_CPU0_VPE3	F
config7RPS_CPU1_VPE0	F
config7RPS_CPU1_VPE1	F
config7RPS_CPU1_VPE2	F
config7RPS_CPU1_VPE3	F
config7RPS_CPU2_VPE0	F
config7RPS_CPU2_VPE1	F

config7RPS_CPU2_VPE2	F
config7RPS_CPU2_VPE3	F
config7RPS_CPU3_VPE0	F
config7RPS_CPU3_VPE1	F
config7RPS_CPU3_VPE2	F
config7RPS_CPU3_VPE3	F
config7RPS_CPU4_VPE0	F
	F
config7RPS_CPU4_VPE1	F
config7RPS_CPU4_VPE2	F
config7RPS_CPU4_VPE3	
config7RPS_CPU5_VPE0	F
config7RPS_CPU5_VPE1	F
config7RPS_CPU5_VPE2	F
config7RPS_CPU5_VPE3	F
config7RPS_CPU6_VPE0	F
config7RPS_CPU6_VPE1	F
config7RPS_CPU6_VPE2	F
config7RPS_CPU6_VPE3	F
config7RPS_CPU7_VPE0	F
config7RPS_CPU7_VPE1	F
config7RPS_CPU7_VPE2	F
$config7RPS\_CPU7\_VPE3$	F
statusFR	F
fcsrABS2008	F
fcsrNAN2008	F
numMaarRegs	6
srsconf0SRS1	0
srsconf0SRS2	0
srsconf0SRS3	0
wiredLimit	0
wiredLimitBits	0
wiredWiredBits	0
cdmmBaseCI	F
parityEnable	1
useMpTb	T
ExceptionBase	0
UseExceptionBase	F
l1BufferCache	F
GCU_EX	F
GIC-EX	F
CPC_EX	F
TIMER_ROUTABLE	F
SWINT_ROUTABLE	F
PERFCNT_ROUTABLE	F
FDC_ROUTABLE	F
I DO TOO INDEE	1

GCR_PCORES	0
GCR_ADDR_REGIONS	0
GCR_NUMAUX	0
GCR_BASE	0
GCR_MINOR_REV	0
GCR_MAJOR_REV	0
GCR_CACHE_MINOR_REV	0
GCR_CACHE_MAJOR_REV	0
GCR_L2_ASSOC	0
GCR_L2_SET_SIZE	0
GCR_SYS_CONFIG2_MAX_VP_WIDTH	0
GCR_IOCU1_MINOR_REV	0
GCR_IOCU1_MAJOR_REV	0
GCR_BEV_BASE	0
GCR_KX_BASE_MODE	F
GCR_MMIO_REQ_LIMIT	0
GCR_MMIO0_BOTTOM	0
GCR_MMIO0_TOP_ADDR	0
GCR_MMIO1_BOTTOM	0
GCR_MMIO1_TOP_ADDR	0
GCR_MMIO2_BOTTOM	0
GCR_MMIO2_TOP_ADDR	0
GCR_MMIO3_BOTTOM	0
GCR_MMIO3_TOP_ADDR	0
GIC_NUMINTERRUPTS	0
GIC_COUNTBITS	0
GIC_MINOR_REV	0
GIC_MAJOR_REV	0
GIC_NUM_TEAMS	7
GIC_TRIG_RESET	0
GIC_PVPES	0
CPC_MICROSTEP	0
CPC_RAILDELAY	0
CPC_RESETLEN	0
CPC_MINOR_REV	0
CPC_MAJOR_REV	0
GIC_SH_GID_CONFIG31_0	0
GIC_SH_GID_CONFIG63_32	0
GIC_SH_GID_CONFIG95_64	0
GIC_SH_GID_CONFIG127_96	0
GIC_SH_GID_CONFIG159_128	0
GIC_SH_GID_CONFIG191_160	0
GIC_SH_GID_CONFIG223_192	0
GIC_SH_GID_CONFIG255_224	0
gicVirtualVPNum_CPU0_VP0	0
810 + 11 0 dail + 1 1 dilli-C1 00 - + 1 0	U

gicVirtualVPNum_CPU0_VP1	0
gicVirtualVPNum_CPU0_VP2	0
gicVirtualVPNum_CPU0_VP3	0
gicVirtualVPNum_CPU1_VP0	0
gicVirtualVPNum_CPU1_VP1	0
gicVirtualVPNum_CPU1_VP2	0
gicVirtualVPNum_CPU1_VP3	0
gicVirtualVPNum_CPU2_VP0	0
gicVirtualVPNum_CPU2_VP1	0
gicVirtualVPNum_CPU2_VP2	0
gicVirtualVPNum_CPU2_VP3	0
gicVirtualVPNum_CPU3_VP0	0
gicVirtualVPNum_CPU3_VP1	0
gicVirtualVPNum_CPU3_VP2	0
gicVirtualVPNum_CPU3_VP3	0
gicVirtualVPNum_CPU4_VP0	0
gicVirtualVPNum_CPU4_VP1	0
gicVirtualVPNum_CPU4_VP2	0
gicVirtualVPNum_CPU4_VP3	0
gicVirtualVPNum_CPU5_VP0	0
gicVirtualVPNum_CPU5_VP1	0
gicVirtualVPNum_CPU5_VP2	0
gicVirtualVPNum_CPU5_VP3	0
gicVirtualVPNum_CPU6_VP0	0
gicVirtualVPNum_CPU6_VP1	0
gicVirtualVPNum_CPU6_VP2	0
gicVirtualVPNum_CPU6_VP3	0
gicVirtualVPNum_CPU7_VP0	0
gicVirtualVPNum_CPU7_VP1	0
gicVirtualVPNum_CPU7_VP2	0
gicVirtualVPNum_CPU7_VP3	0
GCR_C0_RESET_BASE	0
GCR_C1_RESET_BASE	0
GCR_C2_RESET_BASE	0
GCR_C3_RESET_BASE	0
GCR_C4_RESET_BASE	0
GCR_C5_RESET_BASE	0
GCR_C6_RESET_BASE	0
GCR_C7_RESET_BASE	0
GCR_C8_RESET_BASE	0
GCR_C9_RESET_BASE	0
GCR_C0_RESET_EXT_BASE	0
GCR_C1_RESET_EXT_BASE	0
GCR_C2_RESET_EXT_BASE	0
GCR_C3_RESET_EXT_BASE	0

GCR_C4_RESET_EXT_BASE	0
GCR_C5_RESET_EXT_BASE	0
GCR_C6_RESET_EXT_BASE	0
GCR_C7_RESET_EXT_BASE	0
GCR_C8_RESET_EXT_BASE	0
GCR_C9_RESET_EXT_BASE	0
CPC_C0_VP_EN	0
CPC_C1_VP_EN	0
CPC_C2_VP_EN	0
CPC_C3_VP_EN	0
CPC_C4_VP_EN	0
CPC_C5_VP_EN	0
CPC_C6_VP_EN	0
CPC_C7_VP_EN	0
CPC_C8_VP_EN	0
CPC_C9_VP_EN	0
EIC_OPTION	2
guestCtl0RI	0
guestCtl0MC	0
guestCtl0CP0	0
guestCtl0AT	0
guestCtl0GT	0
guestCtl0CG	0
guestCtl0CF	0
guestCtl0G1	0
guestCtl0RAD	0
guestCtl0DRG	0
hasImpl17	F
hasImpl16	F
guestintctlIPTI	0
guestintctlIPFDC	0
guestintctlIPPCI	0
guestintctlIPTI_CPU0_VP0	0
guestintctlIPTI_CPU0_VP1	0
guestintctlIPTI_CPU0_VP2	0
guestintctlIPTI_CPU0_VP3	0
guestintctlIPTI_CPU1_VP0	0
guestintctlIPTI_CPU1_VP1	0
guestintctlIPTI_CPU1_VP2	0
guestintctlIPTI_CPU1_VP3	0
guestintctlIPTI_CPU2_VP0	0
guestintctlIPTI_CPU2_VP1	0
guestintctlIPTI_CPU2_VP2	0
guestintctlIPTI_CPU2_VP3	0
guestintctlIPTI_CPU3_VP0	0

guestintctlIPTI_CPU3_VP1	0
guestintctlIPTI_CPU3_VP2	0
guestintctlIPTI_CPU3_VP3	0
guestintctlIPTI_CPU4_VP0	0
guestintctlIPTI_CPU4_VP1	0
guestintctlIPTI_CPU4_VP2	0
guestintctlIPTI_CPU4_VP3	0
guestintctlIPTI_CPU5_VP0	0
guestintctlIPTI_CPU5_VP1	0
guestintctlIPTI_CPU5_VP2	0
guestintctlIPTI_CPU5_VP3	0
guestintctlIPTI_CPU6_VP0	0
guestintctlIPTI_CPU6_VP1	0
guestintctlIPTI_CPU6_VP2	0
guestintctlIPTI_CPU6_VP3	0
guestintctlIPTI_CPU7_VP0	0
guestintctlIPTI_CPU7_VP1	0
guestintctlIPTI_CPU7_VP2	0
guestintctlIPTI_CPU7_VP3	0
guestintctlIPFDC_CPU0_VP0	0
guestintctlIPFDC_CPU0_VP1	0
guestintctlIPFDC_CPU0_VP2	0
guestintctlIPFDC_CPU0_VP3	0
guestintctlIPFDC_CPU1_VP0	0
guestintctlIPFDC_CPU1_VP1	0
guestintctlIPFDC_CPU1_VP2	0
guestintctlIPFDC_CPU1_VP3	0
guestintctlIPFDC_CPU2_VP0	0
guestintctlIPFDC_CPU2_VP1	0
guestintctlIPFDC_CPU2_VP2	0
guestintctlIPFDC_CPU2_VP3	0
guestintctlIPFDC_CPU3_VP0	0
guestintctlIPFDC_CPU3_VP1	0
guestintctlIPFDC_CPU3_VP2	0
guestintctlIPFDC_CPU3_VP3	0
guestintctlIPFDC_CPU4_VP0	0
guestintctlIPFDC_CPU4_VP1	0
guestintctlIPFDC_CPU4_VP2	0
guestintctlIPFDC_CPU4_VP3	0
guestintctlIPFDC_CPU5_VP0	0
guestintctlIPFDC_CPU5_VP1	0
guestintctlIPFDC_CPU5_VP2	0
guestintctlIPFDC_CPU5_VP3	0
guestintctlIPFDC_CPU6_VP0	0
guestintctlIPFDC_CPU6_VP1	0

1. 1 HIDED C CDITC VD0	
guestintctlIPFDC_CPU6_VP2	0
guestintctlIPFDC_CPU6_VP3	0
guestintctlIPFDC_CPU7_VP0	0
guestintctlIPFDC_CPU7_VP1	0
guestintctlIPFDC_CPU7_VP2	0
guestintctlIPFDC_CPU7_VP3	0
guestintctlIPPCI_CPU0_VP0	0
guestintctlIPPCI_CPU0_VP1	0
guestintctlIPPCI_CPU0_VP2	0
guestintctlIPPCI_CPU0_VP3	0
guestintctlIPPCI_CPU1_VP0	0
guestintctlIPPCI_CPU1_VP1	0
guestintctlIPPCI_CPU1_VP2	0
guestintctlIPPCI_CPU1_VP3	0
guestintctlIPPCI_CPU2_VP0	0
guestintctlIPPCI_CPU2_VP1	0
guestintctlIPPCI_CPU2_VP2	0
guestintctlIPPCI_CPU2_VP3	0
guestintctlIPPCI_CPU3_VP0	0
guestintctlIPPCI_CPU3_VP1	0
guestintctlIPPCI_CPU3_VP2	0
guestintctlIPPCI_CPU3_VP3	0
guestintctlIPPCI_CPU4_VP0	0
guestintctlIPPCI_CPU4_VP1	0
guestintctlIPPCI_CPU4_VP2	0
guestintctlIPPCI_CPU4_VP3	0
guestintctlIPPCI_CPU5_VP0	0
guestintctlIPPCI_CPU5_VP1	0
guestintctlIPPCI_CPU5_VP2	0
guestintctlIPPCI_CPU5_VP3	0
guestintctlIPPCI_CPU6_VP0	0
guestintctlIPPCI_CPU6_VP1	0
guestintctlIPPCI_CPU6_VP2	0
guestintctlIPPCI_CPU6_VP3	0
guestintctlIPPCI_CPU7_VP0	0
guestintctlIPPCI_CPU7_VP1	0
guestintctlIPPCI_CPU7_VP2	0
guestintctlIPPCI_CPU7_VP3	0
ISPRAM_SIZE	0
ISPRAM_BASE	0
ISPRAM_ENABLE	F
ISPRAM_FILE	
DSPRAM_SIZE	0
DSPRAM_BASE	0
DSPRAM_ENABLE	F

DSPRAM_PRESENT	F
USPRAM_SIZE	0
USPRAM_BASE	0
USPRAM_ENABLE	F
USPRAM_FILE	
misalignedDataException	never
commitTlbwErr	F

Table 8.6: Parameter values

## **Execution Modes**

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3

Table 9.1: Modes implemented in: CMP

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3
GUEST_KERNEL	4
GUEST_SUPERVISOR	5
GUEST_USER	6

Table 9.2: Modes implemented in: CPU

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3
GUEST_KERNEL	4
GUEST_SUPERVISOR	5
GUEST_USER	6

Table 9.3: Modes implemented in:  $\operatorname{VP}$ 

# Exceptions

Exception	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9
RI	10
$\mathrm{CpU}$	11
Ov	12
Tr	13
MSAFPE	14
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MSADis	21
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

Table 10.1: Exceptions implemented in: CMP  $\,$ 

Exception	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9
RI	10
CpU	11
Ov	12
Tr	13
MSAFPE	14
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MSADis	21
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

Table 10.2: Exceptions implemented in: CPU

Exception	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9

RI	10
CpU	11
Ov	12
Tr	13
MSAFPE	14
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MSADis	21
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

Table 10.3: Exceptions implemented in: VP

## Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.

OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

#### 11.1 Level 1: CMP

This level in the model hierarchy has 2 commands. This level in the model hierarchy has no register groups. This level in the model hierarchy has 4 children: CPU0, CPU1, CPU2 and CPU3.

## 11.2 Level 2: CPU

This level in the model hierarchy has 2 commands. This level in the model hierarchy has no register groups. This level in the model hierarchy has 2 children: CPU0\_VP0 and CPU0\_VP1.

## 11.3 Level 3: VP

This level in the model hierarchy has 20 commands. This level in the model hierarchy has 10 register groups:

Group name	Registers
Core	65
FPU	34

DSP	9
Shadow	64
COP0	172
MSA	40
CMP_GCR	36
CMP_CPC	14
CMP_GIC	721
Integration_support	1

Table 11.1: Register groups

This level in the model hierarchy has no children.

## **Model Commands**

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

## 12.1 Level 1: CMP

#### 12.1.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.1: isync command arguments

#### 12.1.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-memory	String	show memory accesses by this instruction. Ar-
		gument can be any combination of X (execute),
		L (load or store access) and S (system)
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-processorname	Boolean	Include processor name in all trace lines
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.2: itrace command arguments

## 12.2 Level 2: CPU

## 12.2.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.3: isync command arguments

#### 12.2.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-memory	String	show memory accesses by this instruction. Ar-
		gument can be any combination of X (execute),
		L (load or store access) and S (system)
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-processorname	Boolean	Include processor name in all trace lines
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.4: itrace command arguments

## 12.3 Level 3: VP

## 12.3.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.5: isync command arguments

#### 12.3.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing

-instructioncount	Boolean	include the instruction number in each trace
-memory	String	show memory accesses by this instruction. Ar-
		gument can be any combination of X (execute),
		L (load or store access) and S (system)
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-processorname	Boolean	Include processor name in all trace lines
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.6: itrace command arguments

## 12.3.3 mipsCOP0

query a COP0 register value using <register><select>

Argument	Type	Description
-register	Uns32	specify the COP0 register resource
-select	Uns32	specify the COP0 register select

Table 12.7: mipsCOP0 command arguments

## 12.3.4 mipsCacheDisable

#### 12.3.4.1 Argument description

Disables tag or full cache model

#### 12.3.5 mipsCacheEnable

enable tag or full cache model

Argument	Type	Description
-debug	Int32	set cache model debug flags
-full	Boolean	enable full cache model
-tag	Boolean	enable cache tag line only model

Table 12.8: mipsCacheEnable command arguments

#### 12.3.6 mipsCacheRatio

Report current hit ratio for selected cache

Argument	Type	Description
-dcache	Boolean	report hit ratio for dcache
-icache	Boolean	report hit ratio for icache

Table 12.9: mipsCacheRatio command arguments

## 12.3.7 mipsCacheReport

#### 12.3.7.1 Argument description

Report current cache statistics

#### 12.3.8 mipsCacheReset

#### 12.3.8.1 Argument description

reset the cache model

## 12.3.9 mipsCacheTrace

Control the tracing of cache accesses

Argument	Type	Description
-noartifact	Boolean	
-nocached	Boolean	
-nodcache	Boolean	
-noicache	Boolean	
-notrue	Boolean	
-nouncached	Boolean	
-off	Boolean	turn off the cache tracing
-on	Boolean	turn on the cache tracing

Table 12.10: mipsCacheTrace command arguments

## 12.3.10 mipsDebugFlags

Set the mips model debug value

Argument	Type	Description
-value	Uns32	specify mips model debug flags

Table 12.11: mipsDebugFlags command arguments

#### 12.3.11 mipsReadRegister

Read processor register using <resource><offset>

Argument	Type	Description
-offset	Uns32	the register offset
-resource	Uns32	the register resource

Table 12.12: mipsReadRegister command arguments

## 12.3.12 mipsReadTLBEntry

read a TLB entry specified by the index

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Argument	Type	Description
-index	Uns64	select the TLB entry

Table 12.13: mipsReadTLBEntry command arguments

#### 12.3.13 mipsTLBDump

#### 12.3.13.1 Argument description

Dumps the current contents of the TLB

## 12.3.14 mipsTLBDumpGuest

#### 12.3.14.1 Argument description

Dumps the current contents of the Guest TLB

#### 12.3.15 mipsTLBDumpRoot

#### 12.3.15.1 Argument description

Dumps the current contents of the Root TLB

#### 12.3.16 mipsTLBGetPhys

Reports the entry(s) in the TLB that match the given virtual address and ASID

Argument	Type	Description
-asid	Uns64	ASID
-va	Uns64	virtual address

Table 12.14: mipsTLBGetPhys command arguments

#### 12.3.17 mipsTraceGuest

control tracing of guest

Argument	Type	Description
-off	Boolean	stop tracing
-on	Boolean	start tracing

Table 12.15: mipsTraceGuest command arguments

## 12.3.18 mipsTraceRoot

control tracing on root processor

Argument	Type	Description
-off	Boolean	stop tracing
-on	Boolean	start tracing

Table 12.16: mipsTraceRoot command arguments

## 12.3.19 mipsWriteRegister

Write processor register using <resource><offset><value>

Argument	Type	Description
-offset	Uns32	the register offset
-resource	Uns32	the register resource
-value	Uns64	the value to write to register

Table 12.17: mipsWriteRegister command arguments

## 12.3.20 mipsWriteTLBEntry

Writes values to a TLB entry using the index, lo0, lo1, hi0 and mask fields

Argument	Type	Description
-hi0	Uns64	the TLB entry high address
-index	Uns64	the TLB entry index
-lo0	Uns64	the TLB entry low address 0
-lo1	Uns64	the TLB entry low address 1
-mask	Uns64	the TLB entry mask

Table 12.18: mipsWriteTLBEntry command arguments

# Registers

13.1 Level 1: CMP

No registers.

13.2 Level 2: CPU

No registers.

13.3 Level 3: VP

13.3.1 Core

Registers at level:3, type:VP group:Core

Name	Bits	Initial-Hex	RW	Description
zero	64	0	r-	constant zero
at	64	0	rw	
v0	64	0	rw	
v1	64	0	rw	
a0	64	0	rw	
a1	64	0	rw	
a2	64	0	rw	
a3	64	0	rw	
t0	64	0	rw	
t1	64	0	rw	
t2	64	0	rw	
t3	64	0	rw	
t4	64	0	rw	
t5	64	0	rw	
t6	64	0	rw	
t7	64	0	rw	
s0	64	0	rw	
s1	64	0	rw	
s2	64	0	rw	
s3	64	0	rw	
s4	64	0	rw	
s5	64	0	rw	
s6	64	0	rw	

s7	64	0	rw	
t8	64	0	rw	
t9	64	0	rw	
k0	64	0	rw	
k1	64	0	rw	
	64	0	rw	
gp sp	64	0	rw	stack pointer
sp s8	64	0	rw	frame pointer
ra	64	0	rw	trame pointer
pc	64	fffffff	rw	program counter
pc		bfc00000	1 W	program counter
r0	64	0	r-	constant zero
r1	64	0	rw	
r2	64	0	rw	
r3	64	0	rw	
r4	64	0	rw	
r5	64	0	rw	
r6	64	0	rw	
r7	64	0	rw	
r8	64	0	rw	
r9	64	0	rw	
r10	64	0	rw	
r11	64	0	rw	
r12	64	0	rw	
r13	64	0	rw	
r14	64	0	rw	
r15	64	0	rw	
r16	64	0	rw	
r17	64	0	rw	
r18	64	0	rw	
r19	64	0	rw	
r20	64	0	rw	
r21	64	0	rw	
r22	64	0	rw	
r23	64	0	rw	
r24	64	0	rw	
r25	64	0	rw	
r26	64	0	rw	
r27	64	0	rw	
r28	64	0	rw	
r29	64	0	rw	stack pointer
r30	64	0	rw	frame pointer
r31	64	0	rw	

Table 13.1: Registers at level 3, type:VP group:Core

## 13.3.2 FPU

Registers at level:3, type:VP group:FPU

Name	Bits	Initial-Hex	RW	Description
f0	64	0	rw	
f1	64	0	rw	
f2	64	0	rw	
f3	64	0	rw	
f4	64	0	rw	

f6         64         0         rw           f7         64         0         rw           f8         64         0         rw           f9         64         0         rw           f10         64         0         rw           f11         64         0         rw           f13         64         0         rw           f14         64         0         rw           f15         64         0         rw           f16         64         0         rw           f17         64         0         rw           f18         64         0         rw           f19         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f25         64         0         rw           f26         64         0         rw           f27         64         0         rw           f28         64         0         rw           f28         64         0	0~				
f7         64         0         rw           f8         64         0         rw           f9         64         0         rw           f10         64         0         rw           f11         64         0         rw           f12         64         0         rw           f13         64         0         rw           f15         64         0         rw           f16         64         0         rw           f17         64         0         rw           f18         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f25         64         0         rw           f26         64         0         rw           f27         64         0         rw           f28         64         0         rw           f29         64         0         rw           f28         64         0 <td>f5</td> <td>64</td> <td>0</td> <td>rw</td> <td></td>	f5	64	0	rw	
8         64         0         rw           f9         64         0         rw           f10         64         0         rw           f11         64         0         rw           f12         64         0         rw           f13         64         0         rw           f14         64         0         rw           f15         64         0         rw           f16         64         0         rw           f17         64         0         rw           f18         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f25         64         0         rw           f26         64         0         rw           f28         64         0         rw           f28         64         0         rw           f29         64         0         rw           f29         64         0 <td></td> <td>1</td> <td></td> <td>rw</td> <td></td>		1		rw	
f9         64         0         rw           f10         64         0         rw           f11         64         0         rw           f12         64         0         rw           f13         64         0         rw           f14         64         0         rw           f15         64         0         rw           f16         64         0         rw           f18         64         0         rw           f19         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f25         64         0         rw           f26         64         0         rw           f27         64         0         rw           f29         64         0         rw           f30         64         0         rw           f31         64         0         rw           foctor         foctor				rw	
fil         64         0         rw           fil         64         0<				rw	
fill         64         0         rw           fil2         64         0         rw           fil3         64         0         rw           fil4         64         0         rw           fil5         64         0         rw           fil6         64         0         rw           fil7         64         0         rw           fil9         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f24         64         0         rw           f25         64         0         rw           f26         64         0         rw           f28         64         0         rw           f29         64         0         rw           f31         64         0         rw           f8r         64         cools         rw         floating point status		64		rw	
f12         64         0         rw           f13         64         0         rw           f14         64         0         rw           f15         64         0         rw           f16         64         0         rw           f17         64         0         rw           f18         64         0         rw           f19         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f24         64         0         rw           f25         64         0         rw           f27         64         0         rw           f28         64         0         rw           f29         64         0         rw           f31         64         0         rw           for         64         0000         rw           f8r         64         0000         rw         floating point status		64	0	rw	
f13         64         0         rw           f14         64         0         rw           f15         64         0         rw           f16         64         0         rw           f17         64         0         rw           f18         64         0         rw           f19         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f24         64         0         rw           f25         64         0         rw           f26         64         0         rw           f28         64         0         rw           f29         64         0         rw           f31         64         0         rw           for         64         0         rw           for         64         0         rw		64	0	rw	
f14         64         0         rw           f15         64         0         rw           f16         64         0         rw           f17         64         0         rw           f18         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f24         64         0         rw           f25         64         0         rw           f26         64         0         rw           f28         64         0         rw           f29         64         0         rw           f30         64         0         rw           f31         64         0         rw           fsr         64         cools         rw         floating point status	f12	64	0	rw	
f15         64         0         rw           f16         64         0         rw           f17         64         0         rw           f18         64         0         rw           f19         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f25         64         0         rw           f26         64         0         rw           f27         64         0         rw           f29         64         0         rw           f30         64         0         rw           f31         64         0         rw         floating point status		1		rw	
f16         64         0         rw           f17         64         0         rw           f18         64         0         rw           f19         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f24         64         0         rw           f25         64         0         rw           f26         64         0         rw           f27         64         0         rw           f28         64         0         rw           f30         64         0         rw           f31         64         0         rw         floating point status	f14	64	0	rw	
f17         64         0         rw           f18         64         0         rw           f19         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f24         64         0         rw           f25         64         0         rw           f26         64         0         rw           f27         64         0         rw           f29         64         0         rw           f30         64         0         rw           f31         64         0         rw         floating point status	f15	64	0	rw	
f18         64         0         rw           f19         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f24         64         0         rw           f25         64         0         rw           f26         64         0         rw           f27         64         0         rw           f28         64         0         rw           f30         64         0         rw           f31         64         0         rw           fsr         64         coood         rw         floating point status		64	0	rw	
f19         64         0         rw           f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f24         64         0         rw           f25         64         0         rw           f26         64         0         rw           f27         64         0         rw           f28         64         0         rw           f30         64         0         rw           f31         64         0         rw           fsr         64         c0000         rw         floating point status				rw	
f20         64         0         rw           f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f24         64         0         rw           f25         64         0         rw           f26         64         0         rw           f27         64         0         rw           f28         64         0         rw           f29         64         0         rw           f30         64         0         rw           f31         64         0         rw           fsr         64         co000         rw         floating point status	f18	64	0	rw	
f21         64         0         rw           f22         64         0         rw           f23         64         0         rw           f24         64         0         rw           f25         64         0         rw           f26         64         0         rw           f27         64         0         rw           f28         64         0         rw           f29         64         0         rw           f30         64         0         rw           fsr         64         c0000         rw         floating point status		1		rw	
f22     64     0     rw       f23     64     0     rw       f24     64     0     rw       f25     64     0     rw       f26     64     0     rw       f27     64     0     rw       f28     64     0     rw       f29     64     0     rw       f30     64     0     rw       fsr     64     c0000     rw     floating point status		64	0	rw	
f23     64     0     rw       f24     64     0     rw       f25     64     0     rw       f26     64     0     rw       f27     64     0     rw       f28     64     0     rw       f30     64     0     rw       f31     64     0     rw       fsr     64     c0000     rw     floating point status				rw	
f24     64     0     rw       f25     64     0     rw       f26     64     0     rw       f27     64     0     rw       f28     64     0     rw       f29     64     0     rw       f30     64     0     rw       fsr     64     c0000     rw     floating point status	f22	64	0	rw	
f25     64     0     rw       f26     64     0     rw       f27     64     0     rw       f28     64     0     rw       f29     64     0     rw       f30     64     0     rw       fsr     64     c0000     rw     floating point status	f23	64	0	rw	
f26     64     0     rw       f27     64     0     rw       f28     64     0     rw       f29     64     0     rw       f30     64     0     rw       f31     64     0     rw       fsr     64     c0000     rw     floating point status	f24	64	0	rw	
f27     64     0     rw       f28     64     0     rw       f29     64     0     rw       f30     64     0     rw       f31     64     0     rw       fsr     64     c0000     rw     floating point status		64	0	rw	
f28     64     0     rw       f29     64     0     rw       f30     64     0     rw       f31     64     0     rw       fsr     64     c0000     rw     floating point status	f26	64	0	rw	
f29     64     0     rw       f30     64     0     rw       f31     64     0     rw       fsr     64     c0000     rw     floating point status		1		rw	
f30         64         0         rw           f31         64         0         rw           fsr         64         c0000         rw         floating point status				rw	
f31         64         0         rw           fsr         64         c0000         rw         floating point status		64	0	rw	
fsr 64 c0000 rw floating point status	f30	64	0	rw	
	f31	64	-	rw	
	fsr	64	c0000	rw	floating point status
	fir	64	20f30320	r-	floating point information

Table 13.2: Registers at level 3, type:VP group:FPU

## 13.3.3 DSP

Registers at level:3, type:VP group:DSP

Name	Bits	Initial-Hex	RW	Description
lo	64	0	rw	
hi	64	0	rw	
lo1	64	0	rw	
hi1	64	0	rw	
lo2	64	0	rw	
hi2	64	0	rw	
lo3	64	0	rw	
hi3	64	0	rw	
dspctl	64	0	rw	DSP control

Table 13.3: Registers at level 3, type:VP group:DSP

#### 13.3.4 Shadow

Registers at level:3, type:VP group:Shadow

Name	Bits	Initial-Hex	RW	Description	
zero[0]	64	0	r-	constant zero	

at[0]	64	0	rw	
v0[0]	64	0	rw	
v1[0]	64	0	rw	
a0[0]	64	0	rw	
a1[0]	64	0	rw	
a2[0]	64	0	rw	
a3[0]	64	0	rw	
t0[0]	64	0	rw	
t1[0]	64	0	rw	
t2[0]	64	0	rw	
t3[0]	64	0	rw	
t4[0]	64	0	rw	
t5[0]	64	0	rw	
t6[0]	64	0	rw	
t7[0]	64	0	_	
s0[0]	64	0	rw	
	64	0	rw	
s1[0] s2[0]	64	0	rw	
	64		rw	
s3[0]		0	rw	
s4[0]	64	0	rw	
s5[0]	64	0	rw	
s6[0]	64	0	rw	
s7[0]	64	0	rw	
t8[0]	64	0	rw	
t9[0]	64	0	rw	
k0[0]	64	0	rw	
k1[0]	64	0	rw	
[ [ ]				
gp[0]	64	0	rw	
sp[0]	64	0	rw rw	stack pointer
$\frac{\operatorname{sp}[0]}{\operatorname{s8}[0]}$	64 64	0	_	stack pointer frame pointer
sp[0] s8[0] ra[0]	64 64 64	0 0 0	rw	frame pointer
sp[0] s8[0] ra[0] r0[0]	64 64 64 64	0 0 0	rw rw	
sp[0] s8[0] ra[0] r0[0] r1[0]	64 64 64 64	0 0 0 0	rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0]	64 64 64 64 64	0 0 0 0 0	rw rw rw r-	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0]	64 64 64 64	0 0 0 0	rw rw rw r- rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0]	64 64 64 64 64	0 0 0 0 0	rw rw rw r- rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64	0 0 0 0 0 0	rw rw rw r- rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0]	64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0]	64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0]	64 64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0 0	rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r9[0] r10[0]	64 64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r9[0] r10[0] r11[0] r12[0]	64 64 64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r13[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r13[0] r14[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0]   s8[0]   ra[0]   ra[0]   ra[0]   ra[0]   r2[0]   r3[0]   r4[0]   r5[0]   r6[0]   r7[0]   r8[0]   r10[0]   r11[0]   r12[0]   r13[0]   r14[0]   r15[0]   r3[0]   r15[0]   r15[0]   r3[0]   r15[0]   r15[0]   r3[0]   r3[0]   r15[0]   r3[0]   r3[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0]   s8[0]   ra[0]   ra[0]   ra[0]   ra[0]   r2[0]   r3[0]   r4[0]   r5[0]   r6[0]   r7[0]   r8[0]   r10[0]   r11[0]   r12[0]   r13[0]   r14[0]   r15[0]   r16[0]   rage    rag	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0]   s8[0]   ra[0]   ra[0	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r14[0] r15[0] r15[0] r16[0] r17[0] r18[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r14[0] r15[0] r15[0] r16[0] r17[0] r18[0] r19[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0]   sp[0]   sp[0]   sp[0]   ra[0]   ra[0	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r14[0] r15[0] r15[0] r15[0] r16[0] r17[0] r18[0] r19[0] r20[0] r21[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r9[0] r11[0] r12[0] r14[0] r15[0] r15[0] r15[0] r16[0] r17[0] r18[0] r19[0] r20[0] r22[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0]   s8[0]   ra[0]   ra[0	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer

r25[0]	64	0	rw	
r26[0]	64	0	rw	
r27[0]	64	0	rw	
r28[0]	64	0	rw	
r29[0]	64	0	rw	stack pointer
r30[0]	64	0	rw	frame pointer
r31[0]	64	0	rw	

Table 13.4: Registers at level 3, type:VP group:Shadow

## 13.3.5 COP0

Registers at level:3, type:VP group:COP0

Name	Bits	Initial-Hex	RW	Description
sr	64	4400004	rw	CP0 register 12/0 (status)
bad	64	0	rw	CP0 register 8/0 (badvaddr)
cause	64	0	rw	CP0 register 13/0 (cause)
index	64	0	rw	CP0 register 0/0
vpcontrol	64	0	rw	CP0 register 0/4
entrylo0	64	0	rw	CP0 register 2/0
entrylo1	64	0	rw	CP0 register 3/0
globalnumber	64	0	rw	CP0 register 3/1
context	64	0	rw	CP0 register 4/0
userlocal	64	0	rw	CP0 register 4/2
debugcontextid	64	0	rw	CP0 register 4/4
pagemask	64	0	rw	CP0 register 5/0
pagegrain	64	c8000000	rw	CP0 register 5/1
wired	64	0	rw	CP0 register 6/0
hwrena	64	0	rw	CP0 register 7/0
badvaddr	64	0	rw	CP0 register 8/0
badinstr	64	0	rw	CP0 register 8/1
badinstrp	64	0	rw	CP0 register 8/2
count	64	0	rw	CP0 register 9/0
entryhi	64	0	rw	CP0 register 10/0
guestctl1	64	0	rw	CP0 register 10/4
guestctl2	64	0	rw	CP0 register 10/5
guestctl3	64	0	rw	CP0 register 10/6
compare	64	0	rw	CP0 register 11/0
guestctl0ext	64	80	rw	CP0 register 11/4
status	64	4400004	rw	CP0 register 12/0
intctl	64	e0000000	rw	CP0 register 12/1
srsctl	64	0	rw	CP0 register 12/2
srsmap	64	0	rw	CP0 register 12/3
guestctl0	64	c4c0080	rw	CP0 register 12/6
gtoffset	64	0	rw	CP0 register 12/7
ерс	64	0	rw	CP0 register 14/0
prid	64	1a900	rw	CP0 register 15/0
ebase	64	fffffff	rw	CP0 register 15/1
		80000000		
cdmmbase	64	2	rw	CP0 register $15/2$
cmgcrbase	64	1fbf800	rw	CP0 register 15/3
config	64	8000ca02	rw	CP0 register 16/0
config1	64	9eab5593	rw	CP0 register 16/1
config2	64	80000000	rw	CP0 register 16/2
config3	64	fc8031a9	rw	CP0 register 16/3

0.4	0.4	106.000		CDO 1 10/4
config4	64	d0fc0227	rw	CP0 register 16/4
config5	64	2c98	rw	CP0 register 16/5
config7	64	80000000	rw	CP0 register 16/7
lladdr	64	0	rw	CP0 register 17/0
maar	64	0	rw	CP0 register $17/1$
maari	64	0	rw	CP0 register 17/2
xcontext	64	0	rw	CP0 register $20/0$
debug	64	2030000	rw	CP0 register 23/0
tracecontrol	64	0	rw	CP0 register 23/1
tracecontrol2	64	0	rw	CP0 register 23/2
usertracedata	64	0	rw	CP0 register 23/3
traceibpc	64	0	rw	CP0 register 23/4
tracedbpc	64	0	rw	CP0 register 23/5
ibp2_3_action	64	0	rw	CP0 register 23/7
depc	64	0	rw	CP0 register 24/0
dbp2_3_action	64	0	rw	CP0 register 24/1
tracecontrol3	64	0	rw	CP0 register 24/2
usertracedata2	64	0	rw	CP0 register 24/3
tcbconfig	64	0	rw	CP0 register 24/4
tcbcontrole	64	0	rw	CP0 register 24/5
ibp4_5_action	64	0	rw	CP0 register 24/6
ibp6_7_action	64	0	rw	CP0 register 24/7
perfctl0	64	80000000	rw	CP0 register 25/0
perfect0	64	0	rw	CPO register 25/1
perfettl	64	80000000		CPO register 25/2
perfcnt1	64	0	rw	CPO register 25/3
-	-	-	rw	
perfctl2	64	80000000	rw	CP0 register 25/4
perfcnt2	64	0	rw	CP0 register 25/5
perfctl3	64	0	rw	CP0 register 25/6
perfcnt3	64	0	rw	CP0 register 25/7
errctl	64	0	rw	CP0 register 26/0
tcbcontrold	64	0	rw	CP0 register 26/4
cacheerr	64	0	rw	CP0 register 27/0
itaglo	64	0	rw	CP0 register $28/0$
idatalo	64	0	rw	CP0 register 28/1
dtaglo	64	0	rw	CP0 register 28/2
ddatalo	64	0	rw	CP0 register 28/3
idatahi	64	0	rw	CP0 register 29/1
ddatahi	64	0	rw	CP0 register 29/3
errorepc	64	0	rw	CP0 register 30/0
desave	64	0	rw	CP0 register 31/0
kscratch1	64	0	rw	CP0 register 31/2
kscratch2	64	0	rw	CP0 register 31/3
kscratch3	64	0	rw	CP0 register 31/4
kscratch4	64	0	rw	CP0 register 31/5
kscratch5	64	0	rw	CP0 register 31/6
kscratch6	64	0	rw	CP0 register 31/7
guestindex	64	0	rw	CP0 guest register 0/0
guestvpcontrol	64	0	rw	CP0 guest register 0/4
guestentrylo0	64	0	rw	CP0 guest register 2/0
guestentrylo1	64	0	rw	CP0 guest register 3/0
guestglobalnumber	64	0	rw	CP0 guest register 3/1
guestcontext	64	0	_	CP0 guest register 4/0
guestuserlocal	64	0	rw	CP0 guest register 4/0 CP0 guest register 4/2
_	64		rw	
guestdebugcontextid guestpagemask	64	0	rw	CP0 guest register 4/4 CP0 guest register 5/0
guestpagemask	04	U	rw	Of a green fediener 9/0

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guestpagegrain	64	c8000000	rw	CP0 guest register 5/1
guestwired	64	0	rw	CP0 guest register 6/0
guesthwrena	64	0	rw	CP0 guest register 7/0
guestbadvaddr	64	0	rw	CP0 guest register 8/0
guestbadinstr	64	0	rw	CP0 guest register 8/1
guestbadinstrp	64	0	rw	CP0 guest register 8/2
guestcount	64	0	rw	CP0 guest register 9/0
guestentryhi	64	0	rw	CP0 guest register 10/0
guestguestctl1	64	0	rw	CP0 guest register 10/4
guestguestctl2	64	0	rw	CP0 guest register 10/5
guestguestctl3	64	0	rw	CP0 guest register 10/6
guestcompare	64	0	rw	CP0 guest register 11/0
guestguestctl0ext	64	0	rw	CP0 guest register 11/4
gueststatus	64	4400004	rw	CP0 guest register 12/0
guestintctl	64	e0000000	rw	CP0 guest register 12/1
guestsrsctl	64	0	rw	CP0 guest register 12/2
guestsrsmap	64	0	rw	CP0 guest register 12/3
guestguestctl0	64	0	rw	CP0 guest register 12/6
guestgtoffset	64	0	rw	CP0 guest register 12/7
guestcause	64	0	rw	CP0 guest register 13/0
guestepc	64	0	rw	CP0 guest register 14/0
guestprid	64	0	rw	CP0 guest register 15/0
guestebase	64	fffffff	rw	CP0 guest register 15/1
guesiesase	01	80000000	1 **	CI o guest register 10/1
guestcdmmbase	64	0	rw	CP0 guest register 15/2
guestcmgcrbase	64	0	rw	CP0 guest register 15/3
guestconfig	64	8000ca02	rw	CP0 guest register 16/0
guestconfig1	64	9eab5593	rw	CP0 guest register 16/1
guestconfig2	64	80000000	_	CP0 guest register 16/2
guestconfig3	64	dc003121	rw	CP0 guest register 16/3
guestconfig4	64	d0fc0227	rw	CP0 guest register 16/3 CP0 guest register 16/4
guestconfig5	64	2c98	rw	CP0 guest register 16/5
			rw	- ,
guestconfig7	64	0	rw	CP0 guest register 16/7
guestlladdr	64	0	rw	CP0 guest register 17/0
guestmaar	64	0	rw	CP0 guest register 17/1
guestmaari	64	0	rw	CP0 guest register 17/2
guestxcontext	64	0	rw	CP0 guest register 20/0
guestdebug	64	0	rw	CP0 guest register 23/0
guesttracecontrol	64	0	rw	CP0 guest register 23/1
guesttracecontrol2	64	0	rw	CP0 guest register 23/2
guestusertracedata	64	0	rw	CP0 guest register 23/3
guesttraceibpc	64	0	rw	CP0 guest register 23/4
guesttracedbpc	64	0	rw	CP0 guest register 23/5
guestibp2_3_action	64	0	rw	CP0 guest register 23/7
guestdepc	64	0	rw	CP0 guest register 24/0
guestdbp2_3_action	64	0	rw	CP0 guest register 24/1
guesttracecontrol3	64	0	rw	CP0 guest register 24/2
guestusertracedata2	64	0	rw	CP0 guest register 24/3
guesttcbconfig	64	0	rw	CP0 guest register 24/4
guesttcbcontrole	64	0	rw	CP0 guest register 24/5
guestibp4_5_action	64	0	rw	CP0 guest register 24/6
guestibp6_7_action	64	0	rw	CP0 guest register 24/7
guestperfctl0	64	80000000	rw	CP0 guest register 25/0
guestperfcnt0	64	0	rw	CP0 guest register 25/1
guestperfetl1	64	80000000	rw	CP0 guest register 25/2
guestperfent1	64	0	rw	CP0 guest register 25/3
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guestperfctl2	64	80000000	rw	CP0 guest register 25/4
guestperfcnt2	64	0	rw	CP0 guest register 25/5
guestperfctl3	64	0	rw	CP0 guest register 25/6
guestperfcnt3	64	0	rw	CP0 guest register 25/7
guesterrctl	64	0	rw	CP0 guest register 26/0
guesttcbcontrold	64	0	rw	CP0 guest register 26/4
guestcacheerr	64	0	rw	CP0 guest register 27/0
guestitaglo	64	0	rw	CP0 guest register 28/0
guestidatalo	64	0	rw	CP0 guest register 28/1
guestdtaglo	64	0	rw	CP0 guest register 28/2
guestddatalo	64	0	rw	CP0 guest register 28/3
guestidatahi	64	0	rw	CP0 guest register 29/1
guestddatahi	64	0	rw	CP0 guest register 29/3
guesterrorepc	64	0	rw	CP0 guest register 30/0
guestdesave	64	0	rw	CP0 guest register 31/0
guestkscratch1	64	0	rw	CP0 guest register 31/2
guestkscratch2	64	0	rw	CP0 guest register 31/3
guestkscratch3	64	0	rw	CP0 guest register 31/4
guestkscratch4	64	0	rw	CP0 guest register 31/5
guestkscratch5	64	0	rw	CP0 guest register 31/6
guestkscratch6	64	0	rw	CP0 guest register 31/7

Table 13.5: Registers at level 3, type:VP group:COP0

## 13.3.6 MSA

Registers at level:3, type:VP group:MSA

Name	Bits	Initial-Hex	RW	Description
w0	128	-	rw	
w1	128	-	rw	
w2	128	-	rw	
w3	128	-	rw	
w4	128	-	rw	
w5	128	-	rw	
w6	128	-	rw	
w7	128	-	rw	
w8	128	-	rw	
w9	128	-	rw	
w10	128	-	rw	
w11	128	-	rw	
w12	128	-	rw	
w13	128	-	rw	
w14	128	-	rw	
w15	128	-	rw	
w16	128	-	rw	
w17	128	-	rw	
w18	128	-	rw	
w19	128	-	rw	
w20	128	-	rw	
w21	128	-	rw	
w22	128	-	rw	
w23	128	-	rw	
w24	128	-	rw	
w25	128	-	rw	
w26	128	-	rw	

w27	128	-	rw	
w28	128	-	rw	
w29	128	-	rw	
w30	128	-	rw	
w31	128	-	rw	
msair	64	320	r-	MSA implementation
msacsr	64	0	rw	MSA control and status
msaaccess	64	-	r-	MSA access
msasave	64	-	r-	MSA save
msamodify	64	-	r-	MSA modify
msarequest	64	-	r-	MSA request
msamap	64	-	r-	MSA map
msaunmap	64	-	r-	MSA unmap

Table 13.6: Registers at level 3, type:VP group:MSA

## 13.3.7 CMP\_GCR

Registers at level:3, type: VP group:CMP\_GCR

Name	Bits	Initial-Hex	RW	Description
GCR_CONFIG	64	3	r-	-
GCR_BASE	64	1fbf8000	r-	
GCR_BASE_UPPER	64	0	rw	
GCR_CONTROL	64	40200000	rw	
GCR_REV	64	800	r-	
GCR_ERROR_CONTROL	64	13	rw	
GCR_ERROR_MASK	64	0	rw	
GCR_ERROR_CAUSE	64	0	r-	
GCR_ERROR_ADDR	64	0	r-	
GCR_ERROR_ADDR_UPPER	64	0	_	
GCR_ERROR_MULT	64	0	r-	
GCR_CUSTOM_BASE	64	0	rw	
GCR_CUSTOM_STATUS	64	0	r-	
GCR_GIC_BASE	64	0	rw	
GCR_GIC_BASE_UPPER	64	0	rw	
GCR_CPC_BASE	64	0	rw	
GCR_CPC_BASE_UPPER	64	0	rw	
GCR_GIC_STATUS	64	1	r-	
GCR_CACHE_REV	64	0	r-	
GCR_CPC_STATUS	64	1	r-	
GCR_ACCESS	64	3f	rw	
GCR_L2_CONFIG	64	84003507	rw	
GCR_SYS_CONFIG2	64	4	r-	
GCR_IOCU1_REV	64	400	r-	
GCR_BEV_BASE	64	bfc00000	rw	
GCR_MMIO_REQ_LIMIT	64	0	rw	
GCR_CL_COHERENCE	64	0	rw	
GCR_CL_CONFIG	64	1	r-	
GCR_CL_OTHER	64	0	rw	
GCR_CL_RESET_BASE	64	bfc00001	rw	
GCR_CL_ID	64	0	r-	
GCR_CO_COHERENCE	64	0	rw	
GCR_CO_CONFIG	64	1	r-	
GCR_CO_OTHER	64	0	rw	
GCR_CO_RESET_BASE	64	bfc00001	rw	

GCR_CO_ID	64	0	r-	

Table 13.7: Registers at level 3, type:VP group:CMP\_GCR

## 13.3.8 CMP\_CPC

Registers at level:3, type:VP group:CMP\_CPC

Name	Bits	Initial-Hex	RW	Description
CPC_SEQDEL	64	0	rw	
CPC_RAIL	64	0	rw	
CPC_RESETLEN	64	0	rw	
CPC_REVISION	64	0	r-	
CPC_CMD	64	3	rw	
CPC_STAT_CONF	64	b37203	rw	
CPC_CL_VP_STOP	64	0	rw	
CPC_CL_VP_RUN	64	1	rw	
CPC_CL_VP_RUNNING	64	1	r-	
CPC_CMD	64	3	rw	
CPC_STAT_CONF	64	b37203	rw	
CPC_CO_VP_STOP	64	0	rw	
CPC_CO_VP_RUN	64	1	rw	
CPC_CO_VP_RUNNING	64	1	r-	

Table 13.8: Registers at level 3, type:VP group:CMP\_CPC

## 13.3.9 CMP\_GIC

Registers at level:3, type: VP group:CMP\_GIC

Name	Bits	Initial-Hex	RW	Description
GIC_SH_CONFIG	64	980f0007	rw	
GIC_Counter	64	0	rw	
GIC_SH_REVISION	64	500	r-	
GIC_SH_POL63_0	64	0	rw	
GIC_SH_POL127_64	64	0	rw	
GIC_SH_POL191_128	64	0	rw	
GIC_SH_POL255_192	64	0	rw	
GIC_SH_TRIG63_0	64	0	rw	
GIC_SH_TRIG127_64	64	0	rw	
GIC_SH_TRIG191_128	64	0	rw	
GIC_SH_TRIG255_192	64	0	rw	
GIC_SH_DUAL63_0	64	0	rw	
GIC_SH_DUAL127_64	64	0	rw	
GIC_SH_DUAL191_128	64	0	rw	
GIC_SH_DUAL255_192	64	0	rw	
GIC_SH_WEDGE	64	0	-w	
GIC_SH_RMASK63_0	64	0	-w	
GIC_SH_RMASK127_64	64	0	-w	
GIC_SH_RMASK191_128	64	0	-w	
GIC_SH_RMASK255_192	64	0	-w	
GIC_SH_SMASK63_0	64	0	-w	
GIC_SH_SMASK127_64	64	0	-w	
GIC_SH_SMASK191_128	64	0	-w	
GIC_SH_SMASK255_192	64	0	-w	

GIC_SH_MASK63_0	64	0	r-	
GIC_SH_MASK127_64	64	0	r-	
GIC_SH_MASK191_128	64	0	r-	
GIC_SH_MASK255_192	64	0	r-	
GIC_SH_PEND63_0	64	0	r-	
GIC_SH_PEND127_64	64	0	r-	
GIC_SH_PEND191_128	64	0	r-	
GIC_SH_PEND255_192	64	0	r-	
GIC_SH_MAP000_PIN	64	80000000	rw	
GIC_SH_MAP001_PIN	64	80000000	rw	
GIC_SH_MAP002_PIN	64	80000000	rw	
GIC_SH_MAP003_PIN	64	80000000	rw	
GIC_SH_MAP004_PIN	64	80000000	rw	
GIC_SH_MAP005_PIN	64	80000000	rw	
GIC_SH_MAP006_PIN	64	80000000	rw	
GIC_SH_MAP007_PIN	64	80000000	rw	
GIC_SH_MAP008_PIN	64	80000000	rw	
GIC_SH_MAP009_PIN	64	80000000	rw	
GIC_SH_MAP010_PIN	64	80000000	rw	
GIC_SH_MAP011_PIN	64	80000000	rw	
GIC_SH_MAP012_PIN	64	80000000	rw	
GIC_SH_MAP013_PIN	64	80000000	rw	
GIC_SH_MAP014_PIN	64	80000000	rw	
GIC_SH_MAP015_PIN	64	80000000	rw	
GIC_SH_MAP016_PIN	64	80000000	rw	
GIC_SH_MAP017_PIN	64	80000000		
GIC_SH_MAP018_PIN	64	80000000	rw	
GIC_SH_MAP019_PIN	64	80000000	rw	
GIC_SH_MAP020_PIN	64	80000000	rw	
GIC_SH_MAP021_PIN	64	80000000	rw	
GIC_SH_MAP021_FIN	64	80000000	rw	
GIC_SH_MAP023_PIN	64	80000000	rw	
GIC_SH_MAP023_FIN	64		rw	
		80000000 80000000	rw	
GIC_SH_MAP025_PIN	64		rw	
GIC_SH_MAP026_PIN	64	80000000	rw	
GIC_SH_MAP027_PIN	64	80000000	rw	
GIC_SH_MAP028_PIN	64	80000000	rw	
GIC_SH_MAP029_PIN	64	80000000	rw	
GIC_SH_MAP030_PIN	64	80000000	rw	
GIC_SH_MAP031_PIN	64	80000000	rw	
GIC_SH_MAP032_PIN	64	80000000	rw	
GIC_SH_MAP033_PIN	64	80000000	rw	
GIC_SH_MAP034_PIN	64	80000000	rw	
GIC_SH_MAP035_PIN	64	80000000	rw	
GIC_SH_MAP036_PIN	64	80000000	rw	
GIC_SH_MAP037_PIN	64	80000000	rw	
GIC_SH_MAP038_PIN	64	80000000	rw	
GIC_SH_MAP039_PIN	64	80000000	rw	
GIC_SH_MAP040_PIN	64	80000000	rw	
GIC_SH_MAP041_PIN	64	80000000	rw	
GIC_SH_MAP042_PIN	64	80000000	rw	
GIC_SH_MAP043_PIN	64	80000000	rw	
GIC_SH_MAP044_PIN	64	80000000	rw	
GIC_SH_MAP045_PIN	64	80000000	rw	
GIC_SH_MAP046_PIN	64	80000000	rw	
GIC_SH_MAP047_PIN	64	80000000	rw	
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GIC_SH_MAP048_PIN	64	80000000	rw	
GIC_SH_MAP049_PIN	64	80000000	rw	
GIC_SH_MAP050_PIN	64	80000000	rw	
GIC_SH_MAP051_PIN	64	80000000	rw	
GIC_SH_MAP052_PIN	64	80000000	rw	
GIC_SH_MAP053_PIN	64	80000000	rw	
GIC_SH_MAP054_PIN	64	80000000	rw	
GIC_SH_MAP055_PIN	64	80000000	rw	
GIC_SH_MAP056_PIN	64	80000000	rw	
GIC_SH_MAP057_PIN	64	80000000	rw	
GIC_SH_MAP058_PIN	64	80000000	rw	
GIC_SH_MAP059_PIN	64	80000000	rw	
GIC_SH_MAP060_PIN	64	80000000	rw	
GIC_SH_MAP061_PIN	64	80000000	rw	
GIC_SH_MAP062_PIN	64	80000000	rw	
GIC_SH_MAP063_PIN	64	80000000	rw	
GIC_SH_MAP064_PIN	64	80000000	rw	
GIC_SH_MAP065_PIN	64	80000000	rw	
GIC_SH_MAP066_PIN	64	80000000	rw	
GIC_SH_MAP067_PIN	64	80000000	rw	
GIC_SH_MAP068_PIN	64	80000000	rw	
GIC_SH_MAP069_PIN	64	80000000	rw	
GIC_SH_MAP070_PIN	64	80000000	rw	
GIC_SH_MAP071_PIN	64	80000000	rw	
GIC_SH_MAP072_PIN	64	80000000	rw	
GIC_SH_MAP073_PIN	64	80000000	rw	
GIC_SH_MAP074_PIN	64	80000000	rw	
GIC_SH_MAP075_PIN	64	80000000	rw	
GIC_SH_MAP076_PIN	64	80000000	rw	
GIC_SH_MAP077_PIN	64	80000000	rw	
GIC_SH_MAP078_PIN	64	80000000	rw	
GIC_SH_MAP079_PIN	64	80000000	rw	
GIC_SH_MAP080_PIN	64	80000000	rw	
GIC_SH_MAP081_PIN	64	80000000	rw	
GIC_SH_MAP082_PIN	64	80000000	rw	
GIC_SH_MAP083_PIN	64	80000000	rw	
GIC_SH_MAP084_PIN	64	80000000	rw	
GIC_SH_MAP085_PIN	64	80000000	rw	
GIC_SH_MAP086_PIN	64	80000000	rw	
GIC_SH_MAP087_PIN	64	80000000	rw	
GIC_SH_MAP088_PIN	64	80000000	rw	
GIC_SH_MAP089_PIN	64	80000000	rw	
GIC_SH_MAP090_PIN	64	80000000	rw	
GIC_SH_MAP091_PIN	64	80000000	rw	
GIC_SH_MAP092_PIN	64	80000000	rw	
GIC_SH_MAP093_PIN	64	80000000	rw	
GIC_SH_MAP094_PIN	64	80000000	rw	
GIC_SH_MAP095_PIN	64	80000000	rw	
GIC_SH_MAP096_PIN	64	80000000	rw	
GIC_SH_MAP097_PIN	64	80000000	rw	
GIC_SH_MAP098_PIN	64	80000000	rw	
GIC_SH_MAP099_PIN	64	80000000	rw	
GIC_SH_MAP100_PIN	64	80000000	rw	
GIC_SH_MAP101_PIN	64	80000000	rw	
GIC_SH_MAP102_PIN	64	80000000	rw	
GIC_SH_MAP103_PIN	64	80000000	rw	
~10-011-11111 100-1 111	01	3000000	- *v	

GIC_SH_MAP104_PIN	64	80000000	rw	
GIC_SH_MAP105_PIN	64	80000000	rw	
GIC_SH_MAP106_PIN	64	80000000	rw	
GIC_SH_MAP107_PIN	64	80000000	rw	
GIC_SH_MAP108_PIN	64	80000000	rw	
GIC_SH_MAP109_PIN	64	80000000	rw	
GIC_SH_MAP110_PIN	64	80000000	rw	
GIC_SH_MAP111_PIN	64	80000000	rw	
GIC_SH_MAP112_PIN	64	80000000	rw	
GIC_SH_MAP113_PIN	64	80000000	rw	
GIC_SH_MAP114_PIN	64	80000000	rw	
GIC_SH_MAP115_PIN	64	80000000	rw	
GIC_SH_MAP116_PIN	64	80000000	rw	
GIC_SH_MAP117_PIN	64	80000000	rw	
GIC_SH_MAP118_PIN	64	80000000	rw	
GIC_SH_MAP119_PIN	64	80000000	rw	
GIC_SH_MAP120_PIN	64	80000000	rw	
GIC SH MAP121 PIN	64	80000000	rw	
GIC_SH_MAP122_PIN	64	80000000	rw	
GIC_SH_MAP123_PIN	64	80000000	rw	
GIC_SH_MAP124_PIN	64	80000000	rw	
GIC_SH_MAP125_PIN	64	80000000	rw	
GIC-SH_MAP126_PIN	64	80000000	rw	
GIC_SH_MAP127_PIN	64	80000000	rw	
GIC_SH_MAP128_PIN	64	0	rw	
GIC_SH_MAP129_PIN	64	0	rw	
GIC_SH_MAP130_PIN	64	0	rw	
GIC_SH_MAP131_PIN	64	0	rw	
GIC_SH_MAP132_PIN	64	0	rw	
GIC-SH-MAP133-PIN	64	0	rw	
GIC_SH_MAP134_PIN	64	0	rw	
GIC_SH_MAP135_PIN	64	0	rw	
GIC_SH_MAP136_PIN	64	0		
GIC_SH_MAP137_PIN	64	0	rw	
GIC_SH_MAP138_PIN	64	0	rw	
GIC_SH_MAP139_PIN	64	0	rw	
GIC_SH_MAP140_PIN	64	-	rw	
GIC_SH_MAP141_PIN	64	0	rw	
		_	rw	
GIC_SH_MAP142_PIN	64	0	rw	
GIC_SH_MAP143_PIN	64	0	rw	
GIC_SH_MAP144_PIN	64	0	rw	
GIC_SH_MAP145_PIN	64	0	rw	
GIC_SH_MAP146_PIN	64	0	rw	
GIC_SH_MAP147_PIN	64	0	rw	
GIC_SH_MAP148_PIN	64	0	rw	
GIC_SH_MAP149_PIN	64	0	rw	
GIC_SH_MAP150_PIN	64	0	rw	
GIC_SH_MAP151_PIN	64	0	rw	
GIC_SH_MAP152_PIN	64	0	rw	
GIC_SH_MAP153_PIN	64	0	rw	
GIC_SH_MAP154_PIN	64	0	rw	
GIC_SH_MAP155_PIN	64	0	rw	
GIC_SH_MAP156_PIN	64	0	rw	
GIC_SH_MAP157_PIN	64	0	rw	
GIC_SH_MAP158_PIN	64	0	rw	
GIC_SH_MAP159_PIN	64	0	rw	

		ı	1	
GIC_SH_MAP160_PIN	64	0	rw	
GIC_SH_MAP161_PIN	64	0	rw	
GIC_SH_MAP162_PIN	64	0	rw	
GIC_SH_MAP163_PIN	64	0	rw	
GIC_SH_MAP164_PIN	64	0	rw	
GIC_SH_MAP165_PIN	64	0	rw	
GIC_SH_MAP166_PIN	64	0	rw	
GIC_SH_MAP167_PIN	64	0	rw	
GIC_SH_MAP168_PIN	64	0	rw	
GIC_SH_MAP169_PIN	64	0	rw	
GIC_SH_MAP170_PIN	64	0	rw	
GIC_SH_MAP171_PIN	64	0	rw	
GIC_SH_MAP172_PIN	64	0	rw	
GIC_SH_MAP173_PIN	64	0	rw	
GIC_SH_MAP174_PIN	64	0	rw	
GIC_SH_MAP175_PIN	64	0	rw	
GIC_SH_MAP176_PIN	64	0	rw	
GIC_SH_MAP177_PIN	64	0	rw	
GIC_SH_MAP178_PIN	64	0	rw	
GIC_SH_MAP179_PIN	64	0	rw	
GIC_SH_MAP180_PIN	64	0	rw	
GIC_SH_MAP181_PIN	64	0		
GIC_SH_MAP182_PIN	64	0	rw	
GIC_SH_MAP182_FIN	64	0	rw	
			rw	
GIC_SH_MAP184_PIN	64	0	rw	
GIC_SH_MAP185_PIN	64	0	rw	
GIC_SH_MAP186_PIN	64	0	rw	
GIC_SH_MAP187_PIN	64	0	rw	
GIC_SH_MAP188_PIN	64	0	rw	
GIC_SH_MAP189_PIN	64	0	rw	
GIC_SH_MAP190_PIN	64	0	rw	
GIC_SH_MAP191_PIN	64	0	rw	
GIC_SH_MAP192_PIN	64	0	rw	
GIC_SH_MAP193_PIN	64	0	rw	
GIC_SH_MAP194_PIN	64	0	rw	
GIC_SH_MAP195_PIN	64	0	rw	
GIC_SH_MAP196_PIN	64	0	rw	
GIC_SH_MAP197_PIN	64	0	rw	
GIC_SH_MAP198_PIN	64	0	rw	
GIC_SH_MAP199_PIN	64	0	rw	
GIC_SH_MAP200_PIN	64	0	rw	
GIC_SH_MAP201_PIN	64	0	rw	
GIC_SH_MAP202_PIN	64	0	rw	
GIC_SH_MAP203_PIN	64	0	rw	
GIC_SH_MAP204_PIN	64	0	rw	
GIC_SH_MAP205_PIN	64	0	rw	
GIC_SH_MAP206_PIN	64	0	rw	
GIC_SH_MAP207_PIN	64	0	rw	
GIC_SH_MAP208_PIN	64	0	rw	
GIC_SH_MAP209_PIN	64	0	rw	
GIC_SH_MAP210_PIN	64	0	rw	
GIC_SH_MAP211_PIN	64	0	rw	
GIC_SH_MAP212_PIN	64	0		
GIC_SH_MAP213_PIN	64	0	rw	
			rw	
GIC_SH_MAP214_PIN GIC_SH_MAP215_PIN	64	0	rw	
GIO_5H_MAY215_PIN	64	U	rw	

GIC_SH_MAP216_PIN	64	0	rw	
GIC_SH_MAP217_PIN	64	0	rw	
GIC_SH_MAP218_PIN	64	0	rw	
GIC_SH_MAP219_PIN	64	0	rw	
GIC_SH_MAP220_PIN	64	0	rw	
GIC_SH_MAP221_PIN	64	0	rw	
GIC_SH_MAP222_PIN	64	0	rw	
GIC_SH_MAP223_PIN	64	0	rw	
GIC_SH_MAP224_PIN	64	0	rw	
GIC_SH_MAP225_PIN	64	0	rw	
GIC_SH_MAP226_PIN	64	0	rw	
GIC_SH_MAP227_PIN	64	0	rw	
GIC_SH_MAP228_PIN	64	0	rw	
GIC_SH_MAP229_PIN	64	0		
GIC_SH_MAP230_PIN	64		rw	
	64	0	rw	
GIC_SH_MAP231_PIN	-	0	rw	
GIC_SH_MAP232_PIN	64	0	rw	
GIC_SH_MAP233_PIN	64	0	rw	
GIC_SH_MAP234_PIN	64	0	rw	
GIC_SH_MAP235_PIN	64	0	rw	
GIC_SH_MAP236_PIN	64	0	rw	
GIC_SH_MAP237_PIN	64	0	rw	
GIC_SH_MAP238_PIN	64	0	rw	
GIC_SH_MAP239_PIN	64	0	rw	
GIC_SH_MAP240_PIN	64	0	rw	
GIC_SH_MAP241_PIN	64	0	rw	
GIC_SH_MAP242_PIN	64	0	rw	
GIC_SH_MAP243_PIN	64	0	rw	
GIC_SH_MAP244_PIN	64	0	rw	
GIC_SH_MAP245_PIN	64	0	rw	
GIC_SH_MAP246_PIN	64	0	rw	
GIC_SH_MAP247_PIN	64	0	rw	
GIC_SH_MAP248_PIN	64	0	rw	
GIC_SH_MAP249_PIN	64	0	rw	
GIC_SH_MAP250_PIN	64	0	rw	
GIC_SH_MAP251_PIN	64	0	rw	
GIC_SH_MAP252_PIN	64	0	rw	
GIC_SH_MAP253_PIN	64	0	rw	
GIC_SH_MAP254_PIN	64	0	rw	
GIC_SH_MAP255_PIN	64	0	rw	
GIC_SH_MAP000_VPE31_0	64	0	rw	
GIC_SH_MAP001_VPE31_0	64	0	rw	
GIC_SH_MAP002_VPE31_0	64	0	rw	
GIC_SH_MAP003_VPE31_0	64	0	rw	
GIC_SH_MAP004_VPE31_0	64	0	rw	
GIC_SH_MAP005_VPE31_0	64	0	rw	
GIC_SH_MAP006_VPE31_0	64	0	rw	
GIC_SH_MAP007_VPE31_0	64	0		
GIC_SH_MAP007_VPE31_0	64	0	rw	
GIC_SH_MAP008_VPE31_0	64	0	rw	
GIC_SH_MAP009_VPE31_0	64		rw	
		0	rw	
GIC_SH_MAP011_VPE31_0	64	0	rw	
GIC_SH_MAP012_VPE31_0	64	0	rw	
GIC_SH_MAP013_VPE31_0	64	0	rw	
GIC_SH_MAP014_VPE31_0	64	0	rw	
GIC_SH_MAP015_VPE31_0	64	0	rw	

GIC_SH_MAP016_VPE31_0	64	0	rw	
GIC_SH_MAP017_VPE31_0	64	0	rw	
GIC_SH_MAP018_VPE31_0	64	0	rw	
GIC_SH_MAP019_VPE31_0	64	0	rw	
GIC_SH_MAP020_VPE31_0	64	0	rw	
GIC_SH_MAP021_VPE31_0	64	0	rw	
GIC_SH_MAP022_VPE31_0	64	0	rw	
GIC_SH_MAP023_VPE31_0	64	0	rw	
GIC_SH_MAP024_VPE31_0	64	0	rw	
GIC_SH_MAP025_VPE31_0	64	0	rw	
GIC_SH_MAP026_VPE31_0	64	0	rw	
GIC_SH_MAP027_VPE31_0	64	0	rw	
GIC_SH_MAP028_VPE31_0	64	0	rw	
GIC_SH_MAP029_VPE31_0	64	0	rw	
GIC_SH_MAP030_VPE31_0	64	0	rw	
GIC_SH_MAP031_VPE31_0	64	0	rw	
GIC_SH_MAP032_VPE31_0	64	0	rw	
GIC_SH_MAP033_VPE31_0	64	0	rw	
GIC_SH_MAP034_VPE31_0	64	0	rw	
GIC_SH_MAP035_VPE31_0	64	0	rw	
GIC_SH_MAP036_VPE31_0	64	0	rw	
GIC_SH_MAP037_VPE31_0	64	0	rw	
GIC_SH_MAP038_VPE31_0	64	0	rw	
GIC SH MAP039 VPE31 0	64	0	rw	
GIC_SH_MAP040_VPE31_0	64	0	rw	
GIC_SH_MAP041_VPE31_0	64	0	rw	
GIC_SH_MAP042_VPE31_0	64	0	rw	
GIC_SH_MAP043_VPE31_0	64	0	rw	
GIC_SH_MAP044_VPE31_0	64	0	rw	
GIC_SH_MAP045_VPE31_0	64	0	rw	
GIC_SH_MAP046_VPE31_0	64	0	rw	
GIC_SH_MAP047_VPE31_0	64	0	rw	
GIC_SH_MAP048_VPE31_0	64	0	rw	
GIC_SH_MAP049_VPE31_0	64	0	rw	
GIC_SH_MAP050_VPE31_0	64	0	rw	
GIC_SH_MAP051_VPE31_0	64	0		
GIC_SH_MAP052_VPE31_0	64	0	rw	
GIC_SH_MAP052_VPE31_0	64	0	rw	
GIC_SH_MAP054_VPE31_0	64	0		
GIC_SH_MAP055_VPE31_0	64	0	rw	
GIC_SH_MAP056_VPE31_0	64	0	rw rw	
GIC_SH_MAP057_VPE31_0	64	0	rw	
GIC_SH_MAP057_VPE31_0	64	0		
GIC_SH_MAP058_VPE31_0	64	0	rw	
GIC_SH_MAP059_VPE31_0	64	0	rw	
GIC_SH_MAP060_VPE31_0	64	0	rw	
	64	0	rw	
GIC_SH_MAP062_VPE31_0	-	_	rw	
GIC_SH_MAP063_VPE31_0	64	0	rw	
GIC_SH_MAP064_VPE31_0	64	0	rw	
GIC_SH_MAP065_VPE31_0	64	0	rw	
GIC_SH_MAP066_VPE31_0	64	0	rw	
GIC_SH_MAP067_VPE31_0	64	0	rw	
GIC_SH_MAP068_VPE31_0	64	0	rw	
GIC_SH_MAP069_VPE31_0	64	0	rw	
GIC_SH_MAP070_VPE31_0	64	0	rw	
GIC_SH_MAP071_VPE31_0	64	0	rw	

GIC_SH_MAP072_VPE31_0	64	0	rw	
GIC_SH_MAP073_VPE31_0	64	0	rw	
GIC_SH_MAP074_VPE31_0	64	0	rw	
GIC_SH_MAP075_VPE31_0	64	0	rw	
GIC_SH_MAP076_VPE31_0	64	0	rw	
GIC_SH_MAP077_VPE31_0	64	0	rw	
GIC_SH_MAP078_VPE31_0	64	0	rw	
GIC_SH_MAP079_VPE31_0	64	0	rw	
GIC_SH_MAP080_VPE31_0	64	0	rw	
GIC_SH_MAP081_VPE31_0	64	0	rw	
GIC_SH_MAP082_VPE31_0	64	0	rw	
GIC_SH_MAP083_VPE31_0	64	0	rw	
GIC_SH_MAP084_VPE31_0	64	0	rw	
GIC_SH_MAP085_VPE31_0	64	0	rw	
GIC_SH_MAP086_VPE31_0	64	0	rw	
GIC_SH_MAP087_VPE31_0	64	0	rw	
GIC_SH_MAP088_VPE31_0	64	0	rw	
GIC_SH_MAP089_VPE31_0	64	0		
GIC_SH_MAP090_VPE31_0	64	0	rw	
GIC_SH_MAP090_VPE31_0 GIC_SH_MAP091_VPE31_0	64	0	rw	
GIC_SH_MAP091_VPE31_0	64	0	rw	
GIC_SH_MAP092_VPE31_0	64		rw	
GIC_SH_MAP093_VPE31_0		0	rw	
0.0000000000000000000000000000000000000	64	0	rw	
GIC_SH_MAP095_VPE31_0	64	0	rw	
GIC_SH_MAP096_VPE31_0	64	0	rw	
GIC_SH_MAP097_VPE31_0	64	0	rw	
GIC_SH_MAP098_VPE31_0	64	0	rw	
GIC_SH_MAP099_VPE31_0	64	0	rw	
GIC_SH_MAP100_VPE31_0	64	0	rw	
GIC_SH_MAP101_VPE31_0	64	0	rw	
GIC_SH_MAP102_VPE31_0	64	0	rw	
GIC_SH_MAP103_VPE31_0	64	0	rw	
GIC_SH_MAP104_VPE31_0	64	0	rw	
GIC_SH_MAP105_VPE31_0	64	0	rw	
GIC_SH_MAP106_VPE31_0	64	0	rw	
GIC_SH_MAP107_VPE31_0	64	0	rw	
GIC_SH_MAP108_VPE31_0	64	0	rw	
GIC_SH_MAP109_VPE31_0	64	0	rw	
GIC_SH_MAP110_VPE31_0	64	0	rw	
GIC_SH_MAP111_VPE31_0	64	0	rw	
GIC_SH_MAP112_VPE31_0	64	0	rw	
GIC_SH_MAP113_VPE31_0	64	0	rw	
GIC_SH_MAP114_VPE31_0	64	0	rw	
GIC_SH_MAP115_VPE31_0	64	0	rw	
GIC_SH_MAP116_VPE31_0	64	0	rw	
GIC_SH_MAP117_VPE31_0	64	0	rw	
GIC_SH_MAP118_VPE31_0	64	0	rw	
GIC_SH_MAP119_VPE31_0	64	0	rw	
GIC_SH_MAP120_VPE31_0	64	0	rw	
GIC_SH_MAP121_VPE31_0	64	0	rw	
GIC_SH_MAP122_VPE31_0	64	0	rw	
GIC_SH_MAP123_VPE31_0	64	0	rw	
GIC_SH_MAP124_VPE31_0	64	0	rw	
GIC_SH_MAP125_VPE31_0	64	0	rw	
GIC_SH_MAP126_VPE31_0	64	0	rw	
GIC_SH_MAP127_VPE31_0	64	0	rw	
010_011_WIRT 121_V1 E01_0	1 04		1 44	

GIC_SH_MAP128_VPE31_0	64	0	rw	
GIC_SH_MAP129_VPE31_0	64	0	rw	
GIC_SH_MAP130_VPE31_0	64	0	rw	
GIC_SH_MAP131_VPE31_0	64	0	rw	
GIC_SH_MAP132_VPE31_0	64	0	rw	
GIC_SH_MAP133_VPE31_0	64	0	rw	
GIC_SH_MAP134_VPE31_0	64	0	rw	
GIC_SH_MAP135_VPE31_0	64	0	rw	
GIC_SH_MAP136_VPE31_0	64	0	rw	
GIC_SH_MAP137_VPE31_0	64	0	rw	
GIC_SH_MAP138_VPE31_0	64	0	rw	
GIC_SH_MAP139_VPE31_0	64	0	rw	
GIC_SH_MAP140_VPE31_0	64	0	rw	
GIC_SH_MAP141_VPE31_0	64	0	rw	
GIC_SH_MAP142_VPE31_0	64	0	rw	
GIC_SH_MAP143_VPE31_0	64	0	rw	
GIC_SH_MAP144_VPE31_0	64	0	rw	
GIC_SH_MAP145_VPE31_0	64	0	rw	
GIC_SH_MAP146_VPE31_0	64	0	rw	
GIC_SH_MAP147_VPE31_0	64	0	rw	
GIC_SH_MAP148_VPE31_0	64	0	rw	
GIC_SH_MAP149_VPE31_0	64	0	rw	
GIC_SH_MAP150_VPE31_0	64	0	rw	
GIC SH MAP151 VPE31 0	64	0	rw	
GIC_SH_MAP152_VPE31_0	64	0	rw	
GIC_SH_MAP153_VPE31_0	64	0	rw	
GIC_SH_MAP154_VPE31_0	64	0	rw	
GIC_SH_MAP155_VPE31_0	64	0	rw	
GIC_SH_MAP156_VPE31_0	64	0	rw	
GIC_SH_MAP157_VPE31_0	64	0	rw	
GIC_SH_MAP158_VPE31_0	64	0	rw	
GIC_SH_MAP159_VPE31_0	64	0	rw	
GIC_SH_MAP160_VPE31_0	64	0		
GIC_SH_MAP161_VPE31_0	64	0	rw	
GIC_SH_MAP162_VPE31_0	64	0	rw	
GIC_SH_MAP163_VPE31_0	64	0	rw	
GIC_SH_MAP164_VPE31_0	64	0	rw	
GIC_SH_MAP165_VPE31_0	64	0	rw	
	-	-	rw	
GIC_SH_MAP166_VPE31_0	64	0	rw	
GIC_SH_MAP167_VPE31_0	64	0	rw	
GIC_SH_MAP168_VPE31_0	64	0	rw	
GIC_SH_MAP169_VPE31_0	64	0	rw	
GIC_SH_MAP170_VPE31_0	64	0	rw	
GIC_SH_MAP171_VPE31_0	64	0	rw	
GIC_SH_MAP172_VPE31_0	64	0	rw	
GIC_SH_MAP173_VPE31_0	64	0	rw	
GIC_SH_MAP174_VPE31_0	64	0	rw	
GIC_SH_MAP175_VPE31_0	64	0	rw	
GIC_SH_MAP176_VPE31_0	64	0	rw	
GIC_SH_MAP177_VPE31_0	64	0	rw	
GIC_SH_MAP178_VPE31_0	64	0	rw	
GIC_SH_MAP179_VPE31_0	64	0	rw	
GIC_SH_MAP180_VPE31_0	64	0	rw	
GIC_SH_MAP181_VPE31_0	64	0	rw	
GIC_SH_MAP182_VPE31_0	64	0	rw	
GIC_SH_MAP183_VPE31_0	64	0	rw	
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GIC_SH_MAP184_VPE31_0	64	0	rw	
GIC_SH_MAP185_VPE31_0	64	0	rw	
GIC_SH_MAP186_VPE31_0	64	0	rw	
GIC_SH_MAP187_VPE31_0	64	0	rw	
GIC_SH_MAP188_VPE31_0	64	0	rw	
GIC_SH_MAP189_VPE31_0	64	0	rw	
GIC_SH_MAP190_VPE31_0	64	0	rw	
GIC_SH_MAP191_VPE31_0	64	0	rw	
GIC_SH_MAP192_VPE31_0	64	0	rw	
GIC_SH_MAP193_VPE31_0	64	0	rw	
GIC_SH_MAP194_VPE31_0	64	0	rw	
GIC_SH_MAP195_VPE31_0	64	0	rw	
GIC_SH_MAP196_VPE31_0	64	0	rw	
GIC_SH_MAP197_VPE31_0	64	0	rw	
GIC_SH_MAP198_VPE31_0	64	0	rw	
GIC_SH_MAP199_VPE31_0	64	0		
GIC_SH_MAP200_VPE31_0	64	0	rw	
		-	rw	
GIC_SH_MAP201_VPE31_0	64	0	rw	
GIC_SH_MAP202_VPE31_0	64	0	rw	
GIC_SH_MAP203_VPE31_0	64	0	rw	
GIC_SH_MAP204_VPE31_0	64	0	rw	
GIC_SH_MAP205_VPE31_0	64	0	rw	
GIC_SH_MAP206_VPE31_0	64	0	rw	
GIC_SH_MAP207_VPE31_0	64	0	rw	
GIC_SH_MAP208_VPE31_0	64	0	rw	
GIC_SH_MAP209_VPE31_0	64	0	rw	
GIC_SH_MAP210_VPE31_0	64	0	rw	
GIC_SH_MAP211_VPE31_0	64	0	rw	
GIC_SH_MAP212_VPE31_0	64	0	rw	
GIC_SH_MAP213_VPE31_0	64	0	rw	
GIC_SH_MAP214_VPE31_0	64	0	rw	
GIC_SH_MAP215_VPE31_0	64	0	rw	
GIC_SH_MAP216_VPE31_0	64	0	rw	
GIC_SH_MAP217_VPE31_0	64	0	rw	
GIC_SH_MAP218_VPE31_0	64	0	rw	
GIC_SH_MAP219_VPE31_0	64	0		
GIC_SH_MAP220_VPE31_0	64	0	rw	
GIC_SH_MAP221_VPE31_0	64	0	rw	
	_	-	rw	
GIC_SH_MAP222_VPE31_0	64	0	rw	
GIC_SH_MAP224_VPE31_0	64	0	rw	
GIC_SH_MAP224_VPE31_0	64	0	rw	
GIC_SH_MAP225_VPE31_0	64	0	rw	
GIC_SH_MAP226_VPE31_0	64	0	rw	
GIC_SH_MAP227_VPE31_0	64	0	rw	
GIC_SH_MAP228_VPE31_0	64	0	rw	
GIC_SH_MAP229_VPE31_0	64	0	rw	
GIC_SH_MAP230_VPE31_0	64	0	rw	
GIC_SH_MAP231_VPE31_0	64	0	rw	
GIC_SH_MAP232_VPE31_0	64	0	rw	
GIC_SH_MAP233_VPE31_0	64	0	rw	
GIC_SH_MAP234_VPE31_0	64	0	rw	
GIC_SH_MAP235_VPE31_0	64	0	rw	
GIC_SH_MAP236_VPE31_0	64	0	rw	
GIC_SH_MAP237_VPE31_0	64	0	rw	
GIC_SH_MAP238_VPE31_0	64	0	rw	
GIC_SH_MAP239_VPE31_0	64	0	rw	
010_011_MM1 200_V1 E01_0	1 04		T AA	

GIC_SH_MAP240_VPE31_0	64	0	rw	
GIC_SH_MAP241_VPE31_0	64	0	rw	
GIC_SH_MAP242_VPE31_0	64	0	rw	
GIC_SH_MAP243_VPE31_0	64	0	rw	
GIC_SH_MAP244_VPE31_0	64	0	rw	
GIC_SH_MAP245_VPE31_0	64	0	rw	
GIC_SH_MAP246_VPE31_0	64	0	rw	
GIC_SH_MAP247_VPE31_0	64	0	rw	
GIC_SH_MAP248_VPE31_0	64	0	rw	
GIC_SH_MAP249_VPE31_0	64	0	rw	
GIC_SH_MAP250_VPE31_0	64	0	rw	
GIC_SH_MAP251_VPE31_0	64	0	rw	
GIC_SH_MAP252_VPE31_0	64	0	rw	
GIC_SH_MAP253_VPE31_0	64	0	rw	
GIC_SH_MAP254_VPE31_0	64	0	rw	
GIC_SH_MAP255_VPE31_0	64	0		
GIC_SH_EJTAG_BRK	64	0	rw	
GIC_SH_EJTAG_BRK GIC_SH_TEAMID_LO	_	-	rw	
	64	0	rw	
GIC_SH_TEAMID_HI	64	0	rw	
GIC_SH_TEAMID_EXT	64	0	rw	
GIC_SH_DBG_CONFIG	64	70	rw	
GIC_SH_DINT_PART	64	0	rw	
GIC_SH_DEBUGM_STATUS	64	0	r-	
GIC_VPE_CTL	64	0	rw	
GIC_VPE_PEND	64	0	r-	
GIC_VPE_MASK	64	7f	r-	
GIC_VPE_RMASK	64	0	-w	
GIC_VPE_SMASK	64	0	-w	
GIC_VPE_WD_MAP	64	40000000	rw	
GIC_VPE_COMPARE_MAP	64	80000000	rw	
GIC_VPE_TIMER_MAP	64	80000005	rw	
GIC_VPE_FDC_MAP	64	80000005	rw	
GIC_VPE_PERFCTR_MAP	64	80000005	rw	
GIC_VPE_SWInt0_MAP	64	80000000	rw	
GIC_VPE_SWInt1_MAP	64	80000000	rw	
GIC_VPE_OTHER_ADDRESS	64	0	rw	
GIC-VPE-IDENT	64	0	r-	
GIC_VFE_IDENT GIC_VPE_WD_CONFIG	64	0		
GIC_VPE_WD_CONFIG	64	0	rw	
		0	r-	
GIC_VPE_WD_INITIAL	64	ffffff ffffff	rw	
GIC_VPE_Compare	64		rw	
GIC_VPE_EICSS00	64	0	rw	
GIC_VPE_EICSS01	64	0	rw	
GIC_VPE_EICSS02	64	0	rw	
GIC_VPE_EICSS03	64	0	rw	
GIC_VPE_EICSS04	64	0	rw	
GIC_VPE_EICSS05	64	0	rw	
GIC_VPE_EICSS06	64	0	rw	
GIC_VPE_EICSS07	64	0	rw	
GIC_VPE_EICSS08	64	0	rw	
GIC_VPE_EICSS09	64	0	rw	
GIC_VPE_EICSS10	64	0	rw	
GIC_VPE_EICSS11	64	0	rw	
GIC_VPE_EICSS12	64	0	rw	
GIC-VPE-EICSS13	64	0	rw	
GIC_VPE_EICSS14	64	0	rw	
				i l

GIC_VPE_EICSS15	64	0	rw	
GIC_VPE_EICSS16	64	0	rw	
GIC_VPE_EICSS17	64	0	rw	
GIC_VPE_EICSS18	64	0	rw	
GIC_VPE_EICSS19	64	0	rw	
GIC_VPE_EICSS20	64	0	rw	
GIC_VPE_EICSS21	64	0	rw	
GIC_VPE_EICSS22	64	0	rw	
GIC_VPE_EICSS23	64	0	rw	
GIC_VPE_EICSS24	64	0	rw	
GIC_VPE_EICSS25	64	0	rw	
GIC_VPE_EICSS26	64	0	rw	
GIC_VPE_EICSS27	64	0	rw	
GIC_VPE_EICSS28	64	0	rw	
GIC_VPE_EICSS29	64	0		
GIC_VPE_EICSS29	64	0	rw	
GIC_VPE_EICSS31	64	0	rw	
GIC_VPE_EICSS31	-		rw	
	64	0	rw	
GIC_VPE_EICSS33	64	0	rw	
GIC_VPE_EICSS34	64	1	rw	
GIC_VPE_EICSS35	64	0	rw	
GIC_VPE_EICSS36	64	0	rw	
GIC_VPE_EICSS37	64	0	rw	
GIC_VPE_EICSS38	64	0	rw	
GIC_VPE_EICSS39	64	0	rw	
GIC_VPE_EICSS40	64	0	rw	
GIC_VPE_EICSS41	64	0	rw	
GIC_VPE_EICSS42	64	0	rw	
GIC_VPE_EICSS43	64	0	rw	
GIC_VPE_EICSS44	64	0	rw	
GIC_VPE_EICSS45	64	0	rw	
GIC_VPE_EICSS46	64	0	rw	
GIC_VPE_EICSS47	64	0	rw	
GIC_VPE_EICSS48	64	0	rw	
GIC_VPE_EICSS49	64	0	rw	
GIC_VPE_EICSS50	64	0	rw	
GIC-VPE-EICSS51	64	0	rw	
GIC_VPE_EICSS52	64	0	rw	
GIC_VPE_EICSS53	64	0	rw	
GIC_VPE_EICSS54	64	0		
GIC_VPE_EICSS34 GIC_VPE_EICSS55	64	0	rw	
GIC_VPE_EICSS55	64	0	rw	
			rw	
GIC_VPE_EICSS57	64	0	rw	
GIC_VPE_EICSS58	64	0	rw	
GIC_VPE_EICSS59	64	0	rw	
GIC_VPE_EICSS60	64	0	rw	
GIC_VPE_EICSS61	64	0	rw	
GIC_VPE_EICSS62	64	0	rw	
GIC_VPE_EICSS63	64	0	rw	
GIC_VL_COFFSET	64	0	rw	
GIC_VL_VIRTUAL_VP_NUM	64	0	rw	
GIC_VPE_CTL	64	0	rw	
GIC_VPE_PEND	64	0	r-	
GIC_VPE_MASK	64	7f	r-	
GIC_VPE_RMASK	64	0	-w	
GIC_VPE_SMASK	64	0	-w	
		-		

GIC_VPE_WD_MAP	64	40000000	rw	
GIC_VPE_COMPARE_MAP	64	80000000	rw	
GIC_VPE_TIMER_MAP	64	80000005	rw	
GIC_VPE_FDC_MAP	64	80000005	rw	
GIC_VPE_PERFCTR_MAP	64	80000005	rw	
GIC_VPE_SWInt0_MAP	64	80000000	rw	
GIC_VPE_SWInt1_MAP	64	80000000	rw	
GIC_VPE_OTHER_ADDRESS	64	0	rw	
GIC_VPE_IDENT	64	0	r-	
GIC_VPE_WD_CONFIG	64	0	rw	
GIC_VPE_WD_COUNT	64	0	r-	
GIC_VPE_WD_INITIAL	64	0	rw	
GIC_VPE_Compare	64	TITTITI TITTITI	rw	
GIC_VPE_EICSS00	64	0	rw	
GIC_VPE_EICSS01	64	0	rw	
GIC_VPE_EICSS02	64	0	rw	
GIC_VPE_EICSS03	64	0	rw	
GIC_VPE_EICSS04	64	0	rw	
GIC_VPE_EICSS05	64	0	rw	
GIC_VPE_EICSS06	64	0	rw	
GIC_VPE_EICSS07	64	0	rw	
GIC-VPE-EICSS08	64	0	rw	
GIC_VPE_EICSS09	64	0	rw	
GIC_VPE_EICSS10	64	0	rw	
GIC_VPE_EICSS11	64	0	rw	
GIC_VPE_EICSS12	64	0	rw	
GIC-VPE-EICSS13	64	0	rw	
GIC_VPE_EICSS14	64	0	rw	
GIC_VPE_EICSS15	64	0	rw	
GIC_VPE_EICSS16	64	0	rw	
GIC_VPE_EICSS17	64	0	rw	
GIC_VPE_EICSS18	64	0	rw	
GIC_VPE_EICSS19	64	0	rw	
GIC_VPE_EICSS20	64	0	rw	
GIC_VPE_EICSS21	64	0	rw	
GIC_VPE_EICSS22	64	0	rw	
GIC-VPE-EICSS23	64	0	rw	
GIC_VPE_EICSS24	64	0	rw	
GIC_VPE_EICSS25	64	0	rw	
GIC_VPE_EICSS26	64	0	rw	
GIC_VPE_EICSS27	64	0	rw	
GIC_VFE_EICSS27	64	0	rw	
GIC_VPE_EICSS29	64	0		
GIC_VPE_EICSS29 GIC_VPE_EICSS30	64	0	rw	
GIC_VPE_EICSS30	64	0	rw	
GIC_VPE_EICSS31	64	0	rw	
GIC_VPE_EICSS32 GIC_VPE_EICSS33	64		rw	
GIC_VPE_EICSS33 GIC_VPE_EICSS34	-	0	rw	
GIC_VPE_EICSS34 GIC_VPE_EICSS35	64	1	rw	
GIC_VPE_EICSS35 GIC_VPE_EICSS36	64	0	rw	
	64	0	rw	
GIC_VPE_EICSS37	64	0	rw	
GIC_VPE_EICSS38	64	0	rw	
GIC_VPE_EICSS39	64	0	rw	
GIC_VPE_EICSS40	64	0	rw	
GIC_VPE_EICSS41	64	0	rw	
GIC_VPE_EICSS42	64	0	rw	

GIC_VPE_EICSS43	64	0	rw	
GIC_VPE_EICSS44	64	0	rw	
GIC_VPE_EICSS45	64	0	rw	
GIC_VPE_EICSS46	64	0	rw	
GIC_VPE_EICSS47	64	0	rw	
GIC_VPE_EICSS48	64	0	rw	
GIC_VPE_EICSS49	64	0	rw	
GIC_VPE_EICSS50	64	0	rw	
GIC_VPE_EICSS51	64	0	rw	
GIC_VPE_EICSS52	64	0	rw	
GIC_VPE_EICSS53	64	0	rw	
GIC_VPE_EICSS54	64	0	rw	
GIC_VPE_EICSS55	64	0	rw	
GIC_VPE_EICSS56	64	0	rw	
GIC_VPE_EICSS57	64	0	rw	
GIC_VPE_EICSS58	64	0	rw	
GIC_VPE_EICSS59	64	0	rw	
GIC_VPE_EICSS60	64	0	rw	
GIC_VPE_EICSS61	64	0	rw	
GIC_VPE_EICSS62	64	0	rw	
GIC_VPE_EICSS63	64	0	rw	
GIC_VL_COFFSET	64	0	rw	
GIC_VL_VIRTUAL_VP_NUM	64	0	rw	
GIC_CounterLoUser	64	0	r-	
GIC_CounterHiUser	64	0	r-	

Table 13.9: Registers at level 3, type:VP group:CMP\_GIC

# 13.3.10 Integration\_support

Registers at level:3, type:VP group:Integration\_support

Name	Bits	Initial-Hex	RW	Description
stop	32	0	rw	write with non-zero to stop processor

Table 13.10: Registers at level 3, type:VP group:Integration\_support