Imperas Peripheral Model Guide

Model Specific Information for xilinx.ovpworld.org / zynq_7000-ddrc

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

1.1 Description

Zynq 7000 Platform DDR Memory Controller (DDRC)

1.2 Licensing

Open Source Apache 2.0

1.3 Limitations

This model implements the full set of registers. There is no behavior included.

1.4 Reference

Zynq-7000 TRM
(https://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf)

1.5 Location

The zynq_7000-ddrc peripheral model is located in an Imperas/OVP installation at the VLNV:
xilinx.ovpworld.org / peripheral / zynq_7000-ddrc / 1.0.

2.0 Bus Slave Ports

This model has the following bus slave ports:

2.1 Bus Slave Port: bport1

Table 1. Bus Slave Port: bport1

Name	Size (bytes)	Must Be Connected	Description
bport1	0x1000	T (True)	

Table 2. Bus Slave Port: bport1 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_ddrc_ctrl	0x0	32	DDRC Control		
ab_Two_rank_cfg	0x4	32	Two Rank Configuration		
ab_HPR_reg	0x8	32	HPR Queue control		
ab_LPR_reg	0xc	32	LPR Queue control		
ab_WR_reg	0x10	32	WR Queue control		
ab_DRAM_param_reg0	0x14	32	DRAM Parameters 0		
ab_DRAM_param_reg1	0x18	32	DRAM Parameters 1		
ab_DRAM_param_reg2	0x1c	32	DRAM Parameters 2		

ab_DRAM_param_reg3	0x20	32	DRAM Parameters 3		
ab_DRAM_param_reg4	0x24	32	DRAM Parameters 4		
ab_DRAM_init_param	0x28	32	DRAM Initialization Parameters		
ab_DRAM_EMR_reg	0x2c	32	DRAM EMR2, EMR3 access		
ab_DRAM_EMR_MR_reg	0x30	32	DRAM EMR, MR access		
ab_DRAM_burst8_rdwr	0x34	32	DRAM Burst 8 read/write		
ab_DRAM_disable_DQ	0x38	32	DRAM Disable DQ		
ab_DRAM_addr_map_bank	0x3c	32	Row/Column address bits		
ab_DRAM_addr_map_col	0x40	32	Column address bits		
ab_DRAM_addr_map_row	0x44	32	Select DRAM row address bits		
ab_DRAM_ODT_reg	0x48	32	DRAM ODT control		
ab_phy_dbg_reg	0x4c	32	PHY debug		
ab_phy_cmd_timeout_rddata_cpt	0x50	32	PHY command time out and read data capture FIFO		
ab_mode_sts_reg	0x54	32	Controller operation mode status		
ab_DLL_calib	0x58	32	DLL calibration		
ab_ODT_delay_hold	0x5c	32	ODT delay and ODT hold		
ab_ctrl_reg1	0x60	32	Controller 1		
ab_ctrl_reg2	0x64	32	Controller 2		
ab_ctrl_reg3	0x68	32	Controller 3		
ab_ctrl_reg4	0x6c	32	Controller 4		
ab_ctrl_reg5	0x78	32	Controller register 5		
ab_ctrl_reg6	0x7c	32	Controller register 6		
ab_CHE_REFRESH_TIMER01	0xa0	32	CHE_REFRESH_TIMER01		
ab_CHE_T_ZQ	0xa4	32	ZQ parameters		
ab_CHE_T_ZQ_Short_Interval_Reg	0xa8	32	Misc parameters		
ab_deep_pwrdwn_reg	0xac	32	Deep powerdown (LPDDR2)		
ab_reg_2c	0xb0	32	Training control		
ab_reg_2d	0xb4	32	Misc Debug		
ab_dfi_timing	0xb8	32	DFI timing		
ab_CHE_ECC_CONTROL_REG_OFFSET	0xc4	32	ECC error clear		
ab_CHE_CORR_ECC_LOG_REG_OFFSET	0xc8	32	ECC error correction		
ab_CHE_CORR_ECC_ADDR_REG_OFFSET	0xcc	32	ECC error correction address log		
ab_CHE_CORR_ECC_DATA_31_0_REG_OFFSET	0xd0	32	ECC error correction data log low		
ab_CHE_CORR_ECC_DATA_63_32_REG_OFFSET	0xd4	32	ECC error correction data log mid		

ab_CHE_CORR_ECC_DATA_71_64_REG_OFFSET	0xd8	32	ECC error correction data log high		
ab_CHE_UNCORR_ECC_LOG_REG_OFFSET	0xdc	32	ECC unrecoverable error status		
ab_CHE_UNCORR_ECC_ADDR_REG_OFFSET	0xe0	32	ECC unrecoverable error address		
ab_CHE_UNCORR_ECC_DATA_31_0_REG_OFFSET	0xe4	32	ECC unrecoverable error data low		
ab_CHE_UNCORR_ECC_DATA_63_32_REG_OFFSET	0xe8	32	ECC unrecoverable error data middle		
ab_CHE_UNCORR_ECC_DATA_71_64_REG_OFFSET	0xec	32	ECC unrecoverable error data high		
ab_CHE_ECC_STATS_REG_OFFSET	0xf0	32	ECC error count		
ab_ECC_scrub	0xf4	32	ECC mode/scrub		
ab_CHE_ECC_CORR_BIT_MASK_31_0_REG_OFFSET	0xf8	32	ECC data mask low		
ab_CHE_ECC_CORR_BIT_MASK_63_32_REG_OFFSET	0xfc	32	ECC data mask high		
ab_phy_rcvr_enable	0x114	32	Phy receiver enable register		
ab_PHY_Config0	0x118	32	PHY configuration register for data slice 0.		
ab_PHY_Config1	0x11c	32	PHY configuration register for data slice 1.		
ab_PHY_Config2	0x120	32	PHY configuration register for data slice 2.		
ab_PHY_Config3	0x124	32	PHY configuration register for data slice 3.		
ab_phy_init_ratio0	0x12c	32	PHY init ratio register for data slice 0.		
ab_phy_init_ratio1	0x130	32	PHY init ratio register for data slice 1.		
ab_phy_init_ratio2	0x134	32	PHY init ratio register for data slice 2.		
ab_phy_init_ratio3	0x138	32	PHY init ratio register for data slice 3.		
ab_phy_rd_dqs_cfg0	0x140	32	PHY read DQS configuration register for data slice 0.		
ab_phy_rd_dqs_cfg1	0x144	32	PHY read DQS configuration register for data slice 1.		
ab_phy_rd_dqs_cfg2	0x148	32	PHY read DQS configuration register for data slice 2.		
ab_phy_rd_dqs_cfg3	0x14c	32	PHY read DQS configuration register for data slice 3.		
ab_phy_wr_dqs_cfg0	0x154	32	PHY write DQS		

			configuration register for data slice 0.		
ab_phy_wr_dqs_cfg1	0x158	32	PHY write DQS configuration register for data slice 1.		
ab_phy_wr_dqs_cfg2	0x15c	32	PHY write DQS configuration register for data slice 2.		
ab_phy_wr_dqs_cfg3	0x160	32	PHY write DQS configuration register for data slice 3.		
ab_phy_we_cfg0	0x168	32	PHY FIFO write enable configuration for data slice 0.		
ab_phy_we_cfg1	0x16c	32	PHY FIFO write enable configuration for data slice 1.		
ab_phy_we_cfg2	0x170	32	PHY FIFO write enable configuration for data slice 2.		
ab_phy_we_cfg3	0x174	32	PHY FIFO write enable configuration for data slice 3.		
ab_wr_data_slv0	0x17c	32	PHY write data slave ratio config for data slice 0.		
ab_wr_data_slv1	0x180	32	PHY write data slave ratio config for data slice 1.		
ab_wr_data_slv2	0x184	32	PHY write data slave ratio config for data slice 2.		
ab_wr_data_slv3	0x188	32	PHY write data slave ratio config for data slice 3.		
ab_reg_64	0x190	32	Training control 2		
ab_reg_65	0x194	32	Training control 3		
ab_reg69_6a0	0x1a4	32	Training results for data slice 0.		
ab_reg69_6a1	0x1a8	32	Training results for data slice 1.		
ab_reg6c_6d2	0x1b0	32	Training results for data slice 2.		
ab_reg6c_6d3	0x1b4	32	Training results for data slice 3.		
ab_reg6e_710	0x1b8	32	Training results (2) for data slice 0.		
ab_reg6e_711	0x1bc	32	Training results (2) for data slice 1.		
ab_reg6e_712	0x1c0	32	Training results (2) for data slice 2.		
ab_reg6e_713	0x1c4	32	Training results (2) for data slice 3.		
ab_phy_dll_sts0	0x1cc	32	Slave DLL results for data slice 0.		
ab_phy_dll_sts1	0x1d0	32	Slave DLL results for data slice 1.		

ab_phy_dll_sts2	0x1d4	32	Slave DLL results for data slice 2.		
ab_phy_dll_sts3	0x1d8	32	Slave DLL results for data slice 3.		
ab_dll_lock_sts	0x1e0	32	DLL Lock Status, read		
ab_phy_ctrl_sts	0x1e4	32	PHY Control status, read		
ab_phy_ctrl_sts_reg2	0x1e8	32	PHY Control status (2), read		
ab_axi_id	0x200	32	ID and revision information page_mask 0x00000204 32 rw 0x00000000 Page mask		
ab_axi_priority_wr_port0	0x208	32	AXI Priority control for write port 0.		
ab_axi_priority_wr_port1	0x20c	32	AXI Priority control for write port 1.		
ab_axi_priority_wr_port2	0x210	32	AXI Priority control for write port 2.		
ab_axi_priority_wr_port3	0x214	32	AXI Priority control for write port 3.		
ab_axi_priority_rd_port0	0x218	32	AXI Priority control for read port 0.		
ab_axi_priority_rd_port1	0x21c	32	AXI Priority control for read port 1.		
ab_axi_priority_rd_port2	0x220	32	AXI Priority control for read port 2.		
ab_axi_priority_rd_port3	0x224	32	AXI Priority control for read port 3.		
ab_excl_access_cfg0	0x294	32	Exclusive access configuration for port 0.		
ab_excl_access_cfg1	0x298	32	Exclusive access configuration for port 1.		
ab_excl_access_cfg2	0x29c	32	Exclusive access configuration for port 2.		
ab_excl_access_cfg3	0x2a0	32	Exclusive access configuration for port 3.		
ab_mode_reg_read	0x2a4	32	Mode register read data		
ab_lpddr_ctrl0	0x2a8	32	LPDDR2 Control 0		
ab_lpddr_ctrl1	0x2ac	32	LPDDR2 Control 1		
ab_lpddr_ctrl2	0x2b0	32	LPDDR2 Control 2		
ab_lpddr_ctrl3	0x2b4	32	LPDDR2 Control 3		

3.0 Platforms that use this peripheral component

Peripheral components can be used in many different platforms, including those developed by Imperas or by other users of OVP. You can use this peripheral in your own platforms.

Table 3. Publicly available platforms using peripheral 'zynq_7000-ddrc'

Platform Name	Vendor
Zynq_PS	xilinx.ovpworld.org

4.0 Peripheral components in the library

Table 4. Publicly available Imperas/OVP peripheral models (227 models)

Peripheral	Peripheral	Peripheral
xilinx.ovpworld.org/zynq_7000-devcfg	xilinx.ovpworld.org/zynq_7000-dmac	xilinx.ovpworld.org/zynq_7000-gpio
xilinx.ovpworld.org/zynq_7000-iic	xilinx.ovpworld.org/zynq_7000-ocm	xilinx.ovpworld.org/zynq_7000-qos301
xilinx.ovpworld.org/zynq_7000-qspi	xilinx.ovpworld.org/zynq_7000-sdio	xilinx.ovpworld.org/zynq_7000-slcr
xilinx.ovpworld.org/zynq_7000-spi	xilinx.ovpworld.org/zynq_7000-swdt	xilinx.ovpworld.org/zynq_7000-ttc
xilinx.ovpworld.org/zynq_7000-tz_GPVsecurity	xilinx.ovpworld.org/zynq_7000-tz_security	xilinx.ovpworld.org/zynq_7000-usb
altera.ovpworld.org/dw-apb-timer	altera.ovpworld.org/dw-apb-uart	altera.ovpworld.org/IntervalTimer32Core
altera.ovpworld.org/IntervalTimer64Core	altera.ovpworld.org/JtagUart	altera.ovpworld.org/PerformanceCounterCore
altera.ovpworld.org/RSTMGR	altera.ovpworld.org/SystemIDCore	altera.ovpworld.org/Uart
amd.ovpworld.org/79C970	andes.ovpworld.org/ATCUART100	andes.ovpworld.org/NCEPLIC100
andes.ovpworld.org/NCEPLMT100	arm.ovpworld.org/AaciPL041	arm.ovpworld.org/CompactFlashRegs
arm.ovpworld.org/CoreModule9x6	arm.ovpworld.org/DebugLedAndDipSwitch	arm.ovpworld.org/DMemCtrlPL341
arm.ovpworld.org/IcpControl	arm.ovpworld.org/IcpCounterTimer	arm.ovpworld.org/IntICP
arm.ovpworld.org/IntICP	arm.ovpworld.org/KbPL050	arm.ovpworld.org/L2CachePL310
arm.ovpworld.org/LcdPL110	arm.ovpworld.org/MmciPL181	arm.ovpworld.org/RtcPL031
arm.ovpworld.org/SerBusDviRegs	arm.ovpworld.org/SmartLoaderArm64Linux	arm.ovpworld.org/SmartLoaderArmLinux
arm.ovpworld.org/SMemCtrlPL354	arm.ovpworld.org/SysCtrlSP810	arm.ovpworld.org/TimerSP804
arm.ovpworld.org/TzpcBP147	arm.ovpworld.org/UartPL011	arm.ovpworld.org/VexpressSysRegs
arm.ovpworld.org/WdtSP805	atmel.ovpworld.org/AdvancedInterruptController	atmel.ovpworld.org/ParallelIOController
atmel.ovpworld.org/PowerSaving	atmel.ovpworld.org/SpecialFunction	atmel.ovpworld.org/TimerCounter
atmel.ovpworld.org/UsartInterface	atmel.ovpworld.org/WatchdogTimer	cadence.ovpworld.org/gem
cadence.ovpworld.org/uart	cirrus.ovpworld.org/GD5446	freescale.ovpworld.org/KinetisADC
freescale.ovpworld.org/KinetisAIPS	freescale.ovpworld.org/KinetisAXBS	freescale.ovpworld.org/KinetisCAN
freescale.ovpworld.org/KinetisCMP	freescale.ovpworld.org/KinetisCMT	freescale.ovpworld.org/KinetisCRC
freescale.ovpworld.org/KinetisDAC	freescale.ovpworld.org/KinetisDDR	freescale.ovpworld.org/KinetisDMA
freescale.ovpworld.org/KinetisDMAC	freescale.ovpworld.org/KinetisDMAMUX	freescale.ovpworld.org/KinetisENET
freescale.ovpworld.org/KinetisEWM	freescale.ovpworld.org/KinetisFB	freescale.ovpworld.org/KinetisFMC
freescale.ovpworld.org/KinetisFTFE	freescale.ovpworld.org/KinetisFTM	freescale.ovpworld.org/KinetisGPIO
freescale.ovpworld.org/KinetisI2C	freescale.ovpworld.org/KinetisI2S	freescale.ovpworld.org/KinetisLLWU
freescale.ovpworld.org/KinetisLPTMR	freescale.ovpworld.org/KinetisMCG	freescale.ovpworld.org/KinetisMPU
freescale.ovpworld.org/KinetisNFC	freescale.ovpworld.org/KinetisOSC	freescale.ovpworld.org/KinetisPDB
freescale.ovpworld.org/KinetisPIT	freescale.ovpworld.org/KinetisPMC	freescale.ovpworld.org/KinetisPORT
freescale.ovpworld.org/KinetisRCM	freescale.ovpworld.org/KinetisRFSYS	freescale.ovpworld.org/KinetisRFVBAT
freescale.ovpworld.org/KinetisRNG	freescale.ovpworld.org/KinetisRTC	freescale.ovpworld.org/KinetisSDHC
freescale.ovpworld.org/KinetisSIM	freescale.ovpworld.org/KinetisSMC	freescale.ovpworld.org/KinetisSPI
freescale.ovpworld.org/KinetisTSI	freescale.ovpworld.org/KinetisUART	freescale.ovpworld.org/KinetisUSB
freescale.ovpworld.org/KinetisUSBDCD	freescale.ovpworld.org/KinetisUSBHS	freescale.ovpworld.org/KinetisVREF
freescale.ovpworld.org/KinetisWDOG	freescale.ovpworld.org/Uart	freescale.ovpworld.org/VybridADC
freescale.ovpworld.org/VybridANADIG	freescale.ovpworld.org/VybridCCM	freescale.ovpworld.org/VybridDMA
freescale.ovpworld.org/VybridGPIO	freescale.ovpworld.org/VybridI2C	freescale.ovpworld.org/VybridLCD
freescale.ovpworld.org/VybridQUADSPI	freescale.ovpworld.org/VybridSDHC	freescale.ovpworld.org/VybridSPI
freescale.ovpworld.org/VybridUART	freescale.ovpworld.org/VybridUSB	imperas.ovpworld.org/frameBuffer
imperas.ovpworld.org/uart	imperas.ovpworld.org/usecCounter	intel.ovpworld.org/82077AA
intel.ovpworld.org/82371EB	intel.ovpworld.org/8253	intel.ovpworld.org/8259A

intel.ovpworld.org/NorFlash48F4400	intel.ovpworld.org/PciIDE	intel.ovpworld.org/PciPM
intel.ovpworld.org/PciUSB	intel.ovpworld.org/Ps2Control	marvell.ovpworld.org/GT6412x
maxim.ovpworld.org/max673x	microsemi.ovpworld.org/CoreUARTapb	mips.ovpworld.org/16450C
mips.ovpworld.org/MaltaFPGA	mips.ovpworld.org/SmartLoaderLinux	motorola.ovpworld.org/MC146818
national.ovpworld.org/16450	national.ovpworld.org/16550	national.ovpworld.org/16550_4bytes
nxp.ovpworld.org/iMX6_Analog	nxp.ovpworld.org/iMX6_CCM	nxp.ovpworld.org/iMX6_GPC
nxp.ovpworld.org/iMX6_GPIO	nxp.ovpworld.org/iMX6_GPT	nxp.ovpworld.org/iMX6_MMDC
nxp.ovpworld.org/iMX6_SDHC	nxp.ovpworld.org/iMX6_SRC	nxp.ovpworld.org/iMX6_UART
nxp.ovpworld.org/iMX6_WDOG	ovpworld.org/Alpha2x16Display	ovpworld.org/DynamicBridge
ovpworld.org/FlashDevice	ovpworld.org/ledRegister	ovpworld.org/SerInt
ovpworld.org/SimpleDma	ovpworld.org/switchRegister	ovpworld.org/temperatureSensor
ovpworld.org/trap	ovpworld.org/trap4K	ovpworld.org/vEthernet_Bridge
ovpworld.org/VirtioBlkMMIO	ovpworld.org/VirtioNetMMIO	philips.ovpworld.org/ISP1761
renesas.ovpworld.org/adc	renesas.ovpworld.org/bcu	renesas.ovpworld.org/brg
renesas.ovpworld.org/can	renesas.ovpworld.org/can	renesas.ovpworld.org/clkgen
renesas.ovpworld.org/crc	renesas.ovpworld.org/csib	renesas.ovpworld.org/csie
renesas.ovpworld.org/dma	renesas.ovpworld.org/intc	renesas.ovpworld.org/memc
renesas.ovpworld.org/rng	renesas.ovpworld.org/taa	renesas.ovpworld.org/tms
renesas.ovpworld.org/tmt	renesas.ovpworld.org/uartc	renesas.ovpworld.org/UPD70F3441Logic
riscv.ovpworld.org/CLINT	riscv.ovpworld.org/PLIC	riscv.ovpworld.org/SmartLoaderRV64Linux
safepower.ovpworld.org/node	safepower.ovpworld.org/NostrumNode	safepower.ovpworld.org/ring_oscillator
safepower.ovpworld.org/TTELNode	sifive.ovpworld.org/artyIO	sifive.ovpworld.org/DDRCTL
sifive.ovpworld.org/gpio	sifive.ovpworld.org/MSEL	sifive.ovpworld.org/PLIC
sifive.ovpworld.org/PRCI	sifive.ovpworld.org/pwm	sifive.ovpworld.org/spi
sifive.ovpworld.org/teststatus	sifive.ovpworld.org/UART	smsc.ovpworld.org/LAN9118
smsc.ovpworld.org/LAN91C111	ti.ovpworld.org/tca6416a	ti.ovpworld.org/UartInterface
ti.ovpworld.org/ucd9012a	ti.ovpworld.org/ucd9248	vendor.com/fifo
xilinx.ovpworld.org/axi-gpio	xilinx.ovpworld.org/axi-intc	xilinx.ovpworld.org/axi-pcie
xilinx.ovpworld.org/axi-timer	xilinx.ovpworld.org/logicore-fit	xilinx.ovpworld.org/mdm
xilinx.ovpworld.org/mpmc	xilinx.ovpworld.org/xps-gpio	xilinx.ovpworld.org/xps-iic
xilinx.ovpworld.org/xps-intc	xilinx.ovpworld.org/xps-ll-temac	xilinx.ovpworld.org/xps-mch-emc
xilinx.ovpworld.org/xps-sysace	xilinx.ovpworld.org/xps-timer	xilinx.ovpworld.org/xps-uartlite
xilinx.ovpworld.org/zynq_7000-can	xilinx.ovpworld.org/zynq_7000-ddrc	

5.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

5.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

6.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: imperas.com/products.

7.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the

implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

8.0 Parts of peripheral models

8.1 Configuring the Peripheral Instance with Parameters

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

8.2 Net Ports

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.
The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

8.3 Bus master ports

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

8.4 Bus slave ports

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

8.5 Packetnets

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: OVP_Peripheral_Modeling_Guide.pdf, OVPsim_and_CpuManager_User_Guide.pdf and the example: $IMPERAS_HOME/Examples/Models/Peripherals/packetnet.

9.0 More information (documentation) on peripheral models and modeling

More information on modeling and APIs can be found at: OVPworld.org/technology_apis.

Specifics on modeling peripherals can be found: OVP_Peripheral_Modeling_Guide.pdf.

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.
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