OVP Guide to Using Processor Models

Model specific information for Renesas_r8c

Imperas Software Limited
Imperas Buildings, North Weston
Thame, Oxfordshire, OX9 2HA, U.K.
docs@imperas.com

Author	Imperas Software Limited
Version	20211118.0
Filename	OVP_Model_Specific_Information_m16c_r8c.pdf
Created	31 December 2021
Status	OVP Standard Release

Copyright Notice

Right to Copy Documentation

Destination Control Statement

Disclaimer

Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

Contents

Chapter 1

Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

M16c Family 16Bit CISC processor model.

1.2 Licensing

1.3 Limitations

Core Instruction Set Architecture only.

Interrupt and Reset Signals are TBD.

1.4 Verification

Model has been validated correct by running through extensive instruction level tests

1.5 Reference

Renesas 16-bit Single-Chip MicroComputerM16C/60, M16C/20, M16C/Tiny Series Software Manual Rev 4.00 2004.01(rej09b0137_m16csm.pdf)

Chapter 2

Configuration

2.1 Location

This model's VLNV is posedgesoft.ovpworld.org/processor/m16c/1.0.
The model source is usually at:
$IMPERAS_HOME/ImperasLib/source/posedgesoft.ovpworld.org/processor/m16c/1.0
The model binary is usually at:
$IMPERAS_HOME/lib/$IMPERAS_ARCH/ImperasLib/posedgesoft.ovpworld.org/processor/m16c/1.0

2.2 GDB Path

The default GDB for this model is: $IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/m32c-elf-gdb.

2.3 Semi-Host Library

The default semi-host library file is posedgesoft.ovpworld.org/semihosting/m16cNewlib/1.0

2.4 Processor Endian-ness

This is a LITTLE endian model.

2.5 QuantumLeap Support

A simulator using this processor will not be able to use QuantumLeap.

2.6 Processor ELF code

ELF codes supported by this model are:0x75 and 0x78.

Chapter 3

All Variants in this model

This model has these variants

Variant	Description
m16c	
r8c	(described in this document)

Table 3.1: All Variants in this model

Chapter 4

Bus Master Ports

This model has these bus master ports.

Name	min	max	Connect?	Description
INSTRUCTION	32	32	mandatory	
DATA	32	32	optional	

Table 4.1: Bus Master Ports

Chapter 5

Bus Slave Ports

This model has no bus slave ports.

Chapter 6

Net Ports

This model has these net ports.

Name	Type	Connect?	Description
reset	input	optional	
nmi	input	optional	
int_per	input	optional	
int_ack	output	optional	

Table 6.1: Net Ports

Chapter 7

FIFO Ports

This model has no FIFO ports.

Chapter 8

Formal Parameters

Name	Type	Description
variant	Enumeration	Selects variant (either a generic ISA or a specific model)
compatibility	Enumeration	Specify compatibility mode (isa, gdb or nopbrk)
verbose	Boolean	Specify verbose output messages

Table 8.1: Parameters

8.1 Parameter values

These are the current parameter values.

Name	Value
(Others)	
variant	r8c
compatibility	isa
verbose	T

Table 8.2: Parameter values

Chapter 9

Execution Modes

This model does not have different execution modes.

Chapter 10

Exceptions

Exception	Code
Undefined	0
Overflow	1
BRK	2
AddressMatch	3
SingleStep	4
Watchdog	5
DBC	6
NMI	7
Reset	8
Fetch	9

Table 10.1: Exceptions implemented by this processor

Chapter 11

Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.
This model documentation shows the settings and hierarchy of the default settings for this model variant.

11.1 Level 1

This level in the model hierarchy has 2 commands.
This level in the model hierarchy has no register groups.
This level in the model hierarchy has no children.

Chapter 12

Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

12.1 Level 1

12.1.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.1: isync command arguments

12.1.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-memory	String	show memory accesses by this instruction. Argument can be any combination of X (execute), L (load or store access) and S (system)
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-processorname	Boolean	Include processor name in all trace lines
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.2: itrace command arguments

Chapter 13

Registers

13.1 Level 1

Name	Bits	Initial-Hex	RW	Description
R0	16	0	rw	
R1	16	0	rw	
R2	16	0	rw	
R3	16	0	rw	
A0	16	0	rw	
A1	16	0	rw	
FB	16	0	rw	
R0B	16	0	rw	
R1B	16	0	rw	
R2B	16	0	rw	
R3B	16	0	rw	
A0B	16	0	rw	
A1B	16	0	rw	
FBB	16	0	rw	
SB	16	0	rw	
USP	16	0	rw	
ISP	16	0	rw	
INTB	20	0	rw	
PC	20	0	rw	program counter
FLG	16	0	rw	

Table 13.1: Registers at level 1