



## Imperas Peripheral Model Guide

### Model Specific Information for freescale.ovpworld.org / KinetisUSB

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Author	Imperas Software Limited
Version	20211118.0
Filename	OVP_Peripheral_Specific_Information_KinetisUSB.pdf
Created	31 December 2021
Status	OVP Standard Release

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## Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit [OVPworld.org](http://OVPworld.org).

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## 1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

### 1.1 Description

Model of the USB peripheral used on the Freescale Kinetis platform

### 1.2 Limitations

Provides the base behaviour for the OVP Freescale Kinetis platforms

### 1.3 Reference

[www.freescale.com/Kinetis](http://www.freescale.com/Kinetis)

### 1.4 Licensing

Open Source Apache 2.0

### 1.5 Location

The KinetisUSB peripheral model is located in an Imperas/OVP installation at the VLNV: [freescale.ovpworld.org / peripheral / KinetisUSB / 1.0](http://freescale.ovpworld.org/peripheral/KinetisUSB/1.0).

## 2.0 Net Ports

This model has the following net ports:

Table 1. Net Ports

Name	Type	Must Be Connected	Description
Reset	input	F (False)	

## 3.0 Bus Slave Ports

This model has the following bus slave ports:

### 3.1 Bus Slave Port: *bport1*

Table 2. Bus Slave Port: *bport1*

Name	Size (bytes)	Must Be Connected	Description
<i>bport1</i>	0x1000	F (False)	

Table 3. Bus Slave Port: *bport1* Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_PERID	0x0	8	Peripheral ID Register, offset: 0x0		

ab_IDCOMP	0x4	8	Peripheral ID Complement Register, offset: 0x4		
ab_REV	0x8	8	Peripheral Revision Register, offset: 0x8		
ab_ADDINFO	0xc	8	Peripheral Additional Info Register, offset: 0xC		
ab_OTGISTAT	0x10	8	OTG Interrupt Status Register, offset: 0x10		
ab_OTGICR	0x14	8	OTG Interrupt Control Register, offset: 0x14		
ab_OTGSTAT	0x18	8	OTG Status Register, offset: 0x18		
ab_OTGCTL	0x1c	8	OTG Control Register, offset: 0x1C		
ab_ISTAT	0x80	8	Interrupt Status Register, offset: 0x80		
ab_INTEN	0x84	8	Interrupt Enable Register, offset: 0x84		
ab_ERRSTAT	0x88	8	Error Interrupt Status Register, offset: 0x88		
ab_ERREN	0x8c	8	Error Interrupt Enable Register, offset: 0x8C		
ab_STAT	0x90	8	Status Register, offset: 0x90		
ab_CTL	0x94	8	Control Register, offset: 0x94		
ab_ADDR	0x98	8	Address Register, offset: 0x98		
ab_BDTPAGE1	0x9c	8	BDT Page Register 1, offset: 0x9C		
ab_FRMNUML	0xa0	8	Frame Number Register Low, offset: 0xA0		
ab_FRMNUMH	0xa4	8	Frame Number Register High, offset: 0xA4		
ab_TOKEN	0xa8	8	Token Register, offset: 0xA8		
ab_SOFTHLD	0xac	8	SOF Threshold Register, offset: 0xAC		
ab_BDTPAGE2	0xb0	8	BDT Page Register 2, offset: 0xB0		
ab_BDTPAGE3	0xb4	8	BDT Page Register 3, offset: 0xB4		
ab_ENDPOINT0	0xc0	8	Endpoint Control Register 0, offset 0xc0		
ab_ENDPOINT1	0xc4	8	Endpoint Control Register 1, offset 0xc4		
ab_ENDPOINT2	0xc8	8	Endpoint Control Register 2, offset 0xc8		
ab_ENDPOINT3	0xcc	8	Endpoint Control Register 3, offset 0xcc		
ab_ENDPOINT4	0xd0	8	Endpoint Control Register 4, offset 0xd0		
ab_ENDPOINT5	0xd4	8	Endpoint Control Register 5, offset 0xd4		

ab_ENDPOINT6	0xd8	8	Endpoint Control Register 6, offset 0xd8		
ab_ENDPOINT7	0xdc	8	Endpoint Control Register 7, offset 0xdc		
ab_ENDPOINT8	0xe0	8	Endpoint Control Register 8, offset 0xe0		
ab_ENDPOINT9	0xe4	8	Endpoint Control Register 9, offset 0xe4		
ab_ENDPOINT10	0xe8	8	Endpoint Control Register 10, offset 0xe8		
ab_ENDPOINT11	0xec	8	Endpoint Control Register 11, offset 0xec		
ab_ENDPOINT12	0xf0	8	Endpoint Control Register 12, offset 0xf0		
ab_ENDPOINT13	0xf4	8	Endpoint Control Register 13, offset 0xf4		
ab_ENDPOINT14	0xf8	8	Endpoint Control Register 14, offset 0xf8		
ab_ENDPOINT15	0xfc	8	Endpoint Control Register 15, offset 0xfc		
ab_USBCTRL	0x100	8	USB Control Register, offset: 0x100		
ab_OBSERVE	0x104	8	USB OTG Observe Register, offset: 0x104		
ab_CONTROL	0x108	8	USB OTG Control Register, offset: 0x108		
ab_USBTRC0	0x10c	8	USB Transceiver Control Register 0, offset: 0x10C		
ab_USBFMRADJUST	0x114	8	Frame Adjust Register, offset: 0x114		

## 4.0 Platforms that use this peripheral component

Peripheral components can be used in many different platforms, including those developed by Imperas or by other users of OVP. You can use this peripheral in your own platforms.

Table 4. Publicly available platforms using peripheral 'KinetisUSB'

Platform Name	Vendor
FreescaleKinetis60	<a href="http://freescale.ovpworld.org">freescale.ovpworld.org</a>
FreescaleKinetis64	<a href="http://freescale.ovpworld.org">freescale.ovpworld.org</a>

## 5.0 Peripheral components in the library

Table 5. Publicly available Imperas/OVP peripheral models (227 models)

Peripheral	Peripheral	Peripheral
<a href="https://freescale.ovpworld.org/KinetisUSBDCD">freescale.ovpworld.org/KinetisUSBDCD</a>	<a href="https://freescale.ovpworld.org/KinetisUSBHS">freescale.ovpworld.org/KinetisUSBHS</a>	<a href="https://freescale.ovpworld.org/KinetisVREF">freescale.ovpworld.org/KinetisVREF</a>
<a href="https://freescale.ovpworld.org/KinetisWDOG">freescale.ovpworld.org/KinetisWDOG</a>	<a href="https://freescale.ovpworld.org/Uart">freescale.ovpworld.org/Uart</a>	<a href="https://freescale.ovpworld.org/VybridADC">freescale.ovpworld.org/VybridADC</a>
<a href="https://freescale.ovpworld.org/VybridANADIG">freescale.ovpworld.org/VybridANADIG</a>	<a href="https://freescale.ovpworld.org/VybridCCM">freescale.ovpworld.org/VybridCCM</a>	<a href="https://freescale.ovpworld.org/VybridDMA">freescale.ovpworld.org/VybridDMA</a>
<a href="https://freescale.ovpworld.org/VybridGPIO">freescale.ovpworld.org/VybridGPIO</a>	<a href="https://freescale.ovpworld.org/VybridI2C">freescale.ovpworld.org/VybridI2C</a>	<a href="https://freescale.ovpworld.org/VybridLCD">freescale.ovpworld.org/VybridLCD</a>
<a href="https://freescale.ovpworld.org/VybridQUADSPI">freescale.ovpworld.org/VybridQUADSPI</a>	<a href="https://freescale.ovpworld.org/VybridSDHC">freescale.ovpworld.org/VybridSDHC</a>	<a href="https://freescale.ovpworld.org/VybridSPI">freescale.ovpworld.org/VybridSPI</a>
<a href="https://freescale.ovpworld.org/VybridUART">freescale.ovpworld.org/VybridUART</a>	<a href="https://freescale.ovpworld.org/VybridUSB">freescale.ovpworld.org/VybridUSB</a>	<a href="https://imperas.ovpworld.org/frameBuffer">imperas.ovpworld.org/frameBuffer</a>
<a href="https://imperas.ovpworld.org/uart">imperas.ovpworld.org/uart</a>	<a href="https://imperas.ovpworld.org/usecCounter">imperas.ovpworld.org/usecCounter</a>	<a href="https://intel.ovpworld.org/82077AA">intel.ovpworld.org/82077AA</a>
<a href="https://intel.ovpworld.org/82371EB">intel.ovpworld.org/82371EB</a>	<a href="https://intel.ovpworld.org/8253">intel.ovpworld.org/8253</a>	<a href="https://intel.ovpworld.org/8259A">intel.ovpworld.org/8259A</a>
<a href="https://intel.ovpworld.org/NorFlash48F4400">intel.ovpworld.org/NorFlash48F4400</a>	<a href="https://intel.ovpworld.org/PciIDE">intel.ovpworld.org/PciIDE</a>	<a href="https://intel.ovpworld.org/PciPM">intel.ovpworld.org/PciPM</a>
<a href="https://intel.ovpworld.org/PciUSB">intel.ovpworld.org/PciUSB</a>	<a href="https://intel.ovpworld.org/Ps2Control">intel.ovpworld.org/Ps2Control</a>	<a href="https://marvell.ovpworld.org/GT6412x">marvell.ovpworld.org/GT6412x</a>
<a href="https://maxim.ovpworld.org/max673x">maxim.ovpworld.org/max673x</a>	<a href="https://microsemi.ovpworld.org/CoreUARTapb">microsemi.ovpworld.org/CoreUARTapb</a>	<a href="https://mips.ovpworld.org/16450C">mips.ovpworld.org/16450C</a>
<a href="https://mips.ovpworld.org/MaltaFPGA">mips.ovpworld.org/MaltaFPGA</a>	<a href="https://mips.ovpworld.org/SmartLoaderLinux">mips.ovpworld.org/SmartLoaderLinux</a>	<a href="https://motorola.ovpworld.org/MC146818">motorola.ovpworld.org/MC146818</a>
<a href="https://national.ovpworld.org/16450">national.ovpworld.org/16450</a>	<a href="https://national.ovpworld.org/16550">national.ovpworld.org/16550</a>	<a href="https://national.ovpworld.org/16550_4bytes">national.ovpworld.org/16550_4bytes</a>
<a href="https://nxp.ovpworld.org/iMX6_Analog">nxp.ovpworld.org/iMX6_Analog</a>	<a href="https://nxp.ovpworld.org/iMX6_CCM">nxp.ovpworld.org/iMX6_CCM</a>	<a href="https://nxp.ovpworld.org/iMX6_GPC">nxp.ovpworld.org/iMX6_GPC</a>
<a href="https://nxp.ovpworld.org/iMX6_GPIO">nxp.ovpworld.org/iMX6_GPIO</a>	<a href="https://nxp.ovpworld.org/iMX6_GPT">nxp.ovpworld.org/iMX6_GPT</a>	<a href="https://nxp.ovpworld.org/iMX6_MMDC">nxp.ovpworld.org/iMX6_MMDC</a>
<a href="https://nxp.ovpworld.org/iMX6_SDHC">nxp.ovpworld.org/iMX6_SDHC</a>	<a href="https://nxp.ovpworld.org/iMX6_SRC">nxp.ovpworld.org/iMX6_SRC</a>	<a href="https://nxp.ovpworld.org/iMX6_UART">nxp.ovpworld.org/iMX6_UART</a>
<a href="https://nxp.ovpworld.org/iMX6_WDOG">nxp.ovpworld.org/iMX6_WDOG</a>	<a href="https://ovpworld.org/Alpha2x16Display">ovpworld.org/Alpha2x16Display</a>	<a href="https://ovpworld.org/DynamicBridge">ovpworld.org/DynamicBridge</a>
<a href="https://ovpworld.org/FlashDevice">ovpworld.org/FlashDevice</a>	<a href="https://ovpworld.org/ledRegister">ovpworld.org/ledRegister</a>	<a href="https://ovpworld.org/SerInt">ovpworld.org/SerInt</a>
<a href="https://ovpworld.org/SimpleDma">ovpworld.org/SimpleDma</a>	<a href="https://ovpworld.org/switchRegister">ovpworld.org/switchRegister</a>	<a href="https://ovpworld.org/temperatureSensor">ovpworld.org/temperatureSensor</a>
<a href="https://ovpworld.org/trap">ovpworld.org/trap</a>	<a href="https://ovpworld.org/trap4K">ovpworld.org/trap4K</a>	<a href="https://ovpworld.org/vEthernet_Bridge">ovpworld.org/vEthernet_Bridge</a>
<a href="https://ovpworld.org/VirtioBlkMMIO">ovpworld.org/VirtioBlkMMIO</a>	<a href="https://ovpworld.org/VirtioNetMMIO">ovpworld.org/VirtioNetMMIO</a>	<a href="https://philips.ovpworld.org/ISP1761">philips.ovpworld.org/ISP1761</a>
<a href="https://renesas.ovpworld.org/adc">renesas.ovpworld.org/adc</a>	<a href="https://renesas.ovpworld.org/bcu">renesas.ovpworld.org/bcu</a>	<a href="https://renesas.ovpworld.org/brg">renesas.ovpworld.org/brg</a>
<a href="https://renesas.ovpworld.org/can">renesas.ovpworld.org/can</a>	<a href="https://renesas.ovpworld.org/can">renesas.ovpworld.org/can</a>	<a href="https://renesas.ovpworld.org/clkgen">renesas.ovpworld.org/clkgen</a>
<a href="https://renesas.ovpworld.org/crc">renesas.ovpworld.org/crc</a>	<a href="https://renesas.ovpworld.org/csib">renesas.ovpworld.org/csib</a>	<a href="https://renesas.ovpworld.org/csie">renesas.ovpworld.org/csie</a>
<a href="https://renesas.ovpworld.org/dma">renesas.ovpworld.org/dma</a>	<a href="https://renesas.ovpworld.org/intc">renesas.ovpworld.org/intc</a>	<a href="https://renesas.ovpworld.org/memc">renesas.ovpworld.org/memc</a>
<a href="https://renesas.ovpworld.org/rng">renesas.ovpworld.org/rng</a>	<a href="https://renesas.ovpworld.org/taa">renesas.ovpworld.org/taa</a>	<a href="https://renesas.ovpworld.org/tms">renesas.ovpworld.org/tms</a>
<a href="https://renesas.ovpworld.org/tmt">renesas.ovpworld.org/tmt</a>	<a href="https://renesas.ovpworld.org/uartc">renesas.ovpworld.org/uartc</a>	<a href="https://renesas.ovpworld.org/UPD70F3441Logic">renesas.ovpworld.org/UPD70F3441Logic</a>
<a href="https://riscv.ovpworld.org/CLINT">riscv.ovpworld.org/CLINT</a>	<a href="https://riscv.ovpworld.org/PLIC">riscv.ovpworld.org/PLIC</a>	<a href="https://riscv.ovpworld.org/SmartLoaderRV64Linux">riscv.ovpworld.org/SmartLoaderRV64Linux</a>
<a href="https://safepower.ovpworld.org/node">safepower.ovpworld.org/node</a>	<a href="https://safepower.ovpworld.org/NostrumNode">safepower.ovpworld.org/NostrumNode</a>	<a href="https://safepower.ovpworld.org/ring_oscillator">safepower.ovpworld.org/ring_oscillator</a>
<a href="https://safepower.ovpworld.org/TTELNode">safepower.ovpworld.org/TTELNode</a>	<a href="https://sifive.ovpworld.org/artyIO">sifive.ovpworld.org/artyIO</a>	<a href="https://sifive.ovpworld.org/DDRCTL">sifive.ovpworld.org/DDRCTL</a>
<a href="https://sifive.ovpworld.org/gpio">sifive.ovpworld.org/gpio</a>	<a href="https://sifive.ovpworld.org/MSEL">sifive.ovpworld.org/MSEL</a>	<a href="https://sifive.ovpworld.org/PLIC">sifive.ovpworld.org/PLIC</a>
<a href="https://sifive.ovpworld.org/PRCI">sifive.ovpworld.org/PRCI</a>	<a href="https://sifive.ovpworld.org/pwm">sifive.ovpworld.org/pwm</a>	<a href="https://sifive.ovpworld.org/spi">sifive.ovpworld.org/spi</a>
<a href="https://sifive.ovpworld.org/teststatus">sifive.ovpworld.org/teststatus</a>	<a href="https://sifive.ovpworld.org/UART">sifive.ovpworld.org/UART</a>	<a href="https://smc.ovpworld.org/LAN9118">smc.ovpworld.org/LAN9118</a>
<a href="https://smc.ovpworld.org/LAN91C111">smc.ovpworld.org/LAN91C111</a>	<a href="https://ti.ovpworld.org/tca6416a">ti.ovpworld.org/tca6416a</a>	<a href="https://ti.ovpworld.org/UartInterface">ti.ovpworld.org/UartInterface</a>
<a href="https://ti.ovpworld.org/ucd9012a">ti.ovpworld.org/ucd9012a</a>	<a href="https://ti.ovpworld.org/ucd9248">ti.ovpworld.org/ucd9248</a>	<a href="https://vendor.com/fifo">vendor.com/fifo</a>
<a href="https://xilinx.ovpworld.org/axi-gpio">xilinx.ovpworld.org/axi-gpio</a>	<a href="https://xilinx.ovpworld.org/axi-intc">xilinx.ovpworld.org/axi-intc</a>	<a href="https://xilinx.ovpworld.org/axi-pcie">xilinx.ovpworld.org/axi-pcie</a>
<a href="https://xilinx.ovpworld.org/axi-timer">xilinx.ovpworld.org/axi-timer</a>	<a href="https://xilinx.ovpworld.org/logiccore-fit">xilinx.ovpworld.org/logiccore-fit</a>	<a href="https://xilinx.ovpworld.org/mdm">xilinx.ovpworld.org/mdm</a>
<a href="https://xilinx.ovpworld.org/mpmc">xilinx.ovpworld.org/mpmc</a>	<a href="https://xilinx.ovpworld.org/xps-gpio">xilinx.ovpworld.org/xps-gpio</a>	<a href="https://xilinx.ovpworld.org/xps-iic">xilinx.ovpworld.org/xps-iic</a>
<a href="https://xilinx.ovpworld.org/xps-intc">xilinx.ovpworld.org/xps-intc</a>	<a href="https://xilinx.ovpworld.org/xps-ll-temac">xilinx.ovpworld.org/xps-ll-temac</a>	<a href="https://xilinx.ovpworld.org/xps-mch-emc">xilinx.ovpworld.org/xps-mch-emc</a>
<a href="https://xilinx.ovpworld.org/xps-sysace">xilinx.ovpworld.org/xps-sysace</a>	<a href="https://xilinx.ovpworld.org/xps-timer">xilinx.ovpworld.org/xps-timer</a>	<a href="https://xilinx.ovpworld.org/xps-uartlite">xilinx.ovpworld.org/xps-uartlite</a>
<a href="https://xilinx.ovpworld.org/zynq_7000-can">xilinx.ovpworld.org/zynq_7000-can</a>	<a href="https://xilinx.ovpworld.org/zynq_7000-ddrc">xilinx.ovpworld.org/zynq_7000-ddrc</a>	<a href="https://xilinx.ovpworld.org/zynq_7000-devcfg">xilinx.ovpworld.org/zynq_7000-devcfg</a>
<a href="https://xilinx.ovpworld.org/zynq_7000-dmac">xilinx.ovpworld.org/zynq_7000-dmac</a>	<a href="https://xilinx.ovpworld.org/zynq_7000-gpio">xilinx.ovpworld.org/zynq_7000-gpio</a>	<a href="https://xilinx.ovpworld.org/zynq_7000-iic">xilinx.ovpworld.org/zynq_7000-iic</a>
<a href="https://xilinx.ovpworld.org/zynq_7000-ocm">xilinx.ovpworld.org/zynq_7000-ocm</a>	<a href="https://xilinx.ovpworld.org/zynq_7000-qos301">xilinx.ovpworld.org/zynq_7000-qos301</a>	<a href="https://xilinx.ovpworld.org/zynq_7000-qspi">xilinx.ovpworld.org/zynq_7000-qspi</a>

<a href="http://xilinx.ovpworld.org/zynq_7000-sdio">xilinx.ovpworld.org/zynq_7000-sdio</a>	<a href="http://xilinx.ovpworld.org/zynq_7000-slcr">xilinx.ovpworld.org/zynq_7000-slcr</a>	<a href="http://xilinx.ovpworld.org/zynq_7000-spi">xilinx.ovpworld.org/zynq_7000-spi</a>
<a href="http://xilinx.ovpworld.org/zynq_7000-swdt">xilinx.ovpworld.org/zynq_7000-swdt</a>	<a href="http://xilinx.ovpworld.org/zynq_7000-ttc">xilinx.ovpworld.org/zynq_7000-ttc</a>	<a href="http://xilinx.ovpworld.org/zynq_7000-tz_GPVsecurity">xilinx.ovpworld.org/zynq_7000-tz_GPVsecurity</a>
<a href="http://xilinx.ovpworld.org/zynq_7000-tz_security">xilinx.ovpworld.org/zynq_7000-tz_security</a>	<a href="http://xilinx.ovpworld.org/zynq_7000-usb">xilinx.ovpworld.org/zynq_7000-usb</a>	<a href="http://altera.ovpworld.org/dw-apb-timer">altera.ovpworld.org/dw-apb-timer</a>
<a href="http://altera.ovpworld.org/dw-apb-uart">altera.ovpworld.org/dw-apb-uart</a>	<a href="http://altera.ovpworld.org/IntervalTimer32Core">altera.ovpworld.org/IntervalTimer32Core</a>	<a href="http://altera.ovpworld.org/IntervalTimer64Core">altera.ovpworld.org/IntervalTimer64Core</a>
<a href="http://altera.ovpworld.org/JtagUart">altera.ovpworld.org/JtagUart</a>	<a href="http://altera.ovpworld.org/PerformanceCounterCore">altera.ovpworld.org/PerformanceCounterCore</a>	<a href="http://altera.ovpworld.org/RSTMGR">altera.ovpworld.org/RSTMGR</a>
<a href="http://altera.ovpworld.org/SystemIDCore">altera.ovpworld.org/SystemIDCore</a>	<a href="http://altera.ovpworld.org/Uart">altera.ovpworld.org/Uart</a>	<a href="http://amd.ovpworld.org/79C970">amd.ovpworld.org/79C970</a>
<a href="http://andes.ovpworld.org/ATCUART100">andes.ovpworld.org/ATCUART100</a>	<a href="http://andes.ovpworld.org/NCEPLIC100">andes.ovpworld.org/NCEPLIC100</a>	<a href="http://andes.ovpworld.org/NCEPLMT100">andes.ovpworld.org/NCEPLMT100</a>
<a href="http://arm.ovpworld.org/AaciPL041">arm.ovpworld.org/AaciPL041</a>	<a href="http://arm.ovpworld.org/CompactFlashRegs">arm.ovpworld.org/CompactFlashRegs</a>	<a href="http://arm.ovpworld.org/CoreModule9x6">arm.ovpworld.org/CoreModule9x6</a>
<a href="http://arm.ovpworld.org/DebugLedAndDipSwitch">arm.ovpworld.org/DebugLedAndDipSwitch</a>	<a href="http://arm.ovpworld.org/DMemCtrlPL341">arm.ovpworld.org/DMemCtrlPL341</a>	<a href="http://arm.ovpworld.org/IcpControl">arm.ovpworld.org/IcpControl</a>
<a href="http://arm.ovpworld.org/IcpCounterTimer">arm.ovpworld.org/IcpCounterTimer</a>	<a href="http://arm.ovpworld.org/IntICP">arm.ovpworld.org/IntICP</a>	<a href="http://arm.ovpworld.org/IntICP">arm.ovpworld.org/IntICP</a>
<a href="http://arm.ovpworld.org/KbPL050">arm.ovpworld.org/KbPL050</a>	<a href="http://arm.ovpworld.org/L2CachePL310">arm.ovpworld.org/L2CachePL310</a>	<a href="http://arm.ovpworld.org/LcdPL110">arm.ovpworld.org/LcdPL110</a>
<a href="http://arm.ovpworld.org/MmciPL181">arm.ovpworld.org/MmciPL181</a>	<a href="http://arm.ovpworld.org/RtcPL031">arm.ovpworld.org/RtcPL031</a>	<a href="http://arm.ovpworld.org/SerBusDviRegs">arm.ovpworld.org/SerBusDviRegs</a>
<a href="http://arm.ovpworld.org/SmartLoaderArm64Linux">arm.ovpworld.org/SmartLoaderArm64Linux</a>	<a href="http://arm.ovpworld.org/SmartLoaderArmLinux">arm.ovpworld.org/SmartLoaderArmLinux</a>	<a href="http://arm.ovpworld.org/SMemCtrlPL354">arm.ovpworld.org/SMemCtrlPL354</a>
<a href="http://arm.ovpworld.org/SysCtrlSP810">arm.ovpworld.org/SysCtrlSP810</a>	<a href="http://arm.ovpworld.org/TimerSP804">arm.ovpworld.org/TimerSP804</a>	<a href="http://arm.ovpworld.org/TzpcBP147">arm.ovpworld.org/TzpcBP147</a>
<a href="http://arm.ovpworld.org/UartPL011">arm.ovpworld.org/UartPL011</a>	<a href="http://arm.ovpworld.org/VexpressSysRegs">arm.ovpworld.org/VexpressSysRegs</a>	<a href="http://arm.ovpworld.org/WdtSP805">arm.ovpworld.org/WdtSP805</a>
<a href="http://atmel.ovpworld.org/AdvancedInterruptController">atmel.ovpworld.org/AdvancedInterruptController</a>	<a href="http://atmel.ovpworld.org/ParallelIOController">atmel.ovpworld.org/ParallelIOController</a>	<a href="http://atmel.ovpworld.org/PowerSaving">atmel.ovpworld.org/PowerSaving</a>
<a href="http://atmel.ovpworld.org/SpecialFunction">atmel.ovpworld.org/SpecialFunction</a>	<a href="http://atmel.ovpworld.org/TimerCounter">atmel.ovpworld.org/TimerCounter</a>	<a href="http://atmel.ovpworld.org/UsartInterface">atmel.ovpworld.org/UsartInterface</a>
<a href="http://atmel.ovpworld.org/WatchdogTimer">atmel.ovpworld.org/WatchdogTimer</a>	<a href="http://cadence.ovpworld.org/gem">cadence.ovpworld.org/gem</a>	<a href="http://cadence.ovpworld.org/uart">cadence.ovpworld.org/uart</a>
<a href="http://cirrus.ovpworld.org/GD5446">cirrus.ovpworld.org/GD5446</a>	<a href="http://freescale.ovpworld.org/KinetisADC">freescale.ovpworld.org/KinetisADC</a>	<a href="http://freescale.ovpworld.org/KinetisAIPS">freescale.ovpworld.org/KinetisAIPS</a>
<a href="http://freescale.ovpworld.org/KinetisAXBS">freescale.ovpworld.org/KinetisAXBS</a>	<a href="http://freescale.ovpworld.org/KinetisCAN">freescale.ovpworld.org/KinetisCAN</a>	<a href="http://freescale.ovpworld.org/KinetisCMP">freescale.ovpworld.org/KinetisCMP</a>
<a href="http://freescale.ovpworld.org/KinetisCMT">freescale.ovpworld.org/KinetisCMT</a>	<a href="http://freescale.ovpworld.org/KinetisCRC">freescale.ovpworld.org/KinetisCRC</a>	<a href="http://freescale.ovpworld.org/KinetisDAC">freescale.ovpworld.org/KinetisDAC</a>
<a href="http://freescale.ovpworld.org/KinetisDDR">freescale.ovpworld.org/KinetisDDR</a>	<a href="http://freescale.ovpworld.org/KinetisDMA">freescale.ovpworld.org/KinetisDMA</a>	<a href="http://freescale.ovpworld.org/KinetisDMAC">freescale.ovpworld.org/KinetisDMAC</a>
<a href="http://freescale.ovpworld.org/KinetisDMAMUX">freescale.ovpworld.org/KinetisDMAMUX</a>	<a href="http://freescale.ovpworld.org/KinetisENET">freescale.ovpworld.org/KinetisENET</a>	<a href="http://freescale.ovpworld.org/KinetisEWM">freescale.ovpworld.org/KinetisEWM</a>
<a href="http://freescale.ovpworld.org/KinetisFB">freescale.ovpworld.org/KinetisFB</a>	<a href="http://freescale.ovpworld.org/KinetisFMC">freescale.ovpworld.org/KinetisFMC</a>	<a href="http://freescale.ovpworld.org/KinetisFTFE">freescale.ovpworld.org/KinetisFTFE</a>
<a href="http://freescale.ovpworld.org/KinetisFTM">freescale.ovpworld.org/KinetisFTM</a>	<a href="http://freescale.ovpworld.org/KinetisGPIO">freescale.ovpworld.org/KinetisGPIO</a>	<a href="http://freescale.ovpworld.org/KinetisI2C">freescale.ovpworld.org/KinetisI2C</a>
<a href="http://freescale.ovpworld.org/KinetisI2S">freescale.ovpworld.org/KinetisI2S</a>	<a href="http://freescale.ovpworld.org/KinetisLLWU">freescale.ovpworld.org/KinetisLLWU</a>	<a href="http://freescale.ovpworld.org/KinetisLPTMR">freescale.ovpworld.org/KinetisLPTMR</a>
<a href="http://freescale.ovpworld.org/KinetisMCG">freescale.ovpworld.org/KinetisMCG</a>	<a href="http://freescale.ovpworld.org/KinetisMPU">freescale.ovpworld.org/KinetisMPU</a>	<a href="http://freescale.ovpworld.org/KinetisNFC">freescale.ovpworld.org/KinetisNFC</a>
<a href="http://freescale.ovpworld.org/KinetisOSC">freescale.ovpworld.org/KinetisOSC</a>	<a href="http://freescale.ovpworld.org/KinetisPDB">freescale.ovpworld.org/KinetisPDB</a>	<a href="http://freescale.ovpworld.org/KinetisPIT">freescale.ovpworld.org/KinetisPIT</a>
<a href="http://freescale.ovpworld.org/KinetisPMC">freescale.ovpworld.org/KinetisPMC</a>	<a href="http://freescale.ovpworld.org/KinetisPORT">freescale.ovpworld.org/KinetisPORT</a>	<a href="http://freescale.ovpworld.org/KinetisRCM">freescale.ovpworld.org/KinetisRCM</a>
<a href="http://freescale.ovpworld.org/KinetisRFSYS">freescale.ovpworld.org/KinetisRFSYS</a>	<a href="http://freescale.ovpworld.org/KinetisRFVBAT">freescale.ovpworld.org/KinetisRFVBAT</a>	<a href="http://freescale.ovpworld.org/KinetisRNG">freescale.ovpworld.org/KinetisRNG</a>
<a href="http://freescale.ovpworld.org/KinetisRTC">freescale.ovpworld.org/KinetisRTC</a>	<a href="http://freescale.ovpworld.org/KinetisSDHC">freescale.ovpworld.org/KinetisSDHC</a>	<a href="http://freescale.ovpworld.org/KinetisSIM">freescale.ovpworld.org/KinetisSIM</a>
<a href="http://freescale.ovpworld.org/KinetisSMC">freescale.ovpworld.org/KinetisSMC</a>	<a href="http://freescale.ovpworld.org/KinetisSPI">freescale.ovpworld.org/KinetisSPI</a>	<a href="http://freescale.ovpworld.org/KinetisTSI">freescale.ovpworld.org/KinetisTSI</a>
<a href="http://freescale.ovpworld.org/KinetisUART">freescale.ovpworld.org/KinetisUART</a>	<a href="http://freescale.ovpworld.org/KinetisUSB">freescale.ovpworld.org/KinetisUSB</a>	



## 6.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

### 6.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

## 7.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: [imperas.com/products](http://imperas.com/products).

## 8.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the

implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

## 9.0 Parts of peripheral models

### *9.1 Configuring the Peripheral Instance with Parameters*

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

### *9.2 Net Ports*

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.

The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

### *9.3 Bus master ports*

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

### *9.4 Bus slave ports*

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

### *9.5 Packetnets*

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: [OVP\\_Peripheral\\_Modeling\\_Guide.pdf](#), [OVPSim\\_and\\_CpuManager\\_User\\_Guide.pdf](#) and the example: [\\$IMPERAS\\_HOME/Examples/Models/Peripherals/packetnet](#).

## 10.0 More information (documentation) on peripheral models and modeling

More information on modeling and APIs can be found at: [OVPworld.org/technology\\_apis](http://OVPworld.org/technology_apis).

Specifics on modeling peripherals can be found: [OVP Peripheral Modeling Guide.pdf](#).

A full list of the currently available OVP documentation is available: [OVPworld.org/documentation](#).

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