# Imperas Peripheral Model Guide

# Model Specific Information for cadence.ovpworld.org / gem

## Imperas Software Limited

Imperas Buildings, North Weston
Thame, Oxfordshire, OX9 2HA, U.K.
docs@imperas.com.

MULTICORE DESIGN SIMPLIFIED

imperas

| Author | Imperas Software Limited |
|---|---|
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# Copyright Notice

## Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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# 1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

## 1.1 Description

Model of Cadence Gigabit Ethernet Controller (GEM). For further details please consult README-EMAC.txt

This model is based upon the data and use in the Xilinx Zynq

Basic network Tx/Rx functionality tested using Xilinx Linux Kernel using wget and other similar tools

Tested with Xilinx SDK Example driver.

## 1.2 Licensing

Open Source Apache 2.0

## 1.3 Limitations

This model is based upon the data from the Xilinx Zynq platform, other registers may not be included.

Does not implement: VLAN, pause frames, filtering or timestamps.

## 1.4 Reference

Zynq-7000 TRM
(https://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf)

## 1.5 Location

The gem peripheral model is located in an Imperas/OVP installation at the VLNV: cadence.ovpworld.org / peripheral / gem / 1.0.

# 2.0 Peripheral Instance Parameters

This model accepts the following parameters:

Table 1. Peripheral Parameters

| Name | Type | Description |
|------|------|-------------|
| pollDelay | uns32 | Read pollDelay |
| outfile | string | Wireshark capture file |
| record | string | Record external events into this file |
| replay | string | Replay external events from this file |

| tapDevice | string | The name of the TAP device |
|---|---|---|
| redir | string | User mode redirection of host port to virtual port (using SLiRP), command format <protocol>:<host port>:<ip address>:<virtual port> |
| tftpPrefix | string | Path to the root of the tftp directory. To use tftp, fetch from the host (gw) IP address. |
| macaddress | uns64 | The MAC address (hex number) |
| macprefix | uns32 | The first two bytes of MAC addresses (hex number) on the VLAN |
| network | string | The (v4) IP address of the local network device. |
| logfile | string | The file to which Ethernet frames should be logged. Uses pcap file format, viewable by Wireshark and other programs. Do not use if this device is connected to a packetnet |

## 3.0 Net Ports

This model has the following net ports:

Table 2. Net Ports

| Name | Type | Must Be Connected | Description |
|---|---|---|---|
| irq | output | F (False) | IRQ Pin |

## 4.0 Bus Master Ports

This model has the following bus master ports:

### 4.1 Bus Master Port: bport2

Table 3. bport2

| Name | Address Width (bits) | Description |
|---|---|---|
| bport2 | 32 | DMA Master Port |

## 5.0 Bus Slave Ports

This model has the following bus slave ports:

### 5.1 Bus Slave Port: bport1

Table 4. Bus Slave Port: bport1

| Name | Size (bytes) | Must Be Connected | Description |
|---|---|---|---|
| bport1 | 0x1000 | T (True) | |

Table 5. Bus Slave Port: bport1 Registers:

| Name | Offset | Width (bits) | Description | R/W | is Volatile |
|---|---|---|---|---|---|
| ab_net_ctrl | 0x0 | 32 | Network Control | | |
| ab_net_cfg | 0x4 | 32 | Network Configuration | | |
| ab_net_status | 0x8 | 32 | Network Status | | |
| ab_user_io | 0xc | 32 | User IO (Not in TRM) | | |
| ab_dma_cfg | 0x10 | 32 | DMA Configuration | | |
| ab_tx_status | 0x14 | 32 | Transmit Status | | |

| ab_rx_qbar | 0x18 | 32 | Receive Buffer Queue Base Address | | |
| ab_tx_qbar | 0x1c | 32 | Transmit Buffer Queue Base Address | | |
| ab_rx_status | 0x20 | 32 | Receive Status | | |
| ab_intr_status | 0x24 | 32 | Interrupt Status | | |
| ab_intr_en | 0x28 | 32 | Interrupt Enable | | |
| ab_intr_dis | 0x2c | 32 | Interrupt Disable | | |
| ab_intr_mask | 0x30 | 32 | Interrupt Mask Status | | |
| ab_phy_maint | 0x34 | 32 | PHY Maintenance | | |
| ab_rx_pauseq | 0x38 | 32 | Received Pause Quantum | | |
| ab_tx_pauseq | 0x3c | 32 | Transmit Pause Quantum | | |
| ab_gem_jml | 0x48 | 32 | GEM Jumbo Max Length | | |
| ab_hash_bot | 0x80 | 32 | Hash Register Bottom [31:0] | | |
| ab_hash_top | 0x84 | 32 | Hash Register Top [63:32] | | |
| ab_spec_addr1_bot | 0x88 | 32 | Specific Address 1 Bottom [31:0] | | |
| ab_spec_addr1_top | 0x8c | 32 | Specific Address 1 Top [47:32] | | |
| ab_spec_addr2_bot | 0x90 | 32 | Specific Address 2 Bottom [31:0] | | |
| ab_spec_addr2_top | 0x94 | 32 | Specific Address 2 Top [47:32] | | |
| ab_spec_addr3_bot | 0x98 | 32 | Specific Address 3 Bottom [31:0] | | |
| ab_spec_addr3_top | 0x9c | 32 | Specific Address 3 Top [47:32] | | |
| ab_spec_addr4_bot | 0xa0 | 32 | Specific Address 4 Bottom [31:0] | | |
| ab_spec_addr4_top | 0xa4 | 32 | Specific Address 4 Top [47:32] | | |
| ab_type_id_match1 | 0xa8 | 32 | Type ID Match 1 | | |
| ab_type_id_match2 | 0xac | 32 | Type ID Match 2 | | |
| ab_type_id_match3 | 0xb0 | 32 | Type ID Match 3 | | |
| ab_type_id_match4 | 0xb4 | 32 | Type ID Match 4 | | |
| ab_wake_on_lan | 0xb8 | 32 | Wake on LAN Register | | |
| ab_ipg_stretch | 0xbc | 32 | IPG stretch register | | |
| ab_stacked_vlan | 0xc0 | 32 | Stacked VLAN Register | | |
| ab_tx_pfc_pause | 0xc4 | 32 | Transmit PFC Pause Register | | |
| ab_spec_addr1_mask_bot | 0xc8 | 32 | Specific Address Mask 1 Bottom [31:0] | | |
| ab_spec_addr1_mask_top | 0xcc | 32 | Specific Address Mask 1 Top [47:32] | | |
| ab_rx_ptp_uni | 0xd4 | 32 | PTP RX Unicast address (Not in TRM) | | |
| ab_tx_ptp_uni | 0xd8 | 32 | PTP TX Unicast address (Not in TRM) | | |
| ab_module_id | 0xfc | 32 | Module ID | | |
| ab_octets_tx_bot | 0x100 | 32 | Octets transmitted [31:0] (in frames without error) | | |

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| ab_octets_tx_top | 0x104 | 32 | Octets transmitted [47:32] (in frames without error) | | |
|---|---|---|---|---|---|
| ab_frames_tx | 0x108 | 32 | Frames Transmitted | | |
| ab_broadcast_frames_tx | 0x10c | 32 | Broadcast frames Tx | | |
| ab_multi_frames_tx | 0x110 | 32 | Multicast frames Tx | | |
| ab_pause_frames_tx | 0x114 | 32 | Pause frames Tx | | |
| ab_frames_64b_tx | 0x118 | 32 | Frames Tx, 64-byte length | | |
| ab_frames_65to127b_tx | 0x11c | 32 | Frames Tx, 65 to 127-byte length | | |
| ab_frames_128to255b_tx | 0x120 | 32 | Frames Tx, 128 to 255-byte length | | |
| ab_frames_256to511b_tx | 0x124 | 32 | Frames Tx, 256 to 511-byte length | | |
| ab_frames_512to1023b_tx | 0x128 | 32 | Frames Tx, 512 to 1023-byte length | | |
| ab_frames_1024to1518b_tx | 0x12c | 32 | Frame Tx, 1024 to 1518-byte length | | |
| ab_frames_1519bplus_tx | 0x130 | 32 | Frame Tx, 1519+byte length (Not in TRM) | | |
| ab_tx_under_runs | 0x134 | 32 | Transmit under runs | | |
| ab_single_collisn_frames | 0x138 | 32 | Single Collision Frames | | |
| ab_multi_collisn_frames | 0x13c | 32 | Multiple Collision Frames | | |
| ab_excessive_collisns | 0x140 | 32 | Excessive Collisions | | |
| ab_late_collisns | 0x144 | 32 | Late Collisions | | |
| ab_deferred_tx_frames | 0x148 | 32 | Deferred Transmission Frames | | |
| ab_carrier_sense_errs | 0x14c | 32 | Carrier Sense Errors. | | |
| ab_octets_rx_bot | 0x150 | 32 | Octets Received [31:0] | | |
| ab_octets_rx_top | 0x154 | 32 | Octets Received [47:32] | | |
| ab_frames_rx | 0x158 | 32 | Frames Received | | |
| ab_bdcast_frames_rx | 0x15c | 32 | Broadcast Frames Rx | | |
| ab_multi_frames_rx | 0x160 | 32 | Multicast Frames Rx | | |
| ab_pause_rx | 0x164 | 32 | Pause Frames Rx | | |
| ab_frames_64b_rx | 0x168 | 32 | Frames Rx, 64-byte length | | |
| ab_frames_65to127b_rx | 0x16c | 32 | Frames Rx, 65 to 127-byte length | | |
| ab_frames_128to255b_rx | 0x170 | 32 | Frames Rx, 128 to 255-byte length | | |
| ab_frames_256to511b_rx | 0x174 | 32 | Frames Rx, 256 to 511-byte length | | |
| ab_frames_512to1023b_rx | 0x178 | 32 | Frames Rx, 512 to 1023-byte length | | |
| ab_frames_1024to1518b_rx | 0x17c | 32 | Frames Rx, 1024 to 1518-byte length | | |
| ab_frames_1519bplus_rx | 0x180 | 32 | Frames Rx, 1519+byte length (Not in TRM) | | |
| ab_undersz_rx | 0x184 | 32 | Undersize frames received | | |
| ab_oversz_rx | 0x188 | 32 | Oversize frames received | | |
| ab_jab_rx | 0x18c | 32 | Jabbers received | | |

| ab_fcs_errors | 0x190 | 32 | Frame check sequence errors | | |
|---|---|---|---|---|---|
| ab_length_field_errors | 0x194 | 32 | Length field frame errors | | |
| ab_rx_symbol_errors | 0x198 | 32 | Receive symbol errors | | |
| ab_align_errors | 0x19c | 32 | Alignment errors | | |
| ab_rx_resource_errors | 0x1a0 | 32 | Receive resource errors | | |
| ab_rx_overrun_errors | 0x1a4 | 32 | Receive overrun errors | | |
| ab_ip_hdr_csum_errors | 0x1a8 | 32 | IP header checksum errors | | |
| ab_tcp_csum_errors | 0x1ac | 32 | TCP checksum errors | | |
| ab_udp_csum_errors | 0x1b0 | 32 | UDP checksum error | | |
| ab_timer_strobe_s | 0x1c8 | 32 | 1588 timer sync strobe seconds | | |
| ab_timer_strobe_ns | 0x1cc | 32 | 1588 timer sync strobe nanoseconds | | |
| ab_timer_s | 0x1d0 | 32 | 1588 timer seconds | | |
| ab_timer_ns | 0x1d4 | 32 | 1588 timer nanoseconds | | |
| ab_timer_adjust | 0x1d8 | 32 | 1588 timer adjust | | |
| ab_timer_incr | 0x1dc | 32 | 1588 timer increment | | |
| ab_ptp_tx_s | 0x1e0 | 32 | PTP event frame transmitted seconds | | |
| ab_ptp_tx_ns | 0x1e4 | 32 | PTP event frame transmitted nanoseconds | | |
| ab_ptp_rx_s | 0x1e8 | 32 | PTP event frame received seconds | | |
| ab_ptp_rx_ns | 0x1ec | 32 | PTP event frame received nanoseconds. | | |
| ab_ptp_peer_tx_s | 0x1f0 | 32 | PTP peer event frame transmitted seconds | | |
| ab_ptp_peer_tx_ns | 0x1f4 | 32 | PTP peer event frame transmitted nanoseconds | | |
| ab_ptp_peer_rx_s | 0x1f8 | 32 | PTP peer event frame received seconds | | |
| ab_ptp_peer_rx_ns | 0x1fc | 32 | PTP peer event frame received nanoseconds. | | |
| ab_design_cfg1 | 0x280 | 32 | Design Configuration 1 (Not in TRM) | | |
| ab_design_cfg2 | 0x284 | 32 | Design Configuration 2 | | |
| ab_design_cfg3 | 0x288 | 32 | Design Configuration 3 | | |
| ab_design_cfg4 | 0x28c | 32 | Design Configuration 4 | | |
| ab_design_cfg5 | 0x290 | 32 | Design Configuration 5 | | |
| ab_design_cfg6 | 0x294 | 32 | Design Configuration 6 (Not in TRM) | | |
| ab_tx_bd_cntrl | 0x4cc | 32 | TX descriptor control (Not in TRM) | | |
| ab_rx_bd_cntrl | 0x4d0 | 32 | RX descriptor control (Not in TRM) | | |

## 5.2 Bus Slave Port: phyport

Table 6. Bus Slave Port: phyport

| Name | Size (bytes) | Must Be Connected | Description |
|---|---|---|---|
| | | | |

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| phyport | 0x100 | F (False) | |
|---------|-------|-----------|--|

Table 7. Bus Slave Port: phyport Registers:

| Name | Offset | Width (bits) | Description | R/W | is Volatile |
|------|--------|--------------|-------------|-----|-------------|
| ab_MII_BMCR | 0x0 | 16 | Basic mode control register | | |
| ab_MII_BMSR | 0x2 | 16 | Basic mode status register | | |
| ab_MII_PHYSID1 | 0x4 | 16 | PHYS ID 1 | | |
| ab_MII_PHYSID2 | 0x6 | 16 | PHYS ID 2 | | |
| ab_MII_ADVERTISE | 0x8 | 16 | Advertisement control reg | | |
| ab_MII_LPA | 0xa | 16 | Link partner ability reg | | |
| ab_MII_EXPANSION | 0xc | 16 | Expansion register | | |
| ab_MII_DUMMY1 | 0xe | 16 | Dummy | | |
| ab_MII_DUMMY2 | 0x10 | 16 | Dummy | | |
| ab_MII_CTRL1000 | 0x12 | 16 | 1000BASE-T control | | |
| ab_MII_STAT1000 | 0x14 | 16 | 1000BASE-T status | | |
| ab_MII_DUMMY3 | 0x16 | 16 | Dummy | | |
| ab_MII_DUMMY4 | 0x18 | 16 | Dummy | | |
| ab_MII_MMD_CTRL | 0x1a | 16 | MMD Access Control Register | | |
| ab_MII_MMD_DATA | 0x1c | 16 | MMD Access Data Register | | |
| ab_MII_ESTATUS | 0x1e | 16 | Extended Status | | |
| ab_MII_DUMMY5 | 0x20 | 16 | Dummy | | |
| ab_MII_STS | 0x22 | 16 | Status | | |
| ab_MII_DCOUNTER | 0x24 | 16 | Disconnect counter | | |
| ab_MII_FCSCOUNTER | 0x26 | 16 | False carrier counter | | |
| ab_MII_NWAYTEST | 0x28 | 16 | N-way auto-neg test reg | | |
| ab_MII_RERRCOUNTER | 0x2a | 16 | Receive error counter | | |
| ab_MII_SREVISION | 0x2c | 16 | Silicon revision | | |
| ab_MII_LBRERROR | 0x30 | 16 | Lpback, rx, bypass error | | |
| ab_MII_PHYADDR | 0x32 | 16 | PHY address | | |
| ab_MII_TPISTATUS | 0x36 | 16 | TPI status for 10mbps | | |
| ab_MII_NCONFIG | 0x38 | 16 | Network interface config | | |

## 6.0 Packetnet Ports

This model has the following packetnet ports:

### 6.1 Packetnet Port: phy

Table 8. phy

| Name | Maximum Packet Size (bytes) | Must Be Connected | Description |
|------|------------------------------|-------------------|-------------|
| phy | 1524 | F (False) | The port to connect the packetnet virtual network |

## 7.0 Platforms that use this peripheral component

Peripheral components can be used in many different platforms, including those developed by Imperas or by other users of OVP. You can use this peripheral in your own platforms.

Table 9. Publicly available platforms using peripheral 'gem'

| Platform Name | Vendor |
| --- | --- |
| FU540 | sifive.ovpworld.org |
| Zynq_PS | xilinx.ovpworld.org |

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# 8.0 Peripheral components in the library

Table 10. Publicly available Imperas/OVP peripheral models (227 models)

| Peripheral | Peripheral | Peripheral |
|---|---|---|
| cadence.ovpworld.org/uart | cirrus.ovpworld.org/GD5446 | freescale.ovpworld.org/KinetisADC |
| freescale.ovpworld.org/KinetisAIPS | freescale.ovpworld.org/KinetisAXBS | freescale.ovpworld.org/KinetisCAN |
| freescale.ovpworld.org/KinetisCMP | freescale.ovpworld.org/KinetisCMT | freescale.ovpworld.org/KinetisCRC |
| freescale.ovpworld.org/KinetisDAC | freescale.ovpworld.org/KinetisDDR | freescale.ovpworld.org/KinetisDMA |
| freescale.ovpworld.org/KinetisDMAC | freescale.ovpworld.org/KinetisDMAMUX | freescale.ovpworld.org/KinetisENET |
| freescale.ovpworld.org/KinetisEWM | freescale.ovpworld.org/KinetisFB | freescale.ovpworld.org/KinetisFMC |
| freescale.ovpworld.org/KinetisFTFE | freescale.ovpworld.org/KinetisFTM | freescale.ovpworld.org/KinetisGPIO |
| freescale.ovpworld.org/KinetisI2C | freescale.ovpworld.org/KinetisI2S | freescale.ovpworld.org/KinetisLLWU |
| freescale.ovpworld.org/KinetisLPTMR | freescale.ovpworld.org/KinetisMCG | freescale.ovpworld.org/KinetisMPU |
| freescale.ovpworld.org/KinetisNFC | freescale.ovpworld.org/KinetisOSC | freescale.ovpworld.org/KinetisPDB |
| freescale.ovpworld.org/KinetisPIT | freescale.ovpworld.org/KinetisPMC | freescale.ovpworld.org/KinetisPORT |
| freescale.ovpworld.org/KinetisRCM | freescale.ovpworld.org/KinetisRFSYS | freescale.ovpworld.org/KinetisRFVBAT |
| freescale.ovpworld.org/KinetisRNG | freescale.ovpworld.org/KinetisRTC | freescale.ovpworld.org/KinetisSDHC |
| freescale.ovpworld.org/KinetisSIM | freescale.ovpworld.org/KinetisSMC | freescale.ovpworld.org/KinetisSPI |
| freescale.ovpworld.org/KinetisTSI | freescale.ovpworld.org/KinetisUART | freescale.ovpworld.org/KinetisUSB |
| freescale.ovpworld.org/KinetisUSBDCD | freescale.ovpworld.org/KinetisUSBHS | freescale.ovpworld.org/KinetisVREF |
| freescale.ovpworld.org/KinetisWDOG | freescale.ovpworld.org/Uart | freescale.ovpworld.org/VybridADC |
| freescale.ovpworld.org/VybridANADIG | freescale.ovpworld.org/VybridCCM | freescale.ovpworld.org/VybridDMA |
| freescale.ovpworld.org/VybridGPIO | freescale.ovpworld.org/VybridI2C | freescale.ovpworld.org/VybridLCD |
| freescale.ovpworld.org/VybridQUADSPI | freescale.ovpworld.org/VybridSDHC | freescale.ovpworld.org/VybridSPI |
| freescale.ovpworld.org/VybridUART | freescale.ovpworld.org/VybridUSB | imperas.ovpworld.org/frameBuffer |
| imperas.ovpworld.org/uart | imperas.ovpworld.org/usecCounter | intel.ovpworld.org/82077AA |
| intel.ovpworld.org/82371EB | intel.ovpworld.org/8253 | intel.ovpworld.org/8259A |
| intel.ovpworld.org/NorFlash48F4400 | intel.ovpworld.org/PciIDE | intel.ovpworld.org/PciPM |
| intel.ovpworld.org/PciUSB | intel.ovpworld.org/Ps2Control | marvell.ovpworld.org/GT6412x |
| maxim.ovpworld.org/max673x | microsemi.ovpworld.org/CoreUARTapb | mips.ovpworld.org/16450C |
| mips.ovpworld.org/MaltaFPGA | mips.ovpworld.org/SmartLoaderLinux | motorola.ovpworld.org/MC146818 |
| national.ovpworld.org/16450 | national.ovpworld.org/16550 | national.ovpworld.org/16550_4bytes |
| nxp.ovpworld.org/iMX6_Analog | nxp.ovpworld.org/iMX6_CCM | nxp.ovpworld.org/iMX6_GPC |
| nxp.ovpworld.org/iMX6_GPIO | nxp.ovpworld.org/iMX6_GPT | nxp.ovpworld.org/iMX6_MMDC |
| nxp.ovpworld.org/iMX6_SDHC | nxp.ovpworld.org/iMX6_SRC | nxp.ovpworld.org/iMX6_UART |
| nxp.ovpworld.org/iMX6_WDOG | ovpworld.org/Alpha2x16Display | ovpworld.org/DynamicBridge |
| ovpworld.org/FlashDevice | ovpworld.org/ledRegister | ovpworld.org/SerInt |
| ovpworld.org/SimpleDma | ovpworld.org/switchRegister | ovpworld.org/temperatureSensor |
| ovpworld.org/trap | ovpworld.org/trap4K | ovpworld.org/vEthernet_Bridge |
| ovpworld.org/VirtioBlkMMIO | ovpworld.org/VirtioNetMMIO | philips.ovpworld.org/ISP1761 |
| renesas.ovpworld.org/adc | renesas.ovpworld.org/bcu | renesas.ovpworld.org/brg |
| renesas.ovpworld.org/can | renesas.ovpworld.org/can | renesas.ovpworld.org/clkgen |
| renesas.ovpworld.org/crc | renesas.ovpworld.org/csib | renesas.ovpworld.org/csie |
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| renesas.ovpworld.org/tmt | renesas.ovpworld.org/uartc | renesas.ovpworld.org/UPD70F3441Logic |
| riscv.ovpworld.org/CLINT | riscv.ovpworld.org/PLIC | riscv.ovpworld.org/SmartLoaderRV64Linux |

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| | | |
|---|---|---|
| safepower.ovpworld.org/node | safepower.ovpworld.org/NostrumNode | safepower.ovpworld.org/ring_oscillator |
| safepower.ovpworld.org/TTELNode | sifive.ovpworld.org/artyIO | sifive.ovpworld.org/DDRCTL |
| sifive.ovpworld.org/gpio | sifive.ovpworld.org/MSEL | sifive.ovpworld.org/PLIC |
| sifive.ovpworld.org/PRCI | sifive.ovpworld.org/pwm | sifive.ovpworld.org/spi |
| sifive.ovpworld.org/teststatus | sifive.ovpworld.org/UART | smsc.ovpworld.org/LAN9118 |
| smsc.ovpworld.org/LAN91C111 | ti.ovpworld.org/tca6416a | ti.ovpworld.org/UartInterface |
| ti.ovpworld.org/ucd9012a | ti.ovpworld.org/ucd9248 | vendor.com/fifo |
| xilinx.ovpworld.org/axi-gpio | xilinx.ovpworld.org/axi-intc | xilinx.ovpworld.org/axi-pcie |
| xilinx.ovpworld.org/axi-timer | xilinx.ovpworld.org/logicore-fit | xilinx.ovpworld.org/mdm |
| xilinx.ovpworld.org/mpmc | xilinx.ovpworld.org/xps-gpio | xilinx.ovpworld.org/xps-iic |
| xilinx.ovpworld.org/xps-intc | xilinx.ovpworld.org/xps-ll-temac | xilinx.ovpworld.org/xps-mch-emc |
| xilinx.ovpworld.org/xps-sysace | xilinx.ovpworld.org/xps-timer | xilinx.ovpworld.org/xps-uartlite |
| xilinx.ovpworld.org/zynq_7000-can | xilinx.ovpworld.org/zynq_7000-ddrc | xilinx.ovpworld.org/zynq_7000-devcfg |
| xilinx.ovpworld.org/zynq_7000-dmac | xilinx.ovpworld.org/zynq_7000-gpio | xilinx.ovpworld.org/zynq_7000-iic |
| xilinx.ovpworld.org/zynq_7000-ocm | xilinx.ovpworld.org/zynq_7000-qos301 | xilinx.ovpworld.org/zynq_7000-qspi |
| xilinx.ovpworld.org/zynq_7000-sdio | xilinx.ovpworld.org/zynq_7000-slcr | xilinx.ovpworld.org/zynq_7000-spi |
| xilinx.ovpworld.org/zynq_7000-swdt | xilinx.ovpworld.org/zynq_7000-ttc | xilinx.ovpworld.org/zynq_7000-tz_GPVsecurity |
| xilinx.ovpworld.org/zynq_7000-tz_security | xilinx.ovpworld.org/zynq_7000-usb | altera.ovpworld.org/dw-apb-timer |
| altera.ovpworld.org/dw-apb-uart | altera.ovpworld.org/IntervalTimer32Core | altera.ovpworld.org/IntervalTimer64Core |
| altera.ovpworld.org/JtagUart | altera.ovpworld.org/PerformanceCounterCore | altera.ovpworld.org/RSTMGR |
| altera.ovpworld.org/SystemIDCore | altera.ovpworld.org/Uart | amd.ovpworld.org/79C970 |
| andes.ovpworld.org/ATCUART100 | andes.ovpworld.org/NCEPLIC100 | andes.ovpworld.org/NCEPLMT100 |
| arm.ovpworld.org/AaciPL041 | arm.ovpworld.org/CompactFlashRegs | arm.ovpworld.org/CoreModule9x6 |
| arm.ovpworld.org/DebugLedAndDipSwitch | arm.ovpworld.org/DMemCtrlPL341 | arm.ovpworld.org/IcpControl |
| arm.ovpworld.org/IcpCounterTimer | arm.ovpworld.org/IntICP | arm.ovpworld.org/IntICP |
| arm.ovpworld.org/KbPL050 | arm.ovpworld.org/L2CachePL310 | arm.ovpworld.org/LcdPL110 |
| arm.ovpworld.org/MmciPL181 | arm.ovpworld.org/RtcPL031 | arm.ovpworld.org/SerBusDviRegs |
| arm.ovpworld.org/SmartLoaderArm64Linux | arm.ovpworld.org/SmartLoaderArmLinux | arm.ovpworld.org/SMemCtrlPL354 |
| arm.ovpworld.org/SysCtrlSP810 | arm.ovpworld.org/TimerSP804 | arm.ovpworld.org/TzpcBP147 |
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| atmel.ovpworld.org/WatchdogTimer | cadence.ovpworld.org/gem | |

## 9.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

### 9.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

## 10.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: imperas.com/products.

## 11.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the

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implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

## 12.0 Parts of peripheral models

### 12.1 Configuring the Peripheral Instance with Parameters
A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

### 12.2 Net Ports
Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.
The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

### 12.3 Bus master ports
A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

### 12.4 Bus slave ports
A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

### 12.5 Packetnets
A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: OVP_Peripheral_Modeling_Guide.pdf, OVPsim_and_CpuManager_User_Guide.pdf and the example: $IMPERAS_HOME/Examples/Models/Peripherals/packetnet.

## 13.0 More information (documentation) on peripheral models and modeling
More information on modeling and APIs can be found at: OVPworld.org/technology_apis.

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Specifics on modeling peripherals can be found: [OVP_Peripheral_Modeling_Guide.pdf](OVP_Peripheral_Modeling_Guide.pdf).

A full list of the currently available OVP documentation is available: [OVPworld.org/documentation](OVPworld.org/documentation).
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