Imperas Guide to using Virtual Platforms

Platform / Module Specific Information for renesas.ovpworld.org / RenesasUPD70F3441

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1.0 Platform / Module: RenesasUPD70F3441

This document provides the details of the usage of an Imperas OVP Virtual Platform / Module. The first half of the document covers specifics of this particular component. For more information about Imperas OVP virtual platforms, how they are built and used, please see the later sections in this document.

1.1 Virtual Platform / Module Type

Hardware described using OVP can either be a platform, module, processor, or peripheral.
This hardware component is described as being a module. A module is a component that is used in other modules, platforms, or test harnesses. It is normally used to encapsulate a layer in a hierarchical system.

1.2 Licensing

Open Source Apache 2.0

1.3 Description

The Renesas uPD70F3441 - V850/PHO3 platform

1.4 Limitations

Limitiations of peripheral functionality is documented within the peripheral component.
Unimplemented Components:

- System Controller
- Standby Controller
- Bus Control Unit
- Memory Controller
- CAN Controller
- FlexRay
- I/O Ports
- CPU-CRC
- DATA-CRC
- On-chip Debug Unit
- NBD

Partially Implemented Components (not complete - only certain modes or features modeled or tested)

- DMA

1.5 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

1.6 Location

The RenesasUPD70F3441 virtual platform / module is located in an Imperas/OVP installation at the VLNV: renesas.ovpworld.org / module / RenesasUPD70F3441 / 1.0.

1.7 Module Simulation Attributes

Table 1. Module Simulation Attributes

Attribute	Value	Description
stoponctrlc	stoponctrlc	Stop on control-C

2.0 Processor [renesas.ovpworld.org/processor/v850/1.0] instance: CPU

2.1 Processor model type: 'v850' variant 'V850ES' definition

Imperas OVP processor models support multiple variants and details of the variants implemented in this model can be found in:
- the Imperas installation located at ImperasLib/source/renesas.ovpworld.org/processor/v850/1.0/doc
- the OVP website: OVP_Model_Specific_Information_v850_V850ES.pdf

2.1.1 Description

V850 Family Processor Model.

2.1.2 Licensing

Open Source Apache 2.0

2.1.3 Limitations

The following Debug Registers are non-functional DIR, DBPC, DBPSW

2.1.4 Verification

Models have been extensively tested by Imperas, In addition Verification suites have been supplied by Renesas for Feature Set validation

2.1.5 Features

All v850es Instructions are supported.

2.2 Instance Parameters

Several parameters can be specified when a processor is instanced in a platform. For this processor instance 'CPU' it has been instanced with the following parameters:

Table 2. Processor Instance 'CPU' Parameters (Configurations)

Parameter	Value	Description
mips	128	The nominal MIPS for the processor
variant	V850ES	The processor variant

2.3 Memory Map for processor 'CPU' bus: 'vfb'

Processor instance 'CPU' is connected to bus 'vfb' using master port 'INSTRUCTION'.
Processor instance 'CPU' is connected to bus 'vfb' using master port 'DATA'.

Table 3. Memory Map ('CPU' / 'vfb' [width: 28])

Lo Address	Hi Address	Instance	Component
0x0	0xF7FFF	CodeFlash	ram
0x3E00000	0x3E07FFF	DataFlash	ram
0x3FF0000	0x3FFEFFF	iRam	ram
0x8400000	0x84000FF	CAN0	can
0x8400600	0x84006FF	CAN1	can
0xFE00000	0xFE0007F	CRC	crc
0xFFF0000	0xFFFEFFF	bridge_vfb_0x03FF0000_0x0FFF0000	bridge
0xFFFF060	0xFFFF06F	BCU	bcu
0xFFFF100	0xFFFF1FB	INTC	intc
0xFFFF1FC	0xFFFF1FC	LOGIC	UPD70F3441Logic
0xFFFF200	0xFFFF22F	ADC0	adc
0xFFFF240	0xFFFF26F	ADC1	adc
0xFFFF270	0xFFFF270	ADC0	adc
0xFFFF272	0xFFFF272	ADC1	adc
0xFFFF300	0xFFFF3FF	DMA	dma
0xFFFF400	0xFFFF475	LOGIC	UPD70F3441Logic
0xFFFF480	0xFFFF48F	MEMC	memc
0xFFFF580	0xFFFF5A9	TMS0	tms
0xFFFF5C0	0xFFFF5E9	TMS1	tms
0xFFFF600	0xFFFF60F	TAA0	taa
0xFFFF610	0xFFFF61F	TAA1	taa
0xFFFF620	0xFFFF62F	TAA2	taa
0xFFFF630	0xFFFF63F	TAA3	taa
0xFFFF640	0xFFFF64F	TAA4	taa
0xFFFF650	0xFFFF65F	TAA5	taa
0xFFFF660	0xFFFF66F	TAA6	taa
0xFFFF670	0xFFFF67F	TAA7	taa
0xFFFF680	0xFFFF68F	TAA8	taa
0xFFFF690	0xFFFF69F	TMT0	tmt
0xFFFF6A0	0xFFFF6AF	TMT1	tmt
0xFFFF6B0	0xFFFF6BF	TAA9	taa
0xFFFF6D0	0xFFFF6D3	LOGIC	UPD70F3441Logic
0xFFFF700	0xFFFF701	RNG0	rng
0xFFFF860	0xFFFF860	CLKGEN	clkgen
0xFFFF888	0xFFFF893	LOGIC	UPD70F3441Logic
0xFFFF990	0xFFFF991	TMT0	tmt
0xFFFF9A0	0xFFFF9A1	TMT1	tmt
0xFFFFA00	0xFFFFA0F	UARTC0	uartc
0xFFFFA20	0xFFFFA2F	UARTC1	uartc
0xFFFFA40	0xFFFFA4F	UARTC2	uartc
0xFFFFB48	0xFFFFB51	bridge_vfb_0x0FFFF58A_0x0FFFFB48	bridge
0xFFFFB56	0xFFFFB5D	bridge_vfb_0x0FFFF598_0x0FFFFB56	bridge
0xFFFFBC8	0xFFFFBD1	bridge_vfb_0x0FFFF5CA_0x0FFFFBC8	bridge
0xFFFFBD6	0xFFFFBDD	bridge_vfb_0x0FFFF5D8_0x0FFFFBD6	bridge
0xFFFFCA0	0xFFFFCA0	CLKGEN	clkgen

0xFFFFD00	0xFFFFD07	CSIB0	csib
0xFFFFD20	0xFFFFD27	CSIB1	csib
0xFFFFD40	0xFFFFD5F	CSIE0	csie
0xFFFFD80	0xFFFFD9F	CSIE1	csie
0xFFFFDC0	0xFFFFDC1	BRG0	brg
0xFFFFDD0	0xFFFFDD1	BRG1	brg
0xFFFFDE0	0xFFFFDE1	BRG2	brg
0xFFFFE00	0xFFFFE0F	DMA	dma

Table 4. Bridged Memory Map ('CPU' / 'bridge_vfb_0x03FF0000_0x0FFF0000' / 'vfb' [width: 28])

Lo Address	Hi Address	Instance	Component
0x3FF0000	0x3FFEFFF	iRam	ram

Table 5. Bridged Memory Map ('CPU' / 'bridge_vfb_0x0FFFF58A_0x0FFFFB48' / 'vfb' [width: 28])

Lo Address	Hi Address	Instance	Component
0xFFFF580	0xFFFF5A9	TMS0	tms

Table 6. Bridged Memory Map ('CPU' / 'bridge_vfb_0x0FFFF598_0x0FFFFB56' / 'vfb' [width: 28])

Lo Address	Hi Address	Instance	Component
0xFFFF580	0xFFFF5A9	TMS0	tms

Table 7. Bridged Memory Map ('CPU' / 'bridge_vfb_0x0FFFF5CA_0x0FFFFBC8' / 'vfb' [width: 28])

Lo Address	Hi Address	Instance	Component
0xFFFF5C0	0xFFFF5E9	TMS1	tms

Table 8. Bridged Memory Map ('CPU' / 'bridge_vfb_0x0FFFF5D8_0x0FFFFBD6' / 'vfb' [width: 28])

Lo Address	Hi Address	Instance	Component
0xFFFF5C0	0xFFFF5E9	TMS1	tms

2.4 Net Connections to processor: 'CPU'

Table 9. Processor Net Connections ('CPU')

Net Port	Net	Instance	Component
reset	INTRESET	INTC	intc
nmi0	INTNMI	INTC	intc
intp	INTINTP	INTC	intc
mireti	INTMIRETI	INTC	intc
intack	INTINTACK	INTC	intc

3.0 Peripheral Instances

3.1 Peripheral [renesas.ovpworld.org/peripheral/UPD70F3441Logic/1.0] instance: LOGIC

3.1.1 Licensing
Open Source Apache 2.0

3.1.2 Description
Renesas V850PHO3 / UPD70F3441 Glue Logic

3.1.3 Limitations
No known limitations

3.1.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

There are no configuration options set for this peripheral instance.

3.2 Peripheral [renesas.ovpworld.org/peripheral/intc/1.0] instance: INTC

3.2.1 Licensing
Open Source Apache 2.0

3.2.2 Description
Renesas INTC Interrupt Controller

3.2.3 Limitations
Register View Model Only

3.2.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

There are no configuration options set for this peripheral instance.

3.3 Peripheral [renesas.ovpworld.org/peripheral/crc/1.0] instance: CRC

3.3.1 Licensing
Open Source Apache 2.0

3.3.2 Description
Renesas Cyclic Redundancy Generator

3.3.3 Limitations
Register View Model Only

3.3.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

There are no configuration options set for this peripheral instance.

3.4 Peripheral [renesas.ovpworld.org/peripheral/clkgen/1.0] instance: CLKGEN

3.4.1 Licensing
Open Source Apache 2.0

3.4.2 Description
Renesas Clock Generator

3.4.3 Limitations
Register View Model Only

3.4.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

There are no configuration options set for this peripheral instance.

3.5 Peripheral [renesas.ovpworld.org/peripheral/bcu/1.0] instance: BCU

3.5.1 Licensing
Open Source Apache 2.0

3.5.2 Description
Renesas BCU Bus Control Unit

3.5.3 Limitations
Register View Model Only

3.5.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

There are no configuration options set for this peripheral instance.

3.6 Peripheral [renesas.ovpworld.org/peripheral/memc/1.0] instance: MEMC

3.6.1 Licensing
Open Source Apache 2.0

3.6.2 Description

Renesas MEMC Bus Control Unit

3.6.3 Limitations
Register View Model Only

3.6.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

There are no configuration options set for this peripheral instance.

3.7 Peripheral [renesas.ovpworld.org/peripheral/dma/1.0] instance: DMA

3.7.1 Licensing
Open Source Apache 2.0

3.7.2 Description
Renesas DMA Controller

3.7.3 Limitations
Initial implementation to support CAN DMA message transfer only

3.7.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

There are no configuration options set for this peripheral instance.

3.8 Peripheral [renesas.ovpworld.org/peripheral/uartc/1.0] instance: UARTC0

3.8.1 Licensing
Open Source Apache 2.0

3.8.2 Description
Renesas UARTC Asynchronous Serial Interface

3.8.3 Limitations
No Support for pin level transitions

3.8.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 10. Configuration options (attributes) set for instance 'UARTC0'

Attribute	Value	Type	Expression

PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	
console	1	bool	
finishOnDisconnect	1	bool	

3.9 Peripheral [renesas.ovpworld.org/peripheral/uartc/1.0] instance: UARTC1

3.9.1 Licensing
Open Source Apache 2.0

3.9.2 Description
Renesas UARTC Asynchronous Serial Interface

3.9.3 Limitations
No Support for pin level transitions

3.9.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 11. Configuration options (attributes) set for instance 'UARTC1'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	
console	1	bool	
finishOnDisconnect	1	bool	

3.10 Peripheral [renesas.ovpworld.org/peripheral/uartc/1.0] instance: UARTC2

3.10.1 Licensing
Open Source Apache 2.0

3.10.2 Description
Renesas UARTC Asynchronous Serial Interface

3.10.3 Limitations

No Support for pin level transitions

3.10.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 12. Configuration options (attributes) set for instance 'UARTC2'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	
console	1	bool	
finishOnDisconnect	1	bool	

3.11 Peripheral [renesas.ovpworld.org/peripheral/csib/1.0] instance: CSIB0

3.11.1 Licensing

Open Source Apache 2.0

3.11.2 Description

Renesas CSIB Clocked Serial Interface

3.11.3 Limitations

No Support for pin level transitions Clock selection for BRG0, BRG1 or SCKB defaults to PCLK6

3.11.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 13. Configuration options (attributes) set for instance 'CSIB0'

Attribute	Value	Type	Expression
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK6	524288	uns32	

3.12 Peripheral [renesas.ovpworld.org/peripheral/csib/1.0] instance: CSIB1

3.12.1 Licensing
Open Source Apache 2.0

3.12.2 Description
Renesas CSIB Clocked Serial Interface

3.12.3 Limitations
No Support for pin level transitions Clock selection for BRG0, BRG1 or SCKB defaults to PCLK6

3.12.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 14. Configuration options (attributes) set for instance 'CSIB1'

Attribute	Value	Type	Expression
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK6	524288	uns32	

3.13 Peripheral [renesas.ovpworld.org/peripheral/csie/1.0] instance: CSIE0

3.13.1 Licensing
Open Source Apache 2.0

3.13.2 Description
Renesas CSIE Enhanced Queued Clocked Serial Interface

3.13.3 Limitations
Register View Model Only

3.13.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 15. Configuration options (attributes) set for instance 'CSIE0'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	

3.14 Peripheral [renesas.ovpworld.org/peripheral/csie/1.0] instance: CSIE1

3.14.1 Licensing
Open Source Apache 2.0

3.14.2 Description
Renesas CSIE Enhanced Queued Clocked Serial Interface

3.14.3 Limitations
Register View Model Only

3.14.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 16. Configuration options (attributes) set for instance 'CSIE1'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	

3.15 Peripheral [renesas.ovpworld.org/peripheral/can/1.0] instance: CAN0

3.15.1 Description
Renesas CAN interface. This is an interface between the CAN controller register interface and a PacketNet can interface.

3.15.2 Licensing
Open Source Apache 2.0

3.15.3 Limitations
No CRC generation or checking.

3.15.4 Reference
V850E/PHO3 uPD70F3441, uPD70F3483: R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

There are no configuration options set for this peripheral instance.

3.16 Peripheral [renesas.ovpworld.org/peripheral/can/1.0] instance: CAN1

3.16.1 Description
Renesas CAN interface. This is an interface between the CAN controller register interface and a PacketNet can interface.

3.16.2 Licensing
Open Source Apache 2.0

3.16.3 Limitations
No CRC generation or checking.

3.16.4 Reference

V850E/PHO3 uPD70F3441, uPD70F3483: R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

There are no configuration options set for this peripheral instance.

3.17 Peripheral [renesas.ovpworld.org/peripheral/adc/1.0] instance: ADC0

3.17.1 Licensing
Open Source Apache 2.0

3.17.2 Description
Renesas ADC A/D Converter

3.17.3 Limitations
Model supports Modes Select, Scan, 1xBuffer, 4xBuffer - no support for external trigger

3.17.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 17. Configuration options (attributes) set for instance 'ADC0'

Attribute	Value	Type	Expression
PCLK1	16777216	uns32	
sample	100	double	

3.18 Peripheral [renesas.ovpworld.org/peripheral/adc/1.0] instance: ADC1

3.18.1 Licensing
Open Source Apache 2.0

3.18.2 Description
Renesas ADC A/D Converter

3.18.3 Limitations
Model supports Modes Select, Scan, 1xBuffer, 4xBuffer - no support for external trigger

3.18.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 18. Configuration options (attributes) set for instance 'ADC1'

Attribute	Value	Type	Expression
PCLK1	16777216	uns32	
sample	100	double	

3.19 Peripheral [renesas.ovpworld.org/peripheral/taa/1.0] instance: TAA0

3.19.1 Licensing
Open Source Apache 2.0

3.19.2 Description
Renesas TAA Timer/Event Counter AA

3.19.3 Limitations
Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported

3.19.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 19. Configuration options (attributes) set for instance 'TAA0'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.20 Peripheral [renesas.ovpworld.org/peripheral/taa/1.0] instance: TAA1

3.20.1 Licensing
Open Source Apache 2.0

3.20.2 Description
Renesas TAA Timer/Event Counter AA

3.20.3 Limitations
Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported

3.20.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 20. Configuration options (attributes) set for instance 'TAA1'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.21 Peripheral [renesas.ovpworld.org/peripheral/taa/1.0] instance: TAA2

3.21.1 Licensing

Open Source Apache 2.0

3.21.2 Description

Renesas TAA Timer/Event Counter AA

3.21.3 Limitations

Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported

3.21.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 21. Configuration options (attributes) set for instance 'TAA2'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.22 Peripheral [renesas.ovpworld.org/peripheral/taa/1.0] instance: TAA3

3.22.1 Licensing

Open Source Apache 2.0

3.22.2 Description

Renesas TAA Timer/Event Counter AA

3.22.3 Limitations

Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported

3.22.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 22. Configuration options (attributes) set for instance 'TAA3'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.23 Peripheral [renesas.ovpworld.org/peripheral/taa/1.0] instance: TAA4

3.23.1 Licensing

Open Source Apache 2.0

3.23.2 Description

Renesas TAA Timer/Event Counter AA

3.23.3 Limitations

Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported

3.23.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 23. Configuration options (attributes) set for instance 'TAA4'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.24 Peripheral [renesas.ovpworld.org/peripheral/taa/1.0] instance: TAA5

3.24.1 Licensing
Open Source Apache 2.0

3.24.2 Description
Renesas TAA Timer/Event Counter AA

3.24.3 Limitations
Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported

3.24.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 24. Configuration options (attributes) set for instance 'TAA5'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.25 Peripheral [renesas.ovpworld.org/peripheral/taa/1.0] instance: TAA6

3.25.1 Licensing
Open Source Apache 2.0

3.25.2 Description
Renesas TAA Timer/Event Counter AA

3.25.3 Limitations

Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported

3.25.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 25. Configuration options (attributes) set for instance 'TAA6'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.26 Peripheral [renesas.ovpworld.org/peripheral/taa/1.0] instance: TAA7

3.26.1 Licensing

Open Source Apache 2.0

3.26.2 Description

Renesas TAA Timer/Event Counter AA

3.26.3 Limitations

Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported

3.26.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 26. Configuration options (attributes) set for instance 'TAA7'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	

PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.27 Peripheral [renesas.ovpworld.org/peripheral/taa/1.0] instance: TAA8

3.27.1 Licensing

Open Source Apache 2.0

3.27.2 Description

Renesas TAA Timer/Event Counter AA

3.27.3 Limitations

Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported

3.27.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 27. Configuration options (attributes) set for instance 'TAA8'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.28 Peripheral [renesas.ovpworld.org/peripheral/taa/1.0] instance: TAA9

3.28.1 Licensing

Open Source Apache 2.0

3.28.2 Description

Renesas TAA Timer/Event Counter AA

3.28.3 Limitations

Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode -

Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported

3.28.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 28. Configuration options (attributes) set for instance 'TAA9'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.29 Peripheral [renesas.ovpworld.org/peripheral/tms/1.0] instance: TMS0

3.29.1 Licensing

Open Source Apache 2.0

3.29.2 Description

Renesas TMS Timer/Event Counter S

3.29.3 Limitations

Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Untested - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Triangular-Wave PWM Mode - Unsupported - High Accuracy T-PWM Mode - Unsupported - PWM Mode with Dead Time - Unsupported - 120Deg Excitation Mode - Unsupported - Special 120Deg Excitation Mode - Unsupported - Special Pattern Output Mode - Unsupported

3.29.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 29. Configuration options (attributes) set for instance 'TMS0'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	

PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.30 Peripheral [renesas.ovpworld.org/peripheral/tms/1.0] instance: TMS1

3.30.1 Licensing
Open Source Apache 2.0

3.30.2 Description
Renesas TMS Timer/Event Counter S

3.30.3 Limitations
Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Untested - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Triangular-Wave PWM Mode - Unsupported - High Accuracy T-PWM Mode - Unsupported - PWM Mode with Dead Time - Unsupported - 120Deg Excitation Mode - Unsupported - Special 120Deg Excitation Mode - Unsupported - Special Pattern Output Mode - Unsupported

3.30.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 30. Configuration options (attributes) set for instance 'TMS1'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.31 Peripheral [renesas.ovpworld.org/peripheral/tmt/1.0] instance: TMT0

3.31.1 Licensing
Open Source Apache 2.0

3.31.2 Description
Renesas TMT Timer/Event Counter T

3.31.3 Limitations
Status of Modes - Interval Timer Mode - Supported - External Event Count Mode -

Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported - Triangular Wave PWM Mode - Unsupported - Encoder Compare Mode - Unsupported - Encoder Capture Mode - Unsupported - Encoder Capture Compare Mode - Unsupported - Offset Trigger Generation Mode - Unsupported

3.31.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 31. Configuration options (attributes) set for instance 'TMT0'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	
PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.32 Peripheral [renesas.ovpworld.org/peripheral/tmt/1.0] instance: TMT1

3.32.1 Licensing

Open Source Apache 2.0

3.32.2 Description

Renesas TMT Timer/Event Counter T

3.32.3 Limitations

Status of Modes - Interval Timer Mode - Supported - External Event Count Mode - Unsupported - External Trigger Pulse Output Mode - Unsupported - One-Shot Pulse Mode - Unsupported - PWM Mode - Unsupported - Free-Running Mode - Supported - Pulse Width Measurement Mode - Unsupported - Triangular Wave PWM Mode - Unsupported - Encoder Compare Mode - Unsupported - Encoder Capture Mode - Unsupported - Encoder Capture Compare Mode - Unsupported - Offset Trigger Generation Mode - Unsupported

3.32.4 Reference

R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 32. Configuration options (attributes) set for instance 'TMT1'

Attribute	Value	Type	Expression
PCLK0	33554432	uns32	

PCLK1	16777216	uns32	
PCLK2	8388608	uns32	
PCLK3	4194304	uns32	
PCLK4	2097152	uns32	
PCLK5	1048576	uns32	
PCLK7	262144	uns32	
PCLK9	65536	uns32	

3.33 Peripheral [renesas.ovpworld.org/peripheral/rng/1.0] instance: RNG0

3.33.1 Licensing
Open Source Apache 2.0

3.33.2 Description
Random Number Generator (RNG)

3.33.3 Limitations
Register View Model Only

3.33.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

There are no configuration options set for this peripheral instance.

3.34 Peripheral [renesas.ovpworld.org/peripheral/brg/1.0] instance: BRG0

3.34.1 Licensing
Open Source Apache 2.0

3.34.2 Description
Renesas BRG Baud Rate Generator

3.34.3 Limitations
Fully Supported

3.34.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 33. Configuration options (attributes) set for instance 'BRG0'

Attribute	Value	Type	Expression
PCLK	16777216	uns32	

3.35 Peripheral [renesas.ovpworld.org/peripheral/brg/1.0] instance: BRG1

3.35.1 Licensing
Open Source Apache 2.0

3.35.2 Description
Renesas BRG Baud Rate Generator

3.35.3 Limitations
Fully Supported

3.35.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 34. Configuration options (attributes) set for instance 'BRG1'

Attribute	Value	Type	Expression
PCLK	16777216	uns32	

3.36 Peripheral [renesas.ovpworld.org/peripheral/brg/1.0] instance: BRG2

3.36.1 Licensing
Open Source Apache 2.0

3.36.2 Description
Renesas BRG Baud Rate Generator

3.36.3 Limitations
Fully Supported

3.36.4 Reference
R01UH0128ED0700, Rev. 7.00, Oct 06, 2010

Table 35. Configuration options (attributes) set for instance 'BRG2'

Attribute	Value	Type	Expression
PCLK	33554432	uns32	

4.0 Overview of Imperas OVP Virtual Platforms

This document provides the details of the usage of an Imperas OVP Virtual Platform / Module. The first half of the document covers specifics of this particular virtual platform / module.

This second part of the document, includes information about Imperas OVP virtual platforms and modules, how they are built and used.

The Imperas virtual platforms are designed to provide a base for you to run high-speed software simulations of CPU-based SoCs and platforms on any suitable PC. They are typically based on the functionality of vendors fixed or evaluation platforms, enabling you to simulate software on these reference platforms. Typically virtual platforms are fixed and require the vendor to modify or extend them. Imperas virtual platforms are different in that they enable you to extend the functionality of the virtual platform, to closer reflect your own platform, by adding more component models, running different operating systems or adding additional applications.

Imperas virtual platforms are created using the Imperas iGen technology, allowing them to be used with Imperas OVP based simulators and also with Accellera/OSCI compliant SystemC simulators and commercial EDA System Design environments that use SystemC.

Virtual platforms include simulation models of the target devices, including the processor model(s) for the target device plus enough peripheral models to boot an operating system or run bare metal applications. The platform and the peripheral models used in most of the virtual platforms are open source, so that you can easily add new models to the platform as well as modify the existing models. Some models are only provided as binary, normally because the IP owner has restricted the release of the model source. In this case, please contact Imperas for more information.

There are typically several generic flavors of the virtual platforms for specific processor families, some targeting full operating systems, such as Linux, and some which focus on Real Time Operating Systems (RTOS) such as Mentor Nucleus or freeRTOS. OVP models of the processor cores are included in the virtual platforms, and for those processors which support mulitple cores SMP Linux is often supported for that virtual platform. For all of these virtual platforms, many of the peripheral components of the platform are modeled, often including the Ethernet and USB components. The semi-hosting capability of the Imperas virtual platform simulator products enables connection via the Ethernet and USB components from the virtual platform to the real world via the x86 host machine.

The Imperas OVP CPU models are written using the OVP Virtual Machine Interface (VMI) API that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. The processor models are Instruction Accurate and do not model the detailed cycle timing of the processor and they implement functionality at the level of a Programmers View of the processor and peripherals and the software running on them does not know it is not running on hardware. Many models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore

and modify the model. The models are run through an extensive QA and regression testing process and most processor model families are validated using technology provided by the processor IP owners. All the models in this platform are developed with the Open Virtual Platforms APIs and are implemented in C. A platform can be modeled as different levels of hierarchy using separately describable and compilable modules.

More information on modeling and APIs can be found on the www.OVPworld.org site.

5.0 Getting Started with Imperas OVP Virtual Platforms

Virtual platforms are downloadable from the OVPworld website OVPworld.org/downloads. You need to browse and look for '<platform processor name> Examples'. You do need to be registered and logged in on the OVP site to download. OVPworld currently provides 32 bit host versions of packages containing virtual platforms.

When downloading, choose, Linux or Windows host. 32 bit packages can be installed and executed on 32 bit or 64 bit hosts. If you require a 64 bit host version please contact Imperas.

For example, for the ARM Versatile Express platform booting Linux on Cortex-A15MP Single, Dual, and Quad core procesors, you would want the download package: 'OVPsim_demo_Linux_ArmVersatileExpress_arm_Cortex-A15MP'.

Most virtual platform packages contain the platform and all the processor and peripheral models needed. You will need to download a simulator to run the platform. You can use OVPsim, downloadable from OVPworld.org/downloads, or you can use one of the Imperas simulators (imperas.com/products) available commercially from Imperas.

6.0 Simulating Software

6.1 Getting a license key to run

After you have downloaded you will need a runtime license key before the simulators will run. For OVPsim please visit OVPworld.org/likey and provide the required information and an evaluation/demo license key will be automatically sent to you. If you are using Imperas, then please contact Imperas for a license key.

6.2 Normal runs

To run a platform, read the section below on command line control of the platform and the section on setting command line arguments.

6.3 Loading Software

For most virtual platforms the platform is already configured to run the default software application/program and there is normally a script to run that sets some arguments. You can then copy/edit this script to select your own applications etc.

The example application programs are typically .elf format files and are provided pre-compiled. There are normally makefiles and associated scripts to recompile the example applications.

To find more information about compiling and loading software, the following document should be looked at: Imperas_Installation_and_Getting_Started.pdf.

6.4 Semihosting

In a virtual platform, semihosting is not normally used as there is normally hardware that implements the appropriate functionality - for example I/O will be handled by UARTs etc.

6.5 Using a terminal (UART)

If the platform includes one or more UARTs you will need to connect a terminal program to it so that you can see output and type into the simulated program. Review the list of peripherals below and see what configuration options it has been set with. In most cases there is an option to set to instruct the simulator to 'pop up' a terminal window connected to the simulated UART.

6.6 Interacting with the simulation (keyboard and mouse)

If the platform has a simulated UART you can normally set a command to get the simulator to pop up a terminal window allowing you to see output from the simulated UART and also allowing you to type characters into the UART that can be processed by the simulated software.

If your simulated platform has an LCD device then you can often configure it to recognize mouse movements and mouse clicks - allowing full interaction.

To see these interactions in action, have a look at some of the available videos available at OVPworld.org/demosandvideos.

6.7 More Information (Documentation) on Simulation

To find more information about running simulations and more of the options the simulators provide, the following documents should be looked at:
Imperas_Installation_and_Getting_Started.pdf
Simulation_Control_of_Platforms_and_Modules_User_Guide.pdf
Advanced_Simulation_Control_of_Platforms_and_Modules_User_Guide.pdf
OVP_Control_File_User_Guide.pdf

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.

7.0 Debugging Software running on an Imperas OVP Virtual Platform

The Imperas and OVP simulators have several different interfaces to debuggers. These include several proprietary formats and also the standard GNU RSP format is supported allowing many compatible debuggers to be used. Below are some examples that Imperas directly support.

7.1 Debugging with GDB

A GNU debugger (GDB) can be connected to a processor in a platform using the RSP protocol. This allows the application program running on a processor to be debugged using a specific GDB for the processor selected. When using the Imperas Professional products many connections can be made allowing a GDB to be connected to all the processors in the platform.

The use of GDB is documented: OVPsim_Debugging_Applications_with_GDB_User_Guide.pdf.

*7.2 Debugging with Imperas M*DBG*

The Imperas multi-processor debugger can be connected to a platform and through this connection you can debug application programs running on all of the processors instanced within the platform. It is also capable, within this single unified environment, to debug peripheral model behavioral code in conjunction with the processor application programs.

For more information please see the Imperas M*DBG user guide.

The Imperas multi-processor debugger is also capable of controlling the Imperas Verification Analysis aand Profiling (VAP) tools in real time, making them invaluable to application program development, debugging and analysis.

For more information please see the Imperas VAP tools user guide.

7.3 Debugging with the Imperas eGui and GDB

Imperas eGui gives a GUI front end to the use of the GDB debugger. It allows use of all the features of GDB including source level application program debugging on processors.

*7.4 Debugging with the Imperas eGui and M*DBG*

Imperas eGui gives a GUI front end to the Imperas multi-processor debugger. It provides all the features of this debugger but does so with source level application program debugging on processors and source level debugging of the behavioral code on peripheral components in the platform. A context view shows all the processor and peripheral components within the platform and allows switching between them to examine the state of each at the event at which the simulation was stopped

Imperas eGui provides a menu from which the Imperas VAP tools can be controlled.

7.5 Debugging with Imperas eGui and Eclipse

Imperas provide a GUI based on Eclipse called eGui. This provides a GUI front end to use with a standard GDB or the Imperas MPD (Multi-Processor Debugger).

The use of eGui is documented: eGui_Eclipse_User_Guide.pdf.

A standard Eclipse CDT development environment can be connected to one or more processors in a

platform (multiple processors require an Imperas professional product). The simulation platform is started remotely or using the external tool feature in Eclipse, opens a debug port and awaits the connection with Eclipse. All features provided by the Eclipse CDT development environment are available to be used to debug software applications executing on the processors in the platform.

The use of Eclipse is documented: OVPsim_Debugging_Applications_with_Eclipse_User_Guide.pdf.

7.6 Debugging applications running under a simulated operating system

If the simulated platform is running an Operating System and the platform has a UART or Ethernet etc connection then it is often possible to connect an external debugger and debug the applications running under the simulated operating system.

An example would be a simulated platform running the Linux operating system, such as the MIPS Malta, or ARM Versatile Express. Within the simulated Linux you can start a gdbserver that connects from within the simulation through a UART out to the host PC via a port. Within the host PC you start a terminal program and connect to the port with a debugger such as GDB and can then debug the simulated user application.

8.0 Modifying the Platform / Module

8.1 Platforms / Modules use C/C++ and OVP APIs

The Imperas and OVP simulators execute a platform / module that is written in C/C++ and that makes function calls into the simulator's APIs. Thus the virtual platform / module is compiled from C/C++ into a binary shared object that the simulator loads and runs. OVP provides the definition and documentation that defines the C APIs for modeling the platforms, modules, the peripherals, and the processors. You can find more information about these APIs on the OVP website and in the OVP API documentation.

8.2 Platforms/Modules/Peripherals can be easily built with iGen from Imperas

Imperas provides a product 'iGen' that takes an input script file and creates the C/C++ files needed for platforms, modules, and peripherals - it creates the C/C++ file that is compiled into the platform, module or peripheral that is needed as an object file by the simulator. iGen creates the C/C++ files, you then need to add any necessary behaviors or further details etc. For platforms iGen creates either a C platform or a C++ SystemC TLM2 platform. For peripherals or modules iGen creates the C files and also provides a native C++ SystemC TLM2 interface to allow the peripheral/module to be instantiated in SystemC TLM2 platforms.

Information on iGen is available from: imperas.com/products.

8.3 Re-configuring the platform

There will nornmally be several configuration options that you can set when running the platform without the neeed to change any source. Refer to the section above on command line arguments. If these do not allow you to make the changes you need, then you may need to edit and recompile the source of the platform.

The source of the platform, modules, and the source of the peripherals will be installed as part of the packages you are using. The sources are located in the Imperas/OVP installation VLNV source tree. The VLNV term refers to: Vendor (eg arm.ovpworld.org), Library (eg platform), Name, (eg ArmVersatileExpress-CA15), and Version (eg 1.0). To modify the platform, locate the platform source files.

If you are an Imperas user and have access to iGen, we recommend you modify the source script files and regenerate and recompile the C that makes up the platform. Refer to the Imperas iGen model generator guide and the Imperas platform generator guide.

If you are using the C or SystemC TLM2 platforms with OVPsim, then you can edit the C/C++ files, recompile the source directly using the supplied makefiles, and the run the simulator directly with the resultant shared object.

8.4 Replacing peripherals components

If you need to replace peripherals, find the appropriate place in the source of the platform, make the change you need, and recompile etc. Look in the library for documentation on available peripherals and their configuration options.

8.5 Adding new peripherals components

If you need to add peripherals, find the appropriate place in the source, make the additions you need, and recompile etc. Look in the library for documentation on available peripherals and their configuration options.

If you need to create new peripheral components then use iGen to very quickly create the necessary C/C++ files that get you started. With iGen you can create peripherals with register/memory state in a few lines of iGen source. When adding behavior to the peripherals refer to the OVP API documentation.

9.0 Available Virtual Platforms

Table 36. Imperas / OVP Extendable Platform Kits (13 available)

Name	Vendor
AlteraCycloneIII_3c120	altera.ovpworld.org
AlteraCycloneV_HPS	altera.ovpworld.org
ArmIntegratorCP	arm.ovpworld.org
ArmVersatileExpress	arm.ovpworld.org
ArmVersatileExpress-CA15	arm.ovpworld.org
ArmVersatileExpress-CA9	arm.ovpworld.org
AtmelAT91SAM7	atmel.ovpworld.org
FreescaleKinetis60	freescale.ovpworld.org
FreescaleKinetis64	freescale.ovpworld.org
FreescaleVybridVFxx	freescale.ovpworld.org
MipsMalta	mips.ovpworld.org
RenesasUPD70F3441	renesas.ovpworld.org
XilinxML505	xilinx.ovpworld.org

Table 37. Imperas General Virtual Platforms (6 available)

Name	Vendor
arm-ti-eabi	arm.imperas.com
armm-ti-coff	arm.imperas.com
armm-ti-eabi	arm.imperas.com
HeteroAlteraCycloneV_HPS_CycloneIII_3c120	imperas.ovpworld.org
HeteroArmNucleusMIPSLinux	imperas.ovpworld.org
SiFiveFU540	imperas.ovpworld.org

Table 38. Imperas Modules (component of other platforms) (55 available)

Name	Vendor
AlteraCycloneIII_3c120	altera.ovpworld.org
AlteraCycloneV_HPS	altera.ovpworld.org
AE350	andes.ovpworld.org
ARMv8-A-FMv1	arm.ovpworld.org
ArmIntegratorCP	arm.ovpworld.org
ArmVersatileExpress	arm.ovpworld.org
ArmVersatileExpress-CA15	arm.ovpworld.org
ArmVersatileExpress-CA9	arm.ovpworld.org
AtmelAT91SAM7	atmel.ovpworld.org
ArmCortexMFreeRTOS	imperas.ovpworld.org
ArmCortexMuCOS-II	imperas.ovpworld.org
ArmuKernel	imperas.ovpworld.org
ArmuKernelDual	imperas.ovpworld.org
BareMetalMIPS	imperas.ovpworld.org
Dual_ARMv8-A-FMv1_VLAN	imperas.ovpworld.org
Hetero_1xArm_3xMips32	imperas.ovpworld.org
Hetero_ARM_RISCV_NeuralNetwork	imperas.ovpworld.org

Hetero_ARMv8-A-FMv1_Cortex-M3	imperas.ovpworld.org
Hetero_ARMv8-A-FMv1_MIPS_microAptiv	imperas.ovpworld.org
Hetero_AlteraCycloneV_HPS_AlteraCycloneIII_3c120	imperas.ovpworld.org
Hetero_ArmIntegratorCP_XilinxMicroBlaze	imperas.ovpworld.org
Hetero_ArmVersatileExpress_MipsMalta	imperas.ovpworld.org
Hetero_ArmVersatileExpress_XilinxMicroBlaze	imperas.ovpworld.org
Quad_ArmVersatileExpress-CA15	imperas.ovpworld.org
RiscvRV32FreeRTOS	imperas.ovpworld.org
MipsMalta	mips.ovpworld.org
iMX6S	nxp.ovpworld.org
RenesasUPD70F3441	renesas.ovpworld.org
ghs-multi	renesas.ovpworld.org
virtio	riscv.ovpworld.org
FaultInjection	safepower.ovpworld.org
PublicDemonstrator	safepower.ovpworld.org
Zynq_PL_DualMicroblaze	safepower.ovpworld.org
Zynq_PL_NoC	safepower.ovpworld.org
Zynq_PL_NoC_node	safepower.ovpworld.org
Zynq_PL_NostrumNoC	safepower.ovpworld.org
Zynq_PL_NostrumNoC_node	safepower.ovpworld.org
Zynq_PL_RO	safepower.ovpworld.org
Zynq_PL_SingleMicroblaze	safepower.ovpworld.org
Zynq_PL_TTELNoC	safepower.ovpworld.org
Zynq_PL_TTELNoC_node	safepower.ovpworld.org
Zynq_PL_TTELNoC_processing_node_public_demonstrator	safepower.ovpworld.org
Zynq_PL_TTELNoC_public_demonstrator	safepower.ovpworld.org
Zynq_PL_TTELNoC_sensor_actor_node_public_demonstrator	safepower.ovpworld.org
FU540	sifive.ovpworld.org
S51CC	sifive.ovpworld.org
coreip-s51-arty	sifive.ovpworld.org
coreip-s51-rtl	sifive.ovpworld.org
dualFifo	vendor.com
XilinxML505	xilinx.ovpworld.org
Zynq	xilinx.ovpworld.org
Zynq_PL_Default	xilinx.ovpworld.org
Zynq_PS	xilinx.ovpworld.org
zc702	xilinx.ovpworld.org
zc706	xilinx.ovpworld.org

Table 39. Imperas / OVP Bare Metal Virtual Platforms (22 available)

Name	Vendor
BareMetalNios_IISingle	altera.ovpworld.org
BareMetalArcSingle	arc.ovpworld.org
BareMetalArm7Single	arm.ovpworld.org
BareMetalArmCortexADual	arm.ovpworld.org
BareMetalArmCortexASingle	arm.ovpworld.org
BareMetalArmCortexASingleAngelTrap	arm.ovpworld.org
BareMetalArmCortexMSingle	arm.ovpworld.org

ArmCortexMFreeRTOS	imperas.ovpworld.org
ArmCortexMuCOS-II	imperas.ovpworld.org
BareMetalArmx1Mips32x3	imperas.ovpworld.org
Or1kUclinux	imperas.ovpworld.org
BareMetalM14KSingle	mips.ovpworld.org
BareMetalMips32Dual	mips.ovpworld.org
BareMetalMips32Single	mips.ovpworld.org
BareMetalMips64Single	mips.ovpworld.org
BareMetalMipsDual	mips.ovpworld.org
BareMetalMipsSingle	mips.ovpworld.org
BareMetalOr1kSingle	ovpworld.org
BareMetalM16cSingle	posedgesoft.ovpworld.org
BareMetalPowerPc32Single	power.ovpworld.org
BareMetalV850Single	renesas.ovpworld.org
ghs-multi	renesas.ovpworld.org

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