



## Imperas Peripheral Model Guide

### Model Specific Information for philips.ovpworld.org / ISP1761

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## Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit [OVPworld.org](http://OVPworld.org).

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## 1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

### 1.1 Description

Functional Model of USB Philips ISP1761 for Arm Versatile Express platforms. For full details please consult README-OTG.txt

### 1.2 Licensing

Open Source Apache 2.0

### 1.3 Limitations

- Only host mode is supported. - DMA modes are not supported for the moment, only the mandatory slave mode is implemented. - Control and bulk transfer types are currently implemented. No interrupt and isochronous transfers yet. - Tested only the attachment of a single host device. The HSOTG controller's root hub has a single port, so only one device can be attached to it. This device could be a hub, though. Currently we support only one non-hub device. - Hot plug events are currently unsupported.

### 1.4 Reference

Philips/NXP

### 1.5 Location

The ISP1761 peripheral model is located in an Imperas/OVP installation at the VLNV: philips.ovpworld.org / peripheral / ISP1761 / 1.0.

## 2.0 Peripheral Instance Parameters

This model accepts the following parameters:

Table 1. Peripheral Parameters

Name	Type	Description
usbDevice	string	USB Device to connect to in host mode. Currently supports 'host:VID:PID' or 'host:BUS-PORT'
usbHost	string	USB Host to connect to in device mode. Currently supports 'usbip:PORT'
logfile	string	If set, output packets to logfile in libpcap format.

## 3.0 Net Ports

This model has the following net ports:

Table 2. Net Ports

Name	Type	Must Be Connected	Description
hc_irq	output	F (False)	

## 4.0 Bus Slave Ports

This model has the following bus slave ports:

### 4.1 Bus Slave Port: *bport1*

Table 3. Bus Slave Port: bport1

Name	Size (bytes)	Must Be Connected	Description
bport1	0x10000	F (False)	

Table 4. Bus Slave Port: bport1 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
ab_CAPLENGTH	0x0	32			
ab_HCSPARAMS	0x4	32			
ab_HCCPARAMS	0x8	32			
ab_USBCMD	0x20	32			
ab_USBSTS	0x24	32			
ab_USBINTR	0x28	32			
ab_FRINDEX	0x2c	32			
ab_CTRLDSSEGMENT	0x30	32			
ab_CONFIGFLAG	0x60	32			
ab_PORTSC1	0x64	32			
ab_ISO_PTD_DONE	0x130	32			
ab_ISO_PTD_SKIP	0x134	32			
ab_ISO_PTD_LAST	0x138	32			
ab_INT_PTD_DONE	0x140	32			
ab_INT_PTD_SKIP	0x144	32			
ab_INT_PTD_LAST	0x148	32			
ab_ATL_PTD_DONE	0x150	32			
ab_ATL_PTD_SKIP	0x154	32			
ab_ATL_PTD_LAST	0x158	32			
ab_HW_MODE_CTRL	0x300	32			
ab_HCCHIPID	0x304	32			
ab_HCSCRATCH	0x308	32			
ab_SW_RESET	0x30c	32			
ab_HCDMACONFIG	0x330	32			
ab_HCBUFFSTATUS	0x334	32			
ab_ATL_DONE_TO	0x338	32			
ab_MEMORY	0x33c	32			
ab_EDGE_INT_CNT	0x340	32			
ab_DMA_START	0x344	32			
ab_PWDN_CTRL	0x354	32			
ab_HC_INT	0x310	32			
ab_HC_INT_EN	0x314	32			

ab_ISOMASKOR	0x318	32			
ab_INTMASKOR	0x31c	32			
ab_ATLMASKOR	0x320	32			
ab_ISOMASKAND	0x324	32			
ab_INTMASKAND	0x328	32			
ab_ATLMASKAND	0x32c	32			

## 5.0 Platforms that use this peripheral component

Peripheral components can be used in many different platforms, including those developed by Imperas or by other users of OVP. You can use this peripheral in your own platforms.

Table 5. Publicly available platforms using peripheral 'ISP1761'

Platform Name	Vendor
ArmVersatileExpress	arm.ovpworld.org
ArmVersatileExpress-CA15	arm.ovpworld.org
ArmVersatileExpress-CA9	arm.ovpworld.org
ArmVersatileExpress	arm.ovpworld.org
ArmVersatileExpress-CA15	arm.ovpworld.org
ArmVersatileExpress-CA9	arm.ovpworld.org

## 6.0 Peripheral components in the library

Table 6. Publicly available Imperas/OVP peripheral models (227 models)

Peripheral	Peripheral	Peripheral
renesas.ovpworld.org/adc	renesas.ovpworld.org/bcu	renesas.ovpworld.org/brg
renesas.ovpworld.org/can	renesas.ovpworld.org/can	renesas.ovpworld.org/clkgen
renesas.ovpworld.org/crc	renesas.ovpworld.org/csib	renesas.ovpworld.org/csie
renesas.ovpworld.org/dma	renesas.ovpworld.org/intc	renesas.ovpworld.org/memc
renesas.ovpworld.org/rng	renesas.ovpworld.org/taa	renesas.ovpworld.org/tms
renesas.ovpworld.org/tmt	renesas.ovpworld.org/uartc	renesas.ovpworld.org/UPD70F3441Logic
riscv.ovpworld.org/CLINT	riscv.ovpworld.org/PLIC	riscv.ovpworld.org/SmartLoaderRV64Linux
safePower.ovpworld.org/node	safePower.ovpworld.org/NostrumNode	safePower.ovpworld.org/ring_oscillator
safePower.ovpworld.org/TTElNode	sifive.ovpworld.org/artyo	sifive.ovpworld.org/DDRCTL
sifive.ovpworld.org/gpio	sifive.ovpworld.org/MSEL	sifive.ovpworld.org/PLIC
sifive.ovpworld.org/PRCI	sifive.ovpworld.org/pwm	sifive.ovpworld.org/spi
sifive.ovpworld.org/teststatus	sifive.ovpworld.org/UART	smc.ovpworld.org/LAN9118
smc.ovpworld.org/LAN91C111	ti.ovpworld.org/tca6416a	ti.ovpworld.org/UartInterface
ti.ovpworld.org/ucd9012a	ti.ovpworld.org/ucd9248	vendor.com/fifo
xilinx.ovpworld.org/axi-gpio	xilinx.ovpworld.org/axi-intc	xilinx.ovpworld.org/axi-pcie
xilinx.ovpworld.org/axi-timer	xilinx.ovpworld.org/logicore-fit	xilinx.ovpworld.org/mdm
xilinx.ovpworld.org/mpmc	xilinx.ovpworld.org/xps-gpio	xilinx.ovpworld.org/xps-iic
xilinx.ovpworld.org/xps-intc	xilinx.ovpworld.org/xps-ll-temac	xilinx.ovpworld.org/xps-mch-emc
xilinx.ovpworld.org/xps-sysace	xilinx.ovpworld.org/xps-timer	xilinx.ovpworld.org/xps-uartlite
xilinx.ovpworld.org/zynq_7000-can	xilinx.ovpworld.org/zynq_7000-ddrc	xilinx.ovpworld.org/zynq_7000-devcfg
xilinx.ovpworld.org/zynq_7000-dmac	xilinx.ovpworld.org/zynq_7000-gpio	xilinx.ovpworld.org/zynq_7000-iic
xilinx.ovpworld.org/zynq_7000-ocm	xilinx.ovpworld.org/zynq_7000-qos301	xilinx.ovpworld.org/zynq_7000-qspi
xilinx.ovpworld.org/zynq_7000-sdio	xilinx.ovpworld.org/zynq_7000-slcr	xilinx.ovpworld.org/zynq_7000-spi
xilinx.ovpworld.org/zynq_7000-swdt	xilinx.ovpworld.org/zynq_7000-ttc	xilinx.ovpworld.org/zynq_7000-tz_GPVsecurity
xilinx.ovpworld.org/zynq_7000-tz_security	xilinx.ovpworld.org/zynq_7000-usb	altera.ovpworld.org/dw-apb-timer
altera.ovpworld.org/dw-apb-uart	altera.ovpworld.org/IntervalTimer32Core	altera.ovpworld.org/IntervalTimer64Core
altera.ovpworld.org/JtagUart	altera.ovpworld.org/PerformanceCounterCore	altera.ovpworld.org/RSTMGR
altera.ovpworld.org/SystemIDCore	altera.ovpworld.org/Uart	amd.ovpworld.org/79C970
andes.ovpworld.org/ATCUART100	andes.ovpworld.org/NCEPLIC100	andes.ovpworld.org/NCEPLMT100
arm.ovpworld.org/AciPL041	arm.ovpworld.org/CompactFlashRegs	arm.ovpworld.org/CoreModule9x6
arm.ovpworld.org/DebugLedAndDipSwitch	arm.ovpworld.org/DMemCtrlPL341	arm.ovpworld.org/IcpControl
arm.ovpworld.org/IcpCounterTimer	arm.ovpworld.org/IntICP	arm.ovpworld.org/IntICP
arm.ovpworld.org/KbPL050	arm.ovpworld.org/L2CachePL310	arm.ovpworld.org/LcdPL110
arm.ovpworld.org/MmciPL181	arm.ovpworld.org/RtcPL031	arm.ovpworld.org/SerBusDviRegs
arm.ovpworld.org/SmartLoaderArm64Linux	arm.ovpworld.org/SmartLoaderArmLinux	arm.ovpworld.org/SMemCtrlPL354
arm.ovpworld.org/SysCtrlSP810	arm.ovpworld.org/TimerSP804	arm.ovpworld.org/TzpcBP147
arm.ovpworld.org/UartPL011	arm.ovpworld.org/VexpressSysRegs	arm.ovpworld.org/WdtSP805
atmel.ovpworld.org/AdvancedInterruptController	atmel.ovpworld.org/ParallelIOController	atmel.ovpworld.org/PowerSaving
atmel.ovpworld.org/SpecialFunction	atmel.ovpworld.org/TimerCounter	atmel.ovpworld.org/UsartInterface
atmel.ovpworld.org/WatchdogTimer	cadence.ovpworld.org/gem	cadence.ovpworld.org/uart
cirrus.ovpworld.org/GD5446	freescale.ovpworld.org/KinetisADC	freescale.ovpworld.org/KinetisAIPS
freescale.ovpworld.org/KinetisAXBS	freescale.ovpworld.org/KinetisCAN	freescale.ovpworld.org/KinetisCMP
freescale.ovpworld.org/KinetisCMT	freescale.ovpworld.org/KinetisCRC	freescale.ovpworld.org/KinetisDAC

<a href="https://freescale.ovpworld.org/KinetisDDR">freescale.ovpworld.org/KinetisDDR</a>	<a href="https://freescale.ovpworld.org/KinetisDMA">freescale.ovpworld.org/KinetisDMA</a>	<a href="https://freescale.ovpworld.org/KinetisDMAC">freescale.ovpworld.org/KinetisDMAC</a>
<a href="https://freescale.ovpworld.org/KinetisDMAMUX">freescale.ovpworld.org/KinetisDMAMUX</a>	<a href="https://freescale.ovpworld.org/KinetisENET">freescale.ovpworld.org/KinetisENET</a>	<a href="https://freescale.ovpworld.org/KinetisEWM">freescale.ovpworld.org/KinetisEWM</a>
<a href="https://freescale.ovpworld.org/KinetisFB">freescale.ovpworld.org/KinetisFB</a>	<a href="https://freescale.ovpworld.org/KinetisFMC">freescale.ovpworld.org/KinetisFMC</a>	<a href="https://freescale.ovpworld.org/KinetisFTFE">freescale.ovpworld.org/KinetisFTFE</a>
<a href="https://freescale.ovpworld.org/KinetisFTM">freescale.ovpworld.org/KinetisFTM</a>	<a href="https://freescale.ovpworld.org/KinetisGPIO">freescale.ovpworld.org/KinetisGPIO</a>	<a href="https://freescale.ovpworld.org/KinetisI2C">freescale.ovpworld.org/KinetisI2C</a>
<a href="https://freescale.ovpworld.org/KinetisI2S">freescale.ovpworld.org/KinetisI2S</a>	<a href="https://freescale.ovpworld.org/KinetisLLWU">freescale.ovpworld.org/KinetisLLWU</a>	<a href="https://freescale.ovpworld.org/KinetisLPTMR">freescale.ovpworld.org/KinetisLPTMR</a>
<a href="https://freescale.ovpworld.org/KinetisMCG">freescale.ovpworld.org/KinetisMCG</a>	<a href="https://freescale.ovpworld.org/KinetisMPU">freescale.ovpworld.org/KinetisMPU</a>	<a href="https://freescale.ovpworld.org/KinetisNFC">freescale.ovpworld.org/KinetisNFC</a>
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<a href="https://freescale.ovpworld.org/KinetisRTC">freescale.ovpworld.org/KinetisRTC</a>	<a href="https://freescale.ovpworld.org/KinetisSDHC">freescale.ovpworld.org/KinetisSDHC</a>	<a href="https://freescale.ovpworld.org/KinetisSIM">freescale.ovpworld.org/KinetisSIM</a>
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<a href="https://freescale.ovpworld.org/KinetisUART">freescale.ovpworld.org/KinetisUART</a>	<a href="https://freescale.ovpworld.org/KinetisUSB">freescale.ovpworld.org/KinetisUSB</a>	<a href="https://freescale.ovpworld.org/KinetisUSBDCD">freescale.ovpworld.org/KinetisUSBDCD</a>
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<a href="https://imperas.ovpworld.org/usecCounter">imperas.ovpworld.org/usecCounter</a>	<a href="https://intel.ovpworld.org/82077AA">intel.ovpworld.org/82077AA</a>	<a href="https://intel.ovpworld.org/82371EB">intel.ovpworld.org/82371EB</a>
<a href="https://intel.ovpworld.org/8253">intel.ovpworld.org/8253</a>	<a href="https://intel.ovpworld.org/8259A">intel.ovpworld.org/8259A</a>	<a href="https://intel.ovpworld.org/NorFlash48F4400">intel.ovpworld.org/NorFlash48F4400</a>
<a href="https://intel.ovpworld.org/PciIDE">intel.ovpworld.org/PciIDE</a>	<a href="https://intel.ovpworld.org/PciPM">intel.ovpworld.org/PciPM</a>	<a href="https://intel.ovpworld.org/PciUSB">intel.ovpworld.org/PciUSB</a>
<a href="https://intel.ovpworld.org/Ps2Control">intel.ovpworld.org/Ps2Control</a>	<a href="https://marvell.ovpworld.org/GT6412x">marvell.ovpworld.org/GT6412x</a>	<a href="https://maxim.ovpworld.org/max673x">maxim.ovpworld.org/max673x</a>
<a href="https://microsemi.ovpworld.org/CoreUARTapb">microsemi.ovpworld.org/CoreUARTapb</a>	<a href="https://mips.ovpworld.org/16450C">mips.ovpworld.org/16450C</a>	<a href="https://mips.ovpworld.org/MaltaFPGA">mips.ovpworld.org/MaltaFPGA</a>
<a href="https://mips.ovpworld.org/SmartLoaderLinux">mips.ovpworld.org/SmartLoaderLinux</a>	<a href="https://motorola.ovpworld.org/MC146818">motorola.ovpworld.org/MC146818</a>	<a href="https://national.ovpworld.org/16450">national.ovpworld.org/16450</a>
<a href="https://national.ovpworld.org/16550">national.ovpworld.org/16550</a>	<a href="https://national.ovpworld.org/16550_4bytes">national.ovpworld.org/16550_4bytes</a>	<a href="https://nxp.ovpworld.org/iMX6_Analog">nxp.ovpworld.org/iMX6_Analog</a>
<a href="https://nxp.ovpworld.org/iMX6_CCM">nxp.ovpworld.org/iMX6_CCM</a>	<a href="https://nxp.ovpworld.org/iMX6_GPC">nxp.ovpworld.org/iMX6_GPC</a>	<a href="https://nxp.ovpworld.org/iMX6_GPIO">nxp.ovpworld.org/iMX6_GPIO</a>
<a href="https://nxp.ovpworld.org/iMX6_GPT">nxp.ovpworld.org/iMX6_GPT</a>	<a href="https://nxp.ovpworld.org/iMX6_MMDC">nxp.ovpworld.org/iMX6_MMDC</a>	<a href="https://nxp.ovpworld.org/iMX6_SDHC">nxp.ovpworld.org/iMX6_SDHC</a>
<a href="https://nxp.ovpworld.org/iMX6_SRC">nxp.ovpworld.org/iMX6_SRC</a>	<a href="https://nxp.ovpworld.org/iMX6_UART">nxp.ovpworld.org/iMX6_UART</a>	<a href="https://nxp.ovpworld.org/iMX6_WDOG">nxp.ovpworld.org/iMX6_WDOG</a>
<a href="https://ovpworld.org/Alpha2x16Display">ovpworld.org/Alpha2x16Display</a>	<a href="https://ovpworld.org/DynamicBridge">ovpworld.org/DynamicBridge</a>	<a href="https://ovpworld.org/FlashDevice">ovpworld.org/FlashDevice</a>
<a href="https://ovpworld.org/ledRegister">ovpworld.org/ledRegister</a>	<a href="https://ovpworld.org/SerInt">ovpworld.org/SerInt</a>	<a href="https://ovpworld.org/SimpleDma">ovpworld.org/SimpleDma</a>
<a href="https://ovpworld.org/switchRegister">ovpworld.org/switchRegister</a>	<a href="https://ovpworld.org/temperatureSensor">ovpworld.org/temperatureSensor</a>	<a href="https://ovpworld.org/trap">ovpworld.org/trap</a>
<a href="https://ovpworld.org/trap4K">ovpworld.org/trap4K</a>	<a href="https://ovpworld.org/vEthernet_Bridge">ovpworld.org/vEthernet_Bridge</a>	<a href="https://ovpworld.org/VirtioBlkMMIO">ovpworld.org/VirtioBlkMMIO</a>
<a href="https://ovpworld.org/VirtioNetMMIO">ovpworld.org/VirtioNetMMIO</a>	<a href="https://philips.ovpworld.org/ISP1761">philips.ovpworld.org/ISP1761</a>	



## 7.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

### 7.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

## 8.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: [imperas.com/products](http://imperas.com/products).

## 9.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the

implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

## **10.0 Parts of peripheral models**

### ***10.1 Configuring the Peripheral Instance with Parameters***

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

### ***10.2 Net Ports***

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.

The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

### ***10.3 Bus master ports***

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

### ***10.4 Bus slave ports***

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

### ***10.5 Packetnets***

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: [OVP\\_Peripheral\\_Modeling\\_Guide.pdf](#), [OVPSim\\_and\\_CpuManager\\_User\\_Guide.pdf](#) and the example: [\\$IMPERAS\\_HOME/Examples/Models/Peripherals/packetnet](#).

## **11.0 More information (documentation) on peripheral models and modeling**

More information on modeling and APIs can be found at: [OVPworld.org/technology\\_apis](http://OVPworld.org/technology_apis).

Specifics on modeling peripherals can be found: [OVP\\_Peripheral\\_Modeling\\_Guide.pdf](#).

A full list of the currently available OVP documentation is available: [OVPworld.org/documentation](#).

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