Imperas Peripheral Model Guide

Model Specific Information for andes.ovpworld.org / NCEPLIC100

Imperas Software Limited

Imperas Buildings, North Weston
Thame, Oxfordshire, OX9 2HA, U.K.
docs@imperas.com.

Author	Imperas Software Limited
Version	20211118.0
Filename	OVP_Peripheral_Specific_Information_NCEPLIC100.pdf
Created	31 December 2021
Status	OVP Standard Release

Copyright Notice

Right to Copy Documentation

The license agreement with Imperas permits licensee to make copies of the documentation for its internal use only. Each copy shall include all copyrights, trademarks, service marks, and proprietary rights notices, if any.

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the readers responsibility to determine the applicable regulations and to comply with them.

Disclaimer

IMPERAS SOFTWARE LIMITED, AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

Table Of Contents

1.0 Model Specific Information

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers, other component parts, and configuration options and general information for peripheral modeling with Imperas OVP.

1.1 Licensing

Open Source Apache 2.0

1.2 Description

PLIC Interrupt Controller

Base riscv.ovpworld.org PLIC model plus these Andes extension features:

- Software-programmable interrupt generation (writable pending registers)

- Configurable interrupt trigger types

- Preemptive priority interrupts

- Vectored Interrupts

If vectored interrupts are to be used then additional connections between the plic and processor are required. For an interrupt target port t<x>_eip connected to one of the M/S/UExternalInterrupt ports of a processor, the corresponding ports must be connected as follows:

- The PLIC output port t<x>_eiid must be connected to the M/S/UExternalInterruptID processor port

- The PLIC output port t<x>_eiack must be connected to the M/S/UExternalInterruptACK processor port

1.3 Limitations

The ASYNC_INT configuration option is not configurable since the difference between asynch/synch behavior is not modeled by the simulator

1.4 Reference

Various AndesCore Processor Data Sheets, e.g. AndesCore AX45MP Data Sheet V1.1 (DS185-11)

AndeStar V5 Platform-Level Interrupt Controller Specification - UM166-13

1.5 Location

The NCEPLIC100 peripheral model is located in an Imperas/OVP installation at the VLNV: andes.ovpworld.org / peripheral / NCEPLIC100 / 1.0.

2.0 Peripheral Instance Parameters

This model accepts the following parameters:

Table 1. Peripheral Parameters

Name	Type	Description
num_sources	uns32	Number of Input Interrupt Sources
num_targets	uns32	Number of Output Interrupt Targets
num_priorities	uns32	Number of Priority levels
priority_base	uns32	Base Address offset for Priority Registers
pending_base	uns32	Base Address offset for Pending Registers
enable_base	uns32	Base Address offset for Enable Registers
enable_stride	uns32	Stride size for Enable Register Block
context_base	uns32	Base Address offset for Context Registers, Threshold and Claim/Complete
context_stride	uns32	Stride size for Context Register Block
andes_version	uns32	Andes PLIC design version (value for VersionMaxPriority.VERSION field)
vector_plic_support	bool	Andes Vectored PLIC support - adds t<x>_eiid and t<x>_eack ports when enabled
trigger_type0	uns32	Trigger type register 0 value
trigger_type1	uns32	Trigger type register 1 value
trigger_type2	uns32	Trigger type register 2 value
trigger_type3	uns32	Trigger type register 3 value
trigger_type4	uns32	Trigger type register 4 value
trigger_type5	uns32	Trigger type register 5 value
trigger_type6	uns32	Trigger type register 6 value
trigger_type7	uns32	Trigger type register 7 value
trigger_type8	uns32	Trigger type register 8 value
trigger_type9	uns32	Trigger type register 9 value
trigger_type10	uns32	Trigger type register 10 value
trigger_type11	uns32	Trigger type register 11 value
trigger_type12	uns32	Trigger type register 12 value
trigger_type13	uns32	Trigger type register 13 value
trigger_type14	uns32	Trigger type register 14 value
trigger_type15	uns32	Trigger type register 15 value
trigger_type16	uns32	Trigger type register 16 value
trigger_type17	uns32	Trigger type register 17 value
trigger_type18	uns32	Trigger type register 18 value
trigger_type19	uns32	Trigger type register 19 value
trigger_type20	uns32	Trigger type register 20 value
trigger_type21	uns32	Trigger type register 21 value
trigger_type22	uns32	Trigger type register 22 value
trigger_type23	uns32	Trigger type register 23 value
trigger_type24	uns32	Trigger type register 24 value
trigger_type25	uns32	Trigger type register 25 value

trigger_type26	uns32	Trigger type register 26 value
trigger_type27	uns32	Trigger type register 27 value
trigger_type28	uns32	Trigger type register 28 value
trigger_type29	uns32	Trigger type register 29 value
trigger_type30	uns32	Trigger type register 30 value
trigger_type31	uns32	Trigger type register 31 value

3.0 Net Ports

This model has the following net ports:

Table 2. Net Ports

Name	Type	Must Be Connected	Description
reset	input	F (False)	Reset signal
irqS1	input	F (False)	
irqT0	output	F (False)	
irqS2	input	F (False)	Input Interrupt Port
irqS3	input	F (False)	Input Interrupt Port
irqS4	input	F (False)	Input Interrupt Port
irqS5	input	F (False)	Input Interrupt Port
irqS6	input	F (False)	Input Interrupt Port
irqS7	input	F (False)	Input Interrupt Port
irqS8	input	F (False)	Input Interrupt Port
irqS9	input	F (False)	Input Interrupt Port
irqS10	input	F (False)	Input Interrupt Port
irqS11	input	F (False)	Input Interrupt Port
irqS12	input	F (False)	Input Interrupt Port
irqS13	input	F (False)	Input Interrupt Port
irqS14	input	F (False)	Input Interrupt Port
irqS15	input	F (False)	Input Interrupt Port
irqS16	input	F (False)	Input Interrupt Port
irqS17	input	F (False)	Input Interrupt Port
irqS18	input	F (False)	Input Interrupt Port
irqS19	input	F (False)	Input Interrupt Port
irqS20	input	F (False)	Input Interrupt Port
irqS21	input	F (False)	Input Interrupt Port
irqS22	input	F (False)	Input Interrupt Port
irqS23	input	F (False)	Input Interrupt Port
irqS24	input	F (False)	Input Interrupt Port
irqS25	input	F (False)	Input Interrupt Port
irqS26	input	F (False)	Input Interrupt Port
irqS27	input	F (False)	Input Interrupt Port
irqS28	input	F (False)	Input Interrupt Port
irqS29	input	F (False)	Input Interrupt Port
irqS30	input	F (False)	Input Interrupt Port
irqS31	input	F (False)	Input Interrupt Port
irqS32	input	F (False)	Input Interrupt Port
irqS33	input	F (False)	Input Interrupt Port
irqS34	input	F (False)	Input Interrupt Port

irqS35	input	F (False)	Input Interrupt Port
irqS36	input	F (False)	Input Interrupt Port
irqS37	input	F (False)	Input Interrupt Port
irqS38	input	F (False)	Input Interrupt Port
irqS39	input	F (False)	Input Interrupt Port
irqS40	input	F (False)	Input Interrupt Port
irqS41	input	F (False)	Input Interrupt Port
irqS42	input	F (False)	Input Interrupt Port
irqS43	input	F (False)	Input Interrupt Port
irqS44	input	F (False)	Input Interrupt Port
irqS45	input	F (False)	Input Interrupt Port
irqS46	input	F (False)	Input Interrupt Port
irqS47	input	F (False)	Input Interrupt Port
irqS48	input	F (False)	Input Interrupt Port
irqS49	input	F (False)	Input Interrupt Port
irqS50	input	F (False)	Input Interrupt Port
irqS51	input	F (False)	Input Interrupt Port
irqS52	input	F (False)	Input Interrupt Port
irqS53	input	F (False)	Input Interrupt Port
irqS54	input	F (False)	Input Interrupt Port
irqS55	input	F (False)	Input Interrupt Port
irqS56	input	F (False)	Input Interrupt Port
irqS57	input	F (False)	Input Interrupt Port
irqS58	input	F (False)	Input Interrupt Port
irqS59	input	F (False)	Input Interrupt Port
irqS60	input	F (False)	Input Interrupt Port
irqS61	input	F (False)	Input Interrupt Port
irqS62	input	F (False)	Input Interrupt Port
irqS63	input	F (False)	Input Interrupt Port
t0_eiid	output	F (False)	Vectored Interrupt ID port
t0_eiack	input	F (False)	Vectored Interrupt Acknowledge port

4.0 Bus Slave Ports

This model has the following bus slave ports:

4.1 Bus Slave Port: port0

Table 3. Bus Slave Port: port0

Name	Size (bytes)	Must Be Connected	Description
port0	0x400000	F (False)	

Table 4. Bus Slave Port: port0 Registers:

Name	Offset	Width (bits)	Description	R/W	is Volatile
FeatureEnable	0x0	32	AndesCore PLIC Feature Enable Register		
Priority1	0x4	32	Priority of Input Interrupt Source 1		
Priority2	0x8	32	Priority of Input Interrupt Source 2		

Priority3	0xc	32	Priority of Input Interrupt Source 3		
Priority4	0x10	32	Priority of Input Interrupt Source 4		
Priority5	0x14	32	Priority of Input Interrupt Source 5		
Priority6	0x18	32	Priority of Input Interrupt Source 6		
Priority7	0x1c	32	Priority of Input Interrupt Source 7		
Priority8	0x20	32	Priority of Input Interrupt Source 8		
Priority9	0x24	32	Priority of Input Interrupt Source 9		
Priority10	0x28	32	Priority of Input Interrupt Source 10		
Priority11	0x2c	32	Priority of Input Interrupt Source 11		
Priority12	0x30	32	Priority of Input Interrupt Source 12		
Priority13	0x34	32	Priority of Input Interrupt Source 13		
Priority14	0x38	32	Priority of Input Interrupt Source 14		
Priority15	0x3c	32	Priority of Input Interrupt Source 15		
Priority16	0x40	32	Priority of Input Interrupt Source 16		
Priority17	0x44	32	Priority of Input Interrupt Source 17		
Priority18	0x48	32	Priority of Input Interrupt Source 18		
Priority19	0x4c	32	Priority of Input Interrupt Source 19		
Priority20	0x50	32	Priority of Input Interrupt Source 20		
Priority21	0x54	32	Priority of Input Interrupt Source 21		
Priority22	0x58	32	Priority of Input Interrupt Source 22		
Priority23	0x5c	32	Priority of Input Interrupt Source 23		
Priority24	0x60	32	Priority of Input Interrupt Source 24		
Priority25	0x64	32	Priority of Input Interrupt Source 25		
Priority26	0x68	32	Priority of Input Interrupt Source 26		
Priority27	0x6c	32	Priority of Input Interrupt Source 27		
Priority28	0x70	32	Priority of Input Interrupt Source 28		
Priority29	0x74	32	Priority of Input Interrupt Source 29		
Priority30	0x78	32	Priority of Input Interrupt		

			Source 30		
Priority31	0x7c	32	Priority of Input Interrupt Source 31		
Priority32	0x80	32	Priority of Input Interrupt Source 32		
Priority33	0x84	32	Priority of Input Interrupt Source 33		
Priority34	0x88	32	Priority of Input Interrupt Source 34		
Priority35	0x8c	32	Priority of Input Interrupt Source 35		
Priority36	0x90	32	Priority of Input Interrupt Source 36		
Priority37	0x94	32	Priority of Input Interrupt Source 37		
Priority38	0x98	32	Priority of Input Interrupt Source 38		
Priority39	0x9c	32	Priority of Input Interrupt Source 39		
Priority40	0xa0	32	Priority of Input Interrupt Source 40		
Priority41	0xa4	32	Priority of Input Interrupt Source 41		
Priority42	0xa8	32	Priority of Input Interrupt Source 42		
Priority43	0xac	32	Priority of Input Interrupt Source 43		
Priority44	0xb0	32	Priority of Input Interrupt Source 44		
Priority45	0xb4	32	Priority of Input Interrupt Source 45		
Priority46	0xb8	32	Priority of Input Interrupt Source 46		
Priority47	0xbc	32	Priority of Input Interrupt Source 47		
Priority48	0xc0	32	Priority of Input Interrupt Source 48		
Priority49	0xc4	32	Priority of Input Interrupt Source 49		
Priority50	0xc8	32	Priority of Input Interrupt Source 50		
Priority51	0xcc	32	Priority of Input Interrupt Source 51		
Priority52	0xd0	32	Priority of Input Interrupt Source 52		
Priority53	0xd4	32	Priority of Input Interrupt Source 53		
Priority54	0xd8	32	Priority of Input Interrupt Source 54		
Priority55	0xdc	32	Priority of Input Interrupt Source 55		
Priority56	0xe0	32	Priority of Input Interrupt Source 56		
Priority57	0xe4	32	Priority of Input Interrupt Source 57		

Priority58	0xe8	32	Priority of Input Interrupt Source 58		
Priority59	0xec	32	Priority of Input Interrupt Source 59		
Priority60	0xf0	32	Priority of Input Interrupt Source 60		
Priority61	0xf4	32	Priority of Input Interrupt Source 61		
Priority62	0xf8	32	Priority of Input Interrupt Source 62		
Priority63	0xfc	32	Priority of Input Interrupt Source 63		
Pending0	0x1000	32	Pending Interrupt Register for Interrupts 31 downto 0		
Pending1	0x1004	32	Pending Interrupt Register for Interrupts 63 downto 32		
Target0_Enable0	0x2000	32	Target 0: Enable Register for Interrupts 31 downto 0		
Target0_Enable1	0x2004	32	Target 0: Enable Register for Interrupts 63 downto 32		
Target0_Threshold	0x200000	32	Target 0 Priority Threshold		
Target0_Claim	0x200004	32	Target 0 Claim for Source		
PreemptedPriorityStack0	0x200400	32	Andes preempted priority stack Register for priorities 31 downto 0		
PreemptedPriorityStack1	0x200404	32	Andes preempted priority stack Register for priorities 63 downto 32		
PreemptedPriorityStack2	0x200408	32	Andes preempted priority stack Register for priorities 95 downto 64		
PreemptedPriorityStack3	0x20040c	32	Andes preempted priority stack Register for priorities 127 downto 96		
PreemptedPriorityStack4	0x200410	32	Andes preempted priority stack Register for priorities 159 downto 128		
PreemptedPriorityStack5	0x200414	32	Andes preempted priority stack Register for priorities 191 downto 160		
PreemptedPriorityStack6	0x200418	32	Andes preempted priority stack Register for priorities 223 downto 192		
PreemptedPriorityStack7	0x20041c	32	Andes preempted priority stack Register for priorities 255 downto 224		
PreemptedPriorityStack8	0x200420	32	Andes preempted priority stack Register for priorities 287 downto 256		
TriggerType0	0x1080	32	Andes Trigger Type Register for Interrupts 31 downto 0		

TriggerType1	0x1084	32	Andes Trigger Type Register for Interrupts 63 downto 32		
NumIntsAndTgts	0x1100	32	Andes number of interrupts and targets register		
VersionMaxPriority	0x1104	32	Andes version and max priority register		

5.0 Platforms that use this peripheral component

Peripheral components can be used in many different platforms, including those developed by Imperas or by other users of OVP. You can use this peripheral in your own platforms.

Table 5. Publicly available platforms using peripheral 'NCEPLIC100'

Platform Name	Vendor
AE350	andes.ovpworld.org

6.0 Peripheral components in the library

Table 6. Publicly available Imperas/OVP peripheral models (227 models)

Peripheral	Peripheral	Peripheral
andes.ovpworld.org/NCEPLMT100	arm.ovpworld.org/AaciPL041	arm.ovpworld.org/CompactFlashRegs
arm.ovpworld.org/CoreModule9x6	arm.ovpworld.org/DebugLedAndDipSwitch	arm.ovpworld.org/DMemCtrlPL341
arm.ovpworld.org/IcpControl	arm.ovpworld.org/IcpCounterTimer	arm.ovpworld.org/IntICP
arm.ovpworld.org/IntICP	arm.ovpworld.org/KbPL050	arm.ovpworld.org/L2CachePL310
arm.ovpworld.org/LcdPL110	arm.ovpworld.org/MmciPL181	arm.ovpworld.org/RtcPL031
arm.ovpworld.org/SerBusDviRegs	arm.ovpworld.org/SmartLoaderArm64Linux	arm.ovpworld.org/SmartLoaderArmLinux
arm.ovpworld.org/SMemCtrlPL354	arm.ovpworld.org/SysCtrlSP810	arm.ovpworld.org/TimerSP804
arm.ovpworld.org/TzpcBP147	arm.ovpworld.org/UartPL011	arm.ovpworld.org/VexpressSysRegs
arm.ovpworld.org/WdtSP805	atmel.ovpworld.org/AdvancedInterruptController	atmel.ovpworld.org/ParallelIOController
atmel.ovpworld.org/PowerSaving	atmel.ovpworld.org/SpecialFunction	atmel.ovpworld.org/TimerCounter
atmel.ovpworld.org/UsartInterface	atmel.ovpworld.org/WatchdogTimer	cadence.ovpworld.org/gem
cadence.ovpworld.org/uart	cirrus.ovpworld.org/GD5446	freescale.ovpworld.org/KinetisADC
freescale.ovpworld.org/KinetisAIPS	freescale.ovpworld.org/KinetisAXBS	freescale.ovpworld.org/KinetisCAN
freescale.ovpworld.org/KinetisCMP	freescale.ovpworld.org/KinetisCMT	freescale.ovpworld.org/KinetisCRC
freescale.ovpworld.org/KinetisDAC	freescale.ovpworld.org/KinetisDDR	freescale.ovpworld.org/KinetisDMA
freescale.ovpworld.org/KinetisDMAC	freescale.ovpworld.org/KinetisDMAMUX	freescale.ovpworld.org/KinetisENET
freescale.ovpworld.org/KinetisEWM	freescale.ovpworld.org/KinetisFB	freescale.ovpworld.org/KinetisFMC
freescale.ovpworld.org/KinetisFTFE	freescale.ovpworld.org/KinetisFTM	freescale.ovpworld.org/KinetisGPIO
freescale.ovpworld.org/KinetisI2C	freescale.ovpworld.org/KinetisI2S	freescale.ovpworld.org/KinetisLLWU
freescale.ovpworld.org/KinetisLPTMR	freescale.ovpworld.org/KinetisMCG	freescale.ovpworld.org/KinetisMPU
freescale.ovpworld.org/KinetisNFC	freescale.ovpworld.org/KinetisOSC	freescale.ovpworld.org/KinetisPDB
freescale.ovpworld.org/KinetisPIT	freescale.ovpworld.org/KinetisPMC	freescale.ovpworld.org/KinetisPORT
freescale.ovpworld.org/KinetisRCM	freescale.ovpworld.org/KinetisRFSYS	freescale.ovpworld.org/KinetisRFVBAT
freescale.ovpworld.org/KinetisRNG	freescale.ovpworld.org/KinetisRTC	freescale.ovpworld.org/KinetisSDHC
freescale.ovpworld.org/KinetisSIM	freescale.ovpworld.org/KinetisSMC	freescale.ovpworld.org/KinetisSPI
freescale.ovpworld.org/KinetisTSI	freescale.ovpworld.org/KinetisUART	freescale.ovpworld.org/KinetisUSB
freescale.ovpworld.org/KinetisUSBDCD	freescale.ovpworld.org/KinetisUSBHS	freescale.ovpworld.org/KinetisVREF
freescale.ovpworld.org/KinetisWDOG	freescale.ovpworld.org/Uart	freescale.ovpworld.org/VybridADC
freescale.ovpworld.org/VybridANADIG	freescale.ovpworld.org/VybridCCM	freescale.ovpworld.org/VybridDMA
freescale.ovpworld.org/VybridGPIO	freescale.ovpworld.org/VybridI2C	freescale.ovpworld.org/VybridLCD
freescale.ovpworld.org/VybridQUADSPI	freescale.ovpworld.org/VybridSDHC	freescale.ovpworld.org/VybridSPI
freescale.ovpworld.org/VybridUART	freescale.ovpworld.org/VybridUSB	imperas.ovpworld.org/frameBuffer
imperas.ovpworld.org/uart	imperas.ovpworld.org/usecCounter	intel.ovpworld.org/82077AA
intel.ovpworld.org/82371EB	intel.ovpworld.org/8253	intel.ovpworld.org/8259A
intel.ovpworld.org/NorFlash48F4400	intel.ovpworld.org/PciIDE	intel.ovpworld.org/PciPM
intel.ovpworld.org/PciUSB	intel.ovpworld.org/Ps2Control	marvell.ovpworld.org/GT6412x
maxim.ovpworld.org/max673x	microsemi.ovpworld.org/CoreUARTapb	mips.ovpworld.org/16450C
mips.ovpworld.org/MaltaFPGA	mips.ovpworld.org/SmartLoaderLinux	motorola.ovpworld.org/MC146818
national.ovpworld.org/16450	national.ovpworld.org/16550	national.ovpworld.org/16550_4bytes
nxp.ovpworld.org/iMX6_Analog	nxp.ovpworld.org/iMX6_CCM	nxp.ovpworld.org/iMX6_GPC
nxp.ovpworld.org/iMX6_GPIO	nxp.ovpworld.org/iMX6_GPT	nxp.ovpworld.org/iMX6_MMDC
nxp.ovpworld.org/iMX6_SDHC	nxp.ovpworld.org/iMX6_SRC	nxp.ovpworld.org/iMX6_UART
nxp.ovpworld.org/iMX6_WDOG	ovpworld.org/Alpha2x16Display	ovpworld.org/DynamicBridge

ovpworld.org/FlashDevice	ovpworld.org/ledRegister	ovpworld.org/SerInt
ovpworld.org/SimpleDma	ovpworld.org/switchRegister	ovpworld.org/temperatureSensor
ovpworld.org/trap	ovpworld.org/trap4K	ovpworld.org/vEthernet_Bridge
ovpworld.org/VirtioBlkMMIO	ovpworld.org/VirtioNetMMIO	philips.ovpworld.org/ISP1761
renesas.ovpworld.org/adc	renesas.ovpworld.org/bcu	renesas.ovpworld.org/brg
renesas.ovpworld.org/can	renesas.ovpworld.org/can	renesas.ovpworld.org/clkgen
renesas.ovpworld.org/crc	renesas.ovpworld.org/csib	renesas.ovpworld.org/csie
renesas.ovpworld.org/dma	renesas.ovpworld.org/intc	renesas.ovpworld.org/memc
renesas.ovpworld.org/rng	renesas.ovpworld.org/taa	renesas.ovpworld.org/tms
renesas.ovpworld.org/tmt	renesas.ovpworld.org/uartc	renesas.ovpworld.org/UPD70F3441Logic
riscv.ovpworld.org/CLINT	riscv.ovpworld.org/PLIC	riscv.ovpworld.org/SmartLoaderRV64Linux
safepower.ovpworld.org/node	safepower.ovpworld.org/NostrumNode	safepower.ovpworld.org/ring_oscillator
safepower.ovpworld.org/TTELNode	sifive.ovpworld.org/artyIO	sifive.ovpworld.org/DDRCTL
sifive.ovpworld.org/gpio	sifive.ovpworld.org/MSEL	sifive.ovpworld.org/PLIC
sifive.ovpworld.org/PRCI	sifive.ovpworld.org/pwm	sifive.ovpworld.org/spi
sifive.ovpworld.org/teststatus	sifive.ovpworld.org/UART	smsc.ovpworld.org/LAN9118
smsc.ovpworld.org/LAN91C111	ti.ovpworld.org/tca6416a	ti.ovpworld.org/UartInterface
ti.ovpworld.org/ucd9012a	ti.ovpworld.org/ucd9248	vendor.com/fifo
xilinx.ovpworld.org/axi-gpio	xilinx.ovpworld.org/axi-intc	xilinx.ovpworld.org/axi-pcie
xilinx.ovpworld.org/axi-timer	xilinx.ovpworld.org/logicore-fit	xilinx.ovpworld.org/mdm
xilinx.ovpworld.org/mpmc	xilinx.ovpworld.org/xps-gpio	xilinx.ovpworld.org/xps-iic
xilinx.ovpworld.org/xps-intc	xilinx.ovpworld.org/xps-ll-temac	xilinx.ovpworld.org/xps-mch-emc
xilinx.ovpworld.org/xps-sysace	xilinx.ovpworld.org/xps-timer	xilinx.ovpworld.org/xps-uartlite
xilinx.ovpworld.org/zynq_7000-can	xilinx.ovpworld.org/zynq_7000-ddrc	xilinx.ovpworld.org/zynq_7000-devcfg
xilinx.ovpworld.org/zynq_7000-dmac	xilinx.ovpworld.org/zynq_7000-gpio	xilinx.ovpworld.org/zynq_7000-iic
xilinx.ovpworld.org/zynq_7000-ocm	xilinx.ovpworld.org/zynq_7000-qos301	xilinx.ovpworld.org/zynq_7000-qspi
xilinx.ovpworld.org/zynq_7000-sdio	xilinx.ovpworld.org/zynq_7000-slcr	xilinx.ovpworld.org/zynq_7000-spi
xilinx.ovpworld.org/zynq_7000-swdt	xilinx.ovpworld.org/zynq_7000-ttc	xilinx.ovpworld.org/zynq_7000-tz_GPVsecurity
xilinx.ovpworld.org/zynq_7000-tz_security	xilinx.ovpworld.org/zynq_7000-usb	altera.ovpworld.org/dw-apb-timer
altera.ovpworld.org/dw-apb-uart	altera.ovpworld.org/IntervalTimer32Core	altera.ovpworld.org/IntervalTimer64Core
altera.ovpworld.org/JtagUart	altera.ovpworld.org/PerformanceCounterCore	altera.ovpworld.org/RSTMGR
altera.ovpworld.org/SystemIDCore	altera.ovpworld.org/Uart	amd.ovpworld.org/79C970
andes.ovpworld.org/ATCUART100	andes.ovpworld.org/NCEPLIC100	

7.0 General Information on Peripheral Models

This document provides usage information for an Imperas OVP peripheral behavioral model.

The document is split into sections providing specific information for this peripheral, including any ports for connecting into a platform, registers etc. and configuration options and general information for peripheral modeling with Imperas OVP.

7.1 Background

Imperas OVP simulation technology enables very high performance simulation, debug and analysis of platforms containing multiple processors and peripheral models. The technology is designed to be extensible: you can create new models of processors, peripherals and other platform components using interfaces and libraries defined by OVP.

The peripheral models created using the OVP APIs run on the Peripheral Simulation Engine (PSE).

The model is typically written in C and compiled into an executable for the PSE processor architecture. The model is compiled for speed of execution and to protect IP. It is dynamically loaded by the simulator at run time.

8.0 Building peripherals easily with Imperas iGen

To aid with model creation, Imperas products include iGen, a model generation tool. iGen takes the laborious and error-prone task of constructing the various hardware model and software element files required for a typical model, and automates this process. iGen creates the needed C files. iGen also creates the C++ SystemC TLM2 interface files needed to run peripheral models in SystemC simulations.

iGen takes as input a simple script specification that includes device internals such as registers and memories, port information, component descriptors, and other elements. iGen then builds the C code model files and user editable templates. These include model frameworks with registers, function calls, memory map, and other items. It ensures that all component parts of the model are well-structured using best practices, and are consistent throughout the files, thus eliminating a common source of errors.

More information on iGen can be found: imperas.com/products.

9.0 Peripheral model internals

Each instance of a peripheral model runs on its own virtual machine with an address space large enough for the model. This processor (the PSE) and its memory are separate from any processors, memories and buses in the platform being simulated; they exist only to execute the code of the peripheral model.

Interception of functions defined in the peripheral model allows the use of features of the host system in the

implementation of the behavior of a peripheral. As an example, a real platform might contain a video display device. When simulating this system, it is generally more convenient not to simulate the complete video display device but to use a video package available on the host machine, such as SDL, and to use this to render to the host display. Also models of uarts, ethernet devices and USB components can make use of the host PC resources during simulation, to allow, for example, a simulation to browse the real internet, or the simulation to connect to a real USB device.

10.0 Parts of peripheral models

10.1 Configuring the Peripheral Instance with Parameters

A peripheral can include the behaviour of several configurations. These are controlled when the peripheral is instanced in the platform by setting parameters defined on the peripheral.

10.2 Net Ports

Peripherals may be connected to other peripherals or processors with signal wires (nets). These can be used to act as interrupt signals or used to control behavior between peripherals.
The wires are created in the platform as nets and this net is connected into the peripheral using a net port.

10.3 Bus master ports

A bus master port initiates (and controls the address of) a bus cycle. Bus cycles are generated by behavioral code within the peripheral model.

10.4 Bus slave ports

A peripheral can be defined as having several bus slave ports. The bus slave ports can be split into several address blocks. Each address block be either local memory or memory mapped registers. Both of these can have associated callback functions. A memory mapped register can also be defined as specific read/write access, whether it is volatile, and also whether it is associated with a reset pin and mask. A memory mapped register can also have specific bit fields defined.

10.5 Packetnets

A peripheral can be defined as being connected to packetnet ports. A packetnet is used to model packet based communication such as Ethernet, CAN bus or GSM. A packetnet is created in a platform, then connected to packetnet ports on model instances. A packetnet can have many connections, each able to send or receive packets. A packetnet is used as an efficient method of communication within OVP models.

For more information on modeling with packetnets, please see the peripheral modeling documentation: OVP_Peripheral_Modeling_Guide.pdf, OVPsim_and_CpuManager_User_Guide.pdf and the example: $IMPERAS_HOME/Examples/Models/Peripherals/packetnet.

11.0 More information (documentation) on peripheral models and modeling

More information on modeling and APIs can be found at: OVPworld.org/technology_apis.

Specifics on modeling peripherals can be found: OVP_Peripheral_Modeling_Guide.pdf.

A full list of the currently available OVP documentation is available: OVPworld.org/documentation.
#