

### OVP Guide to Using Processor Models

# Model specific information for MIPS\_MIPS64R6

Imperas Software Limited Imperas Buildings, North Weston Thame, Oxfordshire, OX9 2HA, U.K. docs@imperas.com



Author	Imperas Software Limited
Version	20211118.0
Filename	OVP_Model_Specific_Information_mips64_MIPS64R6.pdf
Created	31 December 2021
Status	OVP Standard Release

### Copyright Notice

Copyright (c) 2021 Imperas Software Limited. All rights reserved. This software and documentation contain information that is the property of Imperas Software Limited. The software and documentation are furnished under a license agreement and may be used or copied only in accordance with the terms of the license agreement. No part of the software and documentation may be reproduced, transmitted, or translated, in any form or by any means, electronic, mechanical, manual, optical, or otherwise, without prior written permission of Imperas Software Limited, or as expressly provided by the license agreement.

### Right to Copy Documentation

The license agreement with Imperas permits licensee to make copies of the documentation for its internal use only. Each copy shall include all copyrights, trademarks, service marks, and proprietary rights notices, if any.

### **Destination Control Statement**

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the readers responsibility to determine the applicable regulations and to comply with them.

#### Disclaimer

IMPERAS SOFTWARE LIMITED, AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

#### Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

# Contents

1	Overview	1
	1.1 Description	1
	1.2 Licensing	1
	1.3 Limitations	2
	1.4 Verification	2
	1.5 Features	2
2	Configuration	3
	2.1 Location	3
	2.2 GDB Path	3
	2.3 Semi-Host Library	3
	2.4 Processor Endian-ness	3
	2.5 QuantumLeap Support	3
	2.6 Processor ELF code	3
3	All Variants in this model	4
4	Bus Master Ports	5
5	Bus Slave Ports	6
6	Net Ports	7
7	FIFO Ports	18
8	Formal Parameters	19
	8.1 Parameter values	38
	8.2 Parameter values	71
	8.3 Parameter values	.05
9	Execution Modes 1	21
10	Exceptions 1	22
11	Hierarchy of the model 1	25
	11.1 Level 1: CMP	25
	11.2 Level 2: CPU	25
	11.2 Lovel 2. VD	

12 Mod	lel Commands 127
12.1	Level 1: CMP
	12.1.1 isync
	12.1.2 itrace
12.2	Level 2: CPU
	12.2.1 isync
	12.2.2 itrace
12.3	Level 3: VP
	12.3.1 isync
	12.3.2 itrace
	12.3.3 mipsCOP0
	12.3.4 mipsCacheDisable
	12.3.4.1 Argument description
	12.3.5 mipsCacheEnable
	12.3.6 mipsCacheRatio
	12.3.7 mipsCacheReport
	12.3.7.1 Argument description
	12.3.8 mipsCacheReset
	12.3.8.1 Argument description
	12.3.9 mipsCacheTrace
	12.3.10 mipsDebugFlags
	12.3.11 mipsReadRegister
	12.3.12 mipsReadTLBEntry
	12.3.13 mipsTLBDump
	12.3.13.11 Argument description
	12.3.13.14 mips TLB Dump Guest
	12.3.14.11 Argument description
	12.3.15 mipsTLBDumpRoot
	12.3.15.1 Argument description
	12.3.16 mipsTLBGetPhys
	12.3.17 mips Trace Guest
	12.3.18 mips TraceRoot
	12.3.19 mipsWriteRegister
	12.3.20 mipsWriteTLBEntry
13 Reg	isters 133
_	Level 1: CMP
	Level 2: CPU
	Level 3: VP
10.0	13.3.1 Core
	13.3.2 FPU
	13.3.3 DSP
	13.3.4 Shadow
	13.3.5 COP0
	13.3.6 MSA
	13.3.7 CMP_GCR
	13.3.8 CMP_CPC
	13.3.9 CMP_GIC
	10.0.0

	_MIPS64R6	for MIPS_N	Documentation	essor Model	Fast Proce	Imperas OVP	
155					n_support	13.3.10 Integration	

### Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

### 1.1 Description

MIPS64 Configurable Processor Model

If you need other variants, these models can be obtained from www.OVPworld.org/ip-vendor-mips.

### 1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

### 1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/ip-vendor-mips.

Cache model does not implement coherency

### 1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

#### 1.5 Features

Only MIPS64 Instruction set implemented

MMU Type: Dual VTLB and FTLB

FPU implemented

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

External interrupt controller implemented

Vectored interrupts implemented

## Configuration

### 2.1 Location

This model's VLNV is mips.ovpworld.org/processor/mips64/1.0.

The model source is usually at:

\$IMPERAS\_HOME/ImperasLib/source/mips.ovpworld.org/processor/mips64/1.0

The model binary is usually at:

\$IMPERAS\_HOME/lib/\$IMPERAS\_ARCH/ImperasLib/mips.ovpworld.org/processor/mips64/1.0

### 2.2 GDB Path

The default GDB for this model is: \$IMPERAS\_HOME/lib/\$IMPERAS\_ARCH/gdb/mips-sde-elf-gdb.

### 2.3 Semi-Host Library

The default semi-host library file is mips.ovpworld.org/semihosting/mips64Newlib/1.0

### 2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

### 2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

### 2.6 Processor ELF code

The ELF code supported by this model is: 0x8.

## All Variants in this model

This model has these variants

Variant	Description
P6600	
I6400	
MIPS64R6	(described in this document)
I6500	

Table 3.1: All Variants in this model

## **Bus Master Ports**

This model has these bus master ports.

Name	ame min max Connect?		Connect?	Description
INSTRUCTION	12	59	mandatory	
DATA	12	59	optional	

Table 4.1: Bus Master Ports

# **Bus Slave Ports**

This model has no bus slave ports.

# Net Ports

This model has these net ports.

Name	Type	Connect?	Description
reset	input	optional	CMP reset
dint	input	optional	Debug external interrupt
int0	input	optional	GIC external interrupt
int1	input	optional	GIC external interrupt
int2	input	optional	GIC external interrupt
int3	input	optional	GIC external interrupt
int4	input	optional	GIC external interrupt
int5	input	optional	GIC external interrupt
int6	input	optional	GIC external interrupt
int7	input	optional	GIC external interrupt
int8	input	optional	GIC external interrupt
int9	input	optional	GIC external interrupt
int10	input	optional	GIC external interrupt
int11	input	optional	GIC external interrupt
int12	input	optional	GIC external interrupt
int13	input	optional	GIC external interrupt
int14	input	optional	GIC external interrupt
int15	input	optional	GIC external interrupt
int16	input	optional	GIC external interrupt
int17	input	optional	GIC external interrupt
int18	input	optional	GIC external interrupt
int19	input	optional	GIC external interrupt
int20	input	optional	GIC external interrupt
int21	input	optional	GIC external interrupt
int22	input	optional	GIC external interrupt
int23	input	optional	GIC external interrupt
int24	input	optional	GIC external interrupt
int25	input	optional	GIC external interrupt
int26	input	optional	GIC external interrupt
int27	input	optional	GIC external interrupt
int28	input	optional	GIC external interrupt

int29	input	optional	GIC external interrupt
int30	input	optional	GIC external interrupt
int31	input	optional	GIC external interrupt
int32	input	optional	GIC external interrupt
int33	input	optional	GIC external interrupt
int34	input	optional	GIC external interrupt
int35	input	optional	GIC external interrupt
int36	input	optional	GIC external interrupt
int37	input	optional	GIC external interrupt
int38	input	optional	GIC external interrupt
int39	input	optional	GIC external interrupt
int40	input	optional	GIC external interrupt
int41	input	optional	GIC external interrupt
int42	input	optional	GIC external interrupt
int43	input	optional	GIC external interrupt
int44	input	optional	GIC external interrupt
int45	input	optional	GIC external interrupt
int46	input	optional	GIC external interrupt
int47	input	optional	GIC external interrupt
int48	input	optional	GIC external interrupt
int49	input	optional	GIC external interrupt
int50	input	optional	GIC external interrupt
int51	input	optional	GIC external interrupt
int52	input	optional	GIC external interrupt
int53	input	optional	GIC external interrupt
int54	input	optional	GIC external interrupt
int55	input	optional	GIC external interrupt
int56	input	optional	GIC external interrupt
int57	input	optional	GIC external interrupt
int58	input	optional	GIC external interrupt
int59	input	optional	GIC external interrupt
int60	input	optional	GIC external interrupt
int61	input	optional	GIC external interrupt
int62	input	optional	GIC external interrupt
int63	input	optional	GIC external interrupt
int64	input	optional	GIC external interrupt
int65	input	optional	GIC external interrupt
int66	input	optional	GIC external interrupt
int67	input	optional	GIC external interrupt
int68	input	optional	GIC external interrupt
int69	input	optional	GIC external interrupt
int70	input	optional	GIC external interrupt
int71	input	optional	GIC external interrupt
int72	input	optional	GIC external interrupt
int73	input	optional	GIC external interrupt
	_		

int74	input	optional	GIC external interrupt
int75	input	optional	GIC external interrupt
int76	input	optional	GIC external interrupt
int77	input	optional	GIC external interrupt
int78	input	optional	GIC external interrupt
int79	input	optional	GIC external interrupt
int80	input	optional	GIC external interrupt
int81	input	optional	GIC external interrupt
int82	input	optional	GIC external interrupt
int83	input	optional	GIC external interrupt
int84	input	optional	GIC external interrupt
int85	input	optional	GIC external interrupt
int86	input	optional	GIC external interrupt
int87	input	optional	GIC external interrupt
int88	input	optional	GIC external interrupt
int89	input	optional	GIC external interrupt
int90	input	optional	GIC external interrupt
int91	input	optional	GIC external interrupt
int92	input	optional	GIC external interrupt
int93	input	optional	GIC external interrupt
int94	input	optional	GIC external interrupt
int95	input	optional	GIC external interrupt
int96	input	optional	GIC external interrupt
int97	input	optional	GIC external interrupt
int98	input	optional	GIC external interrupt
int99	input	optional	GIC external interrupt
int100	input	optional	GIC external interrupt
int101	input	optional	GIC external interrupt
int102	input	optional	GIC external interrupt
int103	input	optional	GIC external interrupt
int104	input	optional	GIC external interrupt
int105	input	optional	GIC external interrupt
int106	input	optional	GIC external interrupt
int107	input	optional	GIC external interrupt
int108	input	optional	GIC external interrupt
int109	input	optional	GIC external interrupt
int110	input	optional	GIC external interrupt
int111	input	optional	GIC external interrupt
int112	input	optional	GIC external interrupt
int113	input	optional	GIC external interrupt
int114	input	optional	GIC external interrupt
int115	input	optional	GIC external interrupt
int116	input	optional	GIC external interrupt
int117	input	optional	GIC external interrupt
int118	input	optional	GIC external interrupt
			<u>*</u>

[440	T.		
int119	input	optional	GIC external interrupt
int120	input	optional	GIC external interrupt
int121	input	optional	GIC external interrupt
int122	input	optional	GIC external interrupt
int 123	input	optional	GIC external interrupt
int 124	input	optional	GIC external interrupt
int125	input	optional	GIC external interrupt
int126	input	optional	GIC external interrupt
int127	input	optional	GIC external interrupt
ej_disable_probe_debug	input	optional	GIC ej_disable_probe_debug
ejtagbrk_override	input	optional	GIC ejtagbrk_override
ej_dint_in	input	optional	GIC ej_dint_in
GCR_CUSTOM_BASE	output	optional	Provides the least significant 32-bits of the value written to the GCR_CUSTOM_BASE register. Second half of GCR_CUSTOM_BASE_HI and GCR_CUSTOM_BASE output.
GCR_CUSTOM_BASE_UPPER	output	optional	Provides the most significant 32-bits of value written to the the GCR_CUSTOM_BASE register. First half of GCR_CUSTOM_BASE_HI and GCR_CUSTOM_BASE output.
dint_CPU0_VP0	input	optional	Debug external interrupt
hwint0_CPU0_VP0	input	optional	External interrupt
hwint1_CPU0_VP0	input	optional	External interrupt
hwint2_CPU0_VP0	input	optional	External interrupt
hwint3_CPU0_VP0	input	optional	External interrupt
hwint4_CPU0_VP0	input	optional	External interrupt
hwint5_CPU0_VP0	input	optional	External interrupt
nmi_CPU0_VP0	input	optional	Non-maskable external interrupt
EICPresent_CPU0_VP0	input	optional	Input signal SLEICPresent per VPE
EIC_RIPL_CPU0_VP0	input	optional	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VP0	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU0_VP0	input	optional	External interrupt controller vector number
EIC_VectorOffset_CPU0_VP0	input	optional	External interrupt controller vector offset
EIC_GID_CPU0_VP0	input	optional	External interrupt controller guest ID
intISS_CPU0_VP0	output	optional	True when interrupt request is serviced
causeTI_CPU0_VP0	output	optional	True when timer interrupt expires
causeIP0_CPU0_VP0	output	optional	Raised for software interrupt request IP0
causeIP1_CPU0_VP0	output	optional	Raised for software interrupt request IP1
si_sleep_CPU0_VP0	output	optional	True when the VPE is in WAIT state
hwint0	input	optional	External interrupt for compatibility
IIW IIIUU	րութա	obnonai	External interrupt for companionity

vc_run_CPU0_VP0	innut	ontional	Set to force stop of execution on processor
VC_run_CPUU_VPU	input	optional	
Cuest EIC DIDL CDIIO VDO	incress	on4: 1	VPE (simulation control only)
Guest.EIC_RIPL_CPU0_VP0	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VP0	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VP0	input	optional	Guest External interrupt controller vector
G + BIG H + Off + CDHO HBO			number
Guest.EIC_VectorOffset_CPU0_VP0	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU0_VP0	input	optional	Guest External interrupt controller guest
G IIGG CDIIO IVDO			ID
Guest.intISS_CPU0_VP0	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU0_VP0	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VP0	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU0_VP0	output	optional	Raised for Guest software interrupt re-
			quest IP1
dint_CPU0_VP1	input	optional	Debug external interrupt
hwint0_CPU0_VP1	input	optional	External interrupt
hwint1_CPU0_VP1	input	optional	External interrupt
hwint2_CPU0_VP1	input	optional	External interrupt
hwint3_CPU0_VP1	input	optional	External interrupt
hwint4_CPU0_VP1	input	optional	External interrupt
hwint5_CPU0_VP1	input	optional	External interrupt
nmi_CPU0_VP1	input	optional	Non-maskable external interrupt
EICPresent_CPU0_VP1	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VP1	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VP1	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU0_VP1	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU0_VP1	input	optional	External interrupt controller vector offset
EIC_GID_CPU0_VP1	input	optional	External interrupt controller guest ID
intISS_CPU0_VP1	output	optional	True when interrupt request is serviced
causeTI_CPU0_VP1	output	optional	True when timer interrupt expires
causeIP0_CPU0_VP1	output	optional	Raised for software interrupt request IP0
causeIP1_CPU0_VP1	output	optional	Raised for software interrupt request IP1
si_sleep_CPU0_VP1	output	optional	True when the VPE is in WAIT state
vc_run_CPU0_VP1	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU0_VP1	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VP1	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VP1	input	optional	Guest External interrupt controller vector
	-	=	number
Guest.EIC_VectorOffset_CPU0_VP1	input	optional	Guest External interrupt controller vector
		-	offset

Guest.EIC_GID_CPU0_VP1	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU0_VP1	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU0_VP1	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VP1	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU0_VP1	output	optional	Raised for Guest software interrupt re-
			quest IP1
dint_CPU0_VP2	input	optional	Debug external interrupt
hwint0_CPU0_VP2	input	optional	External interrupt
hwint1_CPU0_VP2	input	optional	External interrupt
hwint2_CPU0_VP2	input	optional	External interrupt
hwint3_CPU0_VP2	input	optional	External interrupt
hwint4_CPU0_VP2	input	optional	External interrupt
hwint5_CPU0_VP2	input	optional	External interrupt
nmi_CPU0_VP2	input	optional	Non-maskable external interrupt
EICPresent_CPU0_VP2	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VP2	input	optional	External interrupt controller RIPL (alias
		_	of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VP2	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU0_VP2	input	optional	External interrupt controller vector num-
	_	_	ber
EIC_VectorOffset_CPU0_VP2	input	optional	External interrupt controller vector offset
EIC_GID_CPU0_VP2	input	optional	External interrupt controller guest ID
intISS_CPU0_VP2	output	optional	True when interrupt request is serviced
causeTI_CPU0_VP2	output	optional	True when timer interrupt expires
causeIP0_CPU0_VP2	output	optional	Raised for software interrupt request IP0
causeIP1_CPU0_VP2	output	optional	Raised for software interrupt request IP1
si_sleep_CPU0_VP2	output	optional	True when the VPE is in WAIT state
vc_run_CPU0_VP2	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU0_VP2	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VP2	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VP2	input	optional	Guest External interrupt controller vector
		_	number
Guest.EIC_VectorOffset_CPU0_VP2	input	optional	Guest External interrupt controller vector
	_	=	offset
Guest.EIC_GID_CPU0_VP2	input	optional	Guest External interrupt controller guest
		-	ID
Guest.intISS_CPU0_VP2	output	optional	True when Guest interrupt request is ser-
		•	viced
Guest.causeTI_CPU0_VP2	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU0_VP2	output	optional	Raised for Guest software interrupt re-
	•	•	quest IP0
			_ *

C + ID1 CDII0 VD0		ı· 1	
Guest.causeIP1_CPU0_VP2	output	optional	Raised for Guest software interrupt re-
1: 4 CIDITO VIDS	. ,	4. 1	quest IP1
dint_CPU0_VP3	input	optional	Debug external interrupt
hwint0_CPU0_VP3	input	optional	External interrupt
hwint1_CPU0_VP3	input	optional	External interrupt
hwint2_CPU0_VP3	input	optional	External interrupt
hwint3_CPU0_VP3	input	optional	External interrupt
hwint4_CPU0_VP3	input	optional	External interrupt
hwint5_CPU0_VP3	input	optional	External interrupt
nmi_CPU0_VP3	input	optional	Non-maskable external interrupt
EICPresent_CPU0_VP3	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0_VP3	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU0_VP3	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU0_VP3	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU0_VP3	input	optional	External interrupt controller vector offset
EIC_GID_CPU0_VP3	input	optional	External interrupt controller guest ID
intISS_CPU0_VP3	output	optional	True when interrupt request is serviced
causeTI_CPU0_VP3	output	optional	True when timer interrupt expires
causeIP0_CPU0_VP3	output	optional	Raised for software interrupt request IP0
causeIP1_CPU0_VP3	output	optional	Raised for software interrupt request IP1
si_sleep_CPU0_VP3	output	optional	True when the VPE is in WAIT state
vc_run_CPU0_VP3	input	optional	Set to force stop of execution on processor
		· · · · · · · · · · · · · · · · · · ·	VPE (simulation control only)
Guest.EIC_RIPL_CPU0_VP3	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0_VP3	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0_VP3	input	optional	Guest External interrupt controller vector
Guest. Die vectorivanier et et v	inpat	optional	number
Guest.EIC_VectorOffset_CPU0_VP3	input	optional	Guest External interrupt controller vector
Guest. Lie-vector onset-er co-vi s	input	optionar	offset
Guest.EIC_GID_CPU0_VP3	input	optional	Guest External interrupt controller guest
Guest.E1C_G1D_C1 G0_V1 5	Input	optionar	ID
Guest.intISS_CPU0_VP3	output	optional	True when Guest interrupt request is ser-
Guest.intipp_C1 00_v1 5	Սաւթա	optional	viced
Guest.causeTI_CPU0_VP3	output	ontional	True when Guest timer interrupt expires
	output	optional	
Guest.causeIP0_CPU0_VP3	output	optional	Raised for Guest software interrupt re-
Cuest saussID1 CDII0 VD9	0	ont:1	quest IP0
Guest.causeIP1_CPU0_VP3	output	optional	Raised for Guest software interrupt re-
l' + CDII1 VDO		, • 1	quest IP1
dint_CPU1_VP0	input	optional	Debug external interrupt
hwint0_CPU1_VP0	input	optional	External interrupt
hwint1_CPU1_VP0	input	optional	External interrupt
hwint2_CPU1_VP0	input	optional	External interrupt
hwint3_CPU1_VP0	input	optional	External interrupt

hwint4_CPU1_VP0	input	optional	External interrupt
hwint5_CPU1_VP0	input	optional	External interrupt
nmi_CPU1_VP0	input	optional	Non-maskable external interrupt
EICPresent_CPU1_VP0	input	optional	Input signal SLEICPresent per VPE
EIC_RIPL_CPU1_VP0	input	optional	External interrupt controller RIPL (alias
	1	•	of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VP0	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU1_VP0	input	optional	External interrupt controller vector num-
	_		ber
EIC_VectorOffset_CPU1_VP0	input	optional	External interrupt controller vector offset
EIC_GID_CPU1_VP0	input	optional	External interrupt controller guest ID
intISS_CPU1_VP0	output	optional	True when interrupt request is serviced
causeTI_CPU1_VP0	output	optional	True when timer interrupt expires
causeIP0_CPU1_VP0	output	optional	Raised for software interrupt request IP0
causeIP1_CPU1_VP0	output	optional	Raised for software interrupt request IP1
si_sleep_CPU1_VP0	output	optional	True when the VPE is in WAIT state
vc_run_CPU1_VP0	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU1_VP0	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VP0	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VP0	input	optional	Guest External interrupt controller vector
			number
Guest.EIC_VectorOffset_CPU1_VP0	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU1_VP0	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU1_VP0	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU1_VP0	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VP0	output	optional	Raised for Guest software interrupt re-
G IDI GDIH IVD			quest IP0
Guest.causeIP1_CPU1_VP0	output	optional	Raised for Guest software interrupt re-
l' - ODIII VD1	. ,	. 1	quest IP1
dint_CPU1_VP1	input	optional	Debug external interrupt
hwint0_CPU1_VP1	input	optional	External interrupt
hwint1_CPU1_VP1	input	optional	External interrupt
hwint2_CPU1_VP1	input	optional	External interrupt
hwint3_CPU1_VP1 hwint4_CPU1_VP1	input	optional	External interrupt
hwint4_CPU1_VP1 hwint5_CPU1_VP1	input	optional	External interrupt
	input	optional	External interrupt
nmi_CPU1_VP1	input	optional	Non-maskable external interrupt
EICPresent_CPU1_VP1	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VP1	input	optional	External interrupt controller RIPL (alias
EIC_EICSS_CPU1_VP1	innut	ontional	of hwint0 - 5 or 7) External interrupt controller EICSS
EIO-EIOSS-OFUI-VFI	input	optional	External interrupt controller EIC55

EIC_VectorNum_CPU1_VP1	input	optional	External interrupt controller vector num-
EIC_vectorNum_Cr Cr_vrr	mput	optional	ber
EIC_VectorOffset_CPU1_VP1	input	optional	External interrupt controller vector offset
EIC_GID_CPU1_VP1	input	optional	External interrupt controller guest ID
intISS_CPU1_VP1	output	optional	True when interrupt request is serviced
causeTI_CPU1_VP1	output	optional	True when timer interrupt expires
causeIP0_CPU1_VP1	output	optional	Raised for software interrupt request IP0
causeIP1_CPU1_VP1		optional	Raised for software interrupt request IP1
si_sleep_CPU1_VP1	output		True when the VPE is in WAIT state
vc_run_CPU1_VP1	output input	optional optional	Set to force stop of execution on processor
verun er er er	mput	optional	VPE (simulation control only)
Guest.EIC_RIPL_CPU1_VP1	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VP1	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VP1	input	optional	Guest External interrupt controller vector
			number
Guest.EIC_VectorOffset_CPU1_VP1	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU1_VP1	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU1_VP1	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU1_VP1	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VP1	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU1_VP1	output	optional	Raised for Guest software interrupt re-
			quest IP1
dint_CPU1_VP2	input	optional	Debug external interrupt
hwint0_CPU1_VP2	input	optional	External interrupt
hwint1_CPU1_VP2	input	optional	External interrupt
hwint2_CPU1_VP2	input	optional	External interrupt
hwint3_CPU1_VP2	input	optional	External interrupt
hwint4_CPU1_VP2	input	optional	External interrupt
hwint5_CPU1_VP2	input	optional	External interrupt
nmi_CPU1_VP2	input	optional	Non-maskable external interrupt
EICPresent_CPU1_VP2	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VP2	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VP2	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU1_VP2	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU1_VP2	input	optional	External interrupt controller vector offset
EIC_GID_CPU1_VP2	input	optional	External interrupt controller guest ID
intISS_CPU1_VP2	output	optional	True when interrupt request is serviced
causeTI_CPU1_VP2	output	optional	True when timer interrupt expires
causeIP0_CPU1_VP2	output	optional	Raised for software interrupt request IP0

causeIP1_CPU1_VP2	output	optional	Raised for software interrupt request IP1
si_sleep_CPU1_VP2	output	optional	True when the VPE is in WAIT state
vc_run_CPU1_VP2	input	optional	Set to force stop of execution on processor
1011 and 011 11 <b>2</b>	III p a c	орогона	VPE (simulation control only)
Guest.EIC_RIPL_CPU1_VP2	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VP2	input	optional	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1_VP2	input	optional	Guest External interrupt controller vector
	Input	optional	number
Guest.EIC_VectorOffset_CPU1_VP2	input	optional	Guest External interrupt controller vector
	1	1	offset
Guest.EIC_GID_CPU1_VP2	input	optional	Guest External interrupt controller guest
	1	1	ID
Guest.intISS_CPU1_VP2	output	optional	True when Guest interrupt request is ser-
	_	_	viced
Guest.causeTI_CPU1_VP2	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VP2	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU1_VP2	output	optional	Raised for Guest software interrupt re-
			quest IP1
dint_CPU1_VP3	input	optional	Debug external interrupt
hwint0_CPU1_VP3	input	optional	External interrupt
hwint1_CPU1_VP3	input	optional	External interrupt
hwint2_CPU1_VP3	input	optional	External interrupt
hwint3_CPU1_VP3	input	optional	External interrupt
hwint4_CPU1_VP3	input	optional	External interrupt
hwint5_CPU1_VP3	input	optional	External interrupt
nmi_CPU1_VP3	input	optional	Non-maskable external interrupt
EICPresent_CPU1_VP3	input	optional	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1_VP3	input	optional	External interrupt controller RIPL (alias
			of hwint0 - 5 or 7)
EIC_EICSS_CPU1_VP3	input	optional	External interrupt controller EICSS
EIC_VectorNum_CPU1_VP3	input	optional	External interrupt controller vector num-
			ber
EIC_VectorOffset_CPU1_VP3	input	optional	External interrupt controller vector offset
EIC_GID_CPU1_VP3	input	optional	External interrupt controller guest ID
intISS_CPU1_VP3	output	optional	True when interrupt request is serviced
causeTI_CPU1_VP3	output	optional	True when timer interrupt expires
causeIP0_CPU1_VP3	output	optional	Raised for software interrupt request IP0
causeIP1_CPU1_VP3	output	optional	Raised for software interrupt request IP1
si_sleep_CPU1_VP3	output	optional	True when the VPE is in WAIT state
vc_run_CPU1_VP3	input	optional	Set to force stop of execution on processor
			VPE (simulation control only)
Guest.EIC_RIPL_CPU1_VP3	input	optional	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1_VP3	input	optional	Guest External interrupt controller EICSS

Guest.EIC_VectorNum_CPU1_VP3	input	optional	Guest External interrupt controller vector
			number
Guest.EIC_VectorOffset_CPU1_VP3	input	optional	Guest External interrupt controller vector
			offset
Guest.EIC_GID_CPU1_VP3	input	optional	Guest External interrupt controller guest
			ID
Guest.intISS_CPU1_VP3	output	optional	True when Guest interrupt request is ser-
			viced
Guest.causeTI_CPU1_VP3	output	optional	True when Guest timer interrupt expires
Guest.causeIP0_CPU1_VP3	output	optional	Raised for Guest software interrupt re-
			quest IP0
Guest.causeIP1_CPU1_VP3	output	optional	Raised for Guest software interrupt re-
			quest IP1

Table 6.1: Net Ports

# FIFO Ports

This model has no FIFO ports.

## Formal Parameters

Name	Type	Description
variant	Enumeration	Processor variant
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info struc-
		ture
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB
•		exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
gprNames	Boolean	Disassemble the register names from the default
		ABI instead of register numbers for MIPS-format
		trace output
supervisorMode	Boolean	Override whether processor implements supervisor
		mode
busErrors	Boolean	Override bus error exception behavior. When true,
		accesses of memory not defined by platform will
		cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when
		true (sets Config.MT=3, Config.KU/K23=2 and
		Config1.MMUSizeM1=0)
fixedDbgRegSize	Boolean	Enable applications to debug on P5600 with GDB
		version 2015.06-05 and prior
removeDSP	Boolean	Override the DSP-present configuration when true
		(sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true
		(sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true
		(sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true
		(disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from
		ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to
		maximum value to improve performance
perfCounters	Uns32	Performance Counters
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores
		only)

IDON DIDO	TT 90	
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC
IMODINOD	TT 00	implementation (MT cores only)
ITCFIFODepth	Uns32	Specify ITC FIFO cell depth. By default supports
		4.
ITCEmptyOnReset	Boolean	Specify ITC E/F cells reset to a known empty state.
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior,
		2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal
		operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0. Ig-
		nored if less than two VPEs configured.
VPE1MaxTC	Uns32	Specifies the maximum TCs initially on VPE1. Ig-
		nored if less than three VPEs configured.
segBits	Uns32	Override the number of address bits implemented
508210	011002	for 64 bit segments (MIPS64 Only)
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentCon-
		trol_0 register
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentCon-
		trol_0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentCon-
		trol_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentCon-
		trol_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentCon-
		trol_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentCon-
		trol_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentCon-
		trol_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentCon-
•		trol_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentCon-
		trol_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentCon-
inp ac eginenee	011302	trol_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentCon-
inpusegment to	0.11502	trol_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentCon-
inpusegment11	011852	trol_2 register
mpuSegment12	IIma 20	Attributes for segment 12 in MPU2 SegmentCon-
mpusegment12	Uns32	
	TT 00	trol-3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentCon-
9 114	77 00	trol_3 register
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentCon-
~		trol_3 register
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentCon-
		trol_3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
tcDisable	Uns32	Number of disabled TCs
vpeDisable	Uns32	Number of disabled VPEs
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
		<u> </u>

mvpconf1c1f	Boolean	Override MVPConf.C1F
mvpcontrolPolicyMode	Boolean	Override MVPControl.POLICY_MODE
hasFDC	Uns32	Specify the size of Fast Debug Channel register block
licenseWarningDays	Uns32	Specify the number of days before a license expires to start issuing a warning. 0 disables warnings.
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string separated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
TRU_PRESENT	Boolean	Disable or Enable based on TRU presence to control certain fields (e.x.perfCtl.PCTD
ucLLwordsLocked	Uns32	Numbers of words (4 byte) an uncached LL is locking. Maximum: 4K
FUSA	Boolean	Enable Functional Safety
CPC_FAULT_SUPPORTED	Uns32	Specify the value for Functional Safety Supported register
CPC_FAULT_ENABLE	Uns32	Specify the value for Functional Safety Enable register
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object (.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll) defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller (sets Config3 VEIC)
config3VEIC_VPE0	Boolean	Enables an external interrupt controller on VPE0 (sets Config3 VEIC)
config3VEIC_VPE1	Boolean	Enables an external interrupt controller on VPE1 (sets Config3 VEIC)
config3VEIC_VPE2	Boolean	Enables an external interrupt controller on VPE2 (sets Config3 VEIC)
config3VEIC_VPE3	Boolean	Enables an external interrupt controller on VPE3 (sets Config3 VEIC)
${\bf rootFixedMMU}$	Boolean	Override the root MMU type to fixed mapping when true (sets Config.MT=3 and Config.KU/K23=2)
${\bf rootMMUSizeM1}$	Uns32	Override the root MMUSizeM1 field in Config1 register (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
usePreciseFpu	Uns32	Use the precise Floating Point emulation
simulateLite	Enumeration	Run Simulation with optimization. There are several optimizations which coule be combined (NONE, FS, MA or FSMA)
pridCompanyOptions	Uns32	Override the Company Options field in PRId register
pridRevision	Uns32	Override the Revision field in PRId register
Printeriori	0.11502	O verride one reconsion neighbrid in 1 ffid register

globalClusterNum	Uns32	Override the ClusterNum field in GlobalNumber register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intetlIPFDC	Uns32	Override the IPFDC field in IntCtl register
intelliPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	I	
	Uns32	Specify number of WatchLo/WatchHi register pairs
maxVP	Uns32	Specify maximum number of Virtual Processors present in a core
numVP	Uns32	Specify number of Virtual Processors to be present
numVPtoStart	Uns32	Specify number of Virtual Processors to be started
sharedTLBindex	Uns32	Specify first shared TLB Index between Virtual Cores
xconfigSpecified	Boolean	True if the configuration comes from a valid xconfig file
intctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
intctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
intctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
intctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
intctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
intctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
$intctlIPTI\_CPU1\_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
intctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
intctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
intctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
intctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
intctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
intctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
intctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
intctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
intctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
intctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
intctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
intctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
intctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
intctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0

intctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
intctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
intctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
intctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
intctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
intctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
intctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
intctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
intctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
intctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
intctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
intctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
intetlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
intctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
intctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
intctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
intetlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
intctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
intctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
intctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
intctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
intctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
intctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
intctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
intctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
intctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
intctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
intctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0

intctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
intctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
intctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
intctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
intctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
intctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
intctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
intctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
intctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
intctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
intctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
intctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
intctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
intctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
intctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
intctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
intctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
intctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
intctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
intctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
intctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
intctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
intctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
intctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
intctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
intctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
intctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
intctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0

intetIIPPCLCPU3.VPP intetIIPPCLCPU3.VPP intetIIPPCLCPU3.VPP intetIIPPCLCPU3.VPP intetIIPPCLCPU4.VPO intetIIPPCLCPU5.VPO intetI			
intetlIPPCLCPU3.VP3 intetlIPPCLCPU4.VP0 intetlIPPCLCPU4.VP0 intetlIPPCLCPU4.VP1 intetlIPPCLCPU4.VP1 intetlIPPCLCPU4.VP2 intetlIPPCLCPU4.VP2 intetlIPPCLCPU4.VP3 intetlIPPCLCPU4.VP3 intetlIPPCLCPU4.VP3 intetlIPPCLCPU4.VP3 intetlIPPCLCPU4.VP3 intetlIPPCLCPU4.VP3 intetlIPPCLCPU4.VP3 intetlIPPCLCPU5.VP0 intetlIPPCLCPU5.VP0 intetlIPPCLCPU5.VP0 intetlIPPCLCPU5.VP0 intetlIPPCLCPU5.VP0 intetlIPPCLCPU5.VP0 intetlIPPCLCPU5.VP0 intetlIPPCLCPU5.VP0 intetlIPPCLCPU5.VP0 intetlIPPCLCPU5.VP1 intetlIPPCLCPU5.VP1 intetlIPPCLCPU5.VP2 intetlIPPCLCPU5.VP2 intetlIPPCLCPU5.VP3 intetlIPPCLCPU5.VP4 intetlIPPCLCPU5.VP4 intetlIPPCLCPU5.VP4 intetlIPPCLCPU5.VP6 intetlIPPCLCPU5.VP6 intetlIPPCLCPU5.VP7 intetlIPPCLCPU5.VP7 intetlIPPCLCPU5.VP8 intetlIPPCLCPU5.VP8 intetlIPPCLCPU5.VP9 intetlIPPCLCPU5.VP9 intetlIPPCLCPU5.VP9 intetlIPPCLCPU5.VP9 intetlIPPCLCPU5.VP9 intetlIPPCLCPU5.VP9 intetlIPPCLCPU5.VP9 intetlIPPCLCPU5.VP9 intetlIPPCLCPU5.VP9 intetlIPPCLCPU6.VP0 intetlIPPCLCPU6.VP0 intetlIPPCLCPU6.VP1 intetlIPPCLCPU6.VP1 intetlIPPCLCPU6.VP2 intetlIPPCLCPU6.VP2 intetlIPPCLCPU6.VP3 intetlIPPCLCPU6.VP3 intetlIPPCLCPU6.VP4 intetlIPPCLCPU6.VP4 intetlIPPCLCPU6.VP9 intetlIPPCLCPU6.VP9 intetlIPPCLCPU6.VP9 intetlIPPCLCPU6.VP9 intetlIPPCLCPU6.VP9 intetlIPPCLCPU6.VP9 intetlIPPCLCPU7.VP0 intetlIPPCLCPU7.VP0 intetlIPPCLCPU7.VP0 intetlIPPCLCPU7.VP0 intetlIPPCLCPU7.VP0 intetlIPPCLCPU7.VP1 intetlIPPCLCPU7.VP3 intetlIPPCLCPU7.VP4 intetlIPPCLCPU7.VP4 intetlIPPCLCPU7.VP5 intetlIPPCLCPU7.VP6 intetlIPPCLCPU7.VP6 intetlIPPCLCPU7.VP7 intetlIPPCLCPU7.VP7 intetlIPPCLCPU7.VP8 intetlIPPCLCPU7.VP8 intetlIPPCLCPU7.VP9 intetlIPPCLCPU7.VP9 intetlIPPCLCPU7.VP9 intetlIPPCLCPU7.VP9 intetlIPPCLCPU7.VP9 intetlIPPCLCPU7.VP9 intetlIPPCLCPU7.VP9 intetlIPPCLCPU7.VP9 intetlIPPCLCPU7.VP6 intetlIPPCLCPU7.VP6 intetlIPPCLCPU7.VP6 intetlIPPCLCPU7.VP6 intetlIPPCLCPU7.VP6 intetlIPPCLCPU7.VP6 intetl	intctlIPPCI_CPU3_VP1	Uns32	
intetllPPCLCPU4.VP0  IntetllPPCLCPU4.VP0  IntetllPPCLCPU4.VP1  IntetllPPCLCPU4.VP1  IntetllPPCLCPU4.VP1  IntetllPPCLCPU4.VP2  IntetllPPCLCPU4.VP2  IntetllPPCLCPU4.VP3  IntetllPPCLCPU4.VP3  IntetllPPCLCPU5.VP0  IntetllPPCLCPU5.VP0  IntetllPPCLCPU5.VP1  IntetllPPCLCPU5.VP1  IntetllPPCLCPU5.VP1  IntetllPPCLCPU5.VP2  IntetllPPCLCPU5.VP2  IntetllPPCLCPU5.VP2  IntetllPPCLCPU5.VP3  IntetllPPCLCPU5.VP2  IntetllPPCLCPU5.VP3  IntetllPPCLCPU5.VP3  IntetllPPCLCPU5.VP4  IntetllPPCLCPU5.VP4  IntetllPPCLCPU5.VP5  IntetllPPCLCPU5.VP6  IntetllPPCLCPU5.VP7  IntetllPPCLCPU5.VP7  IntetllPPCLCPU5.VP8  IntetllPPCLCPU5.VP8  IntetllPPCLCPU5.VP9  IntetllPPCLCPU6.VP0  IntetllPPCLCPU6.VP0  IntetllPPCLCPU6.VP0  IntetllPPCLCPU6.VP1  IntetllPPCLCPU6.VP1  IntetllPPCLCPU6.VP1  IntetllPPCLCPU6.VP2  IntetllPPCLCPU6.VP2  IntetllPPCLCPU6.VP3  IntetllPPCLCPU6.VP3  IntetllPPCLCPU6.VP3  IntetllPPCLCPU6.VP3  IntetllPPCLCPU6.VP3  IntetllPPCLCPU6.VP3  IntetllPPCLCPU6.VP4  IntetllPPCLCPU6.VP4  IntetllPPCLCPU6.VP4  IntetllPPCLCPU6.VP5  IntetllPPCLCPU6.VP6  IntetllPPCLCPU6.VP6  IntetllPPCLCPU6.VP7  IntetllPPCLCPU6.VP7  IntetllPPCLCPU6.VP7  IntetllPPCLCPU6.VP8  IntetllPPCLCPU6.VP8  IntetllPPCLCPU6.VP9  IntetllPP	intctlIPPCI_CPU3_VP2	Uns32	
intetllPPCLCPU4.VP0  intetllPPCLCPU4.VP1  intetllPPCLCPU4.VP2  intetllPPCLCPU4.VP2  intetllPPCLCPU4.VP3  intetllPPCLCPU4.VP3  intetllPPCLCPU4.VP3  intetllPPCLCPU4.VP3  intetllPPCLCPU5.VP0  intetllPPCLCPU5.VP0  intetllPPCLCPU5.VP0  intetllPPCLCPU5.VP0  intetllPPCLCPU5.VP1  intetllPPCLCPU5.VP1  intetllPPCLCPU5.VP1  intetllPPCLCPU5.VP2  intetllPPCLCPU5.VP2  intetllPPCLCPU5.VP3  intetllPPCLCPU5.VP3  intetllPPCLCPU5.VP4  intetllPPCLCPU5.VP4  intetllPPCLCPU5.VP5  intetllPPCLCPU5.VP6  intetllPPCLCPU5.VP7  intetllPPCLCPU5.VP7  intetllPPCLCPU5.VP8  intetllPPCLCPU5.VP8  intetllPPCLCPU5.VP9  intetllPPCLCPU5.VP9  intetllPPCLCPU5.VP9  intetllPPCLCPU5.VP9  intetllPPCLCPU5.VP9  intetllPPCLCPU5.VP9  intetllPPCLCPU5.VP9  intetllPPCLCPU5.VP9  intetllPPCLCPU6.VP0  intetllPPCLCPU6.VP0  intetllPPCLCPU6.VP0  intetllPPCLCPU6.VP0  intetllPPCLCPU6.VP1  intetllPPCLCPU6.VP1  intetllPPCLCPU6.VP1  intetllPPCLCPU6.VP2  intetllPPCLCPU6.VP2  intetllPPCLCPU6.VP2  intetllPPCLCPU6.VP3  intetllPPCLCPU7.VP0  Uns32  Override the IPPCl field in IntCtl register for CPU7/VP0  intetllPPCLCPU7.VP1  Uns32  Override the IPPCl field in IntCtl register for CPU7/VP1  intetllPPCLCPU7.VP2  Uns32  Override the IPPCl field in IntCtl register for CPU7/VP2  intetllPPCLCPU7.VP3  intetllPPCLCPU7.VP3  Uns32  Set CFG1.PA field of SegCtl1 register segefg1PA  Uns32  Set CFG1.PA field of SegCtl1 register segefg2PA  Uns32  Set CFG3.PA field of SegCtl1 register segefg4MA  Uns32  Set CFG3.PA field of SegCtl1 register segefg4MB  Uns32  Set CFG3.PA field of SegCtl1 register segefg4MBU  Un	intctlIPPCI_CPU3_VP3	Uns32	
intetllPPCLCPU4.VP1  Uns32 Override the IPPCI field in IntCtl register for CPU4/VP2  intetllPPCLCPU4.VP3 Uns32 Override the IPPCI field in IntCtl register for CPU4/VP3  intetllPPCLCPU5.VP0 Uns32 Override the IPPCI field in IntCtl register for CPU4/VP3  intetllPPCLCPU5.VP0 Uns32 Override the IPPCI field in IntCtl register for CPU5/VP0  intetllPPCLCPU5.VP1 Uns32 Override the IPPCI field in IntCtl register for CPU5/VP0  intetllPPCLCPU5.VP1 Uns32 Override the IPPCI field in IntCtl register for CPU5/VP1  intetllPPCLCPU5.VP2 Uns32 Override the IPPCI field in IntCtl register for CPU5/VP2  intetllPPCLCPU5.VP3 Uns32 Override the IPPCI field in IntCtl register for CPU5/VP3  intetllPPCLCPU6.VP0 Uns32 Override the IPPCI field in IntCtl register for CPU6/VP0  intetllPPCLCPU6.VP0 Uns32 Override the IPPCI field in IntCtl register for CPU6/VP0  intetllPPCLCPU6.VP1 Uns32 Override the IPPCI field in IntCtl register for CPU6/VP2  intetllPPCLCPU6.VP2 Uns32 Override the IPPCI field in IntCtl register for CPU6/VP2  intetllPPCLCPU6.VP3 Uns32 Override the IPPCI field in IntCtl register for CPU6/VP3  intetllPPCLCPU7.VP0 Uns32 Override the IPPCI field in IntCtl register for CPU6/VP3  intetllPPCLCPU7.VP0 Uns32 Override the IPPCI field in IntCtl register for CPU7/VP0  intetllPPCLCPU7.VP1 Uns32 Override the IPPCI field in IntCtl register for CPU7/VP0  intetllPPCLCPU7.VP2 Uns32 Override the IPPCI field in IntCtl register for CPU7/VP0  intetllPPCLCPU7.VP3 Uns32 Override the IPPCI field in IntCtl register for CPU7/VP0  intetllPPCLCPU7.VP3 Uns32 Set CFG1.PA field of SegCtll register segcfg1PA Uns32 Set CFG1.PA field of SegCtll register segcfg1PA Uns32 Set CFG3.PA field of SegCtll register segcfg1AM Uns32 Set CFG3.PA field of SegCtll register segcfg1BU Uns32 Set CFG6.PU field of SegCtll register segcfg1BU Uns32 Set CFG6.PU field of	intctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for
intetIIPPCI.CPU4.VP2  intetIIPPCI.CPU4.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU4/VP3  intetIIPPCI.CPU5.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU4/VP3  intetIIPPCI.CPU5.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP0  intetIIPPCI.CPU5.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP1  intetIIPPCI.CPU5.VP2  intetIIPPCI.CPU5.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP2  intetIIPPCI.CPU5.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP2  intetIIPPCI.CPU6.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP0  intetIIPPCI.CPU6.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP0  intetIIPPCI.CPU6.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP1  intetIIPPCI.CPU6.VP2  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP2  intetIIPPCI.CPU6.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP2  intetIIPPCI.CPU7.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP3  intetIIPPCI.CPU7.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP3  intetIIPPCI.CPU7.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP0  intetIIPPCI.CPU7.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP1  intetIIPPCI.CPU7.VP2  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP3  IntetIIPPCI.CPU7.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP3  Set CFG0.PA field of SegCtl0 register segcfg1PA  Uns32  Set CFG0.PA field of SegCtl1 register  segcfg1PA  Uns32  Set CFG0.PA field of SegCtl1 register  segcfg1PA  Uns32  Set CFG0.PA field of SegCtl1 register  segcfg1AM  Uns32  Set CFG0.AM field of SegCtl1 register  segcfg1AM  Uns32  Set CFG0.AM field of SegCtl1 register  segcfg1AM  Uns32  Set CFG0.EU	intctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for
intetlIPPCI.CPU4.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU4/VP3  Override the IPPCI field in IntCtl register for CPU5/VP0  intetlIPPCI.CPU5.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP1  intetlIPPCI.CPU5.VP2  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP2  intetlIPPCI.CPU5.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP3  intetlIPPCI.CPU5.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP3  intetlIPPCI.CPU6.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP0  intetlIPPCI.CPU6.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP0  intetlIPPCI.CPU6.VP2  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP1  intetlIPPCI.CPU6.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP3  intetlIPPCI.CPU6.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP3  intetlIPPCI.CPU7.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP0  intetlIPPCI.CPU7.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP1  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP1  intetlIPPCI.CPU7.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP2  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP3  intetlIPPCI.CPU7.VP2  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP3  Segcfg0PA  Uns32  Set CFG0.PA field of SegCtl0 register Segcfg1PA  Segcfg1PA  Uns32  Set CFG0.PA field of SegCtl1 register Segcfg2PA  Uns32  Set CFG0.PA field of SegCtl1 register Segcfg3PA  Uns32  Set CFG3.PA field of SegCtl1 register Segcfg1AM  Uns32  Set CFG2.AM field of SegCtl1 register Segcfg1AM  Uns32  Set CFG3.AM field of SegCtl1 register Segcfg1AM  Uns32  Set CFG3.AM field of SegCtl1 register Segcfg2AM  Uns32  Set CFG3.AM field of SegCtl1 register Segcfg3AM  Uns32  Set CFG3.AM field of SegCtl1 register Segcfg3AM  Uns32  Set CFG3.EM field of SegCtl1 register Segcfg2AM  Uns32  Set CFG3.EM field of SegCtl1 register Segcfg3AM  Un	intctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for
intetliPPCLCPU5.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP1  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP1  intetliPPCLCPU5.VP2  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP2  intetliPPCLCPU5.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP3  intetliPPCLCPU5.VP3  intetliPPCLCPU6.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP0  intetliPPCLCPU6.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP0  intetliPPCLCPU6.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP1  intetliPPCLCPU6.VP2  intetliPPCLCPU6.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP3  intetliPPCLCPU6.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP3  intetliPPCLCPU7.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP0  intetliPPCLCPU7.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP0  intetliPPCLCPU7.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP1  intetliPPCLCPU7.VP2  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP2  intetliPPCLCPU7.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP3  intetliPPCLCPU7.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP3  intetliPPCLCPU7.VP3  Uns32  Set CFG0.PA field of SegCtl0 register  segcfg1PA  Uns32  Set CFG0.PA field of SegCtl1 register  segcfg1PA  Uns32  Set CFG3.PA field of SegCtl1 register  segcfg3PA  Uns32  Set CFG3.PA field of SegCtl1 register  segcfg4PA  Uns32  Set CFG3.PA field of Se	intctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for
intetlIPPCI_CPU5_VP1  Uns32 Override the IPPCI field in IntCtl register for CPU5_VP1  Uns32 Override the IPPCI field in IntCtl register for CPU5_VP2  intetlIPPCI_CPU5_VP3 Uns32 Override the IPPCI field in IntCtl register for CPU5_VP3  intetlIPPCI_CPU6_VP0 Uns32 Override the IPPCI field in IntCtl register for CPU6_VP0  intetlIPPCI_CPU6_VP0 Uns32 Override the IPPCI field in IntCtl register for CPU6_VP0  intetlIPPCI_CPU6_VP1 Uns32 Override the IPPCI field in IntCtl register for CPU6_VP1  intetlIPPCI_CPU6_VP2 Uns32 Override the IPPCI field in IntCtl register for CPU6_VP1  intetlIPPCI_CPU6_VP3 Uns32 Override the IPPCI field in IntCtl register for CPU6_VP3  intetlIPPCI_CPU7_VP0 Uns32 Override the IPPCI field in IntCtl register for CPU7_VP0  intetlIPPCI_CPU7_VP0 Uns32 Override the IPPCI field in IntCtl register for CPU7_VP0  intetlIPPCI_CPU7_VP1 Uns32 Override the IPPCI field in IntCtl register for CPU7_VP0  intetlIPPCI_CPU7_VP2 Uns32 Override the IPPCI field in IntCtl register for CPU7_VP1  intetlIPPCI_CPU7_VP3 Uns32 Override the IPPCI field in IntCtl register for CPU7_VP1  intetlIPPCI_CPU7_VP3 Uns32 Set CFG0_PA field of SegCtl0 register segcfg1PA Uns32 Set CFG0_PA field of SegCtl0 register segcfg1PA Uns32 Set CFG1_PA field of SegCtl1 register segcfg1PA Uns32 Set CFG1_PA field of SegCtl1 register segcfg1PA Uns32 Set CFG3_PA fiel	intctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for
intetlIPPCI_CPU5_VP2  Uns32  Override the IPPCI field in IntCtl register for CPU5_VP2  Uns32  Override the IPPCI field in IntCtl register for CPU5_VP3  intetlIPPCI_CPU6_VP0  Uns32  Override the IPPCI field in IntCtl register for CPU6_VP0  intetlIPPCI_CPU6_VP0  IntetlIPPCI_CPU6_VP1  Uns32  Override the IPPCI field in IntCtl register for CPU6_VP0  intetlIPPCI_CPU6_VP1  Uns32  Override the IPPCI field in IntCtl register for CPU6_VP1  intetlIPPCI_CPU6_VP2  Uns32  Override the IPPCI field in IntCtl register for CPU6_VP2  intetlIPPCI_CPU6_VP3  IntetlIPPCI_CPU6_VP3  IntetlIPPCI_CPU7_VP0  Uns32  Override the IPPCI field in IntCtl register for CPU7_VP0  intetlIPPCI_CPU7_VP0  Uns32  Override the IPPCI field in IntCtl register for CPU7_VP1  Uns32  Override the IPPCI field in IntCtl register for CPU7_VP1  intetlIPPCI_CPU7_VP1  Uns32  Override the IPPCI field in IntCtl register for CPU7_VP2  intetlIPPCI_CPU7_VP2  IntetlIPPCI_CPU7_VP3  Uns32  Override the IPPCI field in IntCtl register for CPU7_VP2  intetlIPPCI_CPU7_VP3  Uns32  Override the IPPCI field in IntCtl register for CPU7_VP2  intetlIPPCI_CPU7_VP3  Uns32  Override the IPPCI field in IntCtl register for CPU7_VP2  intetlIPPCI_CPU7_VP3  Uns32  Override the IPPCI field in IntCtl register for CPU7_VP2  intetlIPPCI_CPU7_VP3  Uns32  Set CFG0_PA field of SegCtl0 register  segcfg0PA  Uns32  Set CFG0_PA field of SegCtl1 register  segcfg2PA  Uns32  Set CFG1_PA field of SegCtl1 register  segcfg4PA  Uns32  Set CFG3_PA field of SegCtl1 register  segcfg4PA  Uns32  Set CFG3_PA field of SegCtl1 register  segcfg1AM  Uns32  Set CFG3_PA field of SegCtl1 register  segcfg1AM  Uns32  Set CFG3_AM field of SegCtl1 register  segcfg2AM  Uns32  Set CFG3_AM field of SegCtl1 register  segcfg3AM  Uns32  Set CFG3_AM field of SegCtl1 register  segcfg4AM  Uns32  Set CFG3_AM field of SegCtl1 register  segcfg4AM  Uns32  Set CFG3_AM field of SegCtl1 register  segcfg4AM  Uns32  Set CFG3_AM field of SegCtl1 register  segcfg4BU  Uns32  Set CFG3_EU field of SegCtl1 register  segcfg4BU  Uns32  Set CFG3_EU fi	intctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for
intctlIPPCLCPU5_VP3  Uns32  Override the IPPCI field in IntCtl register for CPU5/VP3  Override the IPPCI field in IntCtl register for CPU6/VP0  intctlIPPCLCPU6_VP1  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP1  intctlIPPCLCPU6_VP2  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP2  intctlIPPCLCPU6_VP3  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP3  intctlIPPCLCPU7_VP0  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP3  intctlIPPCLCPU7_VP0  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP0  intctlIPPCLCPU7_VP1  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP1  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP1  intctlIPPCLCPU7_VP2  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP2  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP3  segcfgPA  Uns32  Set CFG_PA field of SegCtl0 register  segcfgPA  Uns32  Set CFG_PA field of SegCtl0 register  segcfgPA  Uns32  Set CFG_PA field of SegCtl1 register  segcfgAM  Uns32  Set CFG_PAM field of SegCtl1 register  seg	intctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for
intctlIPPCLCPU6.VP0  intctlIPPCLCPU6.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP0  intctlIPPCLCPU6.VP2  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP1  intctlIPPCLCPU6.VP2  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP2  intctlIPPCLCPU6.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU6/VP3  intctlIPPCLCPU7.VP0  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP0  intctlIPPCLCPU7.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP0  intctlIPPCLCPU7.VP1  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP1  intctlIPPCLCPU7.VP2  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP2  intctlIPPCLCPU7.VP3  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP2  intctlIPPCLCPU7.VP3  Uns32  Set CFG0.PA field of SegCtl0 register  segcfg1PA  Uns32  Set CFG1.PA field of SegCtl1 register  segcfg2PA  Uns32  Set CFG2.PA field of SegCtl1 register  segcfg4PA  Uns32  Set CFG3.PA field of SegCtl1 register  segcfg5PA  Uns32  Set CFG5.PA field of SegCtl1 register  segcfg1AM  Uns32  Set CFG3.AM field of SegCtl1 register  segcfg1AM  Uns32  Set CFG3.AM field of SegCtl1 register  segcfg3AM  Uns32  Set CFG3.AM field of SegCtl1 register  segcfg4AM  Uns32  Set CFG3.AM field of SegCtl1 register  segcfg5AM  Uns32  Set CFG3.AM field of SegCtl1 register  segcfg4AM  Uns32  Set CFG3.AM field of SegCtl1 register  segcfg5AM  Uns32  Set CFG3.EM field of SegCtl1 register  segcfg5AM  Uns32  Set CFG3.EM field of SegCtl1 register  segcfg1EU  Uns32  Set CFG1.EU field of SegCtl1 register  segcfg1EU  Uns32  Set CFG3.EU field of SegCtl1 register	intctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for
CPU6/VP1	intctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for
CPU6/VP2	intctlIPPCI_CPU6_VP1	Uns32	1
CPU6/VP3	intctlIPPCI_CPU6_VP2	Uns32	1
CPU7/VP0	intctlIPPCI_CPU6_VP3	Uns32	CPU6/VP3
CPU7/VP1	intctlIPPCI_CPU7_VP0	Uns32	
intctlIPPCLCPU7_VP3  Uns32  Override the IPPCI field in IntCtl register for CPU7/VP3  segcfg0PA  Uns32  Set CFG0.PA field of SegCtl0 register  segcfg1PA  Uns32  Set CFG1.PA field of SegCtl0 register  segcfg2PA  Uns32  Set CFG2.PA field of SegCtl1 register  segcfg3PA  Uns32  Set CFG3.PA field of SegCtl1 register  segcfg4PA  Uns32  Set CFG4.PA field of SegCtl1 register  segcfg5PA  Uns32  Set CFG5.PA field of SegCtl2 register  segcfg0AM  SegCfg0AM  Uns32  Set CFG0.AM field of SegCtl2 register  segcfg1AM  Uns32  Set CFG0.AM field of SegCtl2 register  segcfg1AM  Uns32  Set CFG1.AM field of SegCtl0 register  segcfg2AM  SegCfg3AM  Uns32  Set CFG3.AM field of SegCtl1 register  segcfg4AM  Uns32  Set CFG5.AM field of SegCtl2 register  segcfg4AM  Uns32  Set CFG5.AM field of SegCtl2 register  segcfg4AM  Uns32  Set CFG5.AM field of SegCtl2 register  segcfg4EU  Uns32  Set CFG3.EU field of SegCtl1 register  segcfg1EU  segcfg2EU  Uns32  Set CFG3.EU field of SegCtl1 register  segcfg3EU  Uns32  Set CFG3.EU field of SegCtl1 register	intetlIPPCI_CPU7_VP1	Uns32	CPU7/VP1
segcfg0PA         Uns32         Set CFG0.PA field of SegCt10 register           segcfg1PA         Uns32         Set CFG1.PA field of SegCt10 register           segcfg2PA         Uns32         Set CFG2.PA field of SegCt11 register           segcfg3PA         Uns32         Set CFG3.PA field of SegCt11 register           segcfg4PA         Uns32         Set CFG4.PA field of SegCt12 register           segcfg5PA         Uns32         Set CFG5.PA field of SegCt12 register           segcfg0AM         Uns32         Set CFG0.AM field of SegCt10 register           segcfg1AM         Uns32         Set CFG1.AM field of SegCt10 register           segcfg3AM         Uns32         Set CFG3.AM field of SegCt11 register           segcfg4AM         Uns32         Set CFG4.AM field of SegCt12 register           segcfg5AM         Uns32         Set CFG5.AM field of SegCt12 register           segcfg0EU         Uns32         Set CFG0.EU field of SegCt12 register           segcfg1EU         Uns32         Set CFG1.EU field of SegCt10 register           segcfg2EU         Uns32         Set CFG3.EU field of SegCt11 register           segcfg3EU         Uns32         Set CFG3.EU field of SegCt11 register		Uns32	CPU7/VP2
segcfg1PAUns32Set CFG1.PA field of SegCtl0 registersegcfg2PAUns32Set CFG2.PA field of SegCtl1 registersegcfg3PAUns32Set CFG3.PA field of SegCtl1 registersegcfg4PAUns32Set CFG4.PA field of SegCtl2 registersegcfg5PAUns32Set CFG5.PA field of SegCtl2 registersegcfg0AMUns32Set CFG0.AM field of SegCtl0 registersegcfg1AMUns32Set CFG1.AM field of SegCtl0 registersegcfg2AMUns32Set CFG2.AM field of SegCtl1 registersegcfg3AMUns32Set CFG3.AM field of SegCtl1 registersegcfg4AMUns32Set CFG4.AM field of SegCtl2 registersegcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 register	intctlIPPCI_CPU7_VP3	Uns32	
segcfg2PAUns32Set CFG2.PA field of SegCtl1 registersegcfg3PAUns32Set CFG3.PA field of SegCtl1 registersegcfg4PAUns32Set CFG4.PA field of SegCtl2 registersegcfg5PAUns32Set CFG5.PA field of SegCtl2 registersegcfg0AMUns32Set CFG0.AM field of SegCtl0 registersegcfg1AMUns32Set CFG1.AM field of SegCtl0 registersegcfg2AMUns32Set CFG2.AM field of SegCtl1 registersegcfg3AMUns32Set CFG3.AM field of SegCtl1 registersegcfg4AMUns32Set CFG4.AM field of SegCtl2 registersegcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 register	segcfg0PA	Uns32	Set CFG0.PA field of SegCtl0 register
segcfg3PAUns32Set CFG3.PA field of SegCtl1 registersegcfg4PAUns32Set CFG4.PA field of SegCtl2 registersegcfg5PAUns32Set CFG5.PA field of SegCtl2 registersegcfg0AMUns32Set CFG0.AM field of SegCtl0 registersegcfg1AMUns32Set CFG1.AM field of SegCtl0 registersegcfg2AMUns32Set CFG2.AM field of SegCtl1 registersegcfg3AMUns32Set CFG3.AM field of SegCtl1 registersegcfg4AMUns32Set CFG4.AM field of SegCtl2 registersegcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 register	segcfg1PA	Uns32	Set CFG1.PA field of SegCtl0 register
segcfg4PAUns32Set CFG4.PA field of SegCtl2 registersegcfg5PAUns32Set CFG5.PA field of SegCtl2 registersegcfg0AMUns32Set CFG0.AM field of SegCtl0 registersegcfg1AMUns32Set CFG1.AM field of SegCtl0 registersegcfg2AMUns32Set CFG2.AM field of SegCtl1 registersegcfg3AMUns32Set CFG3.AM field of SegCtl1 registersegcfg4AMUns32Set CFG4.AM field of SegCtl2 registersegcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 register	segcfg2PA	Uns32	Set CFG2.PA field of SegCtl1 register
segcfg5PAUns32Set CFG5.PA field of SegCtl2 registersegcfg0AMUns32Set CFG0.AM field of SegCtl0 registersegcfg1AMUns32Set CFG1.AM field of SegCtl0 registersegcfg2AMUns32Set CFG2.AM field of SegCtl1 registersegcfg3AMUns32Set CFG3.AM field of SegCtl1 registersegcfg4AMUns32Set CFG4.AM field of SegCtl2 registersegcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 register	segcfg3PA	Uns32	
segcfg0AMUns32Set CFG0.AM field of SegCtl0 registersegcfg1AMUns32Set CFG1.AM field of SegCtl0 registersegcfg2AMUns32Set CFG2.AM field of SegCtl1 registersegcfg3AMUns32Set CFG3.AM field of SegCtl1 registersegcfg4AMUns32Set CFG4.AM field of SegCtl2 registersegcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 register		Uns32	Set CFG4.PA field of SegCtl2 register
segcfg0AMUns32Set CFG0.AM field of SegCtl0 registersegcfg1AMUns32Set CFG1.AM field of SegCtl0 registersegcfg2AMUns32Set CFG2.AM field of SegCtl1 registersegcfg3AMUns32Set CFG3.AM field of SegCtl1 registersegcfg4AMUns32Set CFG4.AM field of SegCtl2 registersegcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 register	segcfg5PA	Uns32	
segcfg1AMUns32Set CFG1.AM field of SegCtl0 registersegcfg2AMUns32Set CFG2.AM field of SegCtl1 registersegcfg3AMUns32Set CFG3.AM field of SegCtl1 registersegcfg4AMUns32Set CFG4.AM field of SegCtl2 registersegcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl1 register		Uns32	Set CFG0.AM field of SegCtl0 register
segcfg2AMUns32Set CFG2.AM field of SegCtl1 registersegcfg3AMUns32Set CFG3.AM field of SegCtl1 registersegcfg4AMUns32Set CFG4.AM field of SegCtl2 registersegcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl1 register		Uns32	Set CFG1.AM field of SegCtl0 register
segcfg3AMUns32Set CFG3.AM field of SegCtl1 registersegcfg4AMUns32Set CFG4.AM field of SegCtl2 registersegcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl2 register	segcfg2AM	Uns32	Set CFG2.AM field of SegCtl1 register
segcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl2 register		Uns32	Set CFG3.AM field of SegCtl1 register
segcfg5AMUns32Set CFG5.AM field of SegCtl2 registersegcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl2 register			9 9
segcfg0EUUns32Set CFG0.EU field of SegCtl0 registersegcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl2 register			
segcfg1EUUns32Set CFG1.EU field of SegCtl0 registersegcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl2 register		Uns32	
segcfg2EUUns32Set CFG2.EU field of SegCtl1 registersegcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl2 register	segcfg1EU		
segcfg3EUUns32Set CFG3.EU field of SegCtl1 registersegcfg4EUUns32Set CFG4.EU field of SegCtl2 register		Uns32	
segcfg4EU Uns32 Set CFG4.EU field of SegCtl2 register			
segcfg5EU Uns32 Set CFG5.EU field of SegCtl2 register		Uns32	Set CFG4.EU field of SegCtl2 register
	segcfg5EU	Uns32	Set CFG5.EU field of SegCtl2 register

er (burs d RAN pad RAN set Kseg (set Use et Kseg2
d RAM oad RAM eet Kseg (set Use ot Kseg2
d RAM oad RAM oet Kseg (set Use ot Kseg2
d RAM oad RAM oet Kseg (set Use ot Kseg2
d RAM oad RAM oet Kseg (set Use ot Kseg2
d RAM oad RAM oet Kseg (set Use ot Kseg2
d RAM oad RAM oet Kseg (set Use ot Kseg2
d RAM oad RAM oet Kseg (set Use ot Kseg2
d RAM oad RAM oet Kseg (set Use ot Kseg2
d RAM oad RAM oet Kseg (set Use ot Kseg2
et Kseg  set Use  et Kseg2
et Kseg (set Use et Kseg2
et Kseg (set Use et Kseg2
et Kseg (set Use et Kseg2
(set Use et Kseg2
(set Use et Kseg2
et Kseg2
et Kseg2
_
_
ly/divid
15 / 41 / 14
vrite)
71100)
only)
ent)
6e ASE)
(y)
<u>y)</u>
y)
<i>y</i> )
)
C 3 (3 (1
of MMU
register
Counter
Counter ent)

config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.LPA
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
config3VZ	Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3.MSAP
config3CMGCR	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config 4.MMUConfig field (interpretation
Comigativity Comig	011302	depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.With ExtDer  Override Config4.VTLBSizeExt
config4V1LBSizeExt config4KScrExist		Override Config4.V1LBSizeExt Override Config4.KScrExist
	Uns32	9
config5EVA	Boolean	Override Config5.EVA
config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
mips32Macro	Boolean	Enables the MIPS32 SAVE and RESTORE macro
		instructions. Ignored if Config5.CA2 is not set)
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and
		MFHC0 instructions)
config5DEC	Boolean	Override Config5.DEC (to test Dual Endian Capa-
		bility)
config5GI	Uns32	Override Config5.GI (enable GINV)
config5CRCP	Boolean	Override Config5.CRCP (CRCP Present)
config5VP	Boolean	Override Config5.VP
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initializa-
		tion)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction
0011119	Boolean	cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (External-
Comigres	011302	ize sync)
config7WR	Boolean	Override Config7[31] bit (Alternative implementa-
comig/ wit	Doolean	tion of Watch registers)
config7FPR		Override Config7.FPR (one-half FPU clock ratio)
	Booloom	TO A CONTRACT OF A LANGE TO THE PROPERTY OF TH
aonfig7HCD	Boolean	
config7USP	Uns32	Override Config7.USP (USPRAM enable)
config7BTLM	Uns32 Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit
config7BTLM config7BusSlp	Uns32 Boolean Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit Override Config7.BusSlp bit
config7BTLM config7BusSlp config7IVAD	Uns32 Boolean Boolean Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit Override Config7.BusSlp bit Override Config7.IVAD bit
config7BTLM config7BusSlp config7IVAD config7RPS	Uns32 Boolean Boolean Boolean Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit Override Config7.BusSlp bit Override Config7.IVAD bit Override Config7.RPS bit
config7BTLM config7BusSlp config7IVAD config7RPS config7IAR_CPU0_VPE0	Uns32 Boolean Boolean Boolean Boolean Boolean Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit Override Config7.BusSlp bit Override Config7.IVAD bit Override Config7.RPS bit Override Config7.IAR bit for CPU0/VPE0
config7BTLM config7BusSlp config7IVAD config7RPS	Uns32 Boolean Boolean Boolean Boolean	Override Config7.USP (USPRAM enable) Override Config7.BTLM bit Override Config7.BusSlp bit Override Config7.IVAD bit Override Config7.RPS bit

config7IAR_CPU0_VPE3	Boolean	Override Config7.IAR bit for CPU0/VPE3
config7IAR_CPU1_VPE0	Boolean	Override Config7.IAR bit for CPU1/VPE0
config7IAR_CPU1_VPE1	Boolean	Override Config7.IAR bit for CPU1/VPE1
config7IAR_CPU1_VPE2	Boolean	Override Config7.IAR bit for CPU1/VPE2
config7IAR_CPU1_VPE3	Boolean	Override Config7.IAR bit for CPU1/VPE3
config7IAR_CPU2_VPE0	Boolean	Override Config7.IAR bit for CPU2/VPE0
config7IAR_CPU2_VPE1	Boolean	Override Config7.IAR bit for CPU2/VPE1
config7IAR_CPU2_VPE2	Boolean	Override Config7.IAR bit for CPU2/VPE2
config7IAR_CPU2_VPE3	Boolean	Override Config7.IAR bit for CPU2/VPE3
config7IAR_CPU3_VPE0	Boolean	Override Config7.IAR bit for CPU3/VPE0
config7IAR_CPU3_VPE1	Boolean	Override Config7.IAR bit for CPU3/VPE1
config7IAR_CPU3_VPE2	Boolean	Override Config7.IAR bit for CPU3/VPE2
config7IAR_CPU3_VPE3	Boolean	Override Config7.IAR bit for CPU3/VPE3
config7IAR_CPU4_VPE0	Boolean	Override Config7.IAR bit for CPU4/VPE0
config7IAR_CPU4_VPE1	Boolean	Override Config7.IAR bit for CPU4/VPE1
config7IAR_CPU4_VPE2	Boolean	Override Config7.IAR bit for CPU4/VPE2
config7IAR_CPU4_VPE3	Boolean	Override Config7.IAR bit for CPU4/VPE3
config7IAR_CPU5_VPE0	Boolean	Override Config7.IAR bit for CPU5/VPE0
config7IAR_CPU5_VPE1	Boolean	Override Config7.IAR bit for CPU5/VPE1
config7IAR_CPU5_VPE2	Boolean	Override Config7.IAR bit for CPU5/VPE2
config7IAR_CPU5_VPE3	Boolean	Override Config7.IAR bit for CPU5/VPE3
config7IAR_CPU6_VPE0	Boolean	Override Config7.IAR bit for CPU6/VPE0
config7IAR_CPU6_VPE1	Boolean	Override Config7.IAR bit for CPU6/VPE1
config7IAR_CPU6_VPE2	Boolean	Override Config7.IAR bit for CPU6/VPE2
config7IAR_CPU6_VPE3	Boolean	Override Config7.IAR bit for CPU6/VPE3
config7IAR_CPU7_VPE0	Boolean	Override Config7.IAR bit for CPU7/VPE0
config7IAR_CPU7_VPE1	Boolean	Override Config7.IAR bit for CPU7/VPE1
config7IAR_CPU7_VPE2	Boolean	Override Config7.IAR bit for CPU7/VPE2
config7IAR_CPU7_VPE3	Boolean	Override Config7.IAR bit for CPU7/VPE3
config7IVAD_CPU0_VPE0	Boolean	Override Config7.IVAD bit for CPU0/VPE0
config7IVAD_CPU0_VPE1	Boolean	Override Config7.IVAD bit for CPU0/VPE1
config7IVAD_CPU0_VPE2	Boolean	Override Config7.IVAD bit for CPU0/VPE2
config7IVAD_CPU0_VPE3	Boolean	Override Config7.IVAD bit for CPU0/VPE3
config7IVAD_CPU1_VPE0	Boolean	Override Config7.IVAD bit for CPU1/VPE0
config7IVAD_CPU1_VPE1	Boolean	Override Config7.IVAD bit for CPU1/VPE1
config7IVAD_CPU1_VPE2	Boolean	Override Config7.IVAD bit for CPU1/VPE2
config7IVAD_CPU1_VPE3	Boolean	Override Config7.IVAD bit for CPU1/VPE3
config7IVAD_CPU2_VPE0	Boolean	Override Config7.IVAD bit for CPU2/VPE0
config7IVAD_CPU2_VPE1	Boolean	Override Config7.IVAD bit for CPU2/VPE1
config7IVAD_CPU2_VPE2	Boolean	Override Config7.IVAD bit for CPU2/VPE2
config7IVAD_CPU2_VPE3	Boolean	Override Config7.IVAD bit for CPU2/VPE3
config7IVAD_CPU3_VPE0	Boolean	Override Config7.IVAD bit for CPU3/VPE0
config7IVAD_CPU3_VPE1	Boolean	Override Config7.IVAD bit for CPU3/VPE1
config7IVAD_CPU3_VPE2	Boolean	Override Config7.IVAD bit for CPU3/VPE2
config7IVAD_CPU3_VPE3	Boolean	Override Config7.IVAD bit for CPU3/VPE3
config7IVAD_CPU4_VPE0	Boolean	Override Config7.IVAD bit for CPU4/VPE0
config7IVAD_CPU4_VPE1	Boolean	Override Config7.IVAD bit for CPU4/VPE1
config7IVAD_CPU4_VPE2	Boolean	Override Config7.IVAD bit for CPU4/VPE2
config7IVAD_CPU4_VPE3	Boolean	Override Config7.IVAD bit for CPU4/VPE3
config7IVAD_CPU5_VPE0	Boolean	Override Config7.IVAD bit for CPU5/VPE0
config7IVAD_CPU5_VPE1	Boolean	Override Config7.IVAD bit for CPU5/VPE1
config7IVAD_CPU5_VPE2	Boolean	Override Config7.IVAD bit for CPU5/VPE2
config7IVAD_CPU5_VPE3	Boolean	Override Config7.IVAD bit for CPU5/VPE3
config7IVAD_CPU6_VPE0	Boolean	Override Config7.IVAD bit for CPU6/VPE0
config7IVAD_CPU6_VPE1	Boolean	Override Config7.IVAD bit for CPU6/VPE1
config7IVAD_CPU6_VPE2	Boolean	Override Config7.IVAD bit for CPU6/VPE2
0		1

C FINAD CDUC VIDEO	D 1	
config7IVAD_CPU6_VPE3	Boolean	Override Config7.IVAD bit for CPU6/VPE3
config7IVAD_CPU7_VPE0	Boolean	Override Config7.IVAD bit for CPU7/VPE0
config7IVAD_CPU7_VPE1	Boolean	Override Config7.IVAD bit for CPU7/VPE1
config7IVAD_CPU7_VPE2	Boolean	Override Config7.IVAD bit for CPU7/VPE2
config7IVAD_CPU7_VPE3	Boolean	Override Config7.IVAD bit for CPU7/VPE3
config7RPS_CPU0_VPE0	Boolean	Override Config7.RPS bit for CPU0/VPE0
config7RPS_CPU0_VPE1	Boolean	Override Config7.RPS bit for CPU0/VPE1
config7RPS_CPU0_VPE2	Boolean	Override Config7.RPS bit for CPU0/VPE2
config7RPS_CPU0_VPE3	Boolean	Override Config7.RPS bit for CPU0/VPE3
config7RPS_CPU1_VPE0	Boolean	Override Config7.RPS bit for CPU1/VPE0
config7RPS_CPU1_VPE1	Boolean	Override Config7.RPS bit for CPU1/VPE1
config7RPS_CPU1_VPE2	Boolean	Override Config7.RPS bit for CPU1/VPE2
config7RPS_CPU1_VPE3	Boolean	Override Config7.RPS bit for CPU1/VPE3
config7RPS_CPU2_VPE0	Boolean	Override Config7.RPS bit for CPU2/VPE0
config7RPS_CPU2_VPE1	Boolean	Override Config7.RPS bit for CPU2/VPE1
config7RPS_CPU2_VPE2	Boolean	Override Config7.RPS bit for CPU2/VPE2
config7RPS_CPU2_VPE3	Boolean	Override Config7.RPS bit for CPU2/VPE3
config7RPS_CPU3_VPE0	Boolean	Override Config7.RPS bit for CPU3/VPE0
config7RPS_CPU3_VPE1	Boolean	Override Config7.RPS bit for CPU3/VPE1
config7RPS_CPU3_VPE2	Boolean	Override Config7.RPS bit for CPU3/VPE2
config7RPS_CPU3_VPE3	Boolean	Override Config7.RPS bit for CPU3/VPE3
config7RPS_CPU4_VPE0	Boolean	Override Config7.RPS bit for CPU4/VPE0
config7RPS_CPU4_VPE1	Boolean	Override Config7.RPS bit for CPU4/VPE1
config7RPS_CPU4_VPE2	Boolean	Override Config7.RPS bit for CPU4/VPE2
config7RPS_CPU4_VPE3	Boolean	Override Config7.RPS bit for CPU4/VPE3
config7RPS_CPU5_VPE0	Boolean	Override Config7.RPS bit for CPU5/VPE0
config7RPS_CPU5_VPE1	Boolean	Override Config7.RPS bit for CPU5/VPE1
config7RPS_CPU5_VPE2	Boolean	Override Config7.RPS bit for CPU5/VPE2
config7RPS_CPU5_VPE3	Boolean	Override Config7.RPS bit for CPU5/VPE3
config7RPS_CPU6_VPE0	Boolean	1
		Override Config7.RPS bit for CPU6/VPE0
config7RPS_CPU6_VPE1	Boolean	Override Config7.RPS bit for CPU6/VPE1
config7RPS_CPU6_VPE2	Boolean	Override Config7.RPS bit for CPU6/VPE2
config7RPS_CPU6_VPE3	Boolean	Override Config7.RPS bit for CPU6/VPE3
config7RPS_CPU7_VPE0	Boolean	Override Config7.RPS bit for CPU7/VPE0
config7RPS_CPU7_VPE1	Boolean	Override Config7.RPS bit for CPU7/VPE1
config7RPS_CPU7_VPE2	Boolean	Override Config7.RPS bit for CPU7/VPE2
config7RPS_CPU7_VPE3	Boolean	Override Config7.RPS bit for CPU7/VPE3
statusFR	Boolean	Override power on value in Status.FR (Floating
		point register mode)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant
		with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings
		match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
srsconf0SRS1	Uns32	Override the SRS1 field in SRSConf0 register
srsconf0SRS2	Uns32	Override the SRS2 field in SRSConf0 register
srsconf0SRS3	Uns32	Override the SRS3 field in SRSConf0 register
wiredLimit	Uns32	Override Limit field of the Wired register
wiredLimitBits	Uns32	Override width of Limit field of the Wired register
wiredWiredBits	Uns32	Override width of Wired field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
parityEnable	Uns32	Specify error detection support: 0 - none; 1 - parity;
•		2 - ECC
useMpTb	Boolean	Override Use of multi-processor test bench
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use
	0.11002	GCR_Cx_RESET_BASE on CMP processors)

UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the cor-
UseExceptionBase	Boolean	responding BEV address bits
11BufferCache	Boolean	L1 Buffer Cache
GCU_EX	Boolean	CMP system only: GCR custom block present
GIC.EX	Boolean	CMP system only: GCR custom block present  CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: GPC unit present  CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable
SWINT-ROUTABLE	Boolean	within cluster
PERFCNT_ROUTABLE	Boolean	CMP system only: performance counter interrupt
1 ERFONT HOUTABLE	Doolean	routable within cluster
FDC_ROUTABLE	Boolean	CMP system only: fast debug channel interrupt
1 DOI(OO IMBEE	Boolean	routable within cluster
GCR_PCORES	Uns32	CMP system only: override
	011502	GCR_CONFIG.PCORES (number of cores-1)
GCR_ADDR_REGIONS	Uns32	CMP system only: override
001011111111111111111111111111111111111	011502	GCR_CONFIG.ADDR_REGIONS (number of
		MMIO address regions)
GCR_NUMAUX	Uns32	CMP system only: override
	0 0 -	GCR_CONFIG.NUMAUX (number of auxil-
		iary memory ports)
GCR_BASE	Uns64	CMP system only: override
0.010_5110_5	011001	GCR_BASE.GCR_BASE (default GCR regis-
		ter address)
GCR_MINOR_REV	Uns32	CMP system only: override
GOILLIII (OILLI)	011502	GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override
GOIL-IVIII OIL-ILLI V	011302	GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override
GOIL-OIL-OIL-OIL-IVE V	011502	GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override
0 010=01101115=11110 010=10=1	011502	GCR_CACHE_REV.MAJOR_REV
GCR_L2_ASSOC	Uns32	CMP system only: override
		GCR_L2_CONFIG.ASSOC
GCR_L2_SET_SIZE	Uns32	CMP system only: override
		GCR_L2_CONFIG.SET_SIZE
GCR_SYS_CONFIG2_MAX_VP_WIDTH	Uns32	CMP system only: override
		GCR_SYS_CONFIG2.MAX_VP_WIDTH
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override
		GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override
		GCR_IOCU1_REV.MAJOR_REV
GCR_BEV_BASE	Uns32	CMP system only: override GCR_BEV_BASE
GCR_KX_BASE_MODE	Boolean	CMP system only: override BEV_BASE_MODE &
		RESET_BASE_MODE
GCR_MMIO_REQ_LIMIT	Uns32	CMP system only: override
•		GCR_MMIO_REQ_LIMIT.MMIO_REQ_LIMIT
		value
GCR_MMIO0_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO0_BOTTOM register value
GCR_MMIO0_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO0_TOP.TOP_ADDR value
		GOIL-WIWIOU-1 OI . 1 OI -ADDIT value
GCR_MMIO1_BOTTOM	Uns64	CMP system only: override
GCR_MMIO1_BOTTOM	Uns64	
GCR_MMIO1_BOTTOM GCR_MMIO1_TOP_ADDR	Uns64 Uns32	CMP system only: override

GCR_MMIO2_BOTTOM	Uns64	CMP system only: override GCR_MMIO2_BOTTOM register value
GCR_MMIO2_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO2_TOP.TOP_ADDR value
GCR_MMIO3_BOTTOM	Uns64	CMP system only: override GCR_MMIO3_BOTTOM register value
GCR_MMIO3_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO3_TOP.TOP_ADDR value
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override GIC_SH_DBG_CONFIG.NUM_TEAMS
GIC_TRIG_RESET	Uns32	CMP system only: Zero value of GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
gicVirtualVPNum_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
gicVirtualVPNum_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
gicVirtualVPNum_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
gicVirtualVPNum_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3

gicVirtualVPNum_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
gicVirtualVPNum_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
gicVirtualVPNum_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
gicVirtualVPNum_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
gicVirtualVPNum_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
gicVirtualVPNum_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
gicVirtualVPNum_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
gicVirtualVPNum_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
gicVirtualVPNum_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
gicVirtualVPNum_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
gicVirtualVPNum_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
gicVirtualVPNum_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
gicVirtualVPNum_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
gicVirtualVPNum_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
gicVirtualVPNum_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
gicVirtualVPNum_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
gicVirtualVPNum_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
gicVirtualVPNum_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
gicVirtualVPNum_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
gicVirtualVPNum_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
gicVirtualVPNum_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
gicVirtualVPNum_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
gicVirtualVPNum_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
gicVirtualVPNum_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
gicVirtualVPNum_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
gicVirtualVPNum_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
gicVirtualVPNum_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
gicVirtualVPNum_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3

CCD CO DECET DACE	11 00	CMD 1 CCD CL DECETE DAGE C
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GCR_CI_RESEI_DASE	Ulis52	core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GCR-C2-RESET-DASE	Ulisaz	core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
GORLOGIRESETEBASE	Clis52	core 3
GCR_C4_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
	011502	core 4
GCR_C5_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
	011502	core 5
GCR_C6_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
	0 0 -	core 6
GCR_C7_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
		core 7
GCR_C8_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
		core 8
GCR_C9_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for
		core 9
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 3
GCR_C4_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 4
GCR_C5_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 5
GCR_C6_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
	77 00	for core 6
GCR_C7_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GOD GO DEGET DVD DAGE	77 00	for core 7
GCR_C8_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
CCD CO DECET DVT DAGE	11 99	for core 8
GCR_C9_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
CDC CO VD EN	II20	for core 9
CPC_C0_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 0
CPC_C1_VP_EN CPC_C2_VP_EN	Uns32 Uns32	CMP system only: CPC_VP_EN for core 1 CMP system only: CPC_VP_EN for core 2
CPC_C2_VP_EN CPC_C3_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 2  CMP system only: CPC_VP_EN for core 3
CPC_C3_VP_EN CPC_C4_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 3  CMP system only: CPC_VP_EN for core 4
CPC_C4_VP_EN CPC_C5_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 4  CMP system only: CPC_VP_EN for core 5
CPC_C5_VP_EN CPC_C6_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 5  CMP system only: CPC_VP_EN for core 6
CPC_C6_VP_EN CPC_C7_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 6  CMP system only: CPC_VP_EN for core 7
CPC_C7_VP_EN CPC_C8_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 7  CMP system only: CPC_VP_EN for core 8
CPC_C8_VP_EN CPC_C9_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 9
EIC_OPTION	Uns32	Override the external interrupt controller
EIO-OF HON	UIIS32	EIC_OPTION EIC_OPTION
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the KI field in GuestCtl0 register  Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the MC field in GuestCtl0 register  Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the CFO field in GuestCtlO register  Override the AT field in GuestCtlO register
guesi CiloA1	Ulisaz	Override the A1 heid in GuestOtio tegistet.

guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest II TI held in IntCtl register  Override the Guest IPFDC field in IntCtl register
guestintetIIPPCI	Uns32	Override the Guest IPFDC field in IntCtl register  Override the Guest IPPCI field in IntCtl register
guestintctIFFCI guestintctIPTI_CPU0_VP0	Uns32	
		Override the IPTI field in IntCtl register for CPU0/VP0
guestintctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
guestintctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
guestintctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
guestintctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
guestintctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
guestintctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
guestintctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
guestintctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
guestintctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
guestintctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
guestintctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
guestintctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
guestintctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
guestintctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
guestintctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
guestintctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
guestintctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
guestintctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
guestintctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
guestintctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
guestintctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1

guestintctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
guestintctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
guestintctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
guestintctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
guestintctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
guestintctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
guestintctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
guestintctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
guestintctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
guestintctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
guestintctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
guestintctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
guestintctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
guestintctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
guestintctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
guestintctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
guestintctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
guestintctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
guestintctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
guestintctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
guestintctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
guestintctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
guestintctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
guestintctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
guestintctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
guestintctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
guestintctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
guestintctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1

guestintctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
guestintctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
guestintctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
guestintctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
guestintctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
guestintctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
guestintctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
guestintctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
guestintctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
guestintctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
guestintctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
guestintctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
guestintctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
guestintctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
guestintctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
guestintctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
guestintctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
guestintctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
guestintctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
guestintctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
guestintctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
guestintctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
guestintctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
guestintctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
guestintctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
guestintctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
guestintctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
guestintctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1

guestintctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for
		CPU3/VP2
guestintctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
guestintctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
guestintctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
guestintctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
guestintctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
guestintctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
guestintctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
guestintctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
guestintctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
guestintctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
guestintctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
guestintctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
guestintctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
guestintctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
guestintctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
guestintctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
guestintctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2( <ispram bytes="" in="" size="">) - 11)</ispram>
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2( <dspram bytes="" in="" size="">) - 11)</dspram>
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag
		(used to enable the DSPRAM region prior to reset)
DSPRAM_PRESENT	Boolean	DSPRAM is present with SAAR
USPRAM_SIZE	Uns32	Encoded size of the USPRAM region (log2( <uspram bytes="" in="" size="">) - 11)</uspram>
USPRAM_BASE	Uns64	Starting physical address of the USPRAM region
USPRAM_ENABLE	Boolean	Set the enable bit of the USPRAM region's tag
		(used to enable the USPRAM region prior to reset)

USPRAM_FILE	String	Load a MIPS hex file into the USPRAM region		
		prior to reset		
misaligned Data Exception	Enumeration	Select misaligned data access exception signaling: never, checkCCA or always (never, checkCCA or		
		always)		
commitTlbwErr	Boolean	Commit TLBWI/TLBRI on ECC; in		
		MIPS_DV_MODE only		

Table 8.1: Parameters that can be set in: CMP

## 8.1 Parameter values

These are the current parameter values.

Name	Value
(Others)	
variant	MIPS64R6
endian	none
cacheenable	default
cachedebug	0
cacheextbiuinfo	0x0
mipsHexFile	
IMPERAS_MIPS_AVP_OPCODES	F
cacheIndexBypassTLB	F
MIPS_TRACE	F
gprNames	F
supervisorMode	F
busErrors	Т
fixedMMU	F
fixedDbgRegSize	F
removeDSP	F
removeCMP	F
removeFP	F
removeFTLB	F
isISA	F
hiddenTLBentries	F
perfCounters	0
ITCNumEntries	0
ITCNumFIFO	0
ITCFIFODepth	0
ITCEmptyOnReset	F
MTFPU	0
supportDenormals	F
VPE0MaxTC	0
VPE1MaxTC	0
segBits	0
mpuRegions	0
mpuType	0

mpuEnable	F
mpuSegment0	0
mpuSegment1	0
mpuSegment2	0
mpuSegment3	0
mpuSegment4	0
mpuSegment5	0
mpuSegment6	0
mpuSegment7	0
mpuSegment8	0
mpuSegment9	0
mpuSegment10	0
mpuSegment11	0
mpuSegment12	0
mpuSegment13	0
mpuSegment14	0
mpuSegment15	0
mvpconf0vpe	0
tcDisable	0
vpeDisable	0
mvpconf0tc	0
mvpconf0pcp	F
mvpconf0tcp	F
mvpconf1c1f	F
mvpcontrolPolicyMode	F
hasFDC	0
licenseWarningDays	15
MIPS_UHI	F
mipsUhiArgs	
mipsUhiJail	
MIPS_DV_MODE	F
MIPS_MAGIC_OPCODES	F
enableTrickbox	F
fpuexcdisable	F
TRU_PRESENT	F
ucLLwordsLocked	0
FUSA	F
CPC_FAULT_SUPPORTED	0
CPC_FAULT_ENABLE	0
cop2Bits	32
cop2FileName	
udiConfig	0
udiFileName	-
vectoredinterrupt	F
externalinterrupt	F

configNEIC VDEO	F
config3VEIC_VPE0	
config3VEIC_VPE1	F
config3VEIC_VPE2	F
config3VEIC_VPE3	F
rootFixedMMU	F
rootMMUSizeM1	0
srsctlHSS	0
firPS	0
firHas2008	0
usePreciseFpu	0
simulateLite	NONE
pridCompanyOptions	0
pridRevision	0
globalClusterNum	0
intctlIPTI	0
intctlIPFDC	0
intctlIPPCI	0
numWatch	0
maxVP	0
numVP	0
numVPtoStart	0
sharedTLBindex	0
xconfigSpecified	F
intctllPTI_CPU0_VP0	0
intctlIPTI_CPU0_VP1	0
intctlIPTI_CPU0_VP2	0
intctllPTI_CPU0_VP3	0
intetlIPTI_CPU1_VP0	0
intetlIPTI_CPU1_VP1	0
intetlIPTI_CPU1_VP2	0
intctllPTI_CPU1_VP3	0
intctllPTI_CPU2_VP0	0
intctllPTI_CPU2_VP1	0
intctllPTI_CPU2_VP2	0
intetliPTI_CPU2_VP3	0
intctllPTI_CPU3_VP0	0
intctllPTI_CPU3_VP1	0
intctllPTI_CPU3_VP2	-
	0
intctlIPTI_CPU3_VP3	0
intctlIPTI_CPU4_VP0	0
intctlIPTI_CPU4_VP1	0
intctlIPTI_CPU4_VP2	0
intctlIPTI_CPU4_VP3	0
intctlIPTI_CPU5_VP0	0
intctlIPTI_CPU5_VP1	0

intctlIPTLCPU5.VP3         0           intctlIPTLCPU6.VP0         0           intctlIPTLCPU6.VP1         0           intctlIPTLCPU6.VP2         0           intctlIPTLCPU6.VP3         0           intctlIPTLCPU7.VP0         0           intctlIPTLCPU7.VP1         0           intctlIPTLCPU7.VP2         0           intctlIPTLCPU7.VP3         0           intctlIPTDC.CPU0.VP0         0           intctlIPFDC.CPU0.VP1         0           intctlIPFDC.CPU0.VP2         0           intctlIPFDC.CPU0.VP3         0           intctlIPFDC.CPU1.VP0         0           intctlIPFDC.CPU1.VP1         0           intctlIPFDC.CPU1.VP2         0           intctlIPFDC.CPU1.VP3         0           intctlIPFDC.CPU1.VP3         0           intctlIPFDC.CPU2.VP0         0           intctlIPFDC.CPU2.VP1         0           intctlIPFDC.CPU2.VP2         0           intctlIPFDC.CPU2.VP3         0           intctlIPFDC.CPU3.VP0         0           intctlIPFDC.CPU3.VP1         0           intctlIPFDC.CPU3.VP2         0           intctlIPFDC.CPU3.VP3         0           intctlIPFDC.CPU4.VP3         0	L. JIDEL ODIK UDA	
intetlIPTI_CPU6_VP0 intetlIPTI_CPU6_VP2 intetlIPTI_CPU6_VP2 intetlIPTI_CPU7_VP0 intetlIPTI_CPU7_VP0 intetlIPTI_CPU7_VP1 intetlIPTI_CPU7_VP1 intetlIPTI_CPU7_VP2 intetlIPTI_CPU7_VP2 intetlIPTI_CPU7_VP3 intetlIPTI_CPU7_VP3 intetlIPTDC_CPU0_VP0 intetlIPFDC_CPU0_VP0 intetlIPFDC_CPU0_VP1 intetlIPFDC_CPU0_VP2 intetlIPFDC_CPU1_VP0 intetlIPFDC_CPU1_VP0 intetlIPFDC_CPU1_VP0 intetlIPFDC_CPU1_VP1 intetlIPFDC_CPU1_VP2 intetlIPFDC_CPU1_VP3 intetlIPFDC_CPU1_VP3 intetlIPFDC_CPU2_VP0 intetlIPFDC_CPU2_VP0 intetlIPFDC_CPU2_VP0 intetlIPFDC_CPU2_VP1 intetlIPFDC_CPU3_VP2 intetlIPFDC_CPU3_VP2 intetlIPFDC_CPU3_VP0 intetlIPFDC_CPU3_VP0 intetlIPFDC_CPU3_VP1 intetlIPFDC_CPU3_VP1 intetlIPFDC_CPU3_VP2 intetlIPFDC_CPU3_VP3 intetlIPFDC_CPU4_VP0 intetlIPFDC_CPU4_VP0 intetlIPFDC_CPU4_VP0 intetlIPFDC_CPU4_VP1 intetlIPFDC_CPU4_VP2 intetlIPFDC_CPU4_VP2 intetlIPFDC_CPU4_VP3 intetlIPFDC_CPU5_VP0 intetlIPFDC_CPU5_VP1 intetlIPFDC_CPU5_VP1 intetlIPFDC_CPU5_VP2 intetlIPFDC_CPU5_VP3 intetlIPFDC_CPU5_VP4	intctlIPTI_CPU5_VP2	0
intetlIPTI_CPU6_VP2 intetlIPTI_CPU6_VP3 intetlIPTI_CPU7_VP0 intetlIPTI_CPU7_VP0 intetlIPTI_CPU7_VP1 intetlIPTI_CPU7_VP1 intetlIPTI_CPU7_VP2 intetlIPTI_CPU7_VP2 intetlIPTI_CPU7_VP3 intetlIPTD_CPU0_VP0 intetlIPTDC_CPU0_VP0 intetlIPFDC_CPU0_VP1 intetlIPFDC_CPU0_VP2 intetlIPFDC_CPU0_VP3 intetlIPFDC_CPU1_VP0 intetlIPFDC_CPU1_VP0 intetlIPFDC_CPU1_VP1 intetlIPFDC_CPU1_VP2 intetlIPFDC_CPU1_VP2 intetlIPFDC_CPU1_VP3 intetlIPFDC_CPU2_VP0 intetlIPFDC_CPU2_VP0 intetlIPFDC_CPU2_VP1 intetlIPFDC_CPU2_VP2 intetlIPFDC_CPU2_VP3 intetlIPFDC_CPU3_VP0 intetlIPFDC_CPU3_VP0 intetlIPFDC_CPU3_VP0 intetlIPFDC_CPU3_VP1 intetlIPFDC_CPU3_VP1 intetlIPFDC_CPU3_VP2 intetlIPFDC_CPU3_VP3 intetlIPFDC_CPU3_VP3 intetlIPFDC_CPU4_VP0 intetlIPFDC_CPU4_VP0 intetlIPFDC_CPU4_VP0 intetlIPFDC_CPU4_VP1 intetlIPFDC_CPU4_VP2 intetlIPFDC_CPU4_VP2 intetlIPFDC_CPU5_VP0 intetlIPFDC_CPU5_VP0 intetlIPFDC_CPU5_VP0 intetlIPFDC_CPU5_VP1 intetlIPFDC_CPU5_VP2 intetlIPFDC_CPU5_VP3 intetlIPFDC_CPU5_VP0 intetlIPFDC_CPU5_VP		
intetlIPTI_CPU6_VP2 intetlIPTI_CPU7_VP0 intetlIPTI_CPU7_VP1 intetlIPTI_CPU7_VP1 intetlIPTI_CPU7_VP2 intetlIPTI_CPU7_VP3 intetlIPTI_CPU7_VP3 intetlIPTI_CPU7_VP3 intetlIPTDC_CPU0_VP0 intetlIPFDC_CPU0_VP0 intetlIPFDC_CPU0_VP1 intetlIPFDC_CPU0_VP2 intetlIPFDC_CPU1_VP3 intetlIPFDC_CPU1_VP0 intetlIPFDC_CPU1_VP0 intetlIPFDC_CPU1_VP1 intetlIPFDC_CPU1_VP2 intetlIPFDC_CPU1_VP3 intetlIPFDC_CPU1_VP3 intetlIPFDC_CPU2_VP0 intetlIPFDC_CPU2_VP0 intetlIPFDC_CPU2_VP1 intetlIPFDC_CPU2_VP2 intetlIPFDC_CPU3_VP0 intetlIPFDC_CPU3_VP0 intetlIPFDC_CPU3_VP1 intetlIPFDC_CPU3_VP1 intetlIPFDC_CPU3_VP2 intetlIPFDC_CPU3_VP2 intetlIPFDC_CPU3_VP3 intetlIPFDC_CPU3_VP3 intetlIPFDC_CPU4_VP0 intetlIPFDC_CPU4_VP0 intetlIPFDC_CPU4_VP1 intetlIPFDC_CPU4_VP2 intetlIPFDC_CPU4_VP3 intetlIPFDC_CPU4_VP3 intetlIPFDC_CPU4_VP3 intetlIPFDC_CPU5_VP0 intetlIPFDC_CPU5_VP0 intetlIPFDC_CPU5_VP0 intetlIPFDC_CPU5_VP0 intetlIPFDC_CPU6_VP2 intetlIPFDC_CPU6_VP3 intetlIPFDC_CPU6_VP3 intetlIPFDC_CPU6_VP0 intetlIPFDC_CPU6_VP0 intetlIPFDC_CPU6_VP0 intetlIPFDC_CPU6_VP2 intetlIPFDC_CPU6_VP3 intetlIPFDC_CPU6_VP3 intetlIPFDC_CPU7_VP0 intetlIPFDC_CPU7_		
intctlIPTLCPU6_VP3         0           intctlIPTLCPU7_VP0         0           intctlIPTLCPU7_VP1         0           intctlIPTLCPU7_VP2         0           intctlIPTLCPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU0_VP3         0           intctlIPFDC_CPU1_VP0         0           intctlIPFDC_CPU1_VP1         0           intctlIPFDC_CPU1_VP2         0           intctlIPFDC_CPU1_VP3         0           intctlIPFDC_CPU1_VP3         0           intctlIPFDC_CPU1_VP3         0           intctlIPFDC_CPU2_VP0         0           intctlIPFDC_CPU2_VP1         0           intctlIPFDC_CPU2_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU3_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP1         0		
intctlIPTL.CPU7.VP0 intctlIPTL.CPU7.VP1 intctlIPTL.CPU7.VP2 intctlIPTL.CPU7.VP3 intctlIPFDC.CPU0.VP0 intctlIPFDC.CPU0.VP0 intctlIPFDC.CPU0.VP1 intctlIPFDC.CPU0.VP2 intctlIPFDC.CPU0.VP3 intctlIPFDC.CPU1.VP0 intctlIPFDC.CPU1.VP0 intctlIPFDC.CPU1.VP1 intctlIPFDC.CPU1.VP2 intctlIPFDC.CPU1.VP3 intctlIPFDC.CPU1.VP3 intctlIPFDC.CPU1.VP3 intctlIPFDC.CPU2.VP0 intctlIPFDC.CPU2.VP0 intctlIPFDC.CPU2.VP1 intctlIPFDC.CPU3.VP0 intctlIPFDC.CPU3.VP0 intctlIPFDC.CPU3.VP1 intctlIPFDC.CPU3.VP2 intctlIPFDC.CPU3.VP3 intctlIPFDC.CPU3.VP3 intctlIPFDC.CPU4.VP0 intctlIPFDC.CPU4.VP0 intctlIPFDC.CPU4.VP1 intctlIPFDC.CPU4.VP2 intctlIPFDC.CPU4.VP3 intctlIPFDC.CPU4.VP0 intctlIPFDC.CPU4.VP0 intctlIPFDC.CPU4.VP0 intctlIPFDC.CPU5.VP0 intctlIPFDC.CPU5.VP0 intctlIPFDC.CPU5.VP0 intctlIPFDC.CPU5.VP2 intctlIPFDC.CPU6.VP0 intctlIPFDC.CPU6.VP0 intctlIPFDC.CPU6.VP0 intctlIPFDC.CPU6.VP0 intctlIPFDC.CPU6.VP0 intctlIPFDC.CPU6.VP0 intctlIPFDC.CPU6.VP0 intctlIPFDC.CPU7.VP0 intctlIPFDC.C		0
intctlIPTLCPU7_VP1         0           intctlIPTLCPU7_VP3         0           intctlIPTLCPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU1_VP0         0           intctlIPFDC_CPU1_VP0         0           intctlIPFDC_CPU1_VP1         0           intctlIPFDC_CPU1_VP2         0           intctlIPFDC_CPU1_VP3         0           intctlIPFDC_CPU1_VP3         0           intctlIPFDC_CPU2_VP0         0           intctlIPFDC_CPU2_VP1         0           intctlIPFDC_CPU2_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU3_VP0         0           intctlIPFDC_CPU3_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP0         0           intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP2         0 <td></td> <td>0</td>		0
intctlIPTI_CPU7_VP2         0           intctlIPTI_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0           intctlIPFDC_CPU0_VP1         0           intctlIPFDC_CPU0_VP2         0           intctlIPFDC_CPU1_VP0         0           intctlIPFDC_CPU1_VP1         0           intctlIPFDC_CPU1_VP2         0           intctlIPFDC_CPU1_VP3         0           intctlIPFDC_CPU2_VP0         0           intctlIPFDC_CPU2_VP1         0           intctlIPFDC_CPU2_VP2         0           intctlIPFDC_CPU2_VP3         0           intctlIPFDC_CPU3_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU3_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP0         0           intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0		0
intetlIPTI.CPU7.VP3 intetlIPFDC.CPU0.VP0 intetlIPFDC.CPU0.VP1 intetlIPFDC.CPU0.VP2 intetlIPFDC.CPU0.VP3 intetlIPFDC.CPU1.VP0 intetlIPFDC.CPU1.VP0 intetlIPFDC.CPU1.VP1 intetlIPFDC.CPU1.VP2 intetlIPFDC.CPU1.VP3 intetlIPFDC.CPU1.VP3 intetlIPFDC.CPU2.VP0 intetlIPFDC.CPU2.VP1 intetlIPFDC.CPU2.VP2 intetlIPFDC.CPU2.VP3 intetlIPFDC.CPU2.VP3 intetlIPFDC.CPU3.VP0 intetlIPFDC.CPU3.VP0 intetlIPFDC.CPU3.VP1 intetlIPFDC.CPU3.VP2 intetlIPFDC.CPU3.VP3 intetlIPFDC.CPU3.VP3 intetlIPFDC.CPU4.VP0 intetlIPFDC.CPU4.VP0 intetlIPFDC.CPU4.VP1 intetlIPFDC.CPU4.VP2 intetlIPFDC.CPU4.VP3 intetlIPFDC.CPU4.VP3 intetlIPFDC.CPU5.VP0 intetlIPFDC.CPU5.VP0 intetlIPFDC.CPU5.VP1 intetlIPFDC.CPU5.VP2 intetlIPFDC.CPU5.VP3 intetlIPFDC.CPU6.VP0 intetlIPFDC.CPU6.VP0 intetlIPFDC.CPU6.VP0 intetlIPFDC.CPU6.VP1 intetlIPFDC.CPU6.VP2 intetlIPFDC.CPU6.VP3 intetlIPFDC.CPU6.VP3 intetlIPFDC.CPU6.VP3 intetlIPFDC.CPU6.VP3 intetlIPFDC.CPU7.VP0 intetlIPFDC.CPU7.VP0 intetlIPFDC.CPU7.VP0 intetlIPFDC.CPU7.VP1 intetlIPFDC.CPU7.VP2 intetlIPFDC.CPU7.VP3 intetlIPFDC.CPU7.VP3 intetlIPPCL.CPU0.VP0 intetlIPPCL.CPU0.VP0 intetlIPPCL.CPU0.VP0 intetlIPPCL.CPU0.VP0 intetlIPPCL.CPU0.VP0 intetlIPPCL.CPU0.VP0 intetlIPPCL.CPU0.VP0 intetlIPPCL.CPU0.VP1	intctlIPTI_CPU7_VP1	0
intctlIPFDC_CPU0_VP0 intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU1_VP0 intctlIPFDC_CPU1_VP0 intctlIPFDC_CPU1_VP1 intctlIPFDC_CPU1_VP2 intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP1 intctlIPFDC_CPU2_VP2 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP1 intctlIPFDC_CPU3_VP2 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP1 intctlIPFDC_CPU4_VP2 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP1 intctlIPFDC_CPU5_VP2 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP1 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU0_VP0 intctlIPF	intctlIPTI_CPU7_VP2	0
intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU0_VP3 intctlIPFDC_CPU1_VP0 intctlIPFDC_CPU1_VP1 intctlIPFDC_CPU1_VP1 intctlIPFDC_CPU1_VP2 intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP1 intctlIPFDC_CPU2_VP2 intctlIPFDC_CPU2_VP3 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP1 intctlIPFDC_CPU3_VP2 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP1 intctlIPFDC_CPU4_VP2 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP1 intctlIPFDC_CPU5_VP1 intctlIPFDC_CPU5_VP2 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU0_VP0 intctlIPPC_CPU0_VP0 intctlIPPC_C		0
intctlIPFDC_CPU0_VP2 intctlIPFDC_CPU1_VP0 intctlIPFDC_CPU1_VP1 intctlIPFDC_CPU1_VP1 intctlIPFDC_CPU1_VP2 intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP1 intctlIPFDC_CPU2_VP2 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP1 intctlIPFDC_CPU3_VP2 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP1 intctlIPFDC_CPU4_VP2 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP1 intctlIPFDC_CPU5_VP2 intctlIPFDC_CPU5_VP2 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP1 intctlIPFDC_CPU6_VP2 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP0 intctlIPF	intctlIPFDC_CPU0_VP0	0
intctlIPFDC_CPU1_VP0 intctlIPFDC_CPU1_VP1 intctlIPFDC_CPU1_VP2 intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP1 intctlIPFDC_CPU2_VP2 intctlIPFDC_CPU2_VP3 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP1 intctlIPFDC_CPU3_VP2 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP1 intctlIPFDC_CPU4_VP2 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP1 intctlIPFDC_CPU5_VP2 intctlIPFDC_CPU5_VP3 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP1 intctlIPFDC_CPU6_VP2 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP0 intctlIPF	intctlIPFDC_CPU0_VP1	0
intctlIPFDC_CPU1_VP0 intctlIPFDC_CPU1_VP2 intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP1 intctlIPFDC_CPU2_VP2 intctlIPFDC_CPU2_VP3 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP1 intctlIPFDC_CPU3_VP2 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP1 intctlIPFDC_CPU4_VP2 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP1 intctlIPFDC_CPU5_VP2 intctlIPFDC_CPU5_VP2 intctlIPFDC_CPU5_VP3 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP1 intctlIPFDC_CPU6_VP2 intctlIPFDC_CPU6_VP2 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU0_VP0 intctlIPFDC_CPU0_VP0 intctlIPPCL_CPU0_VP0 intctlIPPCL_CPU0_VP0 intctlIPPCL_CPU0_VP0 intctlIPPCL_CPU0_VP0 intctlIPPCL_CPU0_VP0	intctlIPFDC_CPU0_VP2	0
intctlIPFDC_CPU1_VP2         0           intctlIPFDC_CPU1_VP3         0           intctlIPFDC_CPU2_VP0         0           intctlIPFDC_CPU2_VP1         0           intctlIPFDC_CPU2_VP2         0           intctlIPFDC_CPU2_VP3         0           intctlIPFDC_CPU3_VP0         0           intctlIPFDC_CPU3_VP1         0           intctlIPFDC_CPU3_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP0         0           intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPFDC_CPU0_VP0         0	intctlIPFDC_CPU0_VP3	0
intctlIPFDC_CPU1_VP3 intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP1 intctlIPFDC_CPU2_VP1 intctlIPFDC_CPU2_VP2 intctlIPFDC_CPU2_VP3 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP1 intctlIPFDC_CPU3_VP2 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP2 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP2 intctlIPFDC_CPU5_VP3 intctlIPFDC_CPU5_VP3 intctlIPFDC_CPU5_VP3 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP1 intctlIPFDC_CPU6_VP2 intctlIPFDC_CPU6_VP2 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP3 intctlIPPC_CPU0_VP0 intctlIPPC_CPU0_VP0 intctlIPPC_CPU0_VP1	intctlIPFDC_CPU1_VP0	0
intctlIPFDC_CPU2_VP0 intctlIPFDC_CPU2_VP1 intctlIPFDC_CPU2_VP2 intctlIPFDC_CPU2_VP3 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP1 intctlIPFDC_CPU3_VP2 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP1 intctlIPFDC_CPU4_VP2 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP1 intctlIPFDC_CPU5_VP2 intctlIPFDC_CPU5_VP3 intctlIPFDC_CPU5_VP3 intctlIPFDC_CPU5_VP3 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP1 intctlIPFDC_CPU6_VP2 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP3 intctlIPPC_CPU0_VP0 intctlIPPC_CPU0_VP0 intctlIPPC_CPU0_VP1 o	intctlIPFDC_CPU1_VP1	0
intctlIPFDC_CPU2_VP1 intctlIPFDC_CPU2_VP2 intctlIPFDC_CPU2_VP3 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP0 intctlIPFDC_CPU3_VP1 intctlIPFDC_CPU3_VP2 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU3_VP3 intctlIPFDC_CPU4_VP0 intctlIPFDC_CPU4_VP1 intctlIPFDC_CPU4_VP2 intctlIPFDC_CPU4_VP3 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP0 intctlIPFDC_CPU5_VP1 intctlIPFDC_CPU5_VP2 intctlIPFDC_CPU5_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP0 intctlIPFDC_CPU6_VP1 intctlIPFDC_CPU6_VP1 intctlIPFDC_CPU6_VP2 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU6_VP3 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP2 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP3 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP0 intctlIPFDC_CPU7_VP1 intctlIPFDC_CPU7_VP3 intctlIPPC_CPU0_VP0 intctlIPPCL_CPU0_VP1	intctlIPFDC_CPU1_VP2	0
intctlIPFDC_CPU2_VP2         0           intctlIPFDC_CPU2_VP3         0           intctlIPFDC_CPU3_VP0         0           intctlIPFDC_CPU3_VP1         0           intctlIPFDC_CPU3_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP0         0           intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCLCPU0_VP0         0           intctlIPPCLCPU0_VP1         0	intctlIPFDC_CPU1_VP3	0
intctlIPFDC_CPU2_VP2         0           intctlIPFDC_CPU2_VP3         0           intctlIPFDC_CPU3_VP0         0           intctlIPFDC_CPU3_VP1         0           intctlIPFDC_CPU3_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP0         0           intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCLCPU0_VP0         0           intctlIPPCLCPU0_VP0         0	intctlIPFDC_CPU2_VP0	0
intctlIPFDC_CPU2_VP3         0           intctlIPFDC_CPU3_VP0         0           intctlIPFDC_CPU3_VP1         0           intctlIPFDC_CPU3_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP0         0           intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCLCPU0_VP0         0           intctlIPPCLCPU0_VP1         0	intctlIPFDC_CPU2_VP1	0
intctlIPFDC_CPU3_VP1         0           intctlIPFDC_CPU3_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP0         0           intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPC_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0	intctlIPFDC_CPU2_VP2	0
intctlIPFDC_CPU3_VP2         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP0         0           intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPFDC_CPU7_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0	intctlIPFDC_CPU2_VP3	0
intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP0         0           intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCLCPU0_VP0         0           intctlIPPCLCPU0_VP1         0	intctlIPFDC_CPU3_VP0	0
intctlIPFDC_CPU3_VP3         0           intctlIPFDC_CPU4_VP0         0           intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCLCPU0_VP0         0           intctlIPPCLCPU0_VP1         0	intctlIPFDC_CPU3_VP1	0
intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP1         0           intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCL_CPU0_VP0         0           intctlIPPCL_CPU0_VP1         0	intctlIPFDC_CPU3_VP2	0
intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCL_CPU0_VP0         0           intctlIPPCL_CPU0_VP1         0	intctlIPFDC_CPU3_VP3	0
intctlIPFDC_CPU4_VP2         0           intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCL_CPU0_VP0         0           intctlIPPCL_CPU0_VP1         0	intctlIPFDC_CPU4_VP0	0
intctlIPFDC_CPU4_VP3         0           intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCL_CPU0_VP0         0           intctlIPPCL_CPU0_VP1         0		0
intctlIPFDC_CPU5_VP0         0           intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCL_CPU0_VP0         0           intctlIPPCL_CPU0_VP1         0		0
intctlIPFDC_CPU5_VP1         0           intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0		0
intctlIPFDC_CPU5_VP2         0           intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0		
intctlIPFDC_CPU5_VP3         0           intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0		0
intctlIPFDC_CPU6_VP0         0           intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0		0
intctlIPFDC_CPU6_VP1         0           intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0		0
intctlIPFDC_CPU6_VP2         0           intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0	intctlIPFDC_CPU6_VP0	0
intctlIPFDC_CPU6_VP3         0           intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0	intctlIPFDC_CPU6_VP1	0
intctlIPFDC_CPU7_VP0         0           intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0		0
intctlIPFDC_CPU7_VP1         0           intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0	intctlIPFDC_CPU6_VP3	0
intctlIPFDC_CPU7_VP2         0           intctlIPFDC_CPU7_VP3         0           intctlIPPCI_CPU0_VP0         0           intctlIPPCI_CPU0_VP1         0	intctlIPFDC_CPU7_VP0	0
intctlIPFDC_CPU7_VP3 0 intctlIPPCI_CPU0_VP0 0 intctlIPPCI_CPU0_VP1 0		0
intctlIPPCI_CPU0_VP0 0 intctlIPPCI_CPU0_VP1 0		0
intctlIPPCI_CPU0_VP1 0	intctlIPFDC_CPU7_VP3	0
	intctlIPPCI_CPU0_VP0	0
intctlIPPCI_CPU0_VP2 0		0
	intctlIPPCI_CPU0_VP2	0

intctlIPPCI_CPU1_VP1         0           intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP3         0           segcfg3PA         0	intctlIPPCI_CPU0_VP3	0
intctlIPPCI_CPU1_VP2         0           intctlIPPCI_CPU1_VP3         0           intctlIPPCI_CPU2_VP0         0           intctlIPPCI_CPU2_VP1         0           intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0		_
intctIIPPCI_CPU1_VP3         0           intctIIPPCI_CPU2_VP0         0           intctIIPPCI_CPU2_VP1         0           intctIIPPCI_CPU2_VP2         0           intctIIPPCI_CPU2_VP3         0           intctIIPPCI_CPU3_VP0         0           intctIIPPCI_CPU3_VP1         0           intctIIPPCI_CPU3_VP2         0           intctIIPPCI_CPU3_VP3         0           intctIIPPCI_CPU3_VP3         0           intctIIPPCI_CPU4_VP0         0           intctIIPPCI_CPU4_VP1         0           intctIIPPCI_CPU4_VP2         0           intctIIPPCI_CPU4_VP3         0           intctIIPPCI_CPU4_VP3         0           intctIIPPCI_CPU5_VP0         0           intctIIPPCI_CPU5_VP1         0           intctIIPPCI_CPU5_VP2         0           intctIIPPCI_CPU6_VP0         0           intctIIPPCI_CPU6_VP1         0           intctIIPPCI_CPU6_VP2         0           intctIIPPCI_CPU7_VP0         0           intctIIPPCI_CPU7_VP1         0           intctIIPPCI_CPU7_VP2         0           intctIIPPCI_CPU7_VP3         0           segcfg1PA         0           segcfg3PA         0		
intctIIPPCI_CPU2_VP0         0           intctIIPPCI_CPU2_VP1         0           intctIIPPCI_CPU2_VP2         0           intctIIPPCI_CPU2_VP3         0           intctIIPPCI_CPU3_VP0         0           intctIIPPCI_CPU3_VP1         0           intctIIPPCI_CPU3_VP2         0           intctIIPPCI_CPU3_VP2         0           intctIIPPCI_CPU3_VP3         0           intctIIPPCI_CPU4_VP0         0           intctIIPPCI_CPU4_VP1         0           intctIIPPCI_CPU4_VP2         0           intctIIPPCI_CPU4_VP3         0           intctIIPPCI_CPU4_VP3         0           intctIIPPCI_CPU5_VP0         0           intctIIPPCI_CPU5_VP1         0           intctIIPPCI_CPU5_VP2         0           intctIIPPCI_CPU6_VP1         0           intctIIPPCI_CPU6_VP2         0           intctIIPPCI_CPU6_VP3         0           intctIIPPCI_CPU7_VP0         0           intctIIPPCI_CPU7_VP1         0           intctIIPPCI_CPU7_VP2         0           intctIIPPCI_CPU7_VP3         0           segcfg3PA         0           segcfg4PA         0           segcfg4PA         0           segc		
intctlIPPCLCPU2_VP1         0           intctlIPPCLCPU2_VP2         0           intctlIPPCLCPU2_VP3         0           intctlIPPCLCPU3_VP0         0           intctlIPPCLCPU3_VP1         0           intctlIPPCLCPU3_VP2         0           intctlIPPCLCPU3_VP2         0           intctlIPPCLCPU3_VP3         0           intctlIPPCLCPU4_VP0         0           intctlIPPCLCPU4_VP1         0           intctlIPPCLCPU4_VP2         0           intctlIPPCLCPU4_VP3         0           intctlIPPCLCPU4_VP3         0           intctlIPPCLCPU5_VP0         0           intctlIPPCLCPU5_VP1         0           intctlIPPCLCPU5_VP2         0           intctlIPPCLCPU5_VP3         0           intctlIPPCLCPU6_VP0         0           intctlIPPCLCPU6_VP1         0           intctlIPPCLCPU6_VP3         0           intctlIPPCLCPU7_VP0         0           intctlIPPCLCPU7_VP1         0           intctlIPPCLCPU7_VP3         0           segcfg1PA         0           segcfg4PA         0           segcfg4PA         0           segcfg4PA         0           segcfg3AM         0		
intctlIPPCI_CPU2_VP2         0           intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP3         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg5PA         0           segcfg3AM <td< td=""><td></td><td></td></td<>		
intctlIPPCI.CPU2.VP3         0           intctlIPPCI.CPU3.VP0         0           intctlIPPCI.CPU3.VP1         0           intctlIPPCI.CPU3.VP2         0           intctlIPPCI.CPU3.VP3         0           intctlIPPCI.CPU4.VP0         0           intctlIPPCI.CPU4.VP1         0           intctlIPPCI.CPU4.VP2         0           intctlIPPCI.CPU4.VP3         0           intctlIPPCI.CPU5.VP0         0           intctlIPPCI.CPU5.VP1         0           intctlIPPCI.CPU5.VP2         0           intctlIPPCI.CPU5.VP3         0           intctlIPPCI.CPU5.VP3         0           intctlIPPCI.CPU6.VP0         0           intctlIPPCI.CPU6.VP1         0           intctlIPPCI.CPU6.VP3         0           intctlIPPCI.CPU7.VP0         0           intctlIPPCI.CPU7.VP1         0           intctlIPPCI.CPU7.VP2         0           intctlIPPCI.CPU7.VP3         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg5PA         0           segcfg5AM         0           segcfg1EU         0		
intctlIPPCI_CPU2_VP3         0           intctlIPPCI_CPU3_VP0         0           intctlIPPCI_CPU3_VP1         0           intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP3         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg3PA         0           segcfg3AM         0           segcfg3AM         0           segcfg3AM         0           segcfg3EU         0		
intctlIPPCI.CPU3.VP1         0           intctlIPPCI.CPU3.VP2         0           intctlIPPCI.CPU3.VP3         0           intctlIPPCI.CPU4.VP0         0           intctlIPPCI.CPU4.VP1         0           intctlIPPCI.CPU4.VP2         0           intctlIPPCI.CPU4.VP3         0           intctlIPPCI.CPU5.VP0         0           intctlIPPCI.CPU5.VP1         0           intctlIPPCI.CPU5.VP2         0           intctlIPPCI.CPU5.VP3         0           intctlIPPCI.CPU6.VP0         0           intctlIPPCI.CPU6.VP1         0           intctlIPPCI.CPU6.VP2         0           intctlIPPCI.CPU6.VP3         0           intctlIPPCI.CPU7.VP0         0           intctlIPPCI.CPU7.VP1         0           intctlIPPCI.CPU7.VP2         0           intctlIPPCI.CPU7.VP3         0           segcfg3PA         0           segcfg4PA         0           segcfg3PA         0           segcfg3PA         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0		
intctlIPPCI_CPU3_VP2         0           intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VV1         0           intctlIPPCI_CPU5_VV2         0           intctlIPPCI_CPU5_VV3         0           intctlIPPCI_CPU5_VV3         0           intctlIPPCI_CPU6_VV1         0           intctlIPPCI_CPU6_VV2         0           intctlIPPCI_CPU6_VV3         0           intctlIPPCI_CPU6_VV3         0           intctlIPPCI_CPU7_VV1         0           intctlIPPCI_CPU7_VV2         0           intctlIPPCI_CPU7_VV3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg1AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg5AM         0           segcfg1EU         0           segcf		
intctlIPPCI_CPU3_VP3         0           intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VV1         0           intctlIPPCI_CPU5_VV2         0           intctlIPPCI_CPU5_VV3         0           intctlIPPCI_CPU5_VV3         0           intctlIPPCI_CPU6_VV1         0           intctlIPPCI_CPU6_VV2         0           intctlIPPCI_CPU6_VV3         0           intctlIPPCI_CPU6_VV3         0           intctlIPPCI_CPU7_VV1         0           intctlIPPCI_CPU7_VV1         0           intctlIPPCI_CPU7_VV2         0           intctlIPPCI_CPU7_VV3         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg3PA         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg3AM         0           segcfg5AM         0           segcfg1EU         0           segcf		
intctlIPPCI_CPU4_VP0         0           intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg3PA         0           segcfg3PA         0           segcfg3PA         0           segcfg3AM         0           segcfg3AM         0           segcfg3AM         0           segcfg3AM         0           segcfg3EU         0		
intctlIPPCI_CPU4_VP1         0           intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg3PA         0           segcfg3PA         0           segcfg3PA         0           segcfg3AM         0           segcfg3AM         0           segcfg3AM         0           segcfg3AM         0           segcfg3EU         0		
intctlIPPCI_CPU4_VP2         0           intctlIPPCI_CPU4_VP3         0           intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg3PA         0           segcfg1AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg3AM         0           segcfg5AM         0           segcfg1EU         0           segcfg2EU         0		
intctIIPPCI_CPU4_VP3         0           intctIIPPCI_CPU5_VP0         0           intctIIPPCI_CPU5_VP1         0           intctIIPPCI_CPU5_VP2         0           intctIIPPCI_CPU5_VP3         0           intctIIPPCI_CPU5_VP3         0           intctIIPPCI_CPU6_VP0         0           intctIIPPCI_CPU6_VP1         0           intctIIPPCI_CPU6_VP2         0           intctIIPPCI_CPU6_VP3         0           intctIIPPCI_CPU7_VP0         0           intctIIPPCI_CPU7_VP1         0           intctIIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg0AM         0           segcfg1AM         0           segcfg3AM         0           segcfg3AM         0           segcfg5AM         0           segcfg0EU         0           segcfg2EU         0		
intctlIPPCI_CPU5_VP0         0           intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg3PA         0           segcfg4PA         0           segcfg0AM         0           segcfg1AM         0           segcfg3AM         0           segcfg3AM         0           segcfg3AM         0           segcfg3EU         0		
intctIIPPCI_CPU5_VP1         0           intctIIPPCI_CPU5_VP2         0           intctIIPPCI_CPU5_VP3         0           intctIIPPCI_CPU5_VP3         0           intctIIPPCI_CPU6_VP0         0           intctIIPPCI_CPU6_VP1         0           intctIIPPCI_CPU6_VP2         0           intctIIPPCI_CPU6_VP3         0           intctIIPPCI_CPU7_VP0         0           intctIIPPCI_CPU7_VP1         0           intctIIPPCI_CPU7_VP2         0           intctIIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg3PA         0           segcfg3PA         0           segcfg3PA         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg3AM         0           segcfg3AM         0           segcfg3AM         0           segcfg3EU         0		
intctlIPPCI_CPU5_VP1         0           intctlIPPCI_CPU5_VP2         0           intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg5AM         0           segcfg5EU         0		
intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
intctlIPPCI_CPU5_VP3         0           intctlIPPCI_CPU6_VP0         0           intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg5PA         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
intctlIPPCI_CPU6_VP1         0           intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
intctlIPPCI_CPU6_VP2         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg0AM         0           segcfg1AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg0AM         0           segcfg1AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
intctlIPPCI_CPU6_VP3         0           intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg3PA         0           segcfg4PA         0           segcfg0AM         0           segcfg1AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5BU         0           segcfg1EU         0           segcfg2EU         0		
intctlIPPCI_CPU7_VP0         0           intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg0AM         0           segcfg1AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5BU         0           segcfg1EU         0           segcfg2EU         0		
intctlIPPCI_CPU7_VP1         0           intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg0AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
intctlIPPCI_CPU7_VP2         0           intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg5PA         0           segcfg0AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
intctlIPPCI_CPU7_VP3         0           segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg5PA         0           segcfg0AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5BU         0           segcfg1EU         0           segcfg2EU         0		
segcfg0PA         0           segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg5PA         0           segcfg0AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5BU         0           segcfg1EU         0           segcfg2EU         0		
segcfg1PA         0           segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg5PA         0           segcfg0AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5BU         0           segcfg1EU         0           segcfg2EU         0		0
segcfg2PA         0           segcfg3PA         0           segcfg4PA         0           segcfg5PA         0           segcfg0AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0	0 0	
segcfg3PA       0         segcfg4PA       0         segcfg5PA       0         segcfg0AM       0         segcfg1AM       0         segcfg2AM       0         segcfg3AM       0         segcfg4AM       0         segcfg5AM       0         segcfg0EU       0         segcfg1EU       0         segcfg2EU       0	9 9	
segcfg4PA         0           segcfg5PA         0           segcfg0AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
segcfg5PA         0           segcfg0AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
segcfg0AM         0           segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
segcfg1AM         0           segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
segcfg2AM         0           segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
segcfg3AM         0           segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
segcfg4AM         0           segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
segcfg5AM         0           segcfg0EU         0           segcfg1EU         0           segcfg2EU         0	0 0	
segcfg0EU         0           segcfg1EU         0           segcfg2EU         0		
segcfg1EU 0 segcfg2EU 0		
segcfg2EU 0		
	segcfg3EU	0

segcfg5EU         0           segcfg0C         0           segcfg1C         0           segcfg2C         0           segcfg3C         0           segcfg5C         0           cdmmSize         0           configAR         0           configBM         0           configDSP         F           configISP         F           configKU         0           configKU         0           configMM         F           configBDF         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DA         0           config1BS         0           config1B         0           config1B         0           config1W         0           config1BR         0           config1BA         0           config1BA         0           config1BR         0           config1W         0           config1W         0           config1MUSizeM1         0           config1MWusizeM1         0           config1PC<		
segcfg1C         0           segcfg2C         0           segcfg3C         0           segcfg5C         0           segcfg5C         0           cdmmSize         0           configAR         0           configBM         0           configBSP         F           configBSP         F           configKU         0           configKU         0           configMDU         F           configMM         F           configBEP         F           mIPS16eASE         F           config1DA         0           config1DB         0           config1DB         0           config1BP         F           config1B         0           config1B         0           config1W         0           config1W         0           config1MMUSizeM1         0           config1WR         F           config1VR         F           config1VR         F           config1VR         F           config1VR         F           config1VB         F           config2SL	segcfg4EU	0
segcfg1C         0           segcfg3C         0           segcfg4C         0           segcfg5C         0           configAR         0           configBM         0           configDSP         F           configISP         F           configK0         0           configK23         0           configMDU         F           configMM         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DB         0           config1BP         F           config1BW         0           config1BW         0           config1BC         0           config1DL         0           config1DS         0           config1BW         0           config1WR         0           config1MMUSizeM1_VPE1         0           config1WR         F           config1VR         F           config1C2         F           config2SL         0           config2SA         0           config3BI         F           con		
segcfg3C         0           segcfg4C         0           segcfg5C         0           configAR         0           configBM         0           configBP         F           configK0         0           configK1         0           configK23         0           configMDU         F           configMT         0           configBBCP         F           MIPS16eASE         F           config1DA         0           config1DB         0           config1DB         0           config1IA         0           config1IW         0           config1IW         0           config1IW         0           config1IW         0           config1IW         0           config1IW         0           config1MMUSizeM1_VPE1         0           config1WR         F           config2SU         0           config2SS         0           config2SS         0           config3BI         F           config3CDMM         F           config3CDMM         F <td< td=""><td></td><td></td></td<>		
segcfg3C         0           segcfg4C         0           configAR         0           configBM         0           configBM         0           configBP         F           configK0         0           configK1         0           configK23         0           configMDU         F           configMM         F           configMT         0           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1BCP         F           config1IA         0           config1IB         0           config1IM         0           config1MMUSizeM1         0           config1MMUSizeM1.VPE1         0           config1WR         F           config1VR         F           config2SU         0           config2SS         0           config2SA         0           config3BP         F           config3CDMM         F           config3CDMM         F		
segcfg4C         0           segcfg5C         0           configAR         0           configBM         0           configBSP         F           configK0         0           configKU         0           configK23         0           configMDU         F           configMM         F           configBEP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1BF         F           config1IA         0           config1IB         0           config1MMUSizeM1         0           config1MMUSizeM1.VPE1         0           config1PC         F           config2SU         0           config2SS         0           config3BI         F           config3BP         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	0 0	0
segcfg5C         0           cdmmSize         0           configAR         0           configBM         0           configBSP         F           configK0         0           configKU         0           configK23         0           configMDU         F           configMM         F           configMT         0           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1B         0           config1IA         0           config1IB         0           config1IMUSizeM1         0           config1MMUSizeM1.VPE1         0           config1PC         F           config2SU         0           config2SS         0           config3BI         F           config3BP         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	segcfg3C	0
cdmmSize         0           configAR         0           configBM         0           configBSP         F           configISP         F           configK0         0           configKU         0           configMDU         F           configMM         F           configMT         0           configBSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1DS         0           config1IA         0           config1IS         0           config1IMOUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE3         0           config1VR         F           config2S         0           config2SU         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F	segcfg4C	0
configBM         0           configDSP         F           configISP         F           configK0         0           configKU         0           configMDU         F           configMM         F           configMT         0           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1DS         0           config1IA         0           config1IB         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CDMM         F           config3CDMM         F	segcfg5C	0
configBM         0           configDSP         F           configISP         F           configK0         0           configKU         0           configK23         0           configMDU         F           configMM         F           configMT         0           configMT         0           configBCP         F           MIPS16eASE         F           config1DA         0           config1DA         0           config1DS         0           config1DS         0           config1IA         0           config1IA         0           config1IB         0           config1IMMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MWSizeM1_VPE3         0           config1VR         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CDMM         F	cdmmSize	0
configDSP         F           configISP         F           configK0         0           configKU         0           configMDU         F           configMM         F           configMT         0           configBSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1BA         0           config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1VR         F           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F	configAR	0
configISP         F           configK0         0           configKU         0           configMDU         F           configMM         F           configMT         0           configBSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1DS         0           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1PC         F           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	configBM	0
configK0         0           configKU         0           configK23         0           configMDU         F           configMM         F           configMT         0           configMT         0           configBSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DS         0           config1DS         0           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1.VPE1         0           config1MMUSizeM1.VPE3         0           config1VR         F           config1C2         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	configDSP	F
configKU         0           configMDU         F           configMM         F           configMT         0           configBB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1BP         F           config1IL         0           config1IL         0           config1MMUSizeM1         0           config1MMUSizeM1.VPE1         0           config1MMUSizeM1.VPE3         0           config1VR         F           config1PC         F           config2SU         0           config2SL         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	configISP	F
configMDU         F           configMM         F           configMT         0           configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1WRUSizeM1_VPE3         0           config1VR         F           config1PC         F           config2SU         0           config2SL         0           config2SA         0           config3BP         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	configK0	0
configMDU         F           configMM         F           configMT         0           configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE3         0           config1VR         F           config1PC         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	configKU	0
configMM         F           configMT         0           configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1IA         0           config1IL         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE3         0           config1VR         F           config1PC         F           config2SU         0           config2SL         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	configK23	0
configMT         0           configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE3         0           config1VR         F           config1PC         F           config2SU         0           config2SL         0           config2SA         0           config3BI         F           config3CDMM         F           config3CDMM         F           config3CTXTC         F	configMDU	F
configSB         F           configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1PC         F           config1PC         F           config2SU         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	configMM	F
configBCP         F           MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IL         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SL         0           config2SA         0           config3BI         F           config3CDMM         F           config3CTXTC         F	configMT	0
MIPS16eASE         F           config1DA         0           config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IL         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1PC         F           config2SU         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	configSB	F
config1DA         0           config1DS         0           config1EP         F           config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1VPC         F           config2SU         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	configBCP	F
config1DL         0           config1DS         0           config1EP         F           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config2SU         0           config2SS         0           config2SA         0           config3BI         F           config3CDMM         F           config3CTXTC         F	MIPS16eASE	F
config1DS         0           config1EP         F           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1VR         F           config1PC         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F	config1DA	0
config1EP         F           config1IA         0           config1IL         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F		0
config1IA         0           config1IS         0           config1MMUSizeM1         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1VR         F           config1PC         F           config1C2         F           config2SU         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1DS	0
config1IL         0           config1IS         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F	config1EP	F
config1IS         0           config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F		0
config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F		0
config1MMUSizeM1_VPE1         0           config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3CDMM         F           config3CTXTC         F		0
config1MMUSizeM1_VPE2         0           config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1MMUSizeM1	0
config1MMUSizeM1_VPE3         0           config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F		0
config1WR         F           config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1MMUSizeM1_VPE2	0
config1PC         F           config1C2         F           config2SU         0           config2SS         0           config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1MMUSizeM1_VPE3	0
config1C2         F           config2SU         0           config2SS         0           config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1WR	F
config2SU         0           config2SS         0           config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1PC	F
config2SS         0           config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config1C2	F
config2SL         0           config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config2SU	0
config2SA         0           config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F		0
config3BI         F           config3BP         F           config3CDMM         F           config3CTXTC         F	config2SL	0
config3BP F config3CDMM F config3CTXTC F	config2SA	0
config3CDMM F config3CTXTC F	config3BI	F
config3CTXTC F	config3BP	F
	config3CDMM	F
config3DSPP F	config3CTXTC	F
	config3DSPP	F

config3DSP2P	F
config3IPLW	0
config3ISA	0
config3ISAOnExc	F
config3ITL	F
config3LPA	F
config3MCU	F
config3MMAR	0
config3RXI	F
config3SC	F
config3ULRI	F
config3VZ	F
config3MSAP	F
config3CMGCR	F
config3SP	F
config3TL	0
config3PW	F
config4AE	F
config4IE	0
config4MMUConfig	0
config4MMUExtDef	0
config4VTLBSizeExt	0
config4KScrExist	0
config5EVA	F
config5LLB	F
config5MRP	F
config5NFExists	F
mips32Macro	F
config5MSAEn	F
config5MVH	F
config5DEC	F
config5GI	0
config5CRCP	F
config5VP	F
config6FTLBEn	F
config7AR	F
config7DCIDX_MODE	0
config7HCI	F
config7IAR	F
config7WII	F
config7ES	0
config7WR	F
config7FPR	F
config7USP	0
config7BTLM	F
=	<u> </u>

config7BusSlp	F
config7IVAD	F
config7RPS	F
config7IAR_CPU0_VPE0	F
config7IAR_CPU0_VPE1	F
config7IAR_CPU0_VPE2	F
config7IAR_CPU0_VPE3	F
config7IAR_CPU1_VPE0	F
config7IAR_CPU1_VPE1	F
config7IAR_CPU1_VPE2	F
config7IAR_CPU1_VPE3	F
config7IAR_CPU2_VPE0	F
config7IAR_CPU2_VPE1	F
config7IAR_CPU2_VPE2	F
config7IAR_CPU2_VPE3	F
	F
config7IAR_CPU3_VPE0	F
config7IAR_CPU3_VPE1	
config7IAR_CPU3_VPE2	F
config7IAR_CPU3_VPE3	F
config7IAR_CPU4_VPE0	F
config7IAR_CPU4_VPE1	F
config7IAR_CPU4_VPE2	F
config7IAR_CPU4_VPE3	F
config7IAR_CPU5_VPE0	F
config7IAR_CPU5_VPE1	F
config7IAR_CPU5_VPE2	F
config7IAR_CPU5_VPE3	F
config7IAR_CPU6_VPE0	F
config7IAR_CPU6_VPE1	F
config7IAR_CPU6_VPE2	F
config7IAR_CPU6_VPE3	F
config7IAR_CPU7_VPE0	F
config7IAR_CPU7_VPE1	F
config7IAR_CPU7_VPE2	F
config7IAR_CPU7_VPE3	F
config7IVAD_CPU0_VPE0	F
config7IVAD_CPU0_VPE1	F
config7IVAD_CPU0_VPE2	F
config7IVAD_CPU0_VPE3	F
config7IVAD_CPU1_VPE0	F
config7IVAD_CPU1_VPE1	F
config7IVAD_CPU1_VPE2	F
config7IVAD_CPU1_VPE3	F
config7IVAD_CPU2_VPE0	F
config7IVAD_CPU2_VPE1	F

C MINAD CIDITO ADEO	Б
config7IVAD_CPU2_VPE2	F
config7IVAD_CPU2_VPE3	F
config7IVAD_CPU3_VPE0	F
config7IVAD_CPU3_VPE1	F
config7IVAD_CPU3_VPE2	F
config7IVAD_CPU3_VPE3	F
config7IVAD_CPU4_VPE0	F
config7IVAD_CPU4_VPE1	F
config7IVAD_CPU4_VPE2	F
config7IVAD_CPU4_VPE3	$\mathbf{F}$
config7IVAD_CPU5_VPE0	$\mathbf{F}$
config7IVAD_CPU5_VPE1	F
config7IVAD_CPU5_VPE2	F
config7IVAD_CPU5_VPE3	F
config7IVAD_CPU6_VPE0	F
config7IVAD_CPU6_VPE1	F
config7IVAD_CPU6_VPE2	F
config7IVAD_CPU6_VPE3	F
config7IVAD_CPU7_VPE0	F
config7IVAD_CPU7_VPE1	F
config7IVAD_CPU7_VPE2	F
config7IVAD_CPU7_VPE3	F
config7RPS_CPU0_VPE0	F
config7RPS_CPU0_VPE1	F
config7RPS_CPU0_VPE2	F
config7RPS_CPU0_VPE3	F
config7RPS_CPU1_VPE0	F
config7RPS_CPU1_VPE1	F
config7RPS_CPU1_VPE2	F
config7RPS_CPU1_VPE3	F
config7RPS_CPU2_VPE0	F
config7RPS_CPU2_VPE1	F
config7RPS_CPU2_VPE2	F
config7RPS_CPU2_VPE3	F
config7RPS_CPU3_VPE0	F
config7RPS_CPU3_VPE1	F
config7RPS_CPU3_VPE2	F
config7RPS_CPU3_VPE3	F
config7RPS_CPU4_VPE0	F
config7RPS_CPU4_VPE1	F
config7RPS_CPU4_VPE2	F
config7RPS_CPU4_VPE3	F
config7RPS_CPU5_VPE0	F
config7RPS_CPU5_VPE1	F
config7RPS_CPU5_VPE2	F
COMING TRUBLOT UBLV F ELZ	Г

and TDDC CDIE VDE2	F
config7RPS_CPU5_VPE3	
config7RPS_CPU6_VPE0	F
config7RPS_CPU6_VPE1	$\frac{F}{F}$
config7RPS_CPU6_VPE2	F
config7RPS_CPU6_VPE3	F
config7RPS_CPU7_VPE0	F
config7RPS_CPU7_VPE1	F
config7RPS_CPU7_VPE2	F
config7RPS_CPU7_VPE3	F
statusFR	F
fcsrABS2008	F
fcsrNAN2008	F
numMaarRegs	6
srsconf0SRS1	0
srsconf0SRS2	0
srsconf0SRS3	0
wiredLimit	0
wiredLimitBits	0
wiredWiredBits	0
cdmmBaseCI	F
parityEnable	1
useMpTb	Т
ExceptionBase	0
UseExceptionBase	F
l1BufferCache	F
GCU_EX	F
GIC_EX	F
CPC_EX	F
TIMER_ROUTABLE	F
SWINT_ROUTABLE	F
PERFCNT_ROUTABLE	F
FDC_ROUTABLE	F
GCR.PCORES	0
GCR_ADDR_REGIONS	0
GCR_NUMAUX	0
GCR_BASE	
	0
GCR_MINOR_REV	0
GCR_MAJOR_REV	0
GCR_CACHE_MINOR_REV	0
GCR_CACHE_MAJOR_REV	0
GCR_L2_ASSOC	0
GCR_L2_SET_SIZE	0
GCR_SYS_CONFIG2_MAX_VP_WIDTH	0
GCR_IOCU1_MINOR_REV	0
GCR_IOCU1_MAJOR_REV	0

GCR_BEV_BASE	0
GCR_KX_BASE_MODE	F
GCR_MMIO_REQ_LIMIT	0
GCR_MMIO0_BOTTOM	0
GCR_MMIO0_TOP_ADDR	0
GCR_MMIO1_BOTTOM	0
GCR_MMIO1_TOP_ADDR	0
GCR_MMIO2_BOTTOM	0
GCR_MMIO2_TOP_ADDR	0
GCR_MMIO3_BOTTOM	0
GCR_MMIO3_TOP_ADDR	0
GIC_NUMINTERRUPTS	0
GIC_COUNTBITS	
GIC_COUNTBITS GIC_MINOR_REV	0
GIC_MAJOR_REV	
	0
GIC_NUM_TEAMS	7
GIC_TRIG_RESET	0
GIC_PVPES	0
CPC_MICROSTEP	0
CPC_RAILDELAY	0
CPC_RESETLEN	0
CPC_MINOR_REV	0
CPC_MAJOR_REV	0
GIC_SH_GID_CONFIG31_0	0
GIC_SH_GID_CONFIG63_32 GIC_SH_GID_CONFIG95_64	0
GIC_SH_GID_CONFIG95_64 GIC_SH_GID_CONFIG127_96	0 0
GIC_SH_GID_CONFIG127_90 GIC_SH_GID_CONFIG159_128	
GIC_SH_GID_CONFIG199_128 GIC_SH_GID_CONFIG191_160	0
GIC_SH_GID_CONFIG191_100 GIC_SH_GID_CONFIG223_192	0
	0
GIC_SH_GID_CONFIG255_224	0
gicVirtualVPNum_CPU0_VP0	0
gicVirtualVPNum_CPU0_VP1	0
gicVirtualVPNum_CPU0_VP2	0 0
gicVirtualVPNum_CPU0_VP3	
gicVirtualVPNum_CPU1_VP0	0
gicVirtualVPNum_CPU1_VP1	0
gicVirtualVPNum_CPU1_VP2	0
gicVirtualVPNum_CPU1_VP3	0
gicVirtualVPNum_CPU2_VP0	0
gicVirtualVPNum_CPU2_VP1	0
gicVirtualVPNum_CPU2_VP2	0
gicVirtualVPNum_CPU2_VP3	0
gicVirtualVPNum_CPU3_VP0	0
gicVirtualVPNum_CPU3_VP1	0

gicVirtualVPNum_CPU3_VP2	0
gicVirtualVPNum_CPU3_VP3	0
gicVirtualVPNum_CPU4_VP0	0
gicVirtualVPNum_CPU4_VP1	0
gicVirtualVPNum_CPU4_VP2	0
gicVirtualVPNum_CPU4_VP3	0
gicVirtualVPNum_CPU5_VP0	0
gicVirtualVPNum_CPU5_VP1	0
gicVirtualVPNum_CPU5_VP2	0
gicVirtualVPNum_CPU5_VP3	0
gicVirtualVPNum_CPU6_VP0	0
gicVirtualVPNum_CPU6_VP1	0
gicVirtualVPNum_CPU6_VP2	0
gicVirtualVPNum_CPU6_VP3	0
gicVirtualVPNum_CPU7_VP0	0
gicVirtualVPNum_CPU7_VP1	0
gicVirtualVPNum_CPU7_VP2	0
gicVirtualVPNum_CPU7_VP3	0
GCR_C0_RESET_BASE	0
GCR_C1_RESET_BASE	0
GCR_C2_RESET_BASE	0
GCR_C3_RESET_BASE	0
GCR_C4_RESET_BASE	0
GCR_C5_RESET_BASE	0
GCR_C6_RESET_BASE	0
GCR_C7_RESET_BASE	0
GCR_C8_RESET_BASE	0
GCR_C9_RESET_BASE	0
GCR_C0_RESET_EXT_BASE	0
GCR_C1_RESET_EXT_BASE	0
GCR_C2_RESET_EXT_BASE	0
GCR_C3_RESET_EXT_BASE	0
GCR_C4_RESET_EXT_BASE	0
GCR_C5_RESET_EXT_BASE	0
GCR_C6_RESET_EXT_BASE	0
GCR_C7_RESET_EXT_BASE	0
GCR_C8_RESET_EXT_BASE	0
GCR_C9_RESET_EXT_BASE	0
CPC_C0_VP_EN	0
CPC_C1_VP_EN	0
CPC_C2_VP_EN	0
CPC_C3_VP_EN	0
CPC_C4_VP_EN	0
CPC_C5_VP_EN	0
CPC_C6_VP_EN	0

CDC CZ VD EN	0
CPC_C7_VP_EN	0
CPC_C8_VP_EN	0
CPC_C9_VP_EN	0
EIC_OPTION	2
guestCtl0RI	0
guestCtl0MC	0
guestCtl0CP0	0
guestCtl0AT	0
guestCtl0GT	0
guestCtl0CG	0
guestCtl0CF	0
guestCtl0G1	0
guestCtl0RAD	0
guestCtl0DRG	0
hasImpl17	F
hasImpl16	F
guestintctlIPTI	0
guestintctlIPFDC	0
guestintctlIPPCI	0
guestintctlIPTI_CPU0_VP0	0
guestintctlIPTI_CPU0_VP1	0
guestintctlIPTI_CPU0_VP2	0
guestintctlIPTI_CPU0_VP3	0
guestintctlIPTI_CPU1_VP0	0
guestintctlIPTI_CPU1_VP1	0
guestintctlIPTI_CPU1_VP2	0
guestintctlIPTI_CPU1_VP3	0
guestintctlIPTI_CPU2_VP0	0
guestintctlIPTI_CPU2_VP1	0
guestintctlIPTI_CPU2_VP2	0
guestintctlIPTI_CPU2_VP3	0
guestintctlIPTI_CPU3_VP0	0
guestintctlIPTI_CPU3_VP1	0
guestintctlIPTI_CPU3_VP2	0
guestintctlIPTLCPU3_VP3	0
guestintctlIPTI_CPU4_VP0	0
guestintctlIPTI_CPU4_VP1	0
guestintctllPTI_CPU4_VP2	0
guestintetllPTLCPU4_VP3	0
guestintetllPTI_CPU5_VP0	0
guestintctllPTI_CPU5_VP1	0
guestintctllPTI_CPU5_VP2	0
guestintctllPTI_CPU5_VP3	0
guestintctIIPTI_CPU6_VP0	0
guestintctIIPTI_CPU6_VP1	0
guestilitetti 11-OF UU_VF1	U

COLLO AND	
guestintctlIPTI_CPU6_VP2	0
guestintctlIPTI_CPU6_VP3	0
guestintctlIPTI_CPU7_VP0	0
guestintctlIPTI_CPU7_VP1	0
guestintctlIPTI_CPU7_VP2	0
guestintctlIPTI_CPU7_VP3	0
guestintctlIPFDC_CPU0_VP0	0
guestintctlIPFDC_CPU0_VP1	0
guestintctlIPFDC_CPU0_VP2	0
guestintctlIPFDC_CPU0_VP3	0
guestintctlIPFDC_CPU1_VP0	0
guestintctlIPFDC_CPU1_VP1	0
guestintctlIPFDC_CPU1_VP2	0
guestintctlIPFDC_CPU1_VP3	0
guestintctlIPFDC_CPU2_VP0	0
guestintctlIPFDC_CPU2_VP1	0
guestintctlIPFDC_CPU2_VP2	0
guestintctlIPFDC_CPU2_VP3	0
guestintctlIPFDC_CPU3_VP0	0
guestintctlIPFDC_CPU3_VP1	0
guestintctlIPFDC_CPU3_VP2	0
guestintctlIPFDC_CPU3_VP3	0
guestintctlIPFDC_CPU4_VP0	0
guestintctlIPFDC_CPU4_VP1	0
guestintctlIPFDC_CPU4_VP2	0
guestintctlIPFDC_CPU4_VP3	0
guestintctlIPFDC_CPU5_VP0	0
guestintctlIPFDC_CPU5_VP1	0
guestintctlIPFDC_CPU5_VP2	0
guestintctlIPFDC_CPU5_VP3	0
guestintctlIPFDC_CPU6_VP0	0
guestintctlIPFDC_CPU6_VP1	0
guestintctlIPFDC_CPU6_VP2	0
guestintctlIPFDC_CPU6_VP3	0
guestintctlIPFDC_CPU7_VP0	0
guestintctlIPFDC_CPU7_VP1	0
guestintctlIPFDC_CPU7_VP2	0
guestintctlIPFDC_CPU7_VP3	0
guestintctlIPPCI_CPU0_VP0	0
guestintctlIPPCI_CPU0_VP1	0
guestintctlIPPCI_CPU0_VP2	0
guestintctlIPPCI_CPU0_VP3	0
guestintctlIPPCI_CPU1_VP0	0
guestintctlIPPCI_CPU1_VP1	0
guestintctlIPPCI_CPU1_VP2	0

guestintctlIPPCI_CPU1_VP3	0
	0
guestintctlIPPCI_CPU2_VP0	0
guestintctlIPPCI_CPU2_VP1	0
guestintctlIPPCI_CPU2_VP2	0
guestintctlIPPCI_CPU2_VP3	0
guestintctlIPPCI_CPU3_VP0	0
guestintctlIPPCI_CPU3_VP1	0
guestintctlIPPCI_CPU3_VP2	0
guestintctlIPPCI_CPU3_VP3	0
guestintctlIPPCI_CPU4_VP0	0
guestintctlIPPCI_CPU4_VP1	0
guestintctlIPPCI_CPU4_VP2	0
guestintctlIPPCI_CPU4_VP3	0
guestintctlIPPCI_CPU5_VP0	0
guestintctlIPPCI_CPU5_VP1	0
guestintctlIPPCI_CPU5_VP2	0
guestintctlIPPCI_CPU5_VP3	0
guestintctlIPPCI_CPU6_VP0	0
guestintctlIPPCI_CPU6_VP1	0
guestintctlIPPCI_CPU6_VP2	0
guestintctlIPPCI_CPU6_VP3	0
guestintctlIPPCI_CPU7_VP0	0
guestintctlIPPCI_CPU7_VP1	0
guestintctlIPPCI_CPU7_VP2	0
guestintctlIPPCI_CPU7_VP3	0
ISPRAM_SIZE	0
ISPRAM_BASE	0
ISPRAM_ENABLE	F
ISPRAM_FILE	
DSPRAM_SIZE	0
DSPRAM_BASE	0
DSPRAM_ENABLE	F
DSPRAM_PRESENT	F
USPRAM_SIZE	0
USPRAM_BASE	0
USPRAM_ENABLE	F
USPRAM_FILE	
misalignedDataException	never
commitTlbwErr	F
	1

Table 8.2: Parameter values

Name	Type	Description
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags

cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info struc-
		ture
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
gprNames	Boolean	Disassemble the register names from the default ABI instead of register numbers for MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
fixedDbgRegSize	Boolean	Enable applications to debug on P5600 with GDB version 2015.06-05 and prior
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true (disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
perfCounters	Uns32	Performance Counters
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC implementation (MT cores only)
ITCFIFODepth	Uns32	Specify ITC FIFO cell depth. By default supports 4.
ITCEmptyOnReset	Boolean	Specify ITC E/F cells reset to a known empty state.
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
support Denormals	Boolean	Enable to specify that the FPU supports denormal operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0. Ignored if less than two VPEs configured.
VPE1MaxTC	Uns32	Specifies the maximum TCs initially on VPE1. Ignored if less than three VPEs configured.
segBits	Uns32	Override the number of address bits implemented for 64 bit segments (MIPS64 Only)
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentControl_0 register

mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentCon-
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentControl.0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentCon-
mpusegment2	Ulis52	trol_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentCon-
mpubegmenta	011302	trol-0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentCon-
mpasesment i	0.11502	trol_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentCon-
F and a 9		trol_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentCon-
•		trol_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentCon-
		trol_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentCon-
		trol_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentCon-
		trol_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentCon-
		trol_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentCon-
		trol_2 register
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentCon-
~		trol_3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentCon-
0 114	11 00	trol_3 register
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentCon-
manus Commont 15	Uns32	trol_3 register Attributes for segment 15 in MPU2 SegmentCon-
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentControl.3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
tcDisable	Uns32	Number of disabled TCs
vpeDisable	Uns32	Number of disabled VPEs
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
mvpconf1c1f	Boolean	Override MVPConf.C1F
mvpcontrolPolicyMode	Boolean	Override MVPControl.POLICY_MODE
hasFDC	Uns32	Specify the size of Fast Debug Channel register
		block
licenseWarningDays	Uns32	Specify the number of days before a license expires
		to start issuing a warning. 0 disables warnings.
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string separated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
TRU_PRESENT	Boolean	Disable or Enable based on TRU presence to con-
		trol certain fields (e.x.perfCtl.PCTD
ucLLwordsLocked	Uns32	Numbers of words (4 byte) an uncached LL is lock-
		ing. Maximum: 4K
FUSA	Boolean	Enable Functional Safety
CPC_FAULT_SUPPORTED	Uns32	Specify the value for Functional Safety Supported
		register

CPC_FAULT_ENABLE	Uns32	Specify the value for Functional Safety Enable register
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object
•		(.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll)
		defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller
-		(sets Config3 VEIC)
config3VEIC_VPE0	Boolean	Enables an external interrupt controller on VPE0
_		(sets Config3 VEIC)
config3VEIC_VPE1	Boolean	Enables an external interrupt controller on VPE1
_		(sets Config3 VEIC)
config3VEIC_VPE2	Boolean	Enables an external interrupt controller on VPE2
		(sets Config3 VEIC)
config3VEIC_VPE3	Boolean	Enables an external interrupt controller on VPE3
_		(sets Config3 VEIC)
rootFixedMMU	Boolean	Override the root MMU type to fixed map-
		ping when true (sets Config.MT=3 and Con-
		fig.KU/K23=2)
rootMMUSizeM1	Uns32	Override the root MMUSizeM1 field in Config1 reg-
		ister (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number
		of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
usePreciseFpu	Uns32	Use the precise Floating Point emulation
simulateLite	Enumeration	Run Simulation with optimization. There are
		several optimizations which coule be combined
		(NONE, FS, MA or FSMA)
pridCompanyOptions	Uns32	Override the Company Options field in PRId reg-
		ister
pridRevision	Uns32	Override the Revision field in PRId register
globalClusterNum	Uns32	Override the ClusterNum field in GlobalNumber
		register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intctlIPFDC	Uns32	Override the IPFDC field in IntCtl register
intctlIPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
maxVP	Uns32	Specify maximum number of Virtual Processors
		present in a core
numVP	Uns32	Specify number of Virtual Processors to be present
numVPtoStart	Uns32	Specify number of Virtual Processors to be started
sharedTLBindex	Uns32	Specify first shared TLB Index between Virtual
		Cores
xconfigSpecified	Boolean	True if the configuration comes from a valid xconfig
		file
intctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for
		CPU0/VP0
intctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for
		CPU0/VP1
intctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for
		CPU0/VP2

intctlIPTI_CPU0_VP3	II 00	
	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
intctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
intctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
intctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
intctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
intctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
intetlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
intctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
intetlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
intctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
intctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
intctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
intctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
intctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
intctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
intctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
intctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
intctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
intctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
intctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
intctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
intctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
intctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
intctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
intctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
intctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
intctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
intctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2

intctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
intctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
intetlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
intctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
intctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
intctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
intctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
intctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
intctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
intctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
intetlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
intctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
intctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
intctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
intctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
intctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
intetlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
intctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
intctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
intctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
intctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
intctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
intctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
intctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
intctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
intctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
intctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
intctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2

intctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for
		CPU6/VP3
intctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
intctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
intctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
intctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
intctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
intctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
intctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
intctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
intctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
intctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
intctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
intctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
intctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
intetlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
intctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
intctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
intetlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
intctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
intctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
intetlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
intctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
intctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
intctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
intctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
intctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
intctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
intetlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2

intctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
intctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
intctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
intctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
intctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
intctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
intctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
intctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
intctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
segcfg0PA	Uns32	Set CFG0.PA field of SegCtl0 register
segcfg1PA	Uns32	Set CFG1.PA field of SegCtl0 register
segcfg2PA	Uns32	Set CFG2.PA field of SegCtl1 register
segcfg3PA	Uns32	Set CFG3.PA field of SegCtl1 register
segcfg4PA	Uns32	Set CFG4.PA field of SegCtl2 register
segcfg5PA	Uns32	Set CFG5.PA field of SegCtl2 register
segcfg0AM	Uns32	Set CFG0.AM field of SegCtl0 register
segcfg1AM	Uns32	Set CFG1.AM field of SegCtl0 register
segcfg2AM	Uns32	Set CFG2.AM field of SegCtl1 register
segcfg3AM	Uns32	Set CFG3.AM field of SegCtl1 register
segcfg4AM	Uns32	Set CFG4.AM field of SegCtl2 register
segcfg5AM	Uns32	Set CFG5.AM field of SegCtl2 register
segcfg0EU	Uns32	Set CFG0.EU field of SegCtl0 register
segcfg1EU	Uns32	Set CFG1.EU field of SegCtl0 register
segcfg2EU	Uns32	Set CFG2.EU field of SegCtl1 register
segcfg3EU	Uns32	Set CFG3.EU field of SegCtl1 register
segcfg4EU	Uns32	Set CFG4.EU field of SegCtl2 register
segcfg5EU	Uns32	Set CFG5.EU field of SegCtl2 register
segcfg0C	Uns32	Set CFG0.C field of SegCtl0 register
segcfg1C	Uns32	Set CFG1.C field of SegCtl0 register
segcfg2C	Uns32	Set CFG2.C field of SegCtl1 register
segcfg3C	Uns32	Set CFG3.C field of SegCtl1 register
segcfg4C	Uns32	Set CFG4.C field of SegCtl2 register
segcfg5C	Uns32	Set CFG5.C field of SegCtl2 register
cdmmSize	Uns32	Override the cdmmsize reset value
configAR	Uns32	Enables R6 support
configBM	Uns32	Override the BM field in Config register (burst
configDSP	Boolean	mode) Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23 cacheability)

configMDU	Boolean	Override Config.MDU (iterative multiply/divide unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT  Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
configBCP		
MIPS16eASE	Boolean	Override Config.BCP (Buffer Cache Present)
	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Deache associativity)
config1DL	Uns32	Override Config1.DL (Deache line size)
config1DS	Uns32	Override Config1.DS (Dcache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU entries-1)
config1MMUSizeM1_VPE1	Uns32	Override Config1.MMUSizeM1 for VPE1
config1MMUSizeM1_VPE2	Uns32	Override Config1.MMUSizeM1 for VPE2
config1MMUSizeM1_VPE3	Uns32	Override Config1.MMUSizeM1 for VPE3
config1WR	Boolean	Override Config1.WR (watchpoint registers
0011181 1111	Boolean	present)
config1PC	Boolean	Override Config1.PC (Performance Counters
	Boolean	present)
config1C2	Boolean	Override Config1.C2 (Coprocessor 2 present)
config2SU	Uns32	Override Config. C2 (Coprocessor 2 present)  Override the SU field in Config2 register
config2SS	Uns32	Override the SC field in Config2 register  Override the SS field in Config2 register
config2SL	Uns32	Override the SL field in Config2 register  Override the SL field in Config2 register
	Uns32	
config2SA		Override the SA field in Config2 register
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.LPA
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
config3VZ	Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3.MSAP
config3CMGCR	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the SI field in Config3 register  Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register  Override the PW field in Config3 register
config4AE	Boolean	
		Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation
0.0000		depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt

and MICartriat	IIma29	Oromida Canfind I/CanErriat
config4KScrExist	Uns32	Override Config4.KScrExist
config5EVA config5LLB	Boolean Boolean	Override Config5.EVA Override Config5.LLB (LLAddr supports LLbit)
config5MRP		
	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists Enables the MIPS32 SAVE and RESTORE macro
mips32Macro	Boolean	
0.5164.7		instructions. Ignored if Config5.CA2 is not set)
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and
4 FDFG		MFHC0 instructions)
config5DEC	Boolean	Override Config5.DEC (to test Dual Endian Capa-
0.707	***	bility)
config5GI	Uns32	Override Config5.GI (enable GINV)
config5CRCP	Boolean	Override Config5.CRCP (CRCP Present)
config5VP	Boolean	Override Config5.VP
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initializa-
		tion)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction
		cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (External-
		ize sync)
config7WR	Boolean	Override Config7[31] bit (Alternative implementa-
		tion of Watch registers)
config7FPR	Boolean	Override Config7.FPR (one-half FPU clock ratio)
config7USP	Uns32	Override Config7.USP (USPRAM enable)
config7BTLM	Boolean	Override Config7.BTLM bit
config7BusSlp	Boolean	Override Config7.BusSlp bit
config7IVAD	Boolean	Override Config7.IVAD bit
config7RPS	Boolean	Override Config7.RPS bit
config7IAR_CPU0_VPE0	Boolean	Override Config7.IAR bit for CPU0/VPE0
config7IAR_CPU0_VPE1	Boolean	Override Config7.IAR bit for CPU0/VPE1
config7IAR_CPU0_VPE2	Boolean	Override Config7.IAR bit for CPU0/VPE2
config7IAR_CPU0_VPE3	Boolean	Override Config7.IAR bit for CPU0/VPE3
config7IAR_CPU1_VPE0	Boolean	Override Config7.IAR bit for CPU1/VPE0
config7IAR_CPU1_VPE1	Boolean	Override Config7.IAR bit for CPU1/VPE1
config7IAR_CPU1_VPE2	Boolean	Override Config7.IAR bit for CPU1/VPE2
config7IAR_CPU1_VPE3	Boolean	Override Config7.IAR bit for CPU1/VPE3
config7IAR_CPU2_VPE0	Boolean	Override Config7.IAR bit for CPU2/VPE0
config7IAR_CPU2_VPE1	Boolean	Override Config7.IAR bit for CPU2/VPE1
config7IAR_CPU2_VPE2	Boolean	Override Config7.IAR bit for CPU2/VPE2
config7IAR_CPU2_VPE3	Boolean	Override Config7.IAR bit for CPU2/VPE3
config7IAR_CPU3_VPE0	Boolean	Override Config7.IAR bit for CPU3/VPE0
config7IAR_CPU3_VPE1	Boolean	Override Config7.IAR bit for CPU3/VPE1
config7IAR_CPU3_VPE2	Boolean	Override Config7.IAR bit for CPU3/VPE2
config7IAR_CPU3_VPE3	Boolean	Override Config7.IAR bit for CPU3/VPE3
config7IAR_CPU4_VPE0	Boolean	Override Config7.IAR bit for CPU4/VPE0
config7IAR_CPU4_VPE1	Boolean	Override Config7.IAR bit for CPU4/VPE1
config7IAR_CPU4_VPE1	Boolean	Override Config7.IAR bit for CPU4/VPE1  Override Config7.IAR bit for CPU4/VPE2
config7IAR_CPU4_VPE2	Boolean	Override Config7.IAR bit for CPU4/VPE2  Override Config7.IAR bit for CPU4/VPE3
_		
config7IAR_CPU5_VPE0	Boolean	Override Config7.IAR bit for CPU5/VPE0
config7IAR_CPU5_VPE1	Boolean	Override Config7.IAR bit for CPU5/VPE1
config7IAR_CPU5_VPE2	Boolean	Override Config7.IAR bit for CPU5/VPE2

config7IAR_CPU5_VPE3	Boolean	Override Config7.IAR bit for CPU5/VPE3
config7IAR_CPU6_VPE0	Boolean	Override Config7.IAR bit for CPU6/VPE0
config7IAR_CPU6_VPE1	Boolean	Override Config7.IAR bit for CPU6/VPE1
config7IAR_CPU6_VPE2	Boolean	Override Config7.IAR bit for CPU6/VPE2
config7IAR_CPU6_VPE3	Boolean	Override Config7.IAR bit for CPU6/VPE3
config7IAR_CPU7_VPE0	Boolean	Override Config7.IAR bit for CPU7/VPE0
config7IAR_CPU7_VPE1	Boolean	Override Config7.IAR bit for CPU7/VPE1
config7IAR_CPU7_VPE2	Boolean	Override Config7.IAR bit for CPU7/VPE2
config7IAR_CPU7_VPE3	Boolean	Override Config7.IAR bit for CPU7/VPE3
config7IVAD_CPU0_VPE0	Boolean	Override Config7.IVAD bit for CPU0/VPE0
config7IVAD_CPU0_VPE1	Boolean	Override Config7.IVAD bit for CPU0/VPE1
config7IVAD_CPU0_VPE2	Boolean	Override Config7.IVAD bit for CPU0/VPE2
config7IVAD_CPU0_VPE3	Boolean	Override Config7.IVAD bit for CPU0/VPE3
config7IVAD_CPU1_VPE0	Boolean	Override Config7.IVAD bit for CPU1/VPE0
config7IVAD_CPU1_VPE1	Boolean	Override Config7.IVAD bit for CPU1/VPE1
config7IVAD_CPU1_VPE2	Boolean	Override Config7.IVAD bit for CPU1/VPE2
config7IVAD_CPU1_VPE3	Boolean	Override Config7.IVAD bit for CPU1/VPE3
config7IVAD_CPU2_VPE0	Boolean	Override Config7.IVAD bit for CPU2/VPE0
config7IVAD_CPU2_VPE1	Boolean	Override Config7.IVAD bit for CPU2/VPE1
config7IVAD_CPU2_VPE2	Boolean	Override Config7.IVAD bit for CPU2/VPE2
config7IVAD_CPU2_VPE3	Boolean	Override Config7.IVAD bit for CPU2/VPE3
config7IVAD_CPU3_VPE0	Boolean	Override Config7.IVAD bit for CPU3/VPE0
config7IVAD_CPU3_VPE1	Boolean	Override Config7.IVAD bit for CPU3/VPE1
config7IVAD_CPU3_VPE2	Boolean	Override Config7.IVAD bit for CPU3/VPE2
config7IVAD_CPU3_VPE3	Boolean	Override Config7.IVAD bit for CPU3/VPE3
config7IVAD_CPU4_VPE0	Boolean	Override Config7.IVAD bit for CPU4/VPE0
config7IVAD_CPU4_VPE1	Boolean	Override Config7.IVAD bit for CPU4/VPE1
config7IVAD_CPU4_VPE2	Boolean	Override Config7.IVAD bit for CPU4/VPE2
config7IVAD_CPU4_VPE3	Boolean	- ,
		Override Config7.IVAD bit for CPU4/VPE3
config7IVAD_CPU5_VPE0	Boolean	Override Config7.IVAD bit for CPU5/VPE0
config7IVAD_CPU5_VPE1	Boolean	Override Config7.IVAD bit for CPU5/VPE1
config7IVAD_CPU5_VPE2	Boolean	Override Config7.IVAD bit for CPU5/VPE2
config7IVAD_CPU5_VPE3	Boolean	Override Config7.IVAD bit for CPU5/VPE3
config7IVAD_CPU6_VPE0	Boolean	Override Config7.IVAD bit for CPU6/VPE0
config7IVAD_CPU6_VPE1	Boolean	Override Config7.IVAD bit for CPU6/VPE1
config7IVAD_CPU6_VPE2	Boolean	Override Config7.IVAD bit for CPU6/VPE2
config7IVAD_CPU6_VPE3	Boolean	Override Config7.IVAD bit for CPU6/VPE3
config7IVAD_CPU7_VPE0	Boolean	Override Config7.IVAD bit for CPU7/VPE0
config7IVAD_CPU7_VPE1	Boolean	Override Config7.IVAD bit for CPU7/VPE1
config7IVAD_CPU7_VPE2	Boolean	Override Config7.IVAD bit for CPU7/VPE2
config7IVAD_CPU7_VPE3	Boolean	Override Config7.IVAD bit for CPU7/VPE3
config7RPS_CPU0_VPE0	Boolean	Override Config7.RPS bit for CPU0/VPE0
config7RPS_CPU0_VPE1	Boolean	Override Config7.RPS bit for CPU0/VPE1
config7RPS_CPU0_VPE2	Boolean	Override Config7.RPS bit for CPU0/VPE2
config7RPS_CPU0_VPE3	Boolean	Override Config7.RPS bit for CPU0/VPE3
config7RPS_CPU1_VPE0	Boolean	Override Config7.RPS bit for CPU1/VPE0
config7RPS_CPU1_VPE1	Boolean	Override Config7.RPS bit for CPU1/VPE1
config7RPS_CPU1_VPE2	Boolean	Override Config7.RPS bit for CPU1/VPE2
config7RPS_CPU1_VPE3	Boolean	Override Config7.RPS bit for CPU1/VPE3
config7RPS_CPU2_VPE0	Boolean	Override Config7.RPS bit for CPU2/VPE0
config7RPS_CPU2_VPE1	Boolean	Override Config7.RPS bit for CPU2/VPE1
config7RPS_CPU2_VPE2	Boolean	Override Config7.RPS bit for CPU2/VPE2
config7RPS_CPU2_VPE3	Boolean	Override Config7.RPS bit for CPU2/VPE3
Comig/Iti 5_Ci U2_Vi E5		
		Override Config7.RPS bit for CPU3/VPE0
config7RPS_CPU3_VPE0 config7RPS_CPU3_VPE1	Boolean Boolean	Override Config7.RPS bit for CPU3/VPE0 Override Config7.RPS bit for CPU3/VPE1

and 7DDC CDII2 VDE2	Boolean	Override Config7.RPS bit for CPU3/VPE3
config7RPS_CPU3_VPE3		
config7RPS_CPU4_VPE0	Boolean	Override Config7.RPS bit for CPU4/VPE0
config7RPS_CPU4_VPE1	Boolean	Override Config7.RPS bit for CPU4/VPE1
config7RPS_CPU4_VPE2	Boolean	Override Config7.RPS bit for CPU4/VPE2
config7RPS_CPU4_VPE3	Boolean	Override Config7.RPS bit for CPU4/VPE3
config7RPS_CPU5_VPE0	Boolean	Override Config7.RPS bit for CPU5/VPE0
config7RPS_CPU5_VPE1	Boolean	Override Config7.RPS bit for CPU5/VPE1
config7RPS_CPU5_VPE2	Boolean	Override Config7.RPS bit for CPU5/VPE2
config7RPS_CPU5_VPE3	Boolean	Override Config7.RPS bit for CPU5/VPE3
config7RPS_CPU6_VPE0	Boolean	Override Config7.RPS bit for CPU6/VPE0
config7RPS_CPU6_VPE1	Boolean	Override Config7.RPS bit for CPU6/VPE1
config7RPS_CPU6_VPE2	Boolean	Override Config7.RPS bit for CPU6/VPE2
config7RPS_CPU6_VPE3	Boolean	Override Config7.RPS bit for CPU6/VPE3
config7RPS_CPU7_VPE0	Boolean	Override Config7.RPS bit for CPU7/VPE0
config7RPS_CPU7_VPE1	Boolean	Override Config7.RPS bit for CPU7/VPE1
config7RPS_CPU7_VPE2	Boolean	Override Config7.RPS bit for CPU7/VPE2
config7RPS_CPU7_VPE3	Boolean	Override Config7.RPS bit for CPU7/VPE3
statusFR	Boolean	Override power on value in Status.FR (Floating
Status It	Boolean	point register mode)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant
ICSI ADS 2000	Doolean	with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings
ICSINAIN2006	Doolean	match IEEE 754-2008 recommendation)
	Uns32	Override number of MAAR registers (must be even)
numMaarRegs srsconf0SRS1	Uns32	
		Override the SRS1 field in SRSConf0 register
srsconf0SRS2	Uns32	Override the SRS2 field in SRSConf0 register
srsconf0SRS3	Uns32	Override the SRS3 field in SRSConf0 register
wiredLimit	Uns32	Override Limit field of the Wired register
wiredLimitBits	Uns32	Override width of Limit field of the Wired register
wiredWiredBits	Uns32	Override width of Wired field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
parityEnable	Uns32	Specify error detection support: 0 - none; 1 - parity; 2 - ECC
useMpTb	Boolean	Override Use of multi-processor test bench
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use
_	D 1	GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the cor-
11D # G 1		responding BEV address bits
l1BufferCache	Boolean	L1 Buffer Cache
GCU_EX	Boolean	CMP system only: GCR custom block present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable
		within cluster
$SWINT\_ROUTABLE$	Boolean	CMP system only: software interrupt routable
		within cluster
PERFCNT_ROUTABLE	Boolean	CMP system only: performance counter interrupt
	Boolean	
		routable within cluster
FDC_ROUTABLE	Boolean	CMP system only: fast debug channel interrupt
	Boolean	CMP system only: fast debug channel interrupt routable within cluster
FDC_ROUTABLE  GCR_PCORES		CMP system only: fast debug channel interrupt routable within cluster  CMP system only: override
	Boolean Uns32	CMP system only: fast debug channel interrupt routable within cluster  CMP system only: override GCR_CONFIG.PCORES (number of cores-1)
	Boolean	CMP system only: fast debug channel interrupt routable within cluster  CMP system only: override GCR_CONFIG.PCORES (number of cores-1)  CMP system only: override
GCR_PCORES	Boolean Uns32	CMP system only: fast debug channel interrupt routable within cluster  CMP system only: override GCR_CONFIG.PCORES (number of cores-1)

GCR_NUMAUX	Uns32	CMP system only: override GCR_CONFIG.NUMAUX (number of auxil-
		iary memory ports)
GCR_BASE	Uns64	CMP system only: override GCR_BASE.GCR_BASE (default GCR regis-
CCD MINOD DEV	11 00	ter address)
GCR_MINOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MAJOR_REV
GCR_L2_ASSOC	Uns32	CMP system only: override GCR_L2_CONFIG.ASSOC
GCR_L2_SET_SIZE	Uns32	CMP system only: override GCR_L2_CONFIG.SET_SIZE
GCR_SYS_CONFIG2_MAX_VP_WIDTH	Uns32	CMP system only: override GCR_SYS_CONFIG2.MAX_VP_WIDTH
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GCR_BEV_BASE	Uns32	CMP system only: override GCR_BEV_BASE
GCR_KX_BASE_MODE	Boolean	CMP system only: override BEV_BASE_MODE & RESET_BASE_MODE
GCR_MMIO_REQ_LIMIT	Uns32	CMP system only: override GCR_MMIO_REQ_LIMIT.MMIO_REQ_LIMIT value
GCR_MMIO0_BOTTOM	Uns64	CMP system only: override GCR_MMIO0_BOTTOM register value
GCR_MMIO0_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO0_TOP.TOP_ADDR value
GCR_MMIO1_BOTTOM	Uns64	CMP system only: override GCR_MMIO1_BOTTOM register value
GCR_MMIO1_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO1_TOP.TOP_ADDR value
GCR_MMIO2_BOTTOM	Uns64	CMP system only: override GCR_MMIO2_BOTTOM register value
GCR_MMIO2_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO2_TOP.TOP_ADDR value
GCR_MMIO3_BOTTOM	Uns64	CMP system only: override GCR_MMIO3_BOTTOM register value
GCR_MMIO3_TOP_ADDR	Uns32	CMP system only: override GCR_MMIO3_TOP.TOP_ADDR value
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override GIC_SH_DBG_CONFIG.NUM_TEAMS

GIC_TRIG_RESET	Uns32	CMP system only: Zero value of GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY
CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
gicVirtualVPNum_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
gicVirtualVPNum_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
gicVirtualVPNum_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
gicVirtualVPNum_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
gicVirtualVPNum_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
gicVirtualVPNum_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
gicVirtualVPNum_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
gicVirtualVPNum_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
gicVirtualVPNum_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
gicVirtualVPNum_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
gicVirtualVPNum_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
gicVirtualVPNum_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
gicVirtualVPNum_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0

gicVirtualVPNum_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
gicVirtualVPNum_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
gicVirtualVPNum_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
gicVirtualVPNum_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
gicVirtualVPNum_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
gicVirtualVPNum_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
gicVirtualVPNum_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
gicVirtualVPNum_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
gicVirtualVPNum_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
gicVirtualVPNum_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
gicVirtualVPNum_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
gicVirtualVPNum_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
gicVirtualVPNum_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
gicVirtualVPNum_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
gicVirtualVPNum_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
gicVirtualVPNum_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
gicVirtualVPNum_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
gicVirtualVPNum_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
gicVirtualVPNum_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C4_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 4
GCR_C5_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 5
GCR_C6_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 6
GCR_C7_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 7
GCR_C8_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 8

GCR_C9_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 9
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
GGD Gt DEGET DVT D LGD	** 00	for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
<del> </del>		for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 3
GCR_C4_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 4
GCR_C5_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
	011302	for core 5
GCR_C6_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 6
GCR_C7_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 7
GCR_C8_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 8
GCR_C9_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE
		for core 9
CPC_C0_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 0
CPC_C1_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 1
CPC_C2_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 2
CPC_C3_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 3
CPC_C4_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 4
CPC_C5_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 5
CPC_C6_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 6
CPC_C7_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 7
CPC_C8_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 8
CPC_C9_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 9
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register
guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest IPFDC field in IntCtl register
guestintctlIPPCI	Uns32	Override the Guest IPPCI field in IntCtl register
guestintctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
guestintctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for
L'ALIDET OPTO VIDO	TT 00	CPU0/VP1
guestintctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2

guestintctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
guestintctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
guestintctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
guestintctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
guestintctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
guestintctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
guestintctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
guestintctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
guestintctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
guestintctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
guestintctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
guestintctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
guestintctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
guestintctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
guestintctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
guestintctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
guestintctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
guestintctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
guestintctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
guestintctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
guestintctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
guestintctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
guestintctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
guestintctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
guestintctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
guestintctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
guestintctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
guestintctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2

guestintctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
guestintctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
guestintctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
guestintctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
guestintctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
guestintctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
guestintctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
guestintctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
guestintctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
guestintctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0
guestintctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
guestintctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
guestintctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
guestintctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
guestintctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
guestintctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
guestintctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
guestintctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
guestintctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
guestintctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
guestintctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
guestintctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
guestintctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
guestintctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
guestintctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
guestintctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
guestintctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
guestintctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2

guestintctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
guestintctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
guestintctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
guestintctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
guestintctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
guestintctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
guestintctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
guestintctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
guestintctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
guestintctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0
guestintctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP1
guestintctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
guestintctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
guestintctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
guestintctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
guestintctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
guestintctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
guestintctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
guestintctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
guestintctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
guestintctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
guestintctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
guestintctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
guestintctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
guestintctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
guestintctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
guestintctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
guestintctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2

guestintctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
guestintctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
guestintctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
guestintctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
guestintctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
guestintctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
guestintctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
guestintctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
guestintctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2( <ispram bytes="" in="" size="">) - 11)</ispram>
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2( <dspram bytes="" in="" size="">) - 11)</dspram>
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag (used to enable the DSPRAM region prior to reset)
DSPRAM_PRESENT	Boolean	DSPRAM is present with SAAR
USPRAM_SIZE	Uns32	Encoded size of the USPRAM region (log2( <uspram bytes="" in="" size="">) - 11)</uspram>
USPRAM_BASE	Uns64	Starting physical address of the USPRAM region
USPRAM_ENABLE	Boolean	Set the enable bit of the USPRAM region's tag (used to enable the USPRAM region prior to reset)
USPRAM_FILE	String	Load a MIPS hex file into the USPRAM region prior to reset
misaligned Data Exception	Enumeration	Select misaligned data access exception signaling: never, checkCCA or always (never, checkCCA or always)
commitTlbwErr	Boolean	Commit TLBWI/TLBRI on ECC; in MIPS_DV_MODE only

Table 8.3: Parameters that can be set in: CPU

## 8.2 Parameter values

These are the current parameter values.

Name	Value
(Others)	
endian	none

	1.6.1
cacheenable	default
cachedebug	0
cacheextbiuinfo	0x0
mipsHexFile	
IMPERAS_MIPS_AVP_OPCODES	F
cacheIndexBypassTLB	F
MIPS_TRACE	F
gprNames	F
supervisorMode	F
busErrors	T
fixedMMU	F
fixedDbgRegSize	F
removeDSP	F
removeCMP	F
removeFP	F
removeFTLB	F
isISA	F
hiddenTLBentries	F
perfCounters	0
ITCNumEntries	0
ITCNumFIFO	0
ITCFIFODepth	0
ITCEmptyOnReset	F
MTFPU	0
supportDenormals	F
VPE0MaxTC	0
VPE1MaxTC	0
segBits	0
mpuRegions	0
mpuType	0
mpuEnable	F
mpuSegment0	0
	0
mpuSegment1 mpuSegment2	0
mpuSegment3	
1 0	0
mpuSegment4	0
mpuSegment5	0
mpuSegment6	0
mpuSegment7	0
mpuSegment8	0
mpuSegment9	0
mpuSegment10	0
mpuSegment11	0
mpuSegment12	0
mpuSegment13	0

mpuSegment14	0
mpuSegment15	0
mvpconf0vpe	0
tcDisable	0
vpeDisable	0
mvpconf0tc	0
mvpconf0pcp	F
mvpconf0tcp	F
mvpconf1c1f	F
mvpcontrolPolicyMode	F
hasFDC	0
licenseWarningDays	15
MIPS_UHI	F
mipsUhiArgs	
mipsUhiJail	
MIPS_DV_MODE	F
MIPS_MAGIC_OPCODES	F
enableTrickbox	F
fpuexcdisable	F
TRU_PRESENT	F
ucLLwordsLocked	0
FUSA	F
CPC_FAULT_SUPPORTED	0
CPC_FAULT_ENABLE	0
cop2Bits	32
cop2FileName	
udiConfig	0
udiFileName	
vectoredinterrupt	F
externalinterrupt	F
config3VEIC_VPE0	F
config3VEIC_VPE1	F
config3VEIC_VPE2	F
config3VEIC_VPE3	F
rootFixedMMU	F
rootMMUSizeM1	0
srsctlHSS	0
firPS	0
firHas2008	0
usePreciseFpu	0
simulateLite	NONE
pridCompanyOptions	0
pridRevision	0
globalClusterNum	0
intctlIPTI	0
1	

intetlIPFDC	0
intelliPPCI	0
numWatch	0
maxVP	0
numVP	0
numVPtoStart	0
sharedTLBindex	0
xconfigSpecified	F
intctlIPTI_CPU0_VP0	0
intctlIPTI_CPU0_VP1	0
intctlIPTI_CPU0_VP2	0
intctlIPTI_CPU0_VP3	0
intctlIPTI_CPU1_VP0	0
intctlIPTI_CPU1_VP1	0
intctlIPTI_CPU1_VP2	0
intctlIPTI_CPU1_VP3	0
intctlIPTI_CPU2_VP0	0
intctlIPTI_CPU2_VP1	0
intctllPTI_CPU2_VP2	0
intctlIPTI_CPU2_VP3	0
intctlIPTI_CPU3_VP0	0
intctlIPTI_CPU3_VP1	0
intctlIPTI_CPU3_VP2	0
intctlIPTI_CPU3_VP3	0
intctlIPTI_CPU4_VP0	0
intctlIPTI_CPU4_VP1	0
intctlIPTI_CPU4_VP2	0
intctlIPTI_CPU4_VP3	0
intctlIPTI_CPU5_VP0	0
intctlIPTI_CPU5_VP1	0
intctlIPTI_CPU5_VP2	0
intctlIPTI_CPU5_VP3	0
intctlIPTI_CPU6_VP0	0
intctlIPTI_CPU6_VP1	0
intctlIPTI_CPU6_VP2	0
intctlIPTI_CPU6_VP3	0
intctlIPTI_CPU7_VP0	0
intctlIPTI_CPU7_VP1	0
intctlIPTI_CPU7_VP2	0
intctlIPTI_CPU7_VP3	0
intctlIPFDC_CPU0_VP0	0
intctlIPFDC_CPU0_VP1	0
intctlIPFDC_CPU0_VP2	0
intctlIPFDC_CPU0_VP3	0
intctlIPFDC_CPU1_VP0	0

intctlIPFDC_CPU1_VP1	0
intctlIPFDC_CPU1_VP2	0
intctlIPFDC_CPU1_VP3	0
intctlIPFDC_CPU2_VP0	0
intctlIPFDC_CPU2_VP1	0
intctlIPFDC_CPU2_VP2	0
intctlIPFDC_CPU2_VP3	0
intctlIPFDC_CPU3_VP0	0
intctlIPFDC_CPU3_VP1	0
intctlIPFDC_CPU3_VP2	0
intctlIPFDC_CPU3_VP3	0
intctlIPFDC_CPU4_VP0	0
intctlIPFDC_CPU4_VP1	0
intctlIPFDC_CPU4_VP2	0
intctlIPFDC_CPU4_VP3	0
intctlIPFDC_CPU5_VP0	0
intctlIPFDC_CPU5_VP1	0
intctlIPFDC_CPU5_VP2	0
intctlIPFDC_CPU5_VP3	0
intctlIPFDC_CPU6_VP0	0
intctlIPFDC_CPU6_VP1	0
intctlIPFDC_CPU6_VP2	0
intctlIPFDC_CPU6_VP3	0
intctlIPFDC_CPU7_VP0	0
intctlIPFDC_CPU7_VP1	0
intctlIPFDC_CPU7_VP2	0
intctlIPFDC_CPU7_VP3	0
intctlIPPCI_CPU0_VP0	0
intctlIPPCI_CPU0_VP1	0
intctlIPPCI_CPU0_VP2	0
intctlIPPCI_CPU0_VP3	0
intctlIPPCI_CPU1_VP0	0
intctlIPPCI_CPU1_VP1	0
intetlIPPCI_CPU1_VP2	0
intetliPPCI_CPU1_VP3	0
intetlIPPCI_CPU2_VP0	0
intetliPPCI_CPU2_VP1	0
intetlIPPCI_CPU2_VP2	0
intetlIPPCI_CPU2_VP3	0
intetliPPCI_CPU3_VP0	0
intetlIPPCI_CPU3_VP1	0
intctllPPCI_CPU3_VP2	0
intctllPPCI_CPU3_VP3	0
intctllPPCI_CPU3_VP3	_
intctllPPCI_CPU4_VP0	0
IIIICUIFFOI_OFU4_VFI	0

C. A AIDD CL CDITA MD2	
intctlIPPCI_CPU4_VP2	0
intctlIPPCI_CPU4_VP3	0
intctlIPPCI_CPU5_VP0	0
intctlIPPCI_CPU5_VP1	0
intctlIPPCI_CPU5_VP2	0
intctlIPPCI_CPU5_VP3	0
intctlIPPCI_CPU6_VP0	0
intctlIPPCI_CPU6_VP1	0
intctlIPPCI_CPU6_VP2	0
intctlIPPCI_CPU6_VP3	0
intctlIPPCI_CPU7_VP0	0
intctlIPPCI_CPU7_VP1	0
intctlIPPCI_CPU7_VP2	0
intctlIPPCI_CPU7_VP3	0
segcfg0PA	0
segcfg1PA	0
segcfg2PA	0
segcfg3PA	0
segcfg4PA	0
segcfg5PA	0
segcfg0AM	0
segcfg1AM	0
segcfg2AM	0
segcfg3AM	0
segcfg4AM	0
segcfg5AM	0
segcfg0EU	0
segcfg1EU	0
segcfg2EU	0
segcfg3EU	0
segcfg4EU	0
segcfg5EU	0
segcfg0C	0
segcfg1C	0
segcfg2C	0
segcfg3C	0
segcfg4C	0
segcfg5C	0
cdmmSize	0
configAR	0
configBM	0
configDSP	F
configISP	F
configK0	0
configKU	0
0	

configK23	0
configMDU	F
configMM	F
configMT	0
configSB	F
configBCP	F
MIPS16eASE	F
config1DA	0
config1DL	0
config1DS	0
config1EP	F
config1IA	0
config1IL	0
config1IS	0
config1MMUSizeM1	0
config1MMUSizeM1_VPE1	0
config1MMUSizeM1_VPE2	0
config1MMUSizeM1_VPE3	0
config1WR	F
config1PC	F
config1C2	F
config2SU	0
config2SS	0
config2SL	0
config2SA	0
config3BI	F
config3BP	F
config3CDMM	F
config3CTXTC	F
config3DSPP	F
config3DSP2P	F
config3IPLW	0
config3ISA	0
config3ISAOnExc	F
config3ITL	F
config3LPA	F
config3MCU	F
config3MMAR	0
config3RXI	F
config3SC	F
config3ULRI	F
config3VZ	F
config3MSAP	F
config3CMGCR	F
config3SP	F
044-	

config3TL	0
config3PW	F
config4AE	F
config4IE	0
config4MMUConfig	0
config4MMUExtDef	0
config4VTLBSizeExt	0
config4KScrExist	0
config5EVA	F
config5LLB	F
config5MRP	F
config5NFExists	F
mips32Macro	F
config5MSAEn	F
config5MVH	F
config5DEC	F
config5GI	0
config5CRCP	F
config5VP	F
config6FTLBEn	F
config7AR	F
config7DCIDX_MODE	0
config7HCI	F
config7IAR	F
config7WII	F
config7ES	0
config7WR	F
config7FPR	F
config7USP	0
config7BTLM	F
config7BusSlp	F
config7IVAD	F
config7RPS	F
config7IAR_CPU0_VPE0	F
config7IAR_CPU0_VPE1	F
config7IAR_CPU0_VPE2	F
config7IAR_CPU0_VPE3	F
config7IAR_CPU1_VPE0	F
config7IAR_CPU1_VPE1	F
config7IAR_CPU1_VPE2	F
config7IAR_CPU1_VPE3	F
config7IAR_CPU2_VPE0	F
config7IAR_CPU2_VPE1	F
config7IAR_CPU2_VPE2	F
config7IAR_CPU2_VPE3	F
comigraticor 02_vr E5	I.

config7IAR_CPU3_VPE1         F           config7IAR_CPU3_VPE2         F           config7IAR_CPU3_VPE3         F           config7IAR_CPU4_VPE0         F           config7IAR_CPU4_VPE1         F           config7IAR_CPU4_VPE2         F           config7IAR_CPU4_VPE3         F           config7IAR_CPU5_VPE0         F           config7IAR_CPU5_VPE1         F           config7IAR_CPU5_VPE2         F           config7IAR_CPU5_VPE3         F           config7IAR_CPU5_VPE3         F           config7IAR_CPU5_VPE3         F           config7IAR_CPU6_VPE0         F           config7IAR_CPU6_VPE1         F           config7IAR_CPU6_VPE3         F           config7IAR_CPU6_VPE3         F           config7IAR_CPU7_VPE0         F           config7IAR_CPU7_VPE3         F           config7IAR_CPU7_VPE3         F           config7IAR_CPU7_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU2_VPE3         F </th <th></th> <th></th>		
config7IAR.CPU3.VPE3         F           config7IAR.CPU3.VPE3         F           config7IAR.CPU4.VPE0         F           config7IAR.CPU4.VPE1         F           config7IAR.CPU4.VPE2         F           config7IAR.CPU5.VPE0         F           config7IAR.CPU5.VPE0         F           config7IAR.CPU5.VPE1         F           config7IAR.CPU5.VPE2         F           config7IAR.CPU5.VPE3         F           config7IAR.CPU5.VPE3         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU6.VPE1         F           config7IAR.CPU6.VPE2         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU7.VPE0         F           config7IAR.CPU7.VPE1         F           config7IAR.CPU7.VPE3         F           config7IAR.CPU7.VPE3         F           config7IAR.CPU0.VPE3         F           config7IVAD.CPU0.VPE3         F           config7IVAD.CPU0.VPE3         F           config7IVAD.CPU1.VPE0         F           config7IVAD.CPU1.VPE3         F           config7IVAD.CPU1.VPE3         F           config7IVAD.CPU2.VPE3         F           config7IVAD.CPU3.VPE3         F<	_	
config7IAR.CPU3.VPE3         F           config7IAR.CPU4.VPE0         F           config7IAR.CPU4.VPE1         F           config7IAR.CPU4.VPE2         F           config7IAR.CPU5.VPE0         F           config7IAR.CPU5.VPE1         F           config7IAR.CPU5.VPE2         F           config7IAR.CPU5.VPE3         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU6.VPE0         F           config7IAR.CPU6.VPE1         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU7.VPE0         F           config7IAR.CPU7.VPE1         F           config7IAR.CPU7.VPE2         F           config7IAR.CPU7.VPE3         F           config7IVAD.CPU0.VPE0         F           config7IVAD.CPU0.VPE1         F           config7IVAD.CPU0.VPE2         F           config7IVAD.CPU1.VPE3         F           config7IVAD.CPU1.VPE3         F           config7IVAD.CPU2.VPE3         F           config7IVAD.CPU2.VPE3         F           config7IVAD.CPU3.VPE3         F           config7IVAD.CPU3.VPE3		
config7IAR.CPU4.VPE0         F           config7IAR.CPU4.VPE1         F           config7IAR.CPU4.VPE2         F           config7IAR.CPU5.VPE0         F           config7IAR.CPU5.VPE1         F           config7IAR.CPU5.VPE2         F           config7IAR.CPU5.VPE3         F           config7IAR.CPU6.VPE0         F           config7IAR.CPU6.VPE1         F           config7IAR.CPU6.VPE2         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU7.VPE0         F           config7IAR.CPU7.VPE1         F           config7IAR.CPU7.VPE2         F           config7IAR.CPU7.VPE3         F           config7IVAD.CPU0.VPE3         F           config7IVAD.CPU0.VPE3         F           config7IVAD.CPU1.VPE3         F           config7IVAD.CPU1.VPE3         F           config7IVAD.CPU1.VPE3         F           config7IVAD.CPU2.VPE3         F           config7IVAD.CPU2.VPE3         F           config7IVAD.CPU3.VPE3         F           config7IVAD.CPU3.VPE3         F           config7IVAD.CPU3.VPE3 <td< td=""><td></td><td></td></td<>		
config7IAR.CPU4.VPE1         F           config7IAR.CPU4.VPE2         F           config7IAR.CPU4.VPE3         F           config7IAR.CPU5.VPE0         F           config7IAR.CPU5.VPE1         F           config7IAR.CPU5.VPE2         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU6.VPE0         F           config7IAR.CPU6.VPE2         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU7.VPE0         F           config7IAR.CPU7.VPE1         F           config7IAR.CPU7.VPE2         F           config7IAR.CPU7.VPE3         F           config7IAR.CPU7.VPE3         F           config7IVAD.CPU0.VPE0         F           config7IVAD.CPU0.VPE3         F           config7IVAD.CPU0.VPE3         F           config7IVAD.CPU1.VPE0         F           config7IVAD.CPU1.VPE2         F           config7IVAD.CPU1.VPE3         F           config7IVAD.CPU2.VPE0         F           config7IVAD.CPU2.VPE3         F           config7IVAD.CPU3.VPE0         F           config7IVAD.CPU3.VPE3         F           config7IVAD.CPU3.VPE3         F           config7IVAD.CPU4.VPE0         <	config7IAR_CPU3_VPE3	
config7IAR.CPU4.VPE3         F           config7IAR.CPU4.VPE3         F           config7IAR.CPU5.VPE0         F           config7IAR.CPU5.VPE1         F           config7IAR.CPU5.VPE2         F           config7IAR.CPU5.VPE3         F           config7IAR.CPU6.VPE0         F           config7IAR.CPU6.VPE1         F           config7IAR.CPU6.VPE2         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU7.VPE0         F           config7IAR.CPU7.VPE1         F           config7IAR.CPU7.VPE2         F           config7IAR.CPU7.VPE3         F           config7IAR.CPU7.VPE3         F           config7IVAD.CPU0.VPE0         F           config7IVAD.CPU0.VPE3         F           config7IVAD.CPU1.VPE0         F           config7IVAD.CPU1.VPE1         F           config7IVAD.CPU1.VPE2         F           config7IVAD.CPU2.VPE0         F           config7IVAD.CPU2.VPE0         F           config7IVAD.CPU2.VPE3         F           config7IVAD.CPU3.VPE0         F           config7IVAD.CPU3.VPE0         F           config7IVAD.CPU3.VPE3         F           config7IVAD.CPU4.VPE0         <	config7IAR_CPU4_VPE0	F
config7IAR.CPU4.VPE3         F           config7IAR.CPU5.VPE0         F           config7IAR.CPU5.VPE1         F           config7IAR.CPU5.VPE2         F           config7IAR.CPU6.VPE3         F           config7IAR.CPU6.VPE0         F           config7IAR.CPU6.VPE1         F           config7IAR.CPU6.VPE2         F           config7IAR.CPU7.VPE0         F           config7IAR.CPU7.VPE0         F           config7IAR.CPU7.VPE1         F           config7IAR.CPU7.VPE2         F           config7IAR.CPU7.VPE3         F           config7IAR.CPU7.VPE3         F           config7IAR.CPU7.VPE3         F           config7IVAD.CPU0.VPE0         F           config7IVAD.CPU0.VPE3         F           config7IVAD.CPU1.VPE0         F           config7IVAD.CPU1.VPE1         F           config7IVAD.CPU1.VPE3         F           config7IVAD.CPU2.VPE0         F           config7IVAD.CPU2.VPE1         F           config7IVAD.CPU3.VPE1         F           config7IVAD.CPU3.VPE1         F           config7IVAD.CPU3.VPE2         F           config7IVAD.CPU4.VPE3         F           config7IVAD.CPU4.VPE3         <	config7IAR_CPU4_VPE1	F
config7IAR_CPU5_VPE0         F           config7IAR_CPU5_VPE1         F           config7IAR_CPU5_VPE2         F           config7IAR_CPU6_VPE0         F           config7IAR_CPU6_VPE1         F           config7IAR_CPU6_VPE2         F           config7IAR_CPU6_VPE3         F           config7IAR_CPU7_VPE0         F           config7IAR_CPU7_VPE1         F           config7IAR_CPU7_VPE2         F           config7IAR_CPU7_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE0         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU2_VPE0         F           config7IVAD_CPU2_VPE1         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3	config7IAR_CPU4_VPE2	F
config7IAR.CPU5_VPE1         F           config7IAR.CPU5_VPE2         F           config7IAR.CPU6_VPE0         F           config7IAR.CPU6_VPE0         F           config7IAR.CPU6_VPE1         F           config7IAR.CPU6_VPE2         F           config7IAR.CPU6_VPE3         F           config7IAR.CPU7_VPE0         F           config7IAR.CPU7_VPE1         F           config7IAR.CPU7_VPE2         F           config7IAR.CPU7_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE1         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU2_VPE3         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3	config7IAR_CPU4_VPE3	F
config7IAR_CPU5_VPE2         F           config7IAR_CPU5_VPE3         F           config7IAR_CPU6_VPE0         F           config7IAR_CPU6_VPE1         F           config7IAR_CPU6_VPE2         F           config7IAR_CPU6_VPE3         F           config7IAR_CPU7_VPE0         F           config7IAR_CPU7_VPE1         F           config7IAR_CPU7_VPE2         F           config7IAR_CPU7_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE1         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE1         F           config7IVAD_CPU1_VPE2         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU2_VPE0         F           config7IVAD_CPU2_VPE1         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3	config7IAR_CPU5_VPE0	F
config7IAR_CPU5_VPE3         F           config7IAR_CPU6_VPE0         F           config7IAR_CPU6_VPE1         F           config7IAR_CPU6_VPE2         F           config7IAR_CPU6_VPE3         F           config7IAR_CPU7_VPE0         F           config7IAR_CPU7_VPE1         F           config7IAR_CPU7_VPE2         F           config7IAR_CPU7_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE1         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU2_VPE0         F           config7IVAD_CPU2_VPE3         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0	config7IAR_CPU5_VPE1	F
config7IAR_CPU6_VPE0         F           config7IAR_CPU6_VPE1         F           config7IAR_CPU6_VPE2         F           config7IAR_CPU6_VPE3         F           config7IAR_CPU7_VPE0         F           config7IAR_CPU7_VPE1         F           config7IAR_CPU7_VPE2         F           config7IAR_CPU7_VPE3         F           config7IVAD_CPU0_VPE0         F           config7IVAD_CPU0_VPE1         F           config7IVAD_CPU0_VPE2         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE2         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU2_VPE0         F           config7IVAD_CPU2_VPE3         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE1         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0	config7IAR_CPU5_VPE2	F
config7IAR_CPU6_VPE1         F           config7IAR_CPU6_VPE2         F           config7IAR_CPU6_VPE3         F           config7IAR_CPU7_VPE0         F           config7IAR_CPU7_VPE1         F           config7IAR_CPU7_VPE2         F           config7IAR_CPU7_VPE3         F           config7IVAD_CPU0_VPE0         F           config7IVAD_CPU0_VPE1         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE1         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU2_VPE0         F           config7IVAD_CPU2_VPE1         F           config7IVAD_CPU2_VPE3         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE1         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE0	config7IAR_CPU5_VPE3	F
config7IAR_CPU6_VPE3         F           config7IAR_CPU6_VPE3         F           config7IAR_CPU7_VPE0         F           config7IAR_CPU7_VPE1         F           config7IAR_CPU7_VPE2         F           config7IAR_CPU7_VPE3         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU0_VPE1         F           config7IVAD_CPU0_VPE2         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE1         F           config7IVAD_CPU1_VPE2         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU2_VPE0         F           config7IVAD_CPU2_VPE1         F           config7IVAD_CPU2_VPE3         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE3	config7IAR_CPU6_VPE0	F
config7IAR_CPU6_VPE3     config7IAR_CPU7_VPE0     config7IAR_CPU7_VPE1     config7IAR_CPU7_VPE1     config7IAR_CPU7_VPE2     config7IAR_CPU7_VPE3     config7IVAD_CPU0_VPE0     config7IVAD_CPU0_VPE1     config7IVAD_CPU0_VPE2     config7IVAD_CPU0_VPE3     config7IVAD_CPU0_VPE3     config7IVAD_CPU1_VPE0     config7IVAD_CPU1_VPE0     config7IVAD_CPU1_VPE1     config7IVAD_CPU1_VPE2     config7IVAD_CPU1_VPE3     config7IVAD_CPU1_VPE3     config7IVAD_CPU2_VPE0     config7IVAD_CPU2_VPE0     config7IVAD_CPU2_VPE1     config7IVAD_CPU2_VPE2     config7IVAD_CPU2_VPE3     config7IVAD_CPU3_VPE0     config7IVAD_CPU3_VPE0     config7IVAD_CPU3_VPE0     config7IVAD_CPU3_VPE1     config7IVAD_CPU3_VPE3     config7IVAD_CPU3_VPE3     config7IVAD_CPU4_VPE3     config7IVAD_CPU4_VPE0     config7IVAD_CPU4_VPE0     config7IVAD_CPU4_VPE0     config7IVAD_CPU4_VPE1     config7IVAD_CPU4_VPE2     config7IVAD_CPU4_VPE3     config7IVAD_CPU4_VPE3     config7IVAD_CPU4_VPE3     config7IVAD_CPU4_VPE3     config7IVAD_CPU5_VPE0     config7IVAD_CPU5_VPE0     config7IVAD_CPU5_VPE0     config7IVAD_CPU5_VPE2     config7IVAD_CPU5_VPE2     config7IVAD_CPU5_VPE3     F	config7IAR_CPU6_VPE1	F
config7IAR_CPU7_VPE0 config7IAR_CPU7_VPE1 config7IAR_CPU7_VPE2 config7IAR_CPU7_VPE3 config7IVAD_CPU0_VPE0 config7IVAD_CPU0_VPE0 config7IVAD_CPU0_VPE1 config7IVAD_CPU0_VPE2 config7IVAD_CPU0_VPE3 config7IVAD_CPU0_VPE3 config7IVAD_CPU1_VPE0 config7IVAD_CPU1_VPE0 config7IVAD_CPU1_VPE1 config7IVAD_CPU1_VPE2 config7IVAD_CPU1_VPE3 config7IVAD_CPU2_VPE0 config7IVAD_CPU2_VPE0 config7IVAD_CPU2_VPE1 config7IVAD_CPU2_VPE2 config7IVAD_CPU2_VPE3 config7IVAD_CPU2_VPE3 config7IVAD_CPU3_VPE2 config7IVAD_CPU3_VPE0 config7IVAD_CPU3_VPE0 config7IVAD_CPU3_VPE1 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE1 config7IVAD_CPU4_VPE2 config7IVAD_CPU4_VPE3 config7IVAD_CPU4_VPE3 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE2	config7IAR_CPU6_VPE2	F
config7IAR_CPU7_VPE1         F           config7IAR_CPU7_VPE2         F           config7IAR_CPU7_VPE3         F           config7IVAD_CPU0_VPE0         F           config7IVAD_CPU0_VPE1         F           config7IVAD_CPU0_VPE2         F           config7IVAD_CPU0_VPE3         F           config7IVAD_CPU1_VPE0         F           config7IVAD_CPU1_VPE1         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU2_VPE0         F           config7IVAD_CPU2_VPE2         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F	config7IAR_CPU6_VPE3	F
config7IAR_CPU7_VPE3 config7IAR_CPU7_VPE3 config7IVAD_CPU0_VPE0 config7IVAD_CPU0_VPE1 config7IVAD_CPU0_VPE2 config7IVAD_CPU0_VPE3 config7IVAD_CPU0_VPE3 config7IVAD_CPU1_VPE0 config7IVAD_CPU1_VPE1 config7IVAD_CPU1_VPE2 config7IVAD_CPU1_VPE2 config7IVAD_CPU1_VPE3 config7IVAD_CPU2_VPE0 config7IVAD_CPU2_VPE0 config7IVAD_CPU2_VPE1 config7IVAD_CPU2_VPE2 config7IVAD_CPU2_VPE3 config7IVAD_CPU2_VPE3 config7IVAD_CPU3_VPE0 config7IVAD_CPU3_VPE0 config7IVAD_CPU3_VPE1 config7IVAD_CPU3_VPE2 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE1 config7IVAD_CPU4_VPE3 config7IVAD_CPU4_VPE3 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE3 F	config7IAR_CPU7_VPE0	F
config7IAR_CPU7_VPE3 config7IVAD_CPU0_VPE0 config7IVAD_CPU0_VPE1 config7IVAD_CPU0_VPE2 config7IVAD_CPU0_VPE3 config7IVAD_CPU1_VPE0 config7IVAD_CPU1_VPE0 config7IVAD_CPU1_VPE1 config7IVAD_CPU1_VPE2 config7IVAD_CPU1_VPE3 config7IVAD_CPU1_VPE3 config7IVAD_CPU2_VPE0 config7IVAD_CPU2_VPE1 config7IVAD_CPU2_VPE2 config7IVAD_CPU2_VPE3 config7IVAD_CPU2_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE0 config7IVAD_CPU3_VPE1 config7IVAD_CPU3_VPE1 config7IVAD_CPU3_VPE2 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE1 config7IVAD_CPU4_VPE2 config7IVAD_CPU4_VPE3 config7IVAD_CPU4_VPE3 config7IVAD_CPU4_VPE3 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE3 F	config7IAR_CPU7_VPE1	F
config7IAR_CPU7_VPE3 config7IVAD_CPU0_VPE0 config7IVAD_CPU0_VPE1 config7IVAD_CPU0_VPE2 config7IVAD_CPU0_VPE3 config7IVAD_CPU1_VPE0 config7IVAD_CPU1_VPE0 config7IVAD_CPU1_VPE1 config7IVAD_CPU1_VPE2 config7IVAD_CPU1_VPE3 config7IVAD_CPU1_VPE3 config7IVAD_CPU2_VPE0 config7IVAD_CPU2_VPE1 config7IVAD_CPU2_VPE2 config7IVAD_CPU2_VPE3 config7IVAD_CPU2_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE0 config7IVAD_CPU3_VPE1 config7IVAD_CPU3_VPE1 config7IVAD_CPU3_VPE2 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE1 config7IVAD_CPU4_VPE2 config7IVAD_CPU4_VPE3 config7IVAD_CPU4_VPE3 config7IVAD_CPU4_VPE3 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE3 F		F
config7IVAD_CPU0_VPE0 config7IVAD_CPU0_VPE1 config7IVAD_CPU0_VPE2 config7IVAD_CPU0_VPE3 config7IVAD_CPU1_VPE0 config7IVAD_CPU1_VPE1 config7IVAD_CPU1_VPE2 config7IVAD_CPU1_VPE3 config7IVAD_CPU1_VPE3 config7IVAD_CPU1_VPE3 config7IVAD_CPU2_VPE0 config7IVAD_CPU2_VPE1 config7IVAD_CPU2_VPE2 config7IVAD_CPU2_VPE3 config7IVAD_CPU2_VPE3 config7IVAD_CPU3_VPE0 config7IVAD_CPU3_VPE0 config7IVAD_CPU3_VPE1 config7IVAD_CPU3_VPE2 config7IVAD_CPU3_VPE3 config7IVAD_CPU3_VPE3 config7IVAD_CPU4_VPE3 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE0 config7IVAD_CPU4_VPE2 config7IVAD_CPU4_VPE2 config7IVAD_CPU4_VPE3 config7IVAD_CPU4_VPE3 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE0 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE2 config7IVAD_CPU5_VPE3 config7IVAD_CPU5_VPE3		F
config7IVAD_CPU0_VPE1     config7IVAD_CPU0_VPE2     config7IVAD_CPU0_VPE3     config7IVAD_CPU1_VPE0     config7IVAD_CPU1_VPE1     config7IVAD_CPU1_VPE2     config7IVAD_CPU1_VPE3     config7IVAD_CPU1_VPE3     config7IVAD_CPU2_VPE0     config7IVAD_CPU2_VPE1     config7IVAD_CPU2_VPE2     config7IVAD_CPU2_VPE2     config7IVAD_CPU2_VPE3     config7IVAD_CPU3_VPE0     config7IVAD_CPU3_VPE0     config7IVAD_CPU3_VPE1     config7IVAD_CPU3_VPE2     config7IVAD_CPU3_VPE3     config7IVAD_CPU3_VPE3     config7IVAD_CPU3_VPE3     config7IVAD_CPU4_VPE0     config7IVAD_CPU4_VPE0     config7IVAD_CPU4_VPE1     config7IVAD_CPU4_VPE2     config7IVAD_CPU4_VPE3     config7IVAD_CPU4_VPE3     config7IVAD_CPU5_VPE0     config7IVAD_CPU5_VPE0     config7IVAD_CPU5_VPE2     config7IVAD_CPU5_VPE3     F		F
config7IVAD_CPU0_VPE2     config7IVAD_CPU0_VPE3     config7IVAD_CPU1_VPE0     F     config7IVAD_CPU1_VPE1     F     config7IVAD_CPU1_VPE2     F     config7IVAD_CPU1_VPE3     F     config7IVAD_CPU1_VPE3     F     config7IVAD_CPU2_VPE0     F     config7IVAD_CPU2_VPE1     F     config7IVAD_CPU2_VPE2     F     config7IVAD_CPU2_VPE3     F     config7IVAD_CPU2_VPE3     F     config7IVAD_CPU3_VPE0     F     config7IVAD_CPU3_VPE1     F     config7IVAD_CPU3_VPE2     F     config7IVAD_CPU3_VPE2     F     config7IVAD_CPU3_VPE3     F     config7IVAD_CPU4_VPE3     F     config7IVAD_CPU4_VPE0     F     config7IVAD_CPU4_VPE2     F     config7IVAD_CPU4_VPE3     F     config7IVAD_CPU4_VPE3     F     config7IVAD_CPU5_VPE0     F     config7IVAD_CPU5_VPE0     F     config7IVAD_CPU5_VPE2     config7IVAD_CPU5_VPE3     F		F
config7IVAD_CPU0_VPE3     config7IVAD_CPU1_VPE0     F     config7IVAD_CPU1_VPE1     F     config7IVAD_CPU1_VPE2     F     config7IVAD_CPU1_VPE3     F     config7IVAD_CPU2_VPE0     F     config7IVAD_CPU2_VPE1     F     config7IVAD_CPU2_VPE2     F     config7IVAD_CPU2_VPE3     F     config7IVAD_CPU2_VPE3     F     config7IVAD_CPU2_VPE3     F     config7IVAD_CPU3_VPE0     F     config7IVAD_CPU3_VPE1     F     config7IVAD_CPU3_VPE2     F     config7IVAD_CPU3_VPE3     F     config7IVAD_CPU3_VPE3     F     config7IVAD_CPU4_VPE0     F     config7IVAD_CPU4_VPE0     F     config7IVAD_CPU4_VPE1     F     config7IVAD_CPU4_VPE2     F     config7IVAD_CPU4_VPE3     F     config7IVAD_CPU4_VPE3     F     config7IVAD_CPU5_VPE0     F     config7IVAD_CPU5_VPE0     F     config7IVAD_CPU5_VPE2     config7IVAD_CPU5_VPE3     F	9	F
config7IVAD_CPU1_VPE0     config7IVAD_CPU1_VPE1     config7IVAD_CPU1_VPE2     config7IVAD_CPU1_VPE3     config7IVAD_CPU2_VPE0     config7IVAD_CPU2_VPE1     config7IVAD_CPU2_VPE2     config7IVAD_CPU2_VPE3     config7IVAD_CPU2_VPE3     config7IVAD_CPU3_VPE0     config7IVAD_CPU3_VPE1     config7IVAD_CPU3_VPE2     config7IVAD_CPU3_VPE3     config7IVAD_CPU3_VPE3     config7IVAD_CPU3_VPE3     config7IVAD_CPU3_VPE3     config7IVAD_CPU4_VPE0     config7IVAD_CPU4_VPE0     config7IVAD_CPU4_VPE1     config7IVAD_CPU4_VPE2     config7IVAD_CPU4_VPE3     config7IVAD_CPU4_VPE3     config7IVAD_CPU4_VPE3     config7IVAD_CPU5_VPE0     config7IVAD_CPU5_VPE0     config7IVAD_CPU5_VPE2     config7IVAD_CPU5_VPE3     F		F
config7IVAD_CPU1_VPE1     config7IVAD_CPU1_VPE2     config7IVAD_CPU1_VPE3     config7IVAD_CPU2_VPE0     config7IVAD_CPU2_VPE1     config7IVAD_CPU2_VPE2     config7IVAD_CPU2_VPE3     config7IVAD_CPU2_VPE3     config7IVAD_CPU3_VPE0     config7IVAD_CPU3_VPE1     config7IVAD_CPU3_VPE2     config7IVAD_CPU3_VPE3     config7IVAD_CPU3_VPE3     config7IVAD_CPU3_VPE3     config7IVAD_CPU4_VPE0     config7IVAD_CPU4_VPE0     config7IVAD_CPU4_VPE1     config7IVAD_CPU4_VPE2     config7IVAD_CPU4_VPE3     config7IVAD_CPU4_VPE3     config7IVAD_CPU4_VPE3     config7IVAD_CPU5_VPE0     config7IVAD_CPU5_VPE0     config7IVAD_CPU5_VPE2     config7IVAD_CPU5_VPE3     F		F
config7IVAD_CPU1_VPE2         F           config7IVAD_CPU1_VPE3         F           config7IVAD_CPU2_VPE0         F           config7IVAD_CPU2_VPE1         F           config7IVAD_CPU2_VPE2         F           config7IVAD_CPU2_VPE3         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE1         F           config7IVAD_CPU3_VPE2         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE1         F           config7IVAD_CPU4_VPE2         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE1         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F		F
config7IVAD_CPU1_VPE3		F
config7IVAD_CPU2_VPE0         F           config7IVAD_CPU2_VPE1         F           config7IVAD_CPU2_VPE2         F           config7IVAD_CPU2_VPE3         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE1         F           config7IVAD_CPU3_VPE2         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE1         F           config7IVAD_CPU4_VPE2         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE1         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F		F
config7IVAD_CPU2_VPE1         F           config7IVAD_CPU2_VPE2         F           config7IVAD_CPU2_VPE3         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE1         F           config7IVAD_CPU3_VPE2         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE1         F           config7IVAD_CPU4_VPE2         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE1         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F	9	F
config7IVAD_CPU2_VPE2         F           config7IVAD_CPU2_VPE3         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE1         F           config7IVAD_CPU3_VPE2         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE1         F           config7IVAD_CPU4_VPE2         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE1         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F		F
config7IVAD_CPU2_VPE3         F           config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE1         F           config7IVAD_CPU3_VPE2         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE1         F           config7IVAD_CPU4_VPE2         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE1         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F		F
config7IVAD_CPU3_VPE0         F           config7IVAD_CPU3_VPE1         F           config7IVAD_CPU3_VPE2         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE1         F           config7IVAD_CPU4_VPE2         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE1         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F		F
config7IVAD_CPU3_VPE1         F           config7IVAD_CPU3_VPE2         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE1         F           config7IVAD_CPU4_VPE2         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE1         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F		
config7IVAD_CPU3_VPE2         F           config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE1         F           config7IVAD_CPU4_VPE2         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE1         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F		
config7IVAD_CPU3_VPE3         F           config7IVAD_CPU4_VPE0         F           config7IVAD_CPU4_VPE1         F           config7IVAD_CPU4_VPE2         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE1         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F		F
config7IVAD_CPU4_VPE0 F config7IVAD_CPU4_VPE1 F config7IVAD_CPU4_VPE2 F config7IVAD_CPU4_VPE3 F config7IVAD_CPU5_VPE0 F config7IVAD_CPU5_VPE1 F config7IVAD_CPU5_VPE2 F config7IVAD_CPU5_VPE2 F config7IVAD_CPU5_VPE3 F		F
config7IVAD_CPU4_VPE1         F           config7IVAD_CPU4_VPE2         F           config7IVAD_CPU4_VPE3         F           config7IVAD_CPU5_VPE0         F           config7IVAD_CPU5_VPE1         F           config7IVAD_CPU5_VPE2         F           config7IVAD_CPU5_VPE3         F	9	
config7IVAD_CPU4_VPE2 F config7IVAD_CPU4_VPE3 F config7IVAD_CPU5_VPE0 F config7IVAD_CPU5_VPE1 F config7IVAD_CPU5_VPE2 F config7IVAD_CPU5_VPE3 F		
config7IVAD_CPU4_VPE3 F config7IVAD_CPU5_VPE0 F config7IVAD_CPU5_VPE1 F config7IVAD_CPU5_VPE2 F config7IVAD_CPU5_VPE3 F		
config7IVAD_CPU5_VPE0 F config7IVAD_CPU5_VPE1 F config7IVAD_CPU5_VPE2 F config7IVAD_CPU5_VPE3 F	9	
config7IVAD_CPU5_VPE1 F config7IVAD_CPU5_VPE2 F config7IVAD_CPU5_VPE3 F	9	
config7IVAD_CPU5_VPE2 F config7IVAD_CPU5_VPE3 F		
config7IVAD_CPU5_VPE3 F		
0		
COMING I VIND OU VI DO I I'	config7IVAD_CPU6_VPE0	F

config/TIVAD_CPU6_VPE2         F           config/TIVAD_CPU6_VPE3         F           config/TIVAD_CPU7_VPE0         F           config/TIVAD_CPU7_VPE1         F           config/TIVAD_CPU7_VPE2         F           config/TIVAD_CPU7_VPE3         F           config/TIVAD_CPU7_VPE3         F           config/TRPS_CPU0_VPE0         F           config/TRPS_CPU0_VPE1         F           config/TRPS_CPU0_VPE3         F           config/TRPS_CPU0_VPE3         F           config/TRPS_CPU1_VPE0         F           config/TRPS_CPU1_VPE1         F           config/TRPS_CPU1_VPE3         F           config/TRPS_CPU1_VPE3         F           config/TRPS_CPU2_VPE0         F           config/TRPS_CPU2_VPE3         F           config/TRPS_CPU2_VPE3         F           config/TRPS_CPU3_VPE0         F           config/TRPS_CPU3_VPE1         F           config/TRPS_CPU3_VPE3         F           config/TRPS_CPU3_VPE3         F           config/TRPS_CPU3_VPE3         F           config/TRPS_CPU4_VPE3         F           config/TRPS_CPU4_VPE3         F           config/TRPS_CPU5_VPE3         F           config/TRPS_CP	config7IVAD CDII6 VDF1	F
config7IVAD_CPU6_VPE3         F           config7IVAD_CPU7_VPE0         F           config7IVAD_CPU7_VPE1         F           config7IVAD_CPU7_VPE2         F           config7IVAD_CPU7_VPE3         F           config7IVAD_CPU7_VPE3         F           config7RPS_CPU0_VPE0         F           config7RPS_CPU0_VPE1         F           config7RPS_CPU0_VPE3         F           config7RPS_CPU1_VPE0         F           config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE2         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU6_VPE3         F </td <td>config7IVAD_CPU6_VPE1</td> <td></td>	config7IVAD_CPU6_VPE1	
config7IVAD_CPU7_VPE0         F           config7IVAD_CPU7_VPE1         F           config7IVAD_CPU7_VPE2         F           config7IVAD_CPU7_VPE3         F           config7RPS_CPU0_VPE0         F           config7RPS_CPU0_VPE1         F           config7RPS_CPU0_VPE2         F           config7RPS_CPU0_VPE3         F           config7RPS_CPU1_VPE0         F           config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F <td></td> <td></td>		
config7IVAD_CPU7_VPE1         F           config7IVAD_CPU7_VPE2         F           config7IVAD_CPU7_VPE3         F           config7RPS_CPU0_VPE0         F           config7RPS_CPU0_VPE1         F           config7RPS_CPU0_VPE2         F           config7RPS_CPU0_VPE3         F           config7RPS_CPU1_VPE0         F           config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE2         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE2         F		
config7IVAD_CPU7_VPE3         F           config7IVAD_CPU7_VPE3         F           config7RPS_CPU0_VPE0         F           config7RPS_CPU0_VPE1         F           config7RPS_CPU0_VPE2         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU1_VPE0         F           config7RPS_CPU1_VPE2         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE3         F		
config7IVAD_CPU7_VPE3         F           config7RPS_CPU0_VPE0         F           config7RPS_CPU0_VPE1         F           config7RPS_CPU0_VPE2         F           config7RPS_CPU0_VPE3         F           config7RPS_CPU1_VPE0         F           config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE3         F		
config7RPS_CPU0_VPE0         F           config7RPS_CPU0_VPE1         F           config7RPS_CPU0_VPE2         F           config7RPS_CPU0_VPE3         F           config7RPS_CPU1_VPE0         F           config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE2         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE2         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE3         F		
config7RPS_CPU0_VPE1         F           config7RPS_CPU0_VPE2         F           config7RPS_CPU1_VPE0         F           config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE2         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE2         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE3         F           config7RPS_CPU7_VPE3         F           config7RPS_CPU7_VPE3         F		
config7RPS_CPU0_VPE3         F           config7RPS_CPU1_VPE0         F           config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE2         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE2         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE3         F           config7RPS_CPU7_VPE3         F	_	
config7RPS_CPU0_VPE3         F           config7RPS_CPU1_VPE0         F           config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE3         F           config7RPS_CPU7_VPE3         F		
config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE2         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE2         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE3         F           config7RPS_CPU7_VPE3         F		
config7RPS_CPU1_VPE1         F           config7RPS_CPU1_VPE2         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE2         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE3         F           config7RPS_CPU7_VPE3         F           config7RPS_CPU7_VPE3         F           config7RPS_CPU7_VPE3         F           config7RPS_CPU7_VPE3         F		
config7RPS_CPU1_VPE2         F           config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE2         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           n		
config7RPS_CPU1_VPE3         F           config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE2         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SR		
config7RPS_CPU2_VPE0         F           config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE2         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0		
config7RPS_CPU2_VPE1         F           config7RPS_CPU2_VPE2         F           config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0		
config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0		
config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0		
config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	_	
config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0		
config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	_	
config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0		F
config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU3_VPE2	
config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU3_VPE3	F
config7RPS_CPU4_VPE3         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0		
config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0		F
config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU4_VPE2	F
config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	_	F
config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU5_VPE0	F
config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU5_VPE1	F
config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU5_VPE2	F
config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU5_VPE3	F
config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU6_VPE0	F
config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU6_VPE1	F
config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU6_VPE2	F
config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU6_VPE3	F
config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU7_VPE0	F
config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU7_VPE1	F
config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	config7RPS_CPU7_VPE2	F
fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0	_	F
fcsrNAN2008 F numMaarRegs 6 srsconf0SRS1 0	statusFR	F
numMaarRegs6srsconf0SRS10	fcsrABS2008	F
srsconf0SRS1 0	fcsrNAN2008	F
srsconf0SRS1 0	numMaarRegs	6
srsconf0SRS2 0	_	0
	srsconf0SRS2	0

0.00	
srsconf0SRS3	0
wiredLimit	0
wiredLimitBits	0
wiredWiredBits	0
cdmmBaseCI	F
parityEnable	1
useMpTb	Τ
ExceptionBase	0
UseExceptionBase	F
l1BufferCache	F
GCU_EX	F
GIC_EX	F
CPC_EX	F
TIMER_ROUTABLE	F
SWINT_ROUTABLE	F
PERFCNT_ROUTABLE	F
FDC_ROUTABLE	F
GCR_PCORES	0
GCR_ADDR_REGIONS	0
GCR_NUMAUX	0
GCR_BASE	0
GCR_MINOR_REV	0
GCR_MAJOR_REV	0
GCR_CACHE_MINOR_REV	0
GCR_CACHE_MAJOR_REV	0
GCR_L2_ASSOC	0
GCR_L2_SET_SIZE	0
GCR_SYS_CONFIG2_MAX_VP_WIDTH	0
GCR_IOCU1_MINOR_REV	0
GCR_IOCU1_MAJOR_REV	0
GCR_BEV_BASE	0
GCR_KX_BASE_MODE	F
GCR_MMIO_REQ_LIMIT	0
GCR_MMIO0_BOTTOM	0
GCR_MMIO0_TOP_ADDR	0
GCR_MMIO1_BOTTOM	0
GCR_MMIO1_TOP_ADDR	0
GCR_MMIO2_BOTTOM	0
GCR_MMIO2_TOP_ADDR	0
GCR_MMIO3_BOTTOM	0
GCR_MMIO3_TOP_ADDR	0
GIC_NUMINTERRUPTS	0
GIC_COUNTBITS	0
GIC_MINOR_REV	0
GIC_MAJOR_REV	0

GIC_NUM_TEAMS GIC_TRIG_RESET GIC_PVPES CPC_MICROSTEP CPC_RAILDELAY CPC_RESETLEN	7 0 0 0 0
GIC_PVPES CPC_MICROSTEP CPC_RAILDELAY	0 0 0
CPC_MICROSTEP CPC_RAILDELAY	0
CPC_RAILDELAY	0
CPC_MINOR_REV	0
CPC_MAJOR_REV	0
GIC_SH_GID_CONFIG31_0	0
GIC_SH_GID_CONFIG63_32	0
GIC_SH_GID_CONFIG95_64	0
GIC_SH_GID_CONFIG127_96	0
GIC_SH_GID_CONFIG159_128	0
GIC_SH_GID_CONFIG191_160	0
GIC_SH_GID_CONFIG223_192	0
GIC_SH_GID_CONFIG255_224	0
gicVirtualVPNum_CPU0_VP0	0
gicVirtualVPNum_CPU0_VP1	0
gicVirtualVPNum_CPU0_VP2	0
gicVirtualVPNum_CPU0_VP3	0
gicVirtualVPNum_CPU1_VP0	0
gicVirtualVPNum_CPU1_VP1	0
gicVirtualVPNum_CPU1_VP2	0
gicVirtualVPNum_CPU1_VP3	0
gicVirtualVPNum_CPU2_VP0	0
gicVirtualVPNum_CPU2_VP1	0
gicVirtualVPNum_CPU2_VP2	0
gicVirtualVPNum_CPU2_VP3	0
gicVirtualVPNum_CPU3_VP0	0
gicVirtualVPNum_CPU3_VP1	0
gicVirtualVPNum_CPU3_VP2	0
gicVirtualVPNum_CPU3_VP3	0
gicVirtualVPNum_CPU4_VP0	0
gicVirtualVPNum_CPU4_VP1	0
gicVirtualVPNum_CPU4_VP2	0
gicVirtualVPNum_CPU4_VP3	0
gicVirtualVPNum_CPU5_VP0	0
gicVirtualVPNum_CPU5_VP1	0
gicVirtualVPNum_CPU5_VP2	0
gicVirtualVPNum_CPU5_VP3	0
gicVirtualVPNum_CPU6_VP0	0
gicVirtualVPNum_CPU6_VP1	0
gicVirtualVPNum_CPU6_VP2	0
gicVirtualVPNum_CPU6_VP3	0
gicVirtualVPNum_CPU7_VP0	0

gicVirtualVPNum_CPU7_VP1	0
gicVirtualVPNum_CPU7_VP2	0
gicVirtualVPNum_CPU7_VP3	0
GCR_C0_RESET_BASE	0
GCR_C1_RESET_BASE	0
GCR_C2_RESET_BASE	0
GCR_C3_RESET_BASE	0
GCR_C4_RESET_BASE	0
GCR_C5_RESET_BASE	0
GCR_C6_RESET_BASE	0
GCR_C7_RESET_BASE	0
GCR_C8_RESET_BASE	0
GCR_C9_RESET_BASE	0
GCR_C0_RESET_EXT_BASE	0
GCR_C1_RESET_EXT_BASE	0
GCR_C2_RESET_EXT_BASE	0
GCR_C3_RESET_EXT_BASE	0
GCR_C4_RESET_EXT_BASE	0
GCR_C5_RESET_EXT_BASE	0
GCR_C6_RESET_EXT_BASE	0
GCR_C7_RESET_EXT_BASE	0
GCR_C8_RESET_EXT_BASE	0
GCR_C9_RESET_EXT_BASE	0
CPC_C0_VP_EN	0
CPC_C1_VP_EN	0
CPC_C2_VP_EN	0
CPC_C3_VP_EN	0
CPC_C4_VP_EN	0
CPC_C5_VP_EN	0
CPC_C6_VP_EN	0
CPC_C7_VP_EN	0
CPC_C8_VP_EN	0
CPC_C9_VP_EN	0
EIC_OPTION	2
guestCtl0RI	0
guestCtl0MC	0
guestCtl0CP0	0
guestCtl0AT	0
guestCtl0GT	0
guestCtl0CG	0
guestCtl0CF	0
guestCtl0G1	0
guestCtl0RAD	0
guestCtl0DRG	0
hasImpl17	F
P	

hasImpl16	F
guestintctlIPTI	0
guestintctlIPFDC	0
guestintctlIPPCI	0
guestintctlIPTI_CPU0_VP0	0
guestintctlIPTI_CPU0_VP1	0
guestintctlIPTI_CPU0_VP2	0
guestintctlIPTI_CPU0_VP3	0
guestintctlIPTI_CPU1_VP0	0
guestintctlIPTI_CPU1_VP1	0
guestintctlIPTI_CPU1_VP2	0
guestintctlIPTI_CPU1_VP3	0
guestintctlIPTI_CPU2_VP0	0
guestintctlIPTI_CPU2_VP1	0
guestintctlIPTI_CPU2_VP2	0
guestintctlIPTI_CPU2_VP3	0
guestintctlIPTI_CPU3_VP0	0
guestintctlIPTI_CPU3_VP1	0
guestintctlIPTI_CPU3_VP2	0
guestintctlIPTI_CPU3_VP3	0
guestintctlIPTI_CPU4_VP0	0
guestintctlIPTI_CPU4_VP1	0
guestintctlIPTI_CPU4_VP2	0
guestintctlIPTI_CPU4_VP3	0
guestintctlIPTI_CPU5_VP0	0
guestintctlIPTI_CPU5_VP1	0
guestintctlIPTI_CPU5_VP2	0
guestintctlIPTI_CPU5_VP3	0
guestintctlIPTI_CPU6_VP0	0
guestintctlIPTI_CPU6_VP1	0
guestintctlIPTI_CPU6_VP2	0
guestintctlIPTI_CPU6_VP3	0
guestintctlIPTI_CPU7_VP0	0
guestintctlIPTI_CPU7_VP1	0
guestintctlIPTI_CPU7_VP2	0
guestintctlIPTI_CPU7_VP3	0
guestintctlIPFDC_CPU0_VP0	0
guestintctlIPFDC_CPU0_VP1	0
guestintctlIPFDC_CPU0_VP2	0
guestintctlIPFDC_CPU0_VP3	0
guestintctlIPFDC_CPU1_VP0	0
guestintctlIPFDC_CPU1_VP1	0
guestintctlIPFDC_CPU1_VP2	0
guestintctlIPFDC_CPU1_VP3	0
guestintctlIPFDC_CPU2_VP0	0

guestintctlIPFDC_CPU2_VP1	0
guestintctlIPFDC_CPU2_VP2	0
guestintctlIPFDC_CPU2_VP3	0
guestintctlIPFDC_CPU3_VP0	0
guestintctlIPFDC_CPU3_VP1	0
guestintctlIPFDC_CPU3_VP2	0
guestintctlIPFDC_CPU3_VP3	0
guestintctlIPFDC_CPU4_VP0	0
guestintctlIPFDC_CPU4_VP1	0
guestintctlIPFDC_CPU4_VP2	0
guestintctlIPFDC_CPU4_VP3	0
guestintctlIPFDC_CPU5_VP0	0
guestintctlIPFDC_CPU5_VP1	0
guestintctlIPFDC_CPU5_VP2	0
guestintctlIPFDC_CPU5_VP3	0
guestintctlIPFDC_CPU6_VP0	0
guestintctlIPFDC_CPU6_VP1	0
guestintctlIPFDC_CPU6_VP2	0
guestintctlIPFDC_CPU6_VP3	0
guestintctlIPFDC_CPU7_VP0	0
guestintctlIPFDC_CPU7_VP1	0
guestintctlIPFDC_CPU7_VP2	0
guestintctlIPFDC_CPU7_VP3	0
guestintctlIPPCI_CPU0_VP0	0
guestintctlIPPCI_CPU0_VP1	0
guestintctlIPPCI_CPU0_VP2	0
guestintctlIPPCI_CPU0_VP3	0
guestintctlIPPCI_CPU1_VP0	0
guestintctlIPPCI_CPU1_VP1	0
guestintctlIPPCI_CPU1_VP2	0
guestintctlIPPCI_CPU1_VP3	0
guestintctlIPPCI_CPU2_VP0	0
guestintctlIPPCI_CPU2_VP1	0
guestintctlIPPCI_CPU2_VP2	0
guestintctlIPPCI_CPU2_VP3	0
guestintctlIPPCI_CPU3_VP0	0
guestintctlIPPCI_CPU3_VP1	0
guestintctlIPPCI_CPU3_VP2	0
guestintctlIPPCI_CPU3_VP3	0
guestintctlIPPCI_CPU4_VP0	0
guestintctlIPPCI_CPU4_VP1	0
guestintctlIPPCI_CPU4_VP2	0
guestintctlIPPCI_CPU4_VP3	0
guestintctlIPPCI_CPU5_VP0	0
guestintctlIPPCI_CPU5_VP1	0

guestintctlIPPCI_CPU5_VP2	0
guestintctlIPPCI_CPU5_VP3	0
guestintctlIPPCI_CPU6_VP0	0
guestintctlIPPCI_CPU6_VP1	0
guestintctlIPPCI_CPU6_VP2	0
guestintctlIPPCI_CPU6_VP3	0
guestintctlIPPCI_CPU7_VP0	0
guestintctlIPPCI_CPU7_VP1	0
guestintctlIPPCI_CPU7_VP2	0
guestintctlIPPCI_CPU7_VP3	0
ISPRAM_SIZE	0
ISPRAM_BASE	0
ISPRAM_ENABLE	F
ISPRAM_FILE	
DSPRAM_SIZE	0
DSPRAM_BASE	0
DSPRAM_ENABLE	F
DSPRAM_PRESENT	F
USPRAM_SIZE	0
USPRAM_BASE	0
USPRAM_ENABLE	F
USPRAM_FILE	
misalignedDataException	never
commitTlbwErr	F

Table 8.4: Parameter values

Name	Type	Description
endian	Endian	Model endian
cacheenable	Enumeration	Select cache model mode (default, tag or full)
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info struc-
		ture
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
		(specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB
		exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
gprNames	Boolean	Disassemble the register names from the default
		ABI instead of register numbers for MIPS-format
		trace output
supervisorMode	Boolean	Override whether processor implements supervisor
		mode
busErrors	Boolean	Override bus error exception behavior. When true,
		accesses of memory not defined by platform will
		cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when
		true (sets Config.MT=3, Config.KU/K23=2 and
		Config1.MMUSizeM1=0)

fixedDbgRegSize	Boolean	Enable applications to debug on P5600 with GDB
		version 2015.06-05 and prior
removeDSP	Boolean	Override the DSP-present configuration when true
		(sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true
		(sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true
		(sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true
		(disable FTLB)
isISA	Boolean	Enable to specify ISA model (reset address from
		ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to
40	***	maximum value to improve performance
perfCounters	Uns32	Performance Counters
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores
IECNI DIEC	11 90	only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC
ITCFIFODepth	Uns32	implementation (MT cores only)  Specify ITC FIFO cell depth. By default supports
ПСтгорери	Ulis52	Specify 11C F1FO cell depth. By default supports 4.
ITCEmptyOnReset	Boolean	Specify ITC E/F cells reset to a known empty state.
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior,
WIIIO	011852	2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal
supportDenormals	Doolean	operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0. Ig-
VIEGWAXIO	0 11502	nored if less than two VPEs configured.
VPE1MaxTC	Uns32	Specifies the maximum TCs initially on VPE1. Ig-
(1 D11110011 0	0111002	nored if less than three VPEs configured.
segBits	Uns32	Override the number of address bits implemented
		for 64 bit segments (MIPS64 Only)
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentCon-
		trol_0 register
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentCon-
		trol_0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentCon-
		trol_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentCon-
		trol_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentCon-
		trol_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentCon-
		trol_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentCon-
C	77 00	trol_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentCon-
g	*** ***	trol_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentCon-
2 10	77 00	trol_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentCon-
	TT 00	trol_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentCon-
		trol_2 register

mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentControl_2 register
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentControl_3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentControl_3 register
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentControl_3 register
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentControl_3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
tcDisable	Uns32	Number of disabled TCs
vpeDisable	Uns32	Number of disabled VPEs
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
mvpconf1c1f	Boolean	Override MVPConf.C1F
mvpcontrolPolicyMode	Boolean	Override MVPControl.POLICY_MODE
hasFDC	Uns32	Specify the size of Fast Debug Channel register block
licenseWarningDays	Uns32	Specify the number of days before a license expires to start issuing a warning. 0 disables warnings.
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string separated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
TRU_PRESENT	Boolean	Disable or Enable based on TRU presence to control certain fields (e.x.perfCtl.PCTD
ucLLwordsLocked	Uns32	Numbers of words (4 byte) an uncached LL is locking. Maximum: 4K
FUSA	Boolean	Enable Functional Safety
CPC_FAULT_SUPPORTED	Uns32	Specify the value for Functional Safety Supported register
CPC_FAULT_ENABLE	Uns32	Specify the value for Functional Safety Enable register
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object (.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll) defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller (sets Config3 VEIC)
config3VEIC_VPE0	Boolean	Enables an external interrupt controller on VPE0 (sets Config3 VEIC)
config3VEIC_VPE1	Boolean	Enables an external interrupt controller on VPE1 (sets Config3 VEIC)
$config 3 VEIC\_VPE 2$	Boolean	Enables an external interrupt controller on VPE2 (sets Config3 VEIC)
$config 3 VEIC\_VPE 3$	Boolean	Enables an external interrupt controller on VPE3 (sets Config3 VEIC)

${\bf rootFixedMMU}$	Boolean	Override the root MMU type to fixed mapping when true (sets Config.MT=3 and Config.MT(Non-n)
rootMMUSizeM1	Uns32	fig.KU/K23=2) Override the root MMUSizeM1 field in Config1 reg-
		ister (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
usePreciseFpu	Uns32	Use the precise Floating Point emulation
simulateLite	Enumeration	Run Simulation with optimization. There are several optimizations which coule be combined (NONE, FS, MA or FSMA)
pridCompanyOptions	Uns32	Override the Company Options field in PRId register
pridRevision	Uns32	Override the Revision field in PRId register
globalClusterNum	Uns32	Override the ClusterNum field in GlobalNumber register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intetlIPFDC	Uns32	Override the IPFDC field in IntCtl register
intctlIPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
maxVP	Uns32	Specify maximum number of Virtual Processors present in a core
numVP	Uns32	Specify number of Virtual Processors to be present
numVPtoStart	Uns32	Specify number of Virtual Processors to be started
${\it shared TLB index}$	Uns32	Specify first shared TLB Index between Virtual Cores
xconfigSpecified	Boolean	True if the configuration comes from a valid xconfig file
intctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
intctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
intctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
intctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
intctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
intctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
intctlIPTI_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
intctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
intctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
intctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
intctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
intctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
intctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0

L. JADES GDAYS AND	** 00	
intctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
intctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
intctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
intctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
intctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
intctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
intetlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
intetlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
intctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
intctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
intctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
intctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
intctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
intctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
intctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
intctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
intctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
intctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
intctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
intctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
intctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
intctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
intctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
intctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
intctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
intctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
intctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
intetlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0

intctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
intctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
intctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
intctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
intctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
intctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
intctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
intctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
intctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
intctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
intctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
intctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
intctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
intctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
intctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
intctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
intctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
intctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
intctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
intctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
intctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
intctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
intctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
intctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
intctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
intctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
intctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
intctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0

intctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for
		CPU1/VP1
intctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
intctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
intctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
intctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
intctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
intctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
intctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
intctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
intctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
intctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
intctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
intctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
intctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
intctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
intctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
intctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
intctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
intctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
intctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
intctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
intctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
intctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
intctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
intctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
intctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
intctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
segcfg0PA	Uns32	Set CFG0.PA field of SegCtl0 register
segcfg1PA	Uns32	Set CFG1.PA field of SegCtl0 register
segcfg2PA	Uns32	Set CFG2.PA field of SegCtl1 register

segcfg3PA	Uns32	Set CFG3.PA field of SegCtl1 register
segcfg4PA	Uns32	Set CFG4.PA field of SegCtl2 register
segcfg5PA	Uns32	Set CFG5.PA field of SegCtl2 register
segcfg0AM	Uns32	Set CFG0.AM field of SegCtl0 register
segcfg1AM	Uns32	Set CFG1.AM field of SegCtl0 register
segcfg2AM	Uns32	Set CFG2.AM field of SegCtl1 register
segcfg3AM	Uns32	Set CFG3.AM field of SegCtl1 register
segcfg4AM	Uns32	Set CFG4.AM field of SegCtl2 register
segcfg5AM	Uns32	Set CFG5.AM field of SegCtl2 register
segcfg0EU	Uns32	Set CFG0.EU field of SegCtl0 register
segcfg1EU	Uns32	Set CFG1.EU field of SegCtl0 register
segcfg2EU	Uns32	Set CFG2.EU field of SegCtl1 register
segcfg3EU	Uns32	Set CFG3.EU field of SegCtl1 register
segcfg4EU	Uns32	Set CFG4.EU field of SegCtl2 register
segcfg5EU	Uns32	Set CFG5.EU field of SegCtl2 register
segcfg0C	Uns32	Set CFG0.C field of SegCtl0 register
segcfg1C	Uns32	Set CFG1.C field of SegCtl0 register
segcfg2C	Uns32	Set CFG2.C field of SegCtl1 register
segcfg3C	Uns32	Set CFG3.C field of SegCtl1 register
segcfg4C	Uns32	Set CFG4.C field of SegCtl2 register
segcfg5C	Uns32	Set CFG5.C field of SegCtl2 register
cdmmSize	Uns32	Override the cdmmsize reset value
configAR	Uns32	Enables R6 support
configBM	Uns32	Override the BM field in Config register (burst
ComigDivi	011592	mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM
ComgDO1	Boolcan	present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM
comgret	Boolean	present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0
comgri	0 11502	cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg
001118110	0111002	cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23
- Commgri20	011502	cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide
00111181112	20010011	unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
configBCP	Boolean	Override Config.BCP (Buffer Cache Present)
MIPS16eASE	Boolean	Override Config. CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Deache associativity)
config1DL	Uns32	Override Config1.DL (Deache line size)
config1DS	Uns32	Override Config1.DS (Deache line size)  Override Config1.DS (Deache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	
_		Override Config1.IA (Icache associativity)
config1IL config1IS	Uns32	Override Config1.IL (Icache line size)
	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU
C 1MMIIO MA MIDE	11 60	entries-1)
config1MMUSizeM1_VPE1	Uns32	Override Config1.MMUSizeM1 for VPE1
config1MMUSizeM1_VPE2	Uns32	Override Config1.MMUSizeM1 for VPE2
config1MMUSizeM1_VPE3	Uns32	Override Config1.MMUSizeM1 for VPE3
config1WR	Boolean	Override Config1.WR (watchpoint registers
		present)

config1PC	Boolean	Override Config1.PC (Performance Counters present)
config1C2	Boolean	Override Config1.C2 (Coprocessor 2 present)
config2SU	Uns32	Override the SU field in Config2 register
config2SS	Uns32	Override the SS field in Config2 register
config2SL	Uns32	Override the SL field in Config2 register
config2SA	Uns32	Override the SA field in Config2 register
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.LPA
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
config3VZ	Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3.MSAP
config3CMGCR	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation
	011002	depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config4KScrExist	Uns32	Override Config4. KScrExist
config5EVA	Boolean	Override Config5.EVA
config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
mips32Macro	Boolean	Enables the MIPS32 SAVE and RESTORE macro
mips92lviacio	Doolean	instructions. Ignored if Config5.CA2 is not set)
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and
COMINGOINI V II	Doolcan	MFHC0 instructions)
config5DEC	Boolean	Override Config5.DEC (to test Dual Endian Capa-
Comigorno	Doorcan	bility)
config5GI	Uns32	Override Config5.GI (enable GINV)
config5CRCP	Boolean	Override Configs.Gr (enable GIVV)  Override Configs.CRCP (CRCP Present)
config5VP	Boolean	Override Config5.VP
config6FTLBEn	Boolean	Override Config. V1  Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.AR (Anas removed Data cache) Override Config7.DCIDX_MODE
COURT DOIDY INODE		
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initializa-

config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction
C FILL	D 1	cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (External-
C FILID	D 1	ize sync)
config7WR	Boolean	Override Config7[31] bit (Alternative implementa-
C ZEDD	D 1	tion of Watch registers)
config7FPR	Boolean	Override Config7.FPR (one-half FPU clock ratio)
config7USP	Uns32	Override Config7.USP (USPRAM enable)
config7BTLM	Boolean	Override Config7.BTLM bit
config7BusSlp	Boolean	Override Config7.BusSlp bit
config7IVAD	Boolean	Override Config7.IVAD bit
config7RPS	Boolean	Override Config7.RPS bit
config7IAR_CPU0_VPE0	Boolean	Override Config7.IAR bit for CPU0/VPE0
config7IAR_CPU0_VPE1	Boolean	Override Config7.IAR bit for CPU0/VPE1
config7IAR_CPU0_VPE2	Boolean	Override Config7.IAR bit for CPU0/VPE2
config7IAR_CPU0_VPE3	Boolean	Override Config7.IAR bit for CPU0/VPE3
config7IAR_CPU1_VPE0	Boolean	Override Config7.IAR bit for CPU1/VPE0
config7IAR_CPU1_VPE1	Boolean	Override Config7.IAR bit for CPU1/VPE1
config7IAR_CPU1_VPE2	Boolean	Override Config7.IAR bit for CPU1/VPE2
config7IAR_CPU1_VPE3	Boolean	Override Config7.IAR bit for CPU1/VPE3
config7IAR_CPU2_VPE0	Boolean	Override Config7.IAR bit for CPU2/VPE0
config7IAR_CPU2_VPE1	Boolean	Override Config7.IAR bit for CPU2/VPE1
$config7IAR\_CPU2\_VPE2$	Boolean	Override Config7.IAR bit for CPU2/VPE2
config7IAR_CPU2_VPE3	Boolean	Override Config7.IAR bit for CPU2/VPE3
config7IAR_CPU3_VPE0	Boolean	Override Config7.IAR bit for CPU3/VPE0
config7IAR_CPU3_VPE1	Boolean	Override Config7.IAR bit for CPU3/VPE1
config7IAR_CPU3_VPE2	Boolean	Override Config7.IAR bit for CPU3/VPE2
config7IAR_CPU3_VPE3	Boolean	Override Config7.IAR bit for CPU3/VPE3
config7IAR_CPU4_VPE0	Boolean	Override Config7.IAR bit for CPU4/VPE0
config7IAR_CPU4_VPE1	Boolean	Override Config7.IAR bit for CPU4/VPE1
config7IAR_CPU4_VPE2	Boolean	Override Config7.IAR bit for CPU4/VPE2
config7IAR_CPU4_VPE3	Boolean	Override Config7.IAR bit for CPU4/VPE3
config7IAR_CPU5_VPE0	Boolean	Override Config7.IAR bit for CPU5/VPE0
config7IAR_CPU5_VPE1	Boolean	Override Config7.IAR bit for CPU5/VPE1
config7IAR_CPU5_VPE2	Boolean	Override Config7.IAR bit for CPU5/VPE2
config7IAR_CPU5_VPE3	Boolean	Override Config7.IAR bit for CPU5/VPE3
config7IAR_CPU6_VPE0	Boolean	Override Config7.IAR bit for CPU6/VPE0
config7IAR_CPU6_VPE1	Boolean	Override Config7.IAR bit for CPU6/VPE1
config7IAR_CPU6_VPE2	Boolean	Override Config7.IAR bit for CPU6/VPE2
config7IAR_CPU6_VPE3	Boolean	Override Config7.IAR bit for CPU6/VPE3
config7IAR_CPU7_VPE0	Boolean	Override Config7.IAR bit for CPU7/VPE0
config7IAR_CPU7_VPE1	Boolean	Override Config7.IAR bit for CPU7/VPE1
config7IAR_CPU7_VPE2	Boolean	Override Config7.IAR bit for CPU7/VPE2
config7IAR_CPU7_VPE3	Boolean	Override Config7.IAR bit for CPU7/VPE3
config7IVAD_CPU0_VPE0	Boolean	Override Config7.IVAD bit for CPU0/VPE0
config7IVAD_CPU0_VPE1	Boolean	Override Config7.IVAD bit for CPU0/VPE1
config7IVAD_CPU0_VPE2	Boolean	Override Config7.IVAD bit for CPU0/VPE2
config7IVAD_CPU0_VPE3	Boolean	Override Config7.IVAD bit for CPU0/VPE3
config7IVAD_CPU1_VPE0	Boolean	Override Config7.IVAD bit for CPU1/VPE0
config7IVAD_CPU1_VPE1	Boolean	Override Config7.IVAD bit for CPU1/VPE1
config7IVAD_CPU1_VPE2	Boolean	Override Config7.IVAD bit for CPU1/VPE2
config7IVAD_CPU1_VPE3	Boolean	Override Config7.IVAD bit for CPU1/VPE3
config7IVAD_CPU2_VPE0	Boolean	Override Config7.IVAD bit for CPU2/VPE0
config7IVAD_CPU2_VPE1	Boolean	Override Config7.IVAD bit for CPU2/VPE1  Override Config7.IVAD bit for CPU2/VPE1
config7IVAD_CPU2_VPE2	Boolean	Override Config7.IVAD bit for CPU2/VPE1  Override Config7.IVAD bit for CPU2/VPE2
COING (IVAD_OF UZ_VFEZ	Doolean	Override Colligravad bit for CrU2/VrE2

C BIVAD CDITO VIDEO	D I	
config7IVAD_CPU2_VPE3	Boolean	Override Config7.IVAD bit for CPU2/VPE3
config7IVAD_CPU3_VPE0	Boolean	Override Config7.IVAD bit for CPU3/VPE0
config7IVAD_CPU3_VPE1	Boolean	Override Config7.IVAD bit for CPU3/VPE1
config7IVAD_CPU3_VPE2	Boolean	Override Config7.IVAD bit for CPU3/VPE2
config7IVAD_CPU3_VPE3	Boolean	Override Config7.IVAD bit for CPU3/VPE3
config7IVAD_CPU4_VPE0	Boolean	Override Config7.IVAD bit for CPU4/VPE0
config7IVAD_CPU4_VPE1	Boolean	Override Config7.IVAD bit for CPU4/VPE1
config7IVAD_CPU4_VPE2	Boolean	Override Config7.IVAD bit for CPU4/VPE2
config7IVAD_CPU4_VPE3	Boolean	Override Config7.IVAD bit for CPU4/VPE3
config7IVAD_CPU5_VPE0	Boolean	Override Config7.IVAD bit for CPU5/VPE0
config7IVAD_CPU5_VPE1	Boolean	Override Config7.IVAD bit for CPU5/VPE1
config7IVAD_CPU5_VPE2	Boolean	Override Config7.IVAD bit for CPU5/VPE2
config7IVAD_CPU5_VPE3	Boolean	Override Config7.IVAD bit for CPU5/VPE3
config7IVAD_CPU6_VPE0	Boolean	Override Config7.IVAD bit for CPU6/VPE0
config7IVAD_CPU6_VPE1	Boolean	Override Config7.IVAD bit for CPU6/VPE1
config7IVAD_CPU6_VPE2	Boolean	Override Config7.IVAD bit for CPU6/VPE2
config7IVAD_CPU6_VPE3	Boolean	Override Config7.IVAD bit for CPU6/VPE3
config7IVAD_CPU7_VPE0	Boolean	Override Config7.IVAD bit for CPU7/VPE0
config7IVAD_CPU7_VPE1	Boolean	Override Config7.IVAD bit for CPU7/VPE1
config7IVAD_CPU7_VPE2	Boolean	Override Config7.IVAD bit for CPU7/VPE2
config7IVAD_CPU7_VPE3	Boolean	Override Config7.IVAD bit for CPU7/VPE3
config7RPS_CPU0_VPE0	Boolean	Override Config7.RPS bit for CPU0/VPE0
config7RPS_CPU0_VPE1	Boolean	Override Config7.RPS bit for CPU0/VPE1
config7RPS_CPU0_VPE2	Boolean	Override Config7.RPS bit for CPU0/VPE2
config7RPS_CPU0_VPE3	Boolean	Override Config7.RPS bit for CPU0/VPE3
config7RPS_CPU1_VPE0	Boolean	Override Config7.RPS bit for CPU1/VPE0
config7RPS_CPU1_VPE1	Boolean	Override Config7.RPS bit for CPU1/VPE1
config7RPS_CPU1_VPE2	Boolean	Override Config7.RPS bit for CPU1/VPE2
config7RPS_CPU1_VPE3	Boolean	Override Config7.RPS bit for CPU1/VPE3
config7RPS_CPU2_VPE0	Boolean	Override Config7.RPS bit for CPU2/VPE0
config7RPS_CPU2_VPE1	Boolean	Override Config7.RPS bit for CPU2/VPE1
config7RPS_CPU2_VPE2	Boolean	Override Config7.RPS bit for CPU2/VPE2
config7RPS_CPU2_VPE3	Boolean	Override Config7.RPS bit for CPU2/VPE3
config7RPS_CPU3_VPE0	Boolean	Override Config7.RPS bit for CPU3/VPE0
config7RPS_CPU3_VPE1	Boolean	Override Config7.RPS bit for CPU3/VPE1
config7RPS_CPU3_VPE2	Boolean	Override Config7.RPS bit for CPU3/VPE2
config7RPS_CPU3_VPE3	Boolean	Override Config7.RPS bit for CPU3/VPE3
config7RPS_CPU4_VPE0	Boolean	Override Config7.RPS bit for CPU4/VPE0
config7RPS_CPU4_VPE1	Boolean	Override Config7.RPS bit for CPU4/VPE1
config7RPS_CPU4_VPE2	Boolean	Override Config7.RPS bit for CPU4/VPE2
config7RPS_CPU4_VPE3	Boolean	Override Config7.RPS bit for CPU4/VPE3
config7RPS_CPU5_VPE0	Boolean	Override Config7.RPS bit for CPU5/VPE0
config7RPS_CPU5_VPE1	Boolean	Override Config7.RPS bit for CPU5/VPE1
config7RPS_CPU5_VPE2	Boolean	Override Config7.RPS bit for CPU5/VPE2
config7RPS_CPU5_VPE3	Boolean	Override Config7.RPS bit for CPU5/VPE3
config7RPS_CPU6_VPE0	Boolean	Override Config7.RPS bit for CPU6/VPE0
config7RPS_CPU6_VPE1	Boolean	Override Config7.RPS bit for CPU6/VPE1
config7RPS_CPU6_VPE2	Boolean	Override Config7.RPS bit for CPU6/VPE2
config7RPS_CPU6_VPE3	Boolean	Override Config7.RPS bit for CPU6/VPE3
config7RPS_CPU7_VPE0	Boolean	Override Config7.RPS bit for CPU7/VPE0
config7RPS_CPU7_VPE1	Boolean	Override Config7.RPS bit for CPU7/VPE1
config7RPS_CPU7_VPE2	Boolean	Override Config7.RPS bit for CPU7/VPE2
config7RPS_CPU7_VPE3	Boolean	Override Config7.RPS bit for CPU7/VPE3
statusFR	Boolean	Override power on value in Status.FR (Floating
		point register mode)

fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/SNaN encodings
	** 00	match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
srsconf0SRS1	Uns32	Override the SRS1 field in SRSConf0 register
srsconf0SRS2	Uns32	Override the SRS2 field in SRSConf0 register
srsconf0SRS3	Uns32	Override the SRS3 field in SRSConf0 register
wiredLimit	Uns32	Override Limit field of the Wired register
wiredLimitBits	Uns32	Override width of Limit field of the Wired register
wiredWiredBits	Uns32	Override width of Wired field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
parityEnable	Uns32	Specify error detection support: 0 - none; 1 - parity; 2 - ECC
useMpTb	Boolean	Override Use of multi-processor test bench
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use
ExceptionBase	0 11592	GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the cor-
OseExceptionDase	Doolean	responding BEV address bits
l1BufferCache	Boolean	L1 Buffer Cache
GCU_EX	Boolean	
		CMP system only: GCR custom block present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable
SWINTINGOTABLE	Boolean	within cluster
PERFCNT_ROUTABLE	Boolean	CMP system only: performance counter interrupt
		routable within cluster
FDC_ROUTABLE	Boolean	CMP system only: fast debug channel interrupt
		routable within cluster
GCR_PCORES	Uns32	CMP system only: override
		GCR_CONFIG.PCORES (number of cores-1)
GCR_ADDR_REGIONS	Uns32	CMP system only: override
		GCR_CONFIG.ADDR_REGIONS (number of
		MMIO address regions)
GCR_NUMAUX	Uns32	CMP system only: override
		GCR_CONFIG.NUMAUX (number of auxil-
		iary memory ports)
GCR_BASE	Uns64	CMP system only: override
		GCR_BASE.GCR_BASE (default GCR regis-
		ter address)
GCR_MINOR_REV	Uns32	CMP system only: override
	0 0 -	GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override
3 3 10 11 11 11 11 11 11 11 11 11 11 11 11	011502	GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override
COLOR OF THE PROPERTY OF THE P	011502	GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV		CMP system only: override
O C10_C/1C11H_W1/10 O10_10H V	Unc39	
	Uns32	
		GCR_CACHE_REV.MAJOR_REV
GCR_L2_ASSOC	Uns32 Uns32	GCR_CACHE_REV.MAJOR_REV  CMP system only: override
GCR_L2_ASSOC	Uns32	GCR_CACHE_REV.MAJOR_REV  CMP system only: override GCR_L2_CONFIG.ASSOC
		GCR_CACHE_REV.MAJOR_REV  CMP system only: override GCR_L2_CONFIG.ASSOC  CMP system only: override
GCR_L2_ASSOC	Uns32	GCR_CACHE_REV.MAJOR_REV  CMP system only: override GCR_L2_CONFIG.ASSOC

GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override
		GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GCR_BEV_BASE	Uns32	CMP system only: override GCR_BEV_BASE
GCR_KX_BASE_MODE	Boolean	
		CMP system only: override BEV_BASE_MODE & RESET_BASE_MODE
GCR_MMIO_REQ_LIMIT	Uns32	CMP system only: override
		GCR_MMIO_REQ_LIMIT.MMIO_REQ_LIMIT
		value
GCR_MMIO0_BOTTOM	Uns64	CMP system only: override GCR_MMIO0_BOTTOM register value
GCR_MMIO0_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO0_TOP.TOP_ADDR value
GCR_MMIO1_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO1_BOTTOM register value
GCR_MMIO1_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO1_TOP.TOP_ADDR value
GCR_MMIO2_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO2_BOTTOM register value
GCR_MMIO2_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO2_TOP.TOP_ADDR value
GCR_MMIO3_BOTTOM	Uns64	CMP system only: override
		GCR_MMIO3_BOTTOM register value
GCR_MMIO3_TOP_ADDR	Uns32	CMP system only: override
		GCR_MMIO3_TOP.TOP_ADDR value
GIC_NUMINTERRUPTS	Uns32	CMP system only: override
		GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override
		GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override
		GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override
		GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override
		GIC_SH_DBG_CONFIG.NUM_TEAMS
GIC_TRIG_RESET	Uns32	CMP system only: Zero value of
	**	GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override
		GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	· ·
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL_RAILDELAY
CPC_RESETLEN	Uns32	
CPC_RESETLEN	Ulis52	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override
	011502	CMI System only. Override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override
OI OLIVINIOOIGLIGII V	011502	CMI system only. Override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override
	011002	GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override
		GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override
		GIC_SH_GID_CONFIG[95_64]
<u> </u>		

GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
gicVirtualVPNum_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
gicVirtualVPNum_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
gicVirtualVPNum_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
gicVirtualVPNum_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
gicVirtualVPNum_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
gicVirtualVPNum_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
gicVirtualVPNum_CPU1_VP2	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
gicVirtualVPNum_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
gicVirtualVPNum_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
gicVirtualVPNum_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
gicVirtualVPNum_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
gicVirtualVPNum_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
gicVirtualVPNum_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0
gicVirtualVPNum_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
gicVirtualVPNum_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
gicVirtualVPNum_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
gicVirtualVPNum_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
gicVirtualVPNum_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
${\it gicVirtualVPNum\_CPU4\_VP2}$	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
gicVirtualVPNum_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
gicVirtualVPNum_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
gicVirtualVPNum_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
gicVirtualVPNum_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2

gicVirtualVPNum_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
gicVirtualVPNum_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
gicVirtualVPNum_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
gicVirtualVPNum_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
gicVirtualVPNum_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
gicVirtualVPNum_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
gicVirtualVPNum_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
gicVirtualVPNum_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
gicVirtualVPNum_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C4_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 4
GCR_C5_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 5
GCR_C6_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 6
GCR_C7_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 7
GCR_C8_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 8
GCR_C9_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 9
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 2
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 3
GCR_C4_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 4
GCR_C5_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 5
GCR_C6_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 6
GCR_C7_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 7
GCR_C8_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 8

GCR_C9_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 9
CPC_C0_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 0
CPC_C1_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 1
CPC_C2_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 2
CPC_C3_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 3
CPC_C4_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 4
CPC_C5_VP_EN	Uns32	CMP system only: CPC-VP-EN for core 5
CPC_C6_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 6
CPC_C7_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 7
CPC_C8_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 8
CPC_C9_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 9
EIC_OPTION	Uns32	Override the external interrupt controller
		EIC_OPTION
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register
guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register
guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest IPFDC field in IntCtl register
guestintctlIPPCI	Uns32	Override the Guest IPPCI field in IntCtl register
guestintctlIPTI_CPU0_VP0	Uns32	Override the IPTI field in IntCtl register for CPU0/VP0
guestintctlIPTI_CPU0_VP1	Uns32	Override the IPTI field in IntCtl register for CPU0/VP1
guestintctlIPTI_CPU0_VP2	Uns32	Override the IPTI field in IntCtl register for CPU0/VP2
guestintctlIPTI_CPU0_VP3	Uns32	Override the IPTI field in IntCtl register for CPU0/VP3
guestintctlIPTI_CPU1_VP0	Uns32	Override the IPTI field in IntCtl register for CPU1/VP0
guestintctlIPTI_CPU1_VP1	Uns32	Override the IPTI field in IntCtl register for CPU1/VP1
$guestintctlIPTI\_CPU1\_VP2$	Uns32	Override the IPTI field in IntCtl register for CPU1/VP2
guestintctlIPTI_CPU1_VP3	Uns32	Override the IPTI field in IntCtl register for CPU1/VP3
guestintctlIPTI_CPU2_VP0	Uns32	Override the IPTI field in IntCtl register for CPU2/VP0
guestintctlIPTI_CPU2_VP1	Uns32	Override the IPTI field in IntCtl register for CPU2/VP1
guestintctlIPTI_CPU2_VP2	Uns32	Override the IPTI field in IntCtl register for CPU2/VP2
guestintctlIPTI_CPU2_VP3	Uns32	Override the IPTI field in IntCtl register for CPU2/VP3
guestintctlIPTI_CPU3_VP0	Uns32	Override the IPTI field in IntCtl register for CPU3/VP0

guestintctlIPTI_CPU3_VP1	Uns32	Override the IPTI field in IntCtl register for CPU3/VP1
guestintctlIPTI_CPU3_VP2	Uns32	Override the IPTI field in IntCtl register for CPU3/VP2
guestintctlIPTI_CPU3_VP3	Uns32	Override the IPTI field in IntCtl register for CPU3/VP3
guestintctlIPTI_CPU4_VP0	Uns32	Override the IPTI field in IntCtl register for CPU4/VP0
guestintctlIPTI_CPU4_VP1	Uns32	Override the IPTI field in IntCtl register for CPU4/VP1
guestintctlIPTI_CPU4_VP2	Uns32	Override the IPTI field in IntCtl register for CPU4/VP2
guestintctlIPTI_CPU4_VP3	Uns32	Override the IPTI field in IntCtl register for CPU4/VP3
guestintctlIPTI_CPU5_VP0	Uns32	Override the IPTI field in IntCtl register for CPU5/VP0
guestintctlIPTI_CPU5_VP1	Uns32	Override the IPTI field in IntCtl register for CPU5/VP1
guestintctlIPTI_CPU5_VP2	Uns32	Override the IPTI field in IntCtl register for CPU5/VP2
guestintctlIPTI_CPU5_VP3	Uns32	Override the IPTI field in IntCtl register for CPU5/VP3
guestintctlIPTI_CPU6_VP0	Uns32	Override the IPTI field in IntCtl register for CPU6/VP0
guestintctlIPTI_CPU6_VP1	Uns32	Override the IPTI field in IntCtl register for CPU6/VP1
guestintctlIPTI_CPU6_VP2	Uns32	Override the IPTI field in IntCtl register for CPU6/VP2
guestintctlIPTI_CPU6_VP3	Uns32	Override the IPTI field in IntCtl register for CPU6/VP3
guestintctlIPTI_CPU7_VP0	Uns32	Override the IPTI field in IntCtl register for CPU7/VP0
guestintctlIPTI_CPU7_VP1	Uns32	Override the IPTI field in IntCtl register for CPU7/VP1
guestintctlIPTI_CPU7_VP2	Uns32	Override the IPTI field in IntCtl register for CPU7/VP2
guestintctlIPTI_CPU7_VP3	Uns32	Override the IPTI field in IntCtl register for CPU7/VP3
guestintctlIPFDC_CPU0_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP0
guestintctlIPFDC_CPU0_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP1
guestintctlIPFDC_CPU0_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP2
guestintctlIPFDC_CPU0_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU0/VP3
guestintctlIPFDC_CPU1_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP0
guestintctlIPFDC_CPU1_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP1
guestintctlIPFDC_CPU1_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP2
guestintctlIPFDC_CPU1_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU1/VP3
guestintctlIPFDC_CPU2_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP0

guestintctlIPFDC_CPU2_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP1
guestintctlIPFDC_CPU2_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP2
guestintctlIPFDC_CPU2_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU2/VP3
guestintctlIPFDC_CPU3_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP0
guestintctlIPFDC_CPU3_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP1
guestintctlIPFDC_CPU3_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP2
guestintctlIPFDC_CPU3_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU3/VP3
guestintctlIPFDC_CPU4_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP0
guestintctlIPFDC_CPU4_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP1
guestintctlIPFDC_CPU4_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP2
guestintctlIPFDC_CPU4_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU4/VP3
guestintctlIPFDC_CPU5_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP0
guestintctlIPFDC_CPU5_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP1
guestintctlIPFDC_CPU5_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP2
guestintctlIPFDC_CPU5_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU5/VP3
guestintctlIPFDC_CPU6_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP0
guestintctlIPFDC_CPU6_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP1
guestintctlIPFDC_CPU6_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP2
guestintctlIPFDC_CPU6_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU6/VP3
guestintctlIPFDC_CPU7_VP0	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP0
guestintctlIPFDC_CPU7_VP1	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP1
guestintctlIPFDC_CPU7_VP2	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP2
guestintctlIPFDC_CPU7_VP3	Uns32	Override the IPFDC field in IntCtl register for CPU7/VP3
guestintctlIPPCI_CPU0_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP0
guestintctlIPPCI_CPU0_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP1
guestintctlIPPCI_CPU0_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP2
guestintctlIPPCI_CPU0_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU0/VP3
guestintctlIPPCI_CPU1_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP0

guestintctlIPPCI_CPU1_VP1	Uns32	Override the IPPCI field in IntCtl register for
		CPU1/VP1
guestintctlIPPCI_CPU1_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP2
guestintctlIPPCI_CPU1_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU1/VP3
guestintctlIPPCI_CPU2_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP0
guestintctlIPPCI_CPU2_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP1
guestintctlIPPCI_CPU2_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP2
guestintctlIPPCI_CPU2_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU2/VP3
guestintctlIPPCI_CPU3_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP0
guestintctlIPPCI_CPU3_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP1
guestintctlIPPCI_CPU3_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP2
guestintctlIPPCI_CPU3_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU3/VP3
guestintctlIPPCI_CPU4_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP0
guestintctlIPPCI_CPU4_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP1
guestintctlIPPCI_CPU4_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP2
guestintctlIPPCI_CPU4_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU4/VP3
guestintctlIPPCI_CPU5_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP0
guestintctlIPPCI_CPU5_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP1
guestintctlIPPCI_CPU5_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP2
guestintctlIPPCI_CPU5_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU5/VP3
guestintctlIPPCI_CPU6_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP0
guestintctlIPPCI_CPU6_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP1
guestintctlIPPCI_CPU6_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP2
guestintctlIPPCI_CPU6_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU6/VP3
guestintctlIPPCI_CPU7_VP0	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP0
guestintctlIPPCI_CPU7_VP1	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP1
guestintctlIPPCI_CPU7_VP2	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP2
guestintctlIPPCI_CPU7_VP3	Uns32	Override the IPPCI field in IntCtl register for CPU7/VP3
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2( <ispram bytes="" in="" size="">) - 11)</ispram>
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region

ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used
		to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior
		to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region
		$(\log 2(< DSPRAM \text{ size in bytes}) - 11)$
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag
		(used to enable the DSPRAM region prior to re-
		set)
DSPRAM_PRESENT	Boolean	DSPRAM is present with SAAR
USPRAM_SIZE	Uns32	Encoded size of the USPRAM region
		$(\log 2(\langle \text{USPRAM size in bytes} \rangle) - 11)$
USPRAM_BASE	Uns64	Starting physical address of the USPRAM region
USPRAM_ENABLE	Boolean	Set the enable bit of the USPRAM region's tag
		(used to enable the USPRAM region prior to re-
		set)
USPRAM_FILE	String	Load a MIPS hex file into the USPRAM region
		prior to reset
misalignedDataException	Enumeration	Select misaligned data access exception signaling:
		never, checkCCA or always (never, checkCCA or
		always)
commitTlbwErr	Boolean	Commit TLBWI/TLBRI on ECC; in
		MIPS_DV_MODE only

Table 8.5: Parameters that can be set in: VP

## 8.3 Parameter values

These are the current parameter values.

Name	Value
(Others)	
endian	none
cacheenable	default
cachedebug	0
cacheextbiuinfo	0x0
mipsHexFile	
IMPERAS_MIPS_AVP_OPCODES	F
cacheIndexBypassTLB	F
MIPS_TRACE	F
gprNames	F
supervisorMode	F
busErrors	Т
fixedMMU	F
fixedDbgRegSize	F
removeDSP	F
removeCMP	F
removeFP	F
removeFTLB	F
isISA	F

hiddenTLBentries	F
perfCounters	0
ITCNumEntries	0
ITCNumFIFO	0
ITCFIFODepth	0
ITCEmptyOnReset	F
MTFPU	0
	F
supportDenormals VPE0MaxTC	0
VPE1MaxTC	0
	0
segBits	
mpuRegions	0
mpuType	F
mpuEnable	
mpuSegment0	0
mpuSegment1	0
mpuSegment2	0
mpuSegment3	0
mpuSegment4	0
mpuSegment5	0
mpuSegment6	0
mpuSegment7	0
mpuSegment8	0
mpuSegment9	0
mpuSegment10	0
mpuSegment11	0
mpuSegment12	0
mpuSegment13	0
mpuSegment14	0
mpuSegment15	0
mvpconf0vpe	0
tcDisable	0
vpeDisable	0
mvpconf0tc	0
mvpconf0pcp	F
mvpconf0tcp	F
mvpconf1c1f	F
mvpcontrolPolicyMode	F
hasFDC	0
licenseWarningDays	15
MIPS_UHI	F
mipsUhiArgs	
mipsUhiJail	
MIPS_DV_MODE	F
MIPS_MAGIC_OPCODES	F

11 55 11	
enableTrickbox	F
fpuexcdisable	F
TRU_PRESENT	F
ucLLwordsLocked	0
FUSA	F
CPC_FAULT_SUPPORTED	0
CPC_FAULT_ENABLE	0
cop2Bits	32
cop2FileName	
udiConfig	0
udiFileName	
vectoredinterrupt	F
externalinterrupt	F
config3VEIC_VPE0	F
config3VEIC_VPE1	F
config3VEIC_VPE2	F
config3VEIC_VPE3	F
rootFixedMMU	F
rootMMUSizeM1	0
srsctlHSS	0
firPS	0
firHas2008	0
usePreciseFpu	0
simulateLite	
	INONE
	NONE 0
pridCompanyOptions	0 0
pridCompanyOptions pridRevision	0
pridCompanyOptions pridRevision globalClusterNum	0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI	0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC	0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI	0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch	0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP	0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP	0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart	0 0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVP sharedTLBindex	0 0 0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified	0 0 0 0 0 0 0 0 0 0 0 0 F
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0	0 0 0 0 0 0 0 0 0 0 0 0 F
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1	0 0 0 0 0 0 0 0 0 0 0 0 F
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2	0 0 0 0 0 0 0 0 0 0 0 F
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU0_VP3	0 0 0 0 0 0 0 0 0 0 0 F 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU0_VP3 intctlIPTI_CPU1_VP0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU0_VP3 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP1 intctlIPTI_CPU1_VP2	0 0 0 0 0 0 0 0 0 0 0 F 0 0 0 0 0 0 0 0
pridCompanyOptions pridRevision globalClusterNum intctlIPTI intctlIPFDC intctlIPPCI numWatch maxVP numVP numVPtoStart sharedTLBindex xconfigSpecified intctlIPTI_CPU0_VP0 intctlIPTI_CPU0_VP1 intctlIPTI_CPU0_VP2 intctlIPTI_CPU0_VP3 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP0 intctlIPTI_CPU1_VP1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

intctlIPTI_CPU2_VP1	0
intctlIPTI_CPU2_VP2	0
intctlIPTI_CPU2_VP3	0
intctlIPTI_CPU3_VP0	0
intctlIPTI_CPU3_VP1	0
intctlIPTI_CPU3_VP2	0
intctlIPTI_CPU3_VP3	0
intctlIPTI_CPU4_VP0	0
intctlIPTI_CPU4_VP1	0
intctlIPTI_CPU4_VP2	0
intctlIPTI_CPU4_VP3	0
intctlIPTI_CPU5_VP0	0
intctlIPTI_CPU5_VP1	0
intctlIPTI_CPU5_VP2	0
intctlIPTI_CPU5_VP3	0
intctlIPTI_CPU6_VP0	0
intctlIPTI_CPU6_VP1	0
intctlIPTI_CPU6_VP2	0
intctlIPTI_CPU6_VP3	0
intctlIPTI_CPU7_VP0	0
intctlIPTI_CPU7_VP1	0
intctlIPTI_CPU7_VP2	0
intctlIPTI_CPU7_VP3	0
intctlIPFDC_CPU0_VP0	0
intctlIPFDC_CPU0_VP1	0
intctlIPFDC_CPU0_VP2	0
intctlIPFDC_CPU0_VP3	0
intctlIPFDC_CPU1_VP0	0
intctlIPFDC_CPU1_VP1	0
intctlIPFDC_CPU1_VP2	0
intctlIPFDC_CPU1_VP3	0
intctlIPFDC_CPU2_VP0	0
intctlIPFDC_CPU2_VP1	0
intctlIPFDC_CPU2_VP2	0
intctlIPFDC_CPU2_VP3	0
intctlIPFDC_CPU3_VP0	0
intctlIPFDC_CPU3_VP1	0
intctlIPFDC_CPU3_VP2	0
intctlIPFDC_CPU3_VP3	0
intctlIPFDC_CPU4_VP0	0
intctlIPFDC_CPU4_VP1	0
intctlIPFDC_CPU4_VP2	0
intctlIPFDC_CPU4_VP3	0
intctlIPFDC_CPU5_VP0	0
intctlIPFDC_CPU5_VP1	0

intctlIPFDC_CPU5_VP2	0
intetliPFDC_CPU5_VP3	
intetlIPFDC_CPU6_VP0	0
intctlPFDC_CPU6_VP0	0
intctlPFDC_CPU6_VP1	0
intctlPFDC_CPU6_VP2	0
intctlIPFDC_CPU7_VP0	0
intctlIPFDC_CPU7_VP1	0
intetlIPFDC_CPU7_VP2	0
intetlIPFDC_CPU7_VP3	0
intctlIPPCI_CPU0_VP0	0
intctlIPPCI_CPU0_VP1	0
intctlIPPCI_CPU0_VP2	0
intctlIPPCI_CPU0_VP3	0
intctlIPPCI_CPU1_VP0	0
intctlIPPCI_CPU1_VP1	0
intctlIPPCI_CPU1_VP2	0
intctlIPPCI_CPU1_VP3	0
intctlIPPCI_CPU2_VP0	0
intctlIPPCI_CPU2_VP1	0
intctlIPPCI_CPU2_VP2	0
intctlIPPCI_CPU2_VP3	0
intctlIPPCI_CPU3_VP0	0
intctlIPPCI_CPU3_VP1	0
intctlIPPCI_CPU3_VP2	0
intctlIPPCI_CPU3_VP3	0
intctlIPPCI_CPU4_VP0	0
intctlIPPCI_CPU4_VP1	0
intctlIPPCI_CPU4_VP2	0
intctlIPPCI_CPU4_VP3	0
intctlIPPCI_CPU5_VP0	0
intctlIPPCI_CPU5_VP1	0
intctlIPPCI_CPU5_VP2	0
intctlIPPCI_CPU5_VP3	0
intctlIPPCI_CPU6_VP0	0
intctlIPPCI_CPU6_VP1	0
intctlIPPCI_CPU6_VP2	0
intctlIPPCI_CPU6_VP3	0
intctlIPPCI_CPU7_VP0	0
intctlIPPCI_CPU7_VP1	0
intctlIPPCI_CPU7_VP2	0
intctlIPPCI_CPU7_VP3	0
segcfg0PA	0
segcfg1PA	0
segcfg2PA	0

C and	
segcfg3PA	0
segcfg4PA	0
segcfg5PA	0
segcfg0AM	0
segcfg1AM	0
segcfg2AM	0
segcfg3AM	0
segcfg4AM	0
segcfg5AM	0
segcfg0EU	0
segcfg1EU	0
segcfg2EU	0
segcfg3EU	0
segcfg4EU	0
segcfg5EU	0
segcfg0C	0
segcfg1C	0
segcfg2C	0
segcfg3C	0
segcfg4C	0
segcfg5C	0
cdmmSize	0
configAR	0
configBM	0
configDSP	F
configISP	F
configK0	0
configKU	0
configK23	0
configMDU	F
configMM	F
configMT	0
configSB	F
configBCP	F
MIPS16eASE	F
config1DA	0
config1DL	0
config1DS	0
config1EP	F
config1IA	0
config1IL	0
config1IS	0
config1MMUSizeM1	0
config1MMUSizeM1_VPE1	0
config1MMUSizeM1_VPE2	0

config1MMUSizeM1_VPE3	0
config1WR	F
config1PC	F
config1C2	F
config2SU	0
config2SS	0
config2SL	0
config2SA	0
config3BI	F
config3BP	F
config3CDMM	F
config3CTXTC	F
config3DSPP	F
config3DSP2P	F
config3IPLW	0
config3ISA	0
config3ISAOnExc	F
config3ITL	F
config3LPA	F
config3MCU	F
config3MMAR	0
config3RXI	F
config3SC	F
config3ULRI	F
config3VZ	F
config3MSAP	F
config3CMGCR	F
config3SP	F
config3TL	0
config3PW	F
config4AE	F
config4IE	0
config4MMUConfig	0
config4MMUExtDef	0
config4VTLBSizeExt	0
config4KScrExist	0
config5EVA	F
config5LLB	F
config5MRP	F
config5NFExists	F
mips32Macro	F
config5MSAEn	F
config5MVH	F
config5DEC	F
config5GI	0

config5CRCP	F
config5VP	F
config6FTLBEn	F
config7AR	F
config7DCIDX_MODE	0
config7HCI	F
config7IAR	F
config7WII	F
config7ES	0
config7WR	F
config7FPR	F
config7USP	0
config7BTLM	F
config7BusSlp	F
config7IVAD	F
config7RPS	F
config7IAR_CPU0_VPE0	F
config7IAR_CPU0_VPE1	F
config7IAR_CPU0_VPE2	F
config7IAR_CPU0_VPE3	F
config7IAR_CPU1_VPE0	F
config7IAR_CPU1_VPE1	F
config7IAR_CPU1_VPE2	F
config7IAR_CPU1_VPE3	F
config7IAR_CPU2_VPE0	F
config7IAR_CPU2_VPE1	F
config7IAR_CPU2_VPE2	F
config7IAR_CPU2_VPE3	F
config7IAR_CPU3_VPE0	F
config7IAR_CPU3_VPE1	F
config7IAR_CPU3_VPE2	F
config7IAR_CPU3_VPE3	F
config7IAR_CPU4_VPE0	F
config7IAR_CPU4_VPE1	F
config7IAR_CPU4_VPE2	F
config7IAR_CPU4_VPE3	F
config7IAR_CPU5_VPE0	F
config7IAR_CPU5_VPE1	F
$config7IAR\_CPU5\_VPE2$	F
config7IAR_CPU5_VPE3	F
config7IAR_CPU6_VPE0	F
config7IAR_CPU6_VPE1	F
config7IAR_CPU6_VPE2	F
config7IAR_CPU6_VPE3	F
config7IAR_CPU7_VPE0	F

config7IAR_CPU7_VPE1	F
config7IAR_CPU7_VPE2	F
config7IAR_CPU7_VPE3	F
config7IVAD_CPU0_VPE0	F
config7IVAD_CPU0_VPE1	F
config7IVAD_CPU0_VPE2	F
config7IVAD_CPU0_VPE3	F
config7IVAD_CPU1_VPE0	F
config7IVAD_CPU1_VPE1	F
config7IVAD_CPU1_VPE2	F
config7IVAD_CPU1_VPE3	F
config7IVAD_CPU2_VPE0	F
config7IVAD_CPU2_VPE1	F
config7IVAD_CPU2_VPE2	F
config7IVAD_CPU2_VPE3	F
config7IVAD_CPU3_VPE0	F
config7IVAD_CPU3_VPE1	F
config7IVAD_CPU3_VPE2	F
config7IVAD_CPU3_VPE3	F
config7IVAD_CPU4_VPE0	F
config7IVAD_CPU4_VPE1	F
config7IVAD_CPU4_VPE2	F
config7IVAD_CPU4_VPE3	F
config7IVAD_CPU5_VPE0	F
config7IVAD_CPU5_VPE1	F
config7IVAD_CPU5_VPE2	F
config7IVAD_CPU5_VPE3	F
config7IVAD_CPU6_VPE0	F
config7IVAD_CPU6_VPE1	F
config7IVAD_CPU6_VPE2	F
config7IVAD_CPU6_VPE3	F
config7IVAD_CPU7_VPE0	F
config7IVAD_CPU7_VPE1	F
config7IVAD_CPU7_VPE2	F
config7IVAD_CPU7_VPE3	F
config7RPS_CPU0_VPE0	F
config7RPS_CPU0_VPE1	F
config7RPS_CPU0_VPE2	F
config7RPS_CPU0_VPE3	F
config7RPS_CPU1_VPE0	F
config7RPS_CPU1_VPE1	F
config7RPS_CPU1_VPE2	F
config7RPS_CPU1_VPE3	F
config7RPS_CPU2_VPE0	F
config7RPS_CPU2_VPE1	F

config7RPS_CPU2_VPE3         F           config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrNAN2008         F           mumMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         <		
config7RPS_CPU3_VPE0         F           config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredDirectric         F     <	config7RPS_CPU2_VPE2	
config7RPS_CPU3_VPE1         F           config7RPS_CPU3_VPE2         F           config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0     <		
config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           codmmBaseCI         F	config7RPS_CPU3_VPE0	
config7RPS_CPU3_VPE3         F           config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           fcsrABS2008         F           fcsrABS2008         F           fcsrANN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredLimitBits         0           wiredSite         0           cdmmBaseCI         F	config7RPS_CPU3_VPE1	
config7RPS_CPU4_VPE0         F           config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         F           UseException	config7RPS_CPU3_VPE2	F
config7RPS_CPU4_VPE1         F           config7RPS_CPU4_VPE2         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           mumMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         F           IlBufferCache         F           GCU_EX	config7RPS_CPU3_VPE3	F
config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           mumMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         F           IlBufferCache         F           GCU_EX         F           TIMER_ROUTABLE         F	config7RPS_CPU4_VPE0	F
config7RPS_CPU4_VPE3         F           config7RPS_CPU5_VPE0         F           config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         F           IlBufferCache         F           GCU_EX         F           GIC_EX         F	config7RPS_CPU4_VPE1	F
config7RPS_CPU5_VPE0 config7RPS_CPU5_VPE1 config7RPS_CPU5_VPE2 config7RPS_CPU5_VPE3 config7RPS_CPU6_VPE0 config7RPS_CPU6_VPE0 config7RPS_CPU6_VPE1 config7RPS_CPU6_VPE1 config7RPS_CPU6_VPE2 config7RPS_CPU6_VPE3 config7RPS_CPU6_VPE3 config7RPS_CPU7_VPE0 config7RPS_CPU7_VPE0 config7RPS_CPU7_VPE1 config7RPS_CPU7_VPE2 config7RPS_CPU7_VPE3 statusFR fcsrABS2008 fcsrNAN2008 mumMaarRegs 6 srsconf0SRS1 srsconf0SRS2 srsconf0SRS3 wiredLimit 0 wiredLimitBits 0 wiredWiredBits 0 cdmmBaseCI parityEnable useMpTb ExceptionBase IlbufferCache GCU_EX GIC_EX CPC_EX TIMER_ROUTABLE FERFCNT_ROUTABLE FERFCNT_ROUTABLE FERFCNT_ROUTABLE FERFCNT_ROUTABLE FERFCNT_ROUTABLE FF	config7RPS_CPU4_VPE2	F
config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         F           UseExceptionBase         F           IlBufferCache         F           GCU_EX         F           GIC_EX         F           TIMER_ROUTABLE         F	config7RPS_CPU4_VPE3	F
config7RPS_CPU5_VPE1         F           config7RPS_CPU5_VPE2         F           config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         F           IlBufferCache         F           GCU_EX         F           GIC_EX         F           TIMER_ROUTABLE         F           PERFCNT_ROUTABLE         F </td <td>config7RPS_CPU5_VPE0</td> <td>F</td>	config7RPS_CPU5_VPE0	F
config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           IlBufferCache         F           GCU_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           PERFCNT_ROUTABLE         F	config7RPS_CPU5_VPE1	F
config7RPS_CPU5_VPE3         F           config7RPS_CPU6_VPE0         F           config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           IlBufferCache         F           GCU_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           PERFCNT_ROUTABLE         F	config7RPS_CPU5_VPE2	F
config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           I1BufferCache         F           GCU_EX         F           GIC_EX         F           TIMER_ROUTABLE         F           PERFCNT_ROUTABLE         F	_	F
config7RPS_CPU6_VPE1         F           config7RPS_CPU6_VPE2         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           I1BufferCache         F           GCU_EX         F           GIC_EX         F           TIMER_ROUTABLE         F           PERFCNT_ROUTABLE         F	config7RPS_CPU6_VPE0	F
config7RPS_CPU6_VPE3         F           config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F		F
config7RPS_CPU6_VPE3         F           config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         T           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	_	F
config7RPS_CPU7_VPE0         F           config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           I1BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	_	F
config7RPS_CPU7_VPE1         F           config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           I1BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F		F
config7RPS_CPU7_VPE2         F           config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F		F
config7RPS_CPU7_VPE3         F           statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F		F
statusFR         F           fcsrABS2008         F           fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F		F
fcsrNAN2008         F           numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F		F
numMaarRegs         6           srsconf0SRS1         0           srsconf0SRS2         0           wiredLimit         0           wiredLimitBits         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           l1BufferCache         F           GCU_EX         F           GIC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	fcsrABS2008	F
srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	fcsrNAN2008	F
srsconf0SRS1         0           srsconf0SRS2         0           srsconf0SRS3         0           wiredLimit         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	numMaarRegs	6
srsconf0SRS3         0           wiredLimit         0           wiredLimitBits         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           l1BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	srsconf0SRS1	0
wiredLimit         0           wiredLimitBits         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	srsconf0SRS2	0
wiredLimitBits         0           wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	srsconf0SRS3	0
wiredWiredBits         0           cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	wiredLimit	0
cdmmBaseCI         F           parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           11BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	wiredLimitBits	0
parityEnable         1           useMpTb         T           ExceptionBase         0           UseExceptionBase         F           l1BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	wiredWiredBits	0
useMpTb         T           ExceptionBase         0           UseExceptionBase         F           l1BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	cdmmBaseCI	F
useMpTb         T           ExceptionBase         0           UseExceptionBase         F           l1BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F	parityEnable	1
ExceptionBase         0           UseExceptionBase         F           l1BufferCache         F           GCU_EX         F           GIC_EX         F           CPC_EX         F           TIMER_ROUTABLE         F           SWINT_ROUTABLE         F           PERFCNT_ROUTABLE         F		T
UseExceptionBase F  I1BufferCache F  GCU_EX F  GIC_EX F  CPC_EX F  TIMER_ROUTABLE F  SWINT_ROUTABLE F  PERFCNT_ROUTABLE F		0
11BufferCacheFGCU_EXFGIC_EXFCPC_EXFTIMER_ROUTABLEFSWINT_ROUTABLEFPERFCNT_ROUTABLEF		
GCU_EX F GIC_EX F CPC_EX F TIMER_ROUTABLE F SWINT_ROUTABLE F PERFCNT_ROUTABLE F		
GIC_EX F CPC_EX F TIMER_ROUTABLE F SWINT_ROUTABLE F PERFCNT_ROUTABLE F		
CPC_EX F TIMER_ROUTABLE F SWINT_ROUTABLE F PERFCNT_ROUTABLE F		
TIMER_ROUTABLE F SWINT_ROUTABLE F PERFCNT_ROUTABLE F		
SWINT_ROUTABLE F PERFCNT_ROUTABLE F		
PERFCNT_ROUTABLE F		
	FDC_ROUTABLE	

GCR_PCORES	0
GCR_ADDR_REGIONS	0
GCR_NUMAUX	0
GCR_BASE	0
GCR_MINOR_REV	0
GCR_MAJOR_REV	0
GCR_CACHE_MINOR_REV	0
GCR_CACHE_MAJOR_REV	0
GCR_L2_ASSOC	0
GCR_L2_SET_SIZE	0
GCR_SYS_CONFIG2_MAX_VP_WIDTH	0
GCR_IOCU1_MINOR_REV	0
GCR_IOCU1_MAJOR_REV	0
GCR_BEV_BASE	0
GCR_KX_BASE_MODE	F
GCR_MMIO_REQ_LIMIT	0
GCR_MMIO0_BOTTOM	0
GCR_MMIO0_TOP_ADDR	0
GCR_MMIO1_BOTTOM	0
GCR_MMIO1_TOP_ADDR	0
GCR_MMIO2_BOTTOM	0
GCR_MMIO2_TOP_ADDR	0
GCR_MMIO3_BOTTOM	0
GCR_MMIO3_TOP_ADDR	0
GIC_NUMINTERRUPTS	0
GIC_COUNTBITS	0
GIC_MINOR_REV	0
GIC_MAJOR_REV	0
GIC_NUM_TEAMS	7
GIC_TRIG_RESET	0
GIC_PVPES	0
CPC_MICROSTEP	0
CPC_RAILDELAY	0
CPC_RESETLEN	0
CPC_MINOR_REV	0
CPC_MAJOR_REV	0
GIC_SH_GID_CONFIG31_0	0
GIC_SH_GID_CONFIG63_32	0
GIC_SH_GID_CONFIG95_64	0
GIC_SH_GID_CONFIG127_96	0
GIC_SH_GID_CONFIG159_128	0
GIC_SH_GID_CONFIG191_160	0
GIC_SH_GID_CONFIG223_192	0
GIC_SH_GID_CONFIG255_224	0
gicVirtualVPNum_CPU0_VP0	0

gicVirtualVPNum_CPU0_VP1	0
gicVirtualVPNum_CPU0_VP2	0
gicVirtualVPNum_CPU0_VP3	0
gicVirtualVPNum_CPU1_VP0	0
gicVirtualVPNum_CPU1_VP1	0
gicVirtualVPNum_CPU1_VP2	0
gicVirtualVPNum_CPU1_VP3	0
gicVirtualVPNum_CPU2_VP0	0
gicVirtualVPNum_CPU2_VP1	0
gicVirtualVPNum_CPU2_VP2	0
gicVirtualVPNum_CPU2_VP3	0
gicVirtualVPNum_CPU3_VP0	0
gicVirtualVPNum_CPU3_VP1	0
gicVirtualVPNum_CPU3_VP2	0
gicVirtualVPNum_CPU3_VP3	0
gicVirtualVPNum_CPU4_VP0	0
gicVirtualVPNum_CPU4_VP1	0
gicVirtualVPNum_CPU4_VP2	0
gicVirtualVPNum_CPU4_VP3	0
gicVirtualVPNum_CPU5_VP0	0
gicVirtualVPNum_CPU5_VP1	0
gicVirtualVPNum_CPU5_VP2	0
gicVirtualVPNum_CPU5_VP3	0
gicVirtualVPNum_CPU6_VP0	0
gicVirtualVPNum_CPU6_VP1	0
gicVirtualVPNum_CPU6_VP2	0
gicVirtualVPNum_CPU6_VP3	0
gicVirtualVPNum_CPU7_VP0	0
gicVirtualVPNum_CPU7_VP1	0
gicVirtualVPNum_CPU7_VP2	0
gicVirtualVPNum_CPU7_VP3	0
GCR_CO_RESET_BASE	0
GCR_C1_RESET_BASE	0
GCR_C2_RESET_BASE	0
GCR_C3_RESET_BASE	0
GCR_C4_RESET_BASE	0
GCR_C5_RESET_BASE	0
GCR_C6_RESET_BASE	0
GCR_C7_RESET_BASE	0
GCR_C8_RESET_BASE	0
GCR_C9_RESET_BASE	0
GCR_C0_RESET_EXT_BASE	0
GCR_C1_RESET_EXT_BASE	0
GCR_C1_RESET_EXT_BASE GCR_C2_RESET_EXT_BASE	
GCR_C2_RESET_EXT_BASE GCR_C3_RESET_EXT_BASE	0
GOU-O9-UESE1-EV1-DASE	0

GCR_C4_RESET_EXT_BASE	0
GCR_C5_RESET_EXT_BASE	0
GCR_C6_RESET_EXT_BASE	0
GCR_C7_RESET_EXT_BASE	0
GCR_C8_RESET_EXT_BASE	0
GCR_C9_RESET_EXT_BASE	0
CPC_C0_VP_EN	0
CPC_C1_VP_EN	0
CPC_C2_VP_EN	0
CPC_C3_VP_EN	0
CPC_C4_VP_EN	0
CPC_C5_VP_EN	0
CPC_C6_VP_EN	0
CPC_C7_VP_EN	0
CPC_C8_VP_EN	0
CPC_C9_VP_EN	0
EIC_OPTION	2
guestCtl0RI	0
guestCtl0MC	0
guestCtl0CP0	0
guestCtl0AT	0
guestCtl0GT	0
guestCtl0CG	0
guestCtl0CF	0
guestCtl0G1	0
guestCtl0RAD	0
guestCtl0DRG	0
hasImpl17	F
hasImpl16	F
guestintctlIPTI	0
guestintctlIPFDC	0
guestintctlIPPCI	0
guestintctlIPTI_CPU0_VP0	0
guestintctlIPTI_CPU0_VP1	0
guestintctlIPTI_CPU0_VP2	0
guestintctlIPTI_CPU0_VP3	0
guestintctlIPTI_CPU1_VP0	0
guestintctlIPTI_CPU1_VP1	0
guestintctlIPTI_CPU1_VP2	0
guestintctlIPTI_CPU1_VP3	0
guestintctlIPTI_CPU2_VP0	0
guestintctlIPTI_CPU2_VP1	0
guestintctlIPTI_CPU2_VP2	0
guestintctlIPTI_CPU2_VP3	0
guestintctlIPTI_CPU3_VP0	0

guestintctlIPTI_CPU3_VP1	0
guestintctlIPTI_CPU3_VP2	0
guestintctlIPTI_CPU3_VP3	0
guestintctlIPTI_CPU4_VP0	0
guestintctlIPTI_CPU4_VP1	0
guestintctlIPTI_CPU4_VP2	0
guestintctlIPTI_CPU4_VP3	0
guestintctlIPTI_CPU5_VP0	0
guestintctlIPTI_CPU5_VP1	0
guestintctlIPTI_CPU5_VP2	0
guestintctlIPTI_CPU5_VP3	0
guestintctlIPTI_CPU6_VP0	0
guestintctlIPTI_CPU6_VP1	0
guestintctlIPTI_CPU6_VP2	0
guestintctlIPTI_CPU6_VP3	0
guestintctlIPTI_CPU7_VP0	0
guestintctlIPTI_CPU7_VP1	0
guestintctlIPTI_CPU7_VP2	0
guestintctlIPTI_CPU7_VP3	0
guestintctlIPFDC_CPU0_VP0	0
guestintctlIPFDC_CPU0_VP1	0
guestintctlIPFDC_CPU0_VP2	0
guestintctlIPFDC_CPU0_VP3	0
guestintctlIPFDC_CPU1_VP0	0
guestintctlIPFDC_CPU1_VP1	0
guestintctlIPFDC_CPU1_VP2	0
guestintctlIPFDC_CPU1_VP3	0
guestintctlIPFDC_CPU2_VP0	0
guestintctlIPFDC_CPU2_VP1	0
guestintctlIPFDC_CPU2_VP2	0
guestintctlIPFDC_CPU2_VP3	0
guestintctlIPFDC_CPU3_VP0	0
guestintctlIPFDC_CPU3_VP1	0
guestintctlIPFDC_CPU3_VP2	0
guestintctlIPFDC_CPU3_VP3	0
guestintctlIPFDC_CPU4_VP0	0
guestintctlIPFDC_CPU4_VP1	0
guestintctlIPFDC_CPU4_VP2	0
guestintctlIPFDC_CPU4_VP3	0
guestintctlIPFDC_CPU5_VP0	0
guestintctlIPFDC_CPU5_VP1	0
guestintctlIPFDC_CPU5_VP2	0
guestintctlIPFDC_CPU5_VP3	0
guestintctlIPFDC_CPU6_VP0	0
guestintctlIPFDC_CPU6_VP1	0

1. 1 HIDED C CDITC VD0	
guestintctlIPFDC_CPU6_VP2	0
guestintctlIPFDC_CPU6_VP3	0
guestintctlIPFDC_CPU7_VP0	0
guestintctlIPFDC_CPU7_VP1	0
guestintctlIPFDC_CPU7_VP2	0
guestintctlIPFDC_CPU7_VP3	0
guestintctlIPPCI_CPU0_VP0	0
guestintctlIPPCI_CPU0_VP1	0
guestintctlIPPCI_CPU0_VP2	0
guestintctlIPPCI_CPU0_VP3	0
guestintctlIPPCI_CPU1_VP0	0
guestintctlIPPCI_CPU1_VP1	0
guestintctlIPPCI_CPU1_VP2	0
guestintctlIPPCI_CPU1_VP3	0
guestintctlIPPCI_CPU2_VP0	0
guestintctlIPPCI_CPU2_VP1	0
guestintctlIPPCI_CPU2_VP2	0
guestintctlIPPCI_CPU2_VP3	0
guestintctlIPPCI_CPU3_VP0	0
guestintctlIPPCI_CPU3_VP1	0
guestintctlIPPCI_CPU3_VP2	0
guestintctlIPPCI_CPU3_VP3	0
guestintctlIPPCI_CPU4_VP0	0
guestintctlIPPCI_CPU4_VP1	0
guestintctlIPPCI_CPU4_VP2	0
guestintctlIPPCI_CPU4_VP3	0
guestintctlIPPCI_CPU5_VP0	0
guestintctlIPPCI_CPU5_VP1	0
guestintctlIPPCI_CPU5_VP2	0
guestintctlIPPCI_CPU5_VP3	0
guestintctlIPPCI_CPU6_VP0	0
guestintctlIPPCI_CPU6_VP1	0
guestintctlIPPCI_CPU6_VP2	0
guestintctlIPPCI_CPU6_VP3	0
guestintctlIPPCI_CPU7_VP0	0
guestintctlIPPCI_CPU7_VP1	0
guestintctlIPPCI_CPU7_VP2	0
guestintctlIPPCI_CPU7_VP3	0
ISPRAM_SIZE	0
ISPRAM_BASE	0
ISPRAM_ENABLE	F
ISPRAM_FILE	
DSPRAM_SIZE	0
DSPRAM_BASE	0
DSPRAM_ENABLE	F

DSPRAM_PRESENT	F
USPRAM_SIZE	0
USPRAM_BASE	0
USPRAM_ENABLE	F
USPRAM_FILE	
misalignedDataException	never
commitTlbwErr	F

Table 8.6: Parameter values

## **Execution Modes**

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3

Table 9.1: Modes implemented in: CMP

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3
GUEST_KERNEL	4
GUEST_SUPERVISOR	5
GUEST_USER	6

Table 9.2: Modes implemented in: CPU

Mode	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3
GUEST_KERNEL	4
GUEST_SUPERVISOR	5
GUEST_USER	6

Table 9.3: Modes implemented in:  $\operatorname{VP}$ 

# Exceptions

Exception	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9
RI	10
$\mathrm{CpU}$	11
Ov	12
Tr	13
MSAFPE	14
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MSADis	21
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

Table 10.1: Exceptions implemented in: CMP  $\,$ 

Int         0           Mod         1           TLBL         2           TLBS         3           AdEL         4           AdES         5           IBE         6           DBE         7           Sys         8           Bp         9           RI         10           CpU         11           Ov         12           Tr         13           MSAFPE         14           FPE         15           Impl1         16           Impl2         17           C2E         18           TLBRI         19           TLBXI         20           MSADis         21           MDMX         22           WATCH         23           MCheck         24           Thread         25           DSPDis         26           GE         27           Prot         29           CacheErr         30	Exception	Code
TLBL       2         TLBS       3         AdEL       4         AdES       5         IBE       6         DBE       7         Sys       8         Bp       9         RI       10         CpU       11         Ov       12         Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29	Int	0
TLBS       3         AdEL       4         AdES       5         IBE       6         DBE       7         Sys       8         Bp       9         RI       10         CpU       11         Ov       12         Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29	Mod	1
AdEL       4         AdES       5         IBE       6         DBE       7         Sys       8         Bp       9         RI       10         CpU       11         Ov       12         Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29	TLBL	2
AdEL       4         AdES       5         IBE       6         DBE       7         Sys       8         Bp       9         RI       10         CpU       11         Ov       12         Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29	TLBS	3
IBE       6         DBE       7         Sys       8         Bp       9         RI       10         CpU       11         Ov       12         Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29	AdEL	
DBE       7         Sys       8         Bp       9         RI       10         CpU       11         Ov       12         Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29	AdES	
Sys       8         Bp       9         RI       10         CpU       11         Ov       12         Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29		
Bp       9         RI       10         CpU       11         Ov       12         Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29	DBE	
RI 10 CpU 11 Ov 12 Tr 13 MSAFPE 14 FPE 15 Impl1 16 Impl2 17 C2E 18 TLBRI 19 TLBXI 20 MSADis 21 MDMX 22 WATCH 23 MCheck 24 Thread 25 DSPDis 26 GE 27 Prot 29	· ·	
CpU       11         Ov       12         Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29	Вр	
Ov       12         Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29		10
Tr       13         MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29	•	
MSAFPE       14         FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29		
FPE       15         Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29		13
Impl1       16         Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29		
Impl2       17         C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29		
C2E       18         TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29		
TLBRI       19         TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29		
TLBXI       20         MSADis       21         MDMX       22         WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29		
MSADis         21           MDMX         22           WATCH         23           MCheck         24           Thread         25           DSPDis         26           GE         27           Prot         29		
MDMX         22           WATCH         23           MCheck         24           Thread         25           DSPDis         26           GE         27           Prot         29		
WATCH       23         MCheck       24         Thread       25         DSPDis       26         GE       27         Prot       29		
MCheck         24           Thread         25           DSPDis         26           GE         27           Prot         29		
Thread         25           DSPDis         26           GE         27           Prot         29		
DSPDis         26           GE         27           Prot         29		24
GE 27 Prot 29		
Prot 29		
CacheErr 30		
	CacheErr	30

Table 10.2: Exceptions implemented in: CPU

Exception	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Вр	9

RI	10
CpU	11
Ov	12
Tr	13
MSAFPE	14
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MSADis	21
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

Table 10.3: Exceptions implemented in: VP

## Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.

OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

#### 11.1 Level 1: CMP

This level in the model hierarchy has 2 commands. This level in the model hierarchy has no register groups. This level in the model hierarchy has 2 children: CPU0 and CPU1.

## 11.2 Level 2: CPU

This level in the model hierarchy has 2 commands. This level in the model hierarchy has no register groups. This level in the model hierarchy has 4 children: CPU0\_VP0, CPU0\_VP1, CPU0\_VP2 and CPU0\_VP3.

## 11.3 Level 3: VP

This level in the model hierarchy has 20 commands. This level in the model hierarchy has 10 register groups:

Group name	Registers
Core	65
FPU	34

DSP	9
Shadow	64
COP0	174
MSA	40
CMP_GCR	36
CMP_CPC	14
CMP_GIC	721
Integration_support	1

Table 11.1: Register groups

This level in the model hierarchy has no children.

## **Model Commands**

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

## 12.1 Level 1: CMP

#### 12.1.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.1: isync command arguments

#### 12.1.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-memory	String	show memory accesses by this instruction. Ar-
		gument can be any combination of X (execute),
		L (load or store access) and S (system)
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-processorname	Boolean	Include processor name in all trace lines
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.2: itrace command arguments

## 12.2 Level 2: CPU

## 12.2.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.3: isync command arguments

#### 12.2.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-memory	String	show memory accesses by this instruction. Ar-
		gument can be any combination of X (execute),
		L (load or store access) and S (system)
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-processorname	Boolean	Include processor name in all trace lines
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.4: itrace command arguments

## 12.3 Level 3: VP

## 12.3.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.5: isync command arguments

#### 12.3.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing

-instructioncount	Boolean	include the instruction number in each trace
-memory	String	show memory accesses by this instruction. Ar-
		gument can be any combination of X (execute),
		L (load or store access) and S (system)
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-processorname	Boolean	Include processor name in all trace lines
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.6: itrace command arguments

## 12.3.3 mipsCOP0

query a COP0 register value using <register><select>

Argument	Type	Description
-register	Uns32	specify the COP0 register resource
-select	Uns32	specify the COP0 register select

Table 12.7: mipsCOP0 command arguments

## 12.3.4 mipsCacheDisable

#### 12.3.4.1 Argument description

Disables tag or full cache model

## 12.3.5 mipsCacheEnable

enable tag or full cache model

Argument	Type	Description
-debug	Int32	set cache model debug flags
-full	Boolean	enable full cache model
-tag	Boolean	enable cache tag line only model

Table 12.8: mipsCacheEnable command arguments

#### 12.3.6 mipsCacheRatio

Report current hit ratio for selected cache

Argument	Type	Description
-dcache	Boolean	report hit ratio for dcache
-icache	Boolean	report hit ratio for icache

Table 12.9: mipsCacheRatio command arguments

## 12.3.7 mipsCacheReport

#### 12.3.7.1 Argument description

Report current cache statistics

#### 12.3.8 mipsCacheReset

#### 12.3.8.1 Argument description

reset the cache model

## 12.3.9 mipsCacheTrace

Control the tracing of cache accesses

Argument	Type	Description
-noartifact	Boolean	
-nocached	Boolean	
-nodcache	Boolean	
-noicache	Boolean	
-notrue	Boolean	
-nouncached	Boolean	
-off	Boolean	turn off the cache tracing
-on	Boolean	turn on the cache tracing

Table 12.10: mipsCacheTrace command arguments

## 12.3.10 mipsDebugFlags

Set the mips model debug value

Argument	Type	Description
-value	Uns32	specify mips model debug flags

Table 12.11: mipsDebugFlags command arguments

#### 12.3.11 mipsReadRegister

Read processor register using <resource><offset>

Argument	Type	Description
-offset	Uns32	the register offset
-resource	Uns32	the register resource

Table 12.12: mipsReadRegister command arguments

## 12.3.12 mipsReadTLBEntry

read a TLB entry specified by the index

Copyright (c) 2021 Imperas Software Limited OVP License. Release 20211118.0

Argument	Type	Description
-index	Uns64	select the TLB entry

Table 12.13: mipsReadTLBEntry command arguments

#### 12.3.13 mipsTLBDump

## 12.3.13.1 Argument description

Dumps the current contents of the TLB

## 12.3.14 mipsTLBDumpGuest

#### 12.3.14.1 Argument description

Dumps the current contents of the Guest TLB

#### 12.3.15 mipsTLBDumpRoot

#### 12.3.15.1 Argument description

Dumps the current contents of the Root TLB

#### 12.3.16 mipsTLBGetPhys

Reports the entry(s) in the TLB that match the given virtual address and ASID

Argument	Type	Description
-asid	Uns64	ASID
-va	Uns64	virtual address

Table 12.14: mipsTLBGetPhys command arguments

#### 12.3.17 mipsTraceGuest

control tracing of guest

Argument	Type	Description
-off	Boolean	stop tracing
-on	Boolean	start tracing

Table 12.15: mipsTraceGuest command arguments

## 12.3.18 mipsTraceRoot

control tracing on root processor

Argument	Type	Description
-off	Boolean	stop tracing
-on	Boolean	start tracing

Table 12.16: mipsTraceRoot command arguments

## 12.3.19 mipsWriteRegister

Write processor register using <resource><offset><value>

Argument	Type	Description
-offset	Uns32	the register offset
-resource	Uns32	the register resource
-value	Uns64	the value to write to register

Table 12.17: mipsWriteRegister command arguments

## 12.3.20 mipsWriteTLBEntry

Writes values to a TLB entry using the index, lo0, lo1, hi0 and mask fields

Argument	Type	Description
-hi0	Uns64	the TLB entry high address
-index	Uns64	the TLB entry index
-lo0	Uns64	the TLB entry low address 0
-lo1	Uns64	the TLB entry low address 1
-mask	Uns64	the TLB entry mask

Table 12.18: mipsWriteTLBEntry command arguments

## Registers

13.1 Level 1: CMP

No registers.

13.2 Level 2: CPU

No registers.

13.3 Level 3: VP

13.3.1 Core

Registers at level:3, type:VP group:Core

Name	Bits	Initial-Hex	RW	Description
zero	64	0	r-	constant zero
at	64	0	rw	
v0	64	0	rw	
v1	64	0	rw	
a0	64	0	rw	
a1	64	0	rw	
a2	64	0	rw	
a3	64	0	rw	
t0	64	0	rw	
t1	64	0	rw	
t2	64	0	rw	
t3	64	0	rw	
t4	64	0	rw	
t5	64	0	rw	
t6	64	0	rw	
t7	64	0	rw	
s0	64	0	rw	
s1	64	0	rw	
s2	64	0	rw	
s3	64	0	rw	
s4	64	0	rw	
s5	64	0	rw	
s6	64	0	rw	

18	s7	64	0	rw	
t9         64         0         rw           k0         64         0         rw           k1         64         0         rw           gp         64         0         rw           sp         64         0         rw           sp         64         0         rw           ra         64         0         rw           pc         64         ffffffffffffff         rw           r0         64         0         rw           r1         64         0         rw           r2         64         0         rw           r3         64         0         rw           r4         64         0         rw           r5         64         0         rw           r6         64         0         rw           r8         64         0         rw           r8         64         0         rw           r9         64         0         rw           r10         64         0         rw           r11         64         0         rw           r12         64         0					
k0         64         0         rw           gp         64         0         rw           sp         64         0         rw           sp         64         0         rw           s8         64         0         rw           ra         64         0         rw           pc         64         ffffffff         rw           pc         64         0         rw           r0         64         0         rw           r1         64         0         rw           r2         64         0         rw           r3         64         0         rw           r4         64         0         rw           r6         64         0         rw           r6         64         0         rw           r9         64         0         rw           r10         64         0         rw           r12         64         0         rw           r13         64         0         rw           r12         64         0         rw           r12         64         0					
K1					
gp         64         0         rw         stack pointer           s8         64         0         rw         stack pointer           ra         64         0         rw         frame pointer           ra         64         0         rw         program counter           ra         64         0         rw         rconstant zero           ra         64         0         rw         rw           ra         64         0         rw           ra         ra         rw           ra <t< td=""><td></td><td></td><td></td><td></td><td></td></t<>					
sp         64         0         rw         stack pointer           ra         64         0         rw         frame pointer           ra         64         0         rw         frame pointer           ra         64         0         rw         program counter           r0         64         0         rw         rw           r1         64         0         rw           r2         64         0         rw           r3         64         0         rw           r4         64         0         rw           r5         64         0         rw           r6         64         0         rw           r8         64         0         rw           r10         64         0         rw           r11         64         0         rw           r12         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r16         64         0         rw           r17					
s8         64         0         rw         frame pointer           pc         64         0         rw         program counter           pc         64         0         rw         program counter           n0         64         0         rw         respectively           r1         64         0         rw         respectively           r2         64         0         rw         respectively           r3         64         0         rw         respectively           r4         64         0         rw         respectively           r5         64         0         rw         respectively         respectively           r8         64         0         rw         respectively         respectively         respectively           r10         64         0         rw         respectively         respectively         respectively           r12         64         0         rw         respectively         respectively         respectively         respectively           r17         64         0         rw         respectively         respectively         respectively         respectively         respectively         respecti					stack pointer
Ta	sp s8	1			
DC					name pointer
r0         64         0         r-         constant zero           r1         64         0         rw           r2         64         0         rw           r3         64         0         rw           r4         64         0         rw           r5         64         0         rw           r6         64         0         rw           r7         64         0         rw           r9         64         0         rw           r10         64         0         rw           r11         64         0         rw           r13         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r15         64         0         rw           r17         64         0         rw           r19         64         0         rw           r19         64         0         rw           r19         64         0         rw           r20					program counter
r1         64         0         rw           r2         64         0         rw           r3         64         0         rw           r4         64         0         rw           r5         64         0         rw           r6         64         0         rw           r7         64         0         rw           r8         64         0         rw           r9         64         0         rw           r10         64         0         rw           r12         64         0         rw           r13         64         0         rw           r14         64         0         rw           r16         64         0         rw           r17         64         0         rw           r18         64         0         rw           r19         64         0         rw           r12         64         0         rw           r19         64         0         rw           r20         64         0         rw           r22         64         0	рс		bfc00000	1 00	program counter
r2         64         0         rw           r3         64         0         rw           r4         64         0         rw           r5         64         0         rw           r6         64         0         rw           r7         64         0         rw           r8         64         0         rw           r10         64         0         rw           r11         64         0         rw           r11         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r16         64         0         rw           r17         64         0         rw           r18         64         0         rw           r19         64         0         rw           r20         64         0         rw           r21         64         0         rw           r22         64         0         rw           r23         64         0				r-	constant zero
r3         64         0         rw           r4         64         0         rw           r5         64         0         rw           r6         64         0         rw           r7         64         0         rw           r8         64         0         rw           r9         64         0         rw           r10         64         0         rw           r11         64         0         rw           r12         64         0         rw           r13         64         0         rw           r15         64         0         rw           r16         64         0         rw           r17         64         0         rw           r19         64         0         rw           r20         64         0         rw           r21         64         0         rw           r21         64         0         rw           r22         64         0         rw           r23         64         0         rw           r24         64         0				rw	
r4         64         0         rw           r5         64         0         rw           r6         64         0         rw           r7         64         0         rw           r8         64         0         rw           r9         64         0         rw           r10         64         0         rw           r11         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r16         64         0         rw           r18         64         0         rw           r19         64         0         rw           r20         64         0         rw           r21         64         0         rw           r22         64         0         rw           r23         64         0         rw           r24         64         0         rw           r25         64         0         rw           r26         64         0				rw	
r5         64         0         rw           r6         64         0         rw           r7         64         0         rw           r8         64         0         rw           r10         64         0         rw           r11         64         0         rw           r11         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r16         64         0         rw           r18         64         0         rw           r19         64         0         rw           r20         64         0         rw           r21         64         0         rw           r23         64         0         rw           r24         64         0         rw           r25         64         0         rw           r26         64         0         rw           r28         64         0         rw           r29         64         0				rw	
r6         64         0         rw           r7         64         0         rw           r8         64         0         rw           r9         64         0         rw           r10         64         0         rw           r11         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r16         64         0         rw           r17         64         0         rw           r18         64         0         rw           r19         64         0         rw           r20         64         0         rw           r22         64         0         rw           r23         64         0         rw           r25         64         0         rw           r25         64         0         rw           r27         64         0         rw           r28         64         0         rw           r28         64         0				rw	
r7         64         0         rw           r8         64         0         rw           r9         64         0         rw           r10         64         0         rw           r11         64         0         rw           r12         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r16         64         0         rw           r17         64         0         rw           r19         64         0         rw           r20         64         0         rw           r21         64         0         rw           r22         64         0         rw           r23         64         0         rw           r25         64         0         rw           r26         64         0         rw           r28         64         0         rw           r29         64         0         rw         stack pointer           r30				rw	
r8         64         0         rw           r9         64         0         rw           r10         64         0         rw           r11         64         0         rw           r12         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r16         64         0         rw           r17         64         0         rw           r18         64         0         rw           r20         64         0         rw           r21         64         0         rw           r22         64         0         rw           r23         64         0         rw           r25         64         0         rw           r25         64         0         rw           r27         64         0         rw           r28         64         0         rw           r29         64         0         rw         frame pointer				rw	
r9         64         0         rw           r10         64         0         rw           r11         64         0         rw           r12         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r16         64         0         rw           r17         64         0         rw           r18         64         0         rw           r20         64         0         rw           r21         64         0         rw           r22         64         0         rw           r23         64         0         rw           r25         64         0         rw           r26         64         0         rw           r27         64         0         rw           r28         64         0         rw           r29         64         0         rw         frame pointer				rw	
r10         64         0         rw           r11         64         0         rw           r12         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r16         64         0         rw           r17         64         0         rw           r18         64         0         rw           r20         64         0         rw           r21         64         0         rw           r22         64         0         rw           r23         64         0         rw           r24         64         0         rw           r25         64         0         rw           r27         64         0         rw           r28         64         0         rw           r29         64         0         rw         frame pointer				rw	
r11         64         0         rw           r12         64         0         rw           r13         64         0         rw           r14         64         0         rw           r15         64         0         rw           r16         64         0         rw           r17         64         0         rw           r19         64         0         rw           r20         64         0         rw           r21         64         0         rw           r22         64         0         rw           r23         64         0         rw           r24         64         0         rw           r26         64         0         rw           r27         64         0         rw           r28         64         0         rw           r29         64         0         rw         frame pointer				rw	
r12     64     0     rw       r13     64     0     rw       r14     64     0     rw       r15     64     0     rw       r16     64     0     rw       r17     64     0     rw       r19     64     0     rw       r20     64     0     rw       r21     64     0     rw       r22     64     0     rw       r23     64     0     rw       r24     64     0     rw       r25     64     0     rw       r26     64     0     rw       r28     64     0     rw       r29     64     0     rw     frame pointer				rw	
r13     64     0     rw       r14     64     0     rw       r15     64     0     rw       r16     64     0     rw       r17     64     0     rw       r18     64     0     rw       r20     64     0     rw       r21     64     0     rw       r22     64     0     rw       r23     64     0     rw       r24     64     0     rw       r25     64     0     rw       r26     64     0     rw       r27     64     0     rw       r28     64     0     rw     stack pointer       r30     64     0     rw     frame pointer				rw	
r14     64     0     rw       r15     64     0     rw       r16     64     0     rw       r17     64     0     rw       r18     64     0     rw       r20     64     0     rw       r21     64     0     rw       r22     64     0     rw       r23     64     0     rw       r24     64     0     rw       r25     64     0     rw       r26     64     0     rw       r27     64     0     rw       r28     64     0     rw       r29     64     0     rw     frame pointer				rw	
r15     64     0     rw       r16     64     0     rw       r17     64     0     rw       r18     64     0     rw       r19     64     0     rw       r20     64     0     rw       r21     64     0     rw       r22     64     0     rw       r23     64     0     rw       r24     64     0     rw       r25     64     0     rw       r26     64     0     rw       r27     64     0     rw       r28     64     0     rw     stack pointer       r30     64     0     rw     frame pointer				rw	
r16       64       0       rw         r17       64       0       rw         r18       64       0       rw         r19       64       0       rw         r20       64       0       rw         r21       64       0       rw         r22       64       0       rw         r23       64       0       rw         r24       64       0       rw         r25       64       0       rw         r26       64       0       rw         r27       64       0       rw         r28       64       0       rw         r29       64       0       rw       frame pointer				rw	
r17       64       0       rw         r18       64       0       rw         r19       64       0       rw         r20       64       0       rw         r21       64       0       rw         r22       64       0       rw         r23       64       0       rw         r24       64       0       rw         r25       64       0       rw         r26       64       0       rw         r27       64       0       rw         r28       64       0       rw       stack pointer         r30       64       0       rw       frame pointer			0	rw	
r18       64       0       rw         r19       64       0       rw         r20       64       0       rw         r21       64       0       rw         r22       64       0       rw         r23       64       0       rw         r24       64       0       rw         r25       64       0       rw         r26       64       0       rw         r27       64       0       rw         r28       64       0       rw         r29       64       0       rw       frame pointer			0	rw	
r19     64     0     rw       r20     64     0     rw       r21     64     0     rw       r22     64     0     rw       r23     64     0     rw       r24     64     0     rw       r25     64     0     rw       r26     64     0     rw       r27     64     0     rw       r28     64     0     rw       r29     64     0     rw     frame pointer				rw	
r20     64     0     rw       r21     64     0     rw       r22     64     0     rw       r23     64     0     rw       r24     64     0     rw       r25     64     0     rw       r26     64     0     rw       r27     64     0     rw       r28     64     0     rw       r29     64     0     rw     frame pointer				rw	
r21     64     0     rw       r22     64     0     rw       r23     64     0     rw       r24     64     0     rw       r25     64     0     rw       r26     64     0     rw       r27     64     0     rw       r28     64     0     rw       r29     64     0     rw     stack pointer       r30     64     0     rw     frame pointer			0	rw	
r22     64     0     rw       r23     64     0     rw       r24     64     0     rw       r25     64     0     rw       r26     64     0     rw       r27     64     0     rw       r28     64     0     rw       r29     64     0     rw     stack pointer       r30     64     0     rw     frame pointer				rw	
r23     64     0     rw       r24     64     0     rw       r25     64     0     rw       r26     64     0     rw       r27     64     0     rw       r28     64     0     rw       r29     64     0     rw     stack pointer       r30     64     0     rw     frame pointer				rw	
r24     64     0     rw       r25     64     0     rw       r26     64     0     rw       r27     64     0     rw       r28     64     0     rw       r29     64     0     rw     stack pointer       r30     64     0     rw     frame pointer				rw	
r25     64     0     rw       r26     64     0     rw       r27     64     0     rw       r28     64     0     rw       r29     64     0     rw     stack pointer       r30     64     0     rw     frame pointer			0	rw	
r26         64         0         rw           r27         64         0         rw           r28         64         0         rw           r29         64         0         rw         stack pointer           r30         64         0         rw         frame pointer			0	rw	
r27         64         0         rw           r28         64         0         rw           r29         64         0         rw         stack pointer           r30         64         0         rw         frame pointer				rw	
r28         64         0         rw           r29         64         0         rw         stack pointer           r30         64         0         rw         frame pointer				rw	
r29         64         0         rw         stack pointer           r30         64         0         rw         frame pointer				rw	
r30 64 0 rw frame pointer	r28	64	0	rw	
			0	rw	stack pointer
	r30	64	0	rw	
r31 64 0 rw	r31	64	0	rw	

Table 13.1: Registers at level 3, type:VP group:Core

## 13.3.2 FPU

Registers at level:3, type:VP group:FPU

Name	Bits	Initial-Hex	RW	Description
f0	64	0	rw	
f1	64	0	rw	
f2	64	0	rw	
f3	64	0	rw	
f4	64	0	rw	

f5	64	0	rw	
f6	64	0	rw	
f7	64	0	rw	
f8	64	0	rw	
f9	64	0	rw	
f10	64	0	rw	
f11	64	0	rw	
f12	64	0	rw	
f13	64	0	rw	
f14	64	0	rw	
f15	64	0	rw	
f16	64	0	rw	
f17	64	0	rw	
f18	64	0	rw	
f19	64	0	rw	
f20	64	0	rw	
f21	64	0	rw	
f22	64	0	rw	
f23	64	0	rw	
f24	64	0	rw	
f25	64	0	rw	
f26	64	0	rw	
f27	64	0	rw	
f28	64	0	rw	
f29	64	0	rw	
f30	64	0	rw	
f31	64	0	rw	
fsr	64	c0000	rw	floating point status
fir	64	20f30320	r-	floating point information

Table 13.2: Registers at level 3, type:VP group:FPU

## 13.3.3 DSP

Registers at level:3, type:VP group:DSP

Name	Bits	Initial-Hex	RW	Description
lo	64	0	rw	
hi	64	0	rw	
lo1	64	0	rw	
hi1	64	0	rw	
lo2	64	0	rw	
hi2	64	0	rw	
lo3	64	0	rw	
hi3	64	0	rw	
dspctl	64	0	rw	DSP control

Table 13.3: Registers at level 3, type:VP group:DSP

#### 13.3.4 Shadow

Registers at level:3, type:VP group:Shadow

Name	Bits	Initial-Hex	RW	Description	
zero[0]	64	0	r-	constant zero	

at[0]	64	0	rw	
v0[0]	64	0	rw	
v1[0]	64	0	rw	
a0[0]	64	0	rw	
a1[0]	64	0	rw	
a2[0]	64	0	rw	
a3[0]	64	0	rw	
t0[0]	64	0	rw	
t1[0]	64	0	rw	
t2[0]	64	0	rw	
t3[0]	64	0	rw	
t4[0]	64	0	rw	
t5[0]	64	0	rw	
t6[0]	64	0	rw	
t7[0]	64	0	_	
s0[0]	64	0	rw	
	64	0	rw	
s1[0] s2[0]	64	0	rw	
	64		rw	
s3[0]		0	rw	
s4[0]	64	0	rw	
s5[0]	64	0	rw	
s6[0]	64	0	rw	
s7[0]	64	0	rw	
t8[0]	64	0	rw	
t9[0]	64	0	rw	
k0[0]	64	0	rw	
k1[0]	64	0	rw	
[ [ ]				
gp[0]	64	0	rw	
sp[0]	64	0	rw rw	stack pointer
$\frac{\operatorname{sp}[0]}{\operatorname{s8}[0]}$	64 64	0	_	stack pointer frame pointer
sp[0] s8[0] ra[0]	64 64 64	0 0 0	rw	frame pointer
sp[0] s8[0] ra[0] r0[0]	64 64 64 64	0 0 0	rw rw	
sp[0] s8[0] ra[0] r0[0] r1[0]	64 64 64 64	0 0 0 0	rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0]	64 64 64 64 64	0 0 0 0 0	rw rw rw r-	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0]	64 64 64 64	0 0 0 0	rw rw rw r- rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0]	64 64 64 64 64	0 0 0 0 0	rw rw rw r- rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64	0 0 0 0 0 0	rw rw rw r- rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0]	64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0]	64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0]	64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0	rw rw rw r- rw rw rw rw rw rw rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0]	64 64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0 0	rw	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r9[0] r10[0]	64 64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r9[0] r10[0] r11[0] r12[0]	64 64 64 64 64 64 64 64 64 64 64 64 64	0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r13[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r13[0] r14[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0]   s8[0]   ra[0]   ra[0]   ra[0]   ra[0]   r2[0]   r3[0]   r4[0]   r5[0]   r6[0]   r7[0]   r8[0]   r10[0]   r11[0]   r12[0]   r13[0]   r14[0]   r15[0]   r3[0]   r15[0]   r15[0]   r3[0]   r15[0]   r15[0]   r3[0]   r3[0]   r15[0]   r3[0]   r3[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0]   s8[0]   ra[0]   ra[0]   ra[0]   ra[0]   r2[0]   r3[0]   r4[0]   r5[0]   r6[0]   r7[0]   r8[0]   r10[0]   r11[0]   r12[0]   r13[0]   r14[0]   r15[0]   r16[0]   rage    rag	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0]   s8[0]   ra[0]   ra[0	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r14[0] r15[0] r15[0] r16[0] r17[0] r18[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r14[0] r15[0] r15[0] r16[0] r17[0] r18[0] r19[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0]   sp[0]   sp[0]   sp[0]   ra[0]   ra[0	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r10[0] r11[0] r12[0] r14[0] r15[0] r15[0] r15[0] r16[0] r17[0] r18[0] r19[0] r20[0] r21[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0] s8[0] ra[0] r0[0] r1[0] r2[0] r3[0] r4[0] r5[0] r6[0] r7[0] r8[0] r9[0] r11[0] r12[0] r14[0] r15[0] r15[0] r15[0] r16[0] r17[0] r18[0] r19[0] r20[0] r22[0]	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer
sp[0]   s8[0]   ra[0]   ra[0	64 64 64 64 64 64 64 64 64 64 64 64 64 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	rw r	frame pointer

r25[0]	64	0	rw	
r26[0]	64	0	rw	
r27[0]	64	0	rw	
r28[0]	64	0	rw	
r29[0]	64	0	rw	stack pointer
r30[0]	64	0	rw	frame pointer
r31[0]	64	0	rw	

Table 13.4: Registers at level 3, type:VP group:Shadow

## 13.3.5 COP0

Registers at level:3, type:VP group:COP0

Name	Bits	Initial-Hex	RW	Description
sr	64	4400004	rw	CP0 register 12/0 (status)
bad	64	0	rw	CP0 register 8/0 (badvaddr)
cause	64	0	rw	CP0 register 13/0 (cause)
index	64	0	rw	CP0 register 0/0
vpcontrol	64	0	rw	CP0 register 0/4
entrylo0	64	0	rw	CP0 register 2/0
entrylo1	64	0	rw	CP0 register 3/0
globalnumber	64	0	rw	CP0 register 3/1
context	64	0	rw	CP0 register 4/0
userlocal	64	0	rw	CP0 register 4/2
pagemask	64	0	rw	CP0 register 5/0
pagegrain	64	c8000000	rw	CP0 register 5/1
wired	64	0	rw	CP0 register 6/0
hwrena	64	0	rw	CP0 register 7/0
badvaddr	64	0	rw	CP0 register 8/0
badinstr	64	0	rw	CP0 register 8/1
badinstrp	64	0	rw	CP0 register 8/2
count	64	0	rw	CP0 register 9/0
entryhi	64	0	rw	CP0 register 10/0
guestctl1	64	0	rw	CP0 register 10/4
guestctl2	64	0	rw	CP0 register 10/5
guestctl3	64	0	rw	CP0 register 10/6
compare	64	0	rw	CP0 register 11/0
guestctl0ext	64	80	rw	CP0 register 11/4
status	64	4400004	rw	CP0 register 12/0
intctl	64	e0000000	rw	CP0 register 12/1
srsctl	64	0	rw	CP0 register 12/2
srsmap	64	0	rw	CP0 register 12/3
guestctl0	64	c4c0080	rw	CP0 register 12/6
gtoffset	64	0	rw	CP0 register 12/7
epc	64	0	rw	CP0 register 14/0
prid	64	1ac00	rw	CP0 register 15/0
ebase	64	fffffff	rw	CP0 register 15/1
		80000000		
cmgcrbase	64	1fbf800	rw	CP0 register 15/3
config	64	8000ca02	rw	CP0 register 16/0
config1	64	9eab5593	rw	CP0 register 16/1
config2	64	80000000	rw	CP0 register 16/2
config3	64	fc8031e1	rw	CP0 register 16/3
config4	64	d0fc0227	rw	CP0 register 16/4
config5	64	498	rw	CP0 register 16/5

	T 0.4	La		GD0 1 1 10/0
config6	64	0	rw	CP0 register 16/6
config7	64	80000000	rw	CP0 register 16/7
lladdr	64	0	rw	CP0 register 17/0
maar	64	0	rw	CP0 register 17/1
maari	64	0	rw	CP0 register 17/2
xcontext	64	0	rw	CP0 register 20/0
debug	64	2008000	rw	CP0 register 23/0
tracecontrol	64	0	rw	CP0 register 23/1
tracecontrol2	64	0	rw	CP0 register 23/2
usertracedata	64	0	rw	CP0 register 23/3
traceibpc	64	0	rw	CP0 register 23/4
tracedbpc	64	0	rw	CP0 register 23/5
ibp2_3_action	64	0	rw	CP0 register 23/7
depc	64	0	rw	CP0 register 24/0
dbp2_3_action	64	0	rw	CP0 register 24/1
tracecontrol3	64	0	rw	CP0 register 24/2
usertracedata2	64	0	rw	CP0 register 24/3
tcbconfig	64	0	rw	CP0 register 24/4
tcbcontrole	64	0	rw	CP0 register 24/5
ibp4_5_action	64	0	rw	CP0 register 24/6
ibp6_7_action	64	0	rw	CP0 register 24/7
perfctl0	64	80000000	rw	CP0 register 25/0
perfcnt0	64	0	rw	CP0 register 25/1
perfctl1	64	80000000	rw	CP0 register 25/2
perfent1	64	0	rw	CP0 register 25/3
perfettl2	64	80000000	rw	CP0 register 25/4
perfent2	64	0	rw	CP0 register 25/5
perfett3	64	0	rw	CP0 register 25/6
perfent3	64	0	rw	CP0 register 25/7
errctl	64	0	rw	CP0 register 26/0
tcbcontrold	64	0	rw	CP0 register 26/4
cacheerr	64	0	rw	CP0 register 27/0
	64	0		CP0 register 28/0
itaglo idatalo	64	0	rw	CP0 register 28/1
	64	0	rw	CP0 register 28/1 CP0 register 28/2
dtaglo		-	rw	
ddatalo	64	0	rw	CP0 register 28/3
itaghi	64	0	rw	CP0 register 29/0
idatahi	64	0	rw	CP0 register 29/1
dtaghi	64	0	rw	CP0 register 29/2
ddatahi	64	0	rw	CP0 register 29/3
errorepc	64	0	rw	CP0 register 30/0
desave	64	0	rw	CP0 register 31/0
kscratch1	64	0	rw	CP0 register 31/2
kscratch2	64	0	rw	CP0 register 31/3
kscratch3	64	0	rw	CP0 register 31/4
kscratch4	64	0	rw	CP0 register 31/5
kscratch5	64	0	rw	CP0 register 31/6
kscratch6	64	0	rw	CP0 register 31/7
guestindex	64	0	rw	CP0 guest register 0/0
guestvpcontrol	64	0	rw	CP0 guest register 0/4
guestentrylo0	64	0	rw	CP0 guest register 2/0
guestentrylo1	64	0	rw	CP0 guest register 3/0
guestglobalnumber	64	0	rw	CP0 guest register 3/1
guestcontext	64	0	rw	CP0 guest register 4/0
guestuserlocal	64	0	rw	CP0 guest register 4/2
guestpagemask	64	0	rw	CP0 guest register 5/0
OIO	1	L -		

guestpacegrain 61 0 rw CP0 guest register 5/1 guesthwrena 64 0 rw CP0 guest register 6/0 guesthoddr 64 0 rw CP0 guest register 8/0 guesthodinstr 64 0 rw CP0 guest register 8/2 guesthout 64 0 rw CP0 guest register 10/0 guestguesthi 64 0 rw CP0 guest register 10/4 guestguesthi 64 0 rw CP0 guest register 10/4 guestguesthi 64 0 rw CP0 guest register 10/4 guestguesthi 64 0 rw CP0 guest register 10/6 guestguesthodox 64 0 rw CP0 guest register 10/6 guestguesthodox 64 0 rw CP0 guest register 11/4 gueststatus 64 400004 rw CP0 guest register 11/4 gueststatus 64 0 rw CP0 guest register 11/4 gueststatus 64 0 rw CP0 guest register 12/1 guestspacethi 64 0 rw CP0 guest register 12/1 guestguestchi 64 0 rw CP0 guest register 12/1 guestguestchi 64 0 rw CP0 guest register 12/3 guestguestchi 64 0 rw CP0 guest register 12/3 guestguestchi 64 0 rw CP0 guest register 12/3 guestguestchi 64 0 rw CP0 guest register 12/7 guestguestguestchi 64 0 rw CP0 guest register 12/7 guestguestguest general 64 0 rw CP0 guest register 12/7 guestguestguest register 16/0 guestchoac 64 0 rw CP0 guest register 16/0 guestchoac 64 0 rw CP0 guest register 16/0 guestconfig 64 0 solotoon rw CP0 guest register 16/0 guestconfig 64 0 rw CP0 guest register 16/0 guestconfig 64 0 solotoon rw CP0 guest register 16/0 guestconfig 64 0 rw CP0 guest register 17/0 guestguestrand 64 0 rw CP0 guest register 17/0 guestguestrand 64 0 rw CP0 guest register 17/0 guestguestrand 64 0 rw CP0 guest register 24/0 gue				1	
guesthordund				rw	· · · · · · · · · · · · · · · · · · ·
guest badinstr   64   0				rw	
guestbadinistr 64 0 rw CP0 guest register 8/1 guestbadinistry 64 0 rw CP0 guest register 8/2 guestbadinistry 64 0 rw CP0 guest register 9/0 guestpassertil 64 0 rw CP0 guest register 10/4 guestguestctil 64 0 rw CP0 guest register 10/4 guestguestctil 64 0 rw CP0 guest register 10/6 guestguestctil 64 0 rw CP0 guest register 11/0 guestguestctil 64 0 rw CP0 guest register 11/4 gueststatus 64 4400001 rw CP0 guest register 11/4 gueststatus 64 4500000 rw CP0 guest register 12/0 guestsrsctil 64 0 rw CP0 guest register 12/2 guestsrsctil 64 0 rw CP0 guest register 12/2 guestsrsctil 64 0 rw CP0 guest register 12/2 guestsguestctil 64 0 rw CP0 guest register 12/2 guestguestguestctil 64 0 rw CP0 guest register 12/3 guestguestguest 64 0 rw CP0 guest register 12/3 guestguestguest 64 0 rw CP0 guest register 12/6 guestguester 64 0 rw CP0 guest register 13/0 guestpoid 64 0 rw CP0 guest register 13/0 guestcmgcrbase 64 0 rw CP0 guest register 15/0 guestcmgcrbase 64 0 rw CP0 guest register 15/0 guestcmgcrbase 64 0 rw CP0 guest register 15/0 guestcmgcrbase 64 0 rw CP0 guest register 16/1 guestconfig 64 8000000 rw CP0 guest register 16/1 guestconfig 64 8000000 rw CP0 guest register 16/3 guestconfig 64 dofo227 rw CP0 guest register 16/4 guestconfig 64 dofo227 rw CP0 guest register 16/4 guestconfig 64 dofo227 rw CP0 guest register 16/4 guestponfig 64 dofo227 rw C				rw	
guestombur 64 0 rw CP0 guest register 10/0 guestentryhi 64 0 rw CP0 guest register 10/0 guestguestettll 64 0 rw CP0 guest register 10/0 guestguestettll 64 0 rw CP0 guest register 10/6 guestguestettll 64 0 rw CP0 guest register 10/6 guestguestettll 64 0 rw CP0 guest register 10/6 guestguestettll 64 0 rw CP0 guest register 11/0 guestguestettll 64 0 rw CP0 guest register 11/0 guestguestettll 64 0 rw CP0 guest register 11/0 guestguestettll 64 e0000000 rw CP0 guest register 11/4 gueststatus 64 400004 rw CP0 guest register 12/1 guestsrattl 64 0 rw CP0 guest register 12/2 guestsrattl 64 0 rw CP0 guest register 12/2 guestsrattl 64 0 rw CP0 guest register 12/2 guestsramap 64 0 rw CP0 guest register 12/2 guestsramap 64 0 rw CP0 guest register 12/2 guestsramap 64 0 rw CP0 guest register 12/2 guestscuestettll 64 0 rw CP0 guest register 12/6 guestcuestettll 64 0 rw CP0 guest register 12/6 guestcueste 64 0 rw CP0 guest register 12/7 guestcueste 64 0 rw CP0 guest register 13/0 guestcue 64 0 rw CP0 guest register 13/0 guestcue 64 0 rw CP0 guest register 13/0 guestcue 64 0 rw CP0 guest register 15/1 guestcue 64 0 rw CP0 guest register 15/1 guestcue 64 0 rw CP0 guest register 16/0 guestcue 64 0 rw CP0 guest register 16/0 guestcue 64 0 guestcue 64 0 rw CP0 guest register 16/0 guestcue 64 0 guestcue 64 0 guest register 16/0 guestcue 64 0 guestcue 64 0 guest register 16/0 guestcue 64 0 guestcue 64 0 guest register 16/0 guestcue 64 0 guestcue 64 0 guest register 16/0 guestcue 64 0 guest 64 0 guest register 16/0 guestcue 64 0 guest 64 0				rw	
guestonut 64 0 rw CP0 guest register 19/0 guestguestet11 64 0 rw CP0 guest register 10/4 guestguestet12 64 0 rw CP0 guest register 10/4 guestguestet13 64 0 rw CP0 guest register 10/6 guestguestet13 64 0 rw CP0 guest register 10/6 guestguestet13 64 0 rw CP0 guest register 10/6 guestguestet14 64 0 rw CP0 guest register 11/0 guestguestet16 64 0 rw CP0 guest register 11/0 gueststatus 64 4000000 rw CP0 guest register 11/1 gueststatus 64 4000000 rw CP0 guest register 12/0 gueststatus 64 0 rw CP0 guest register 12/1 gueststatus 64 0 rw CP0 guest register 12/2 gueststatus 64 0 rw CP0 guest register 12/2 guestguestet10 64 0 rw CP0 guest register 12/3 guestguestet10 64 0 rw CP0 guest register 12/6 guestguestet10 64 0 rw CP0 guest register 12/6 guestguestet10 64 0 rw CP0 guest register 12/6 guestguestet10 64 0 rw CP0 guest register 13/0 guestepe 64 0 rw CP0 guest register 14/0 guestpuestet10 rw CP0 guest register 15/1 guestet00000 rw CP0 guest register 15/1 guestconfig 64 8000000 rw CP0 guest register 16/0 guestconfig 64 8000000 rw CP0 guest register 16/1 guestconfig 64 8000000 rw CP0 guest register 16/2 guestconfig 64 8000000 rw CP0 guest register 16/2 guestconfig 64 9000000 rw CP0 guest register 16/2 guestconfig 64 0 rw CP0 guest register 16/3 guestconfig 64 0 rw CP0 guest register 17/1 guestracecontor 64 0 rw CP0 guest register 23/1 guesttracecontor 64 0 rw CP0 guest register 23/1 guesttracecontor 64 0 rw CP0 guest register 23/1 guesttracecontor 64 0 rw CP0 guest register 24/2 guesttraceconto				rw	·
guestguestet11	guestbadinstrp			rw	
guestguestet112 64 0 rw CP0 guest register 10/4 guestguestet123 64 0 rw CP0 guest register 10/6 guestguestet13 64 0 rw CP0 guest register 10/6 guestguestet144 64 0 rw CP0 guest register 11/0 guestguestguestet155 64 0 rw CP0 guest register 11/0 gueststatus 64 4400004 rw CP0 guest register 11/4 gueststatus 64 4400004 rw CP0 guest register 12/0 guestinct1 64 0 rw CP0 guest register 12/0 guestsraps 64 0 rw CP0 guest register 12/2 gueststatus 64 0 rw CP0 guest register 12/2 gueststatus 64 0 rw CP0 guest register 12/2 gueststatus 64 0 rw CP0 guest register 12/3 guestsguestguestet10 64 0 rw CP0 guest register 12/3 guestsguestguestet16 64 0 rw CP0 guest register 12/6 guestguestguestet16 64 0 rw CP0 guest register 12/7 guestguestguestet16 64 0 rw CP0 guest register 13/0 guestepe 64 0 rw CP0 guest register 13/0 guestepe 64 0 rw CP0 guest register 13/0 guestending 64 0 rw CP0 guest register 15/0 guestconfig 64 8000000 rw CP0 guest register 15/1 guestconfig 64 8000000 rw CP0 guest register 16/2 guestconfig 64 6000000 rw CP0 guest register 16/2 guestconfig 64 dould from the company of the company	guestcount	64	0	rw	
guestguestet12	guestentryhi	64	0	rw	CP0 guest register 10/0
guestcompare 64 0 rw CP0 guest register 11/6 guestcompare 64 0 rw CP0 guest register 11/6 gueststatus 64 400004 rw CP0 guest register 11/4 gueststatus 64 400004 rw CP0 guest register 12/0 gueststatus 64 4000000 rw CP0 guest register 12/1 guestsractl 64 0 rw CP0 guest register 12/1 guestsractl 64 0 rw CP0 guest register 12/2 guestsractl 64 0 rw CP0 guest register 12/3 guestsractl 64 0 rw CP0 guest register 12/3 guestsractl 64 0 rw CP0 guest register 12/6 guestsfolfset 64 0 rw CP0 guest register 12/6 guestsfolfset 64 0 rw CP0 guest register 12/7 guestsfolfset 64 0 rw CP0 guest register 12/6 guestsfolfset 64 0 rw CP0 guest register 13/0 guestprid 64 0 rw CP0 guest register 13/0 guestprid 64 0 rw CP0 guest register 15/0 guestfolfset 64 0 rw CP0 guest register 15/1 guestcomfig 64 8000000 rw CP0 guest register 16/1 guestcomfig 64 8000000 rw CP0 guest register 16/3 guestcomfig 64 doff0c027 rw CP0 guest register 16/2 guestcomfig 64 doff0c027 rw CP0 guest register 16/2 guestcomfig 64 doff0c027 rw CP0 guest register 16/3 guestcomfig 64 doff0c027 rw CP0 guest register 16/3 guestcomfig 64 doff0c027 rw CP0 guest register 16/6 guestcomfig 64 0 rw CP0 guest register 16/7 guestlandr 64 0 rw CP0 guest register 16/6 guestcomfig 64 0 rw CP0 guest register 16/6 guestcomfig 64 0 rw CP0 guest register 16/6 guestfondr 64 0 rw CP0 guest register 16/7 guestfandr 64 0 rw CP0 guest register 16/6 guestfandr 64 0 rw CP0 guest register 16/6 guestfandr 64 0 rw CP0 guest register 16/6 guestfandr 64 0 rw CP0 guest register 23/6 guestfandr 64 0 rw CP0 guest register 23/6 guestfandr 64 0 rw CP0 guest register	guestguestctl1	64	0	rw	CP0 guest register 10/4
guestcompare guestcollext guesticusextclDext guestistats 64 4400004 rw CP0 guest register 11/0 guestistats 64 4400004 rw CP0 guest register 12/0 guestistats guestintcl 64 e0000000 rw CP0 guest register 12/1 guestistats 64 0 rw CP0 guest register 12/2 guestsrsmap 64 0 rw CP0 guest register 12/3 guestigustictl 64 0 rw CP0 guest register 12/3 guestigustictl 64 0 rw CP0 guest register 12/6 guestigustictl 64 0 rw CP0 guest register 12/7 guestigustictl 64 0 rw CP0 guest register 12/7 guestigustictl 64 0 rw CP0 guest register 13/0 guestigustictl 64 0 rw CP0 guest register 13/0 guestigustictl 64 0 rw CP0 guest register 15/0 guestigustigustictl 64 0 rw CP0 guest register 15/0 guestigustigustigustigustigustigustigustigu	guestguestctl2	64	0	rw	CP0 guest register 10/5
guestguestetl0ext 64 440004 rw CP0 guest register 11/4 guestiatus 64 440004 rw CP0 guest register 12/0 guestintct1 64 e0000000 rw CP0 guest register 12/1 guestintct1 64 0000000 rw CP0 guest register 12/2 guestintsmap 64 0 rw CP0 guest register 12/3 guestguestetl0 61 0 rw CP0 guest register 12/6 guestintsguestetl0 61 0 rw CP0 guest register 12/6 guestintsguestetl0 64 0 rw CP0 guest register 12/7 guestintsguestetl0 64 0 rw CP0 guest register 12/7 guestintsguestetl0 64 0 rw CP0 guest register 13/0 guestintsguestetl0 64 0 rw CP0 guest register 13/0 guestepe 64 0 rw CP0 guest register 15/0 guestepiter 15/0 guestement 64 0 rw CP0 guest register 15/0 guestement 64 0 rw CP0 guest register 15/0 guestement 64 0 rw CP0 guest register 15/0 guestemoning 64 8000000 rw CP0 guest register 16/0 guestonfig 64 9eab5593 rw CP0 guest register 16/0 guestonfig 64 8000000 rw CP0 guest register 16/1 guestonfig 64 dof03161 rw CP0 guest register 16/3 guestonfig 64 dof0227 rw CP0 guest register 16/5 guestonfig 64 dof0 rw CP0 guest register 16/5 guestonfig 64 dof0 rw CP0 guest register 16/6 guestonfig 64 dof0 rw CP0 guest register 17/0 guest guestonfig 64 0 rw CP0 guest register 17/0 guestladdr 64 0 rw CP0 guest register 17/1 guestladdr 64 0 rw CP0 guest register 17/2 guestlandr 64 0 rw CP0 guest register 23/1 guestlandr 64 0 rw CP0 guest register 24/4 guestlandrandrandrandrandrandrandrandrandrandr	guestguestctl3	64	0	rw	CP0 guest register 10/6
guestiatus	guestcompare	64	0	rw	CP0 guest register 11/0
guestinted   64   e0000000   rw   CP0 guest register 12/1   guestinstal   64   0   rw   CP0 guest register 12/2   guestinsmap   64   0   rw   CP0 guest register 12/3   guestinsmap   64   0   rw   CP0 guest register 12/3   guestinsmap   64   0   rw   CP0 guest register 12/5   guestinsmap   64   0   rw   CP0 guest register 12/7   guestinsmap   64   0   rw   CP0 guest register 13/0   guestepe   64   0   rw   CP0 guest register 13/0   guestepe   64   0   rw   CP0 guest register 14/0   guestinsmap   64   60   rw   CP0 guest register 15/1   guestinsmap   64   80000000   rw   CP0 guest register 15/1   guestinsmap   64   9eab5593   rw   CP0 guest register 16/1   guestinsmap   64   dofro227   rw   CP0 guest register 16/2   guestinsmap   64   dofro227   rw   CP0 guest register 16/2   guestinsmap   64   dofro227   rw   CP0 guest register 16/3   guestinsmap   64   dofro227   rw   CP0 guest register 16/5   guestinsmap   64   dofro227   rw   CP0 guest register 16/5   guestinsmap   64   dofro227   rw   CP0 guest register 16/5   guestinsmap   64   dofro227   rw   CP0 guest register 17/0   guestinsmap   64   dofro227   rw   CP0 guest register 23/0   guestitracecontrol   64   dofro227   rw   CP0 guest register 23/0   guestitracecontrol   64   dofro227   rw   CP0 guest register 23/3   guestitracecontrol   64   dofro227   rw   CP0 guest register 23/4   guestitp   2.3.action   64   dofro227   rw   CP0 guest register 24/0   guestitp	guestguestctl0ext	64	0	rw	CP0 guest register 11/4
guestintell         64         6000000         rw         CP0 guest register 12/1           guestsrsmap         64         0         rw         CP0 guest register 12/2           guestguestello         64         0         rw         CP0 guest register 12/3           guestguestello         64         0         rw         CP0 guest register 12/6           guestguestello         64         0         rw         CP0 guest register 12/7           guestcause         64         0         rw         CP0 guest register 13/0           guestcause         64         0         rw         CP0 guest register 15/0           guestcause         64         0         rw         CP0 guest register 15/0           guestcause         64         0         rw         CP0 guest register 15/1           guestconfig         64         0         rw         CP0 guest register 16/0           guestconfig1         64         9eab5593         rw         CP0 guest register 16/2           guestconfig2         64         80000000         rw         CP0 guest register 16/2           guestconfig3         64         do003161         rw         CP0 guest register 16/3           guestconfig3         64         do00227	gueststatus	64	4400004	rw	CP0 guest register 12/0
guestsracht         64         0         rw         CPO guest register 12/2           guestgrusstramap         64         0         rw         CPO guest register 12/3           guestguestculo         64         0         rw         CPO guest register 12/6           guestdoffset         64         0         rw         CPO guest register 13/0           guestdoffset         64         0         rw         CPO guest register 13/0           guestdoffset         64         0         rw         CPO guest register 15/0           guestdoffset         64         0         rw         CPO guest register 15/0           guestdomore         64         ffffffffffffffffffffffffff         rw         CPO guest register 15/3           guestdomfg         64         80000002         rw         CPO guest register 16/0           guestconfig1         64         9eab5593         rw         CPO guest register 16/1           guestconfig2         64         80000000         rw         CPO guest register 16/3           guestconfig3         64         de003161         rw         CPO guest register 16/3           guestconfig4         64         doft0c227         rw         CPO guest register 16/3           guestconfig3		64	e0000000	rw	CP0 guest register 12/1
guestsramap         64         0         rw         CPO guest register 12/3           guestguestcul0         64         0         rw         CPO guest register 12/6           guestguester         64         0         rw         CPO guest register 13/0           guester         64         0         rw         CPO guest register 13/0           guestprid         64         0         rw         CPO guest register 15/0           guestchase         64         ffffffff         rw         CPO guest register 15/1           guestconfig         64         80000000         rw         CPO guest register 16/0           guestconfig         64         80000000         rw         CPO guest register 16/1           guestconfig         64         80000000         rw         CPO guest register 16/3           guestconfig         64         80000000         rw         CPO guest register 16/3           guestconfig         64         40f60227         rw         CPO guest register 16/3           guestconfig         64         40f60227         rw         CPO guest register 16/3           guestconfig         64         0         rw         CPO guest register 16/6           guestconfig         64         0 <td></td> <td>64</td> <td>0</td> <td>rw</td> <td></td>		64	0	rw	
guestguestctl0         64         0         rw         CP0 guest register 12/6           guestdoffset         64         0         rw         CP0 guest register 13/0           guestepe         64         0         rw         CP0 guest register 13/0           guestprid         64         0         rw         CP0 guest register 15/0           guestbase         64         fffffff         rw         CP0 guest register 15/1           guestconfig         64         80000000         rw         CP0 guest register 15/1           guestconfig         64         80000000         rw         CP0 guest register 16/0           guestconfig2         64         80000000         rw         CP0 guest register 16/0           guestconfig2         64         80000000         rw         CP0 guest register 16/2           guestconfig3         64         dof0227         rw         CP0 guest register 16/3           guestconfig5         64         498         rw         CP0 guest register 16/5           guestconfig6         64         0         rw         CP0 guest register 17/0           guestfmaar         64         0         rw         CP0 guest register 17/1           guestfmaar         64         0		64	0	rw	
guestgoffset         64         0         rw         CP0 guest register 12/7           guestepc         64         0         rw         CP0 guest register 13/0           guestprid         64         0         rw         CP0 guest register 15/0           guestchase         64         ffffffffffffffffffffffffffffffffffff		64	0	rw	· · · · · · · · · · · · · · · · · · ·
guesteque         64         0         rw         CPO guest register 13/0           guesteppe         64         0         rw         CPD guest register 14/0           guestrid         64         0         rw         CPO guest register 15/0           guestebase         64         fffffff         rw         CPO guest register 15/1           guestconfig         64         0         rw         CPO guest register 16/2           guestconfig         64         8000ca02         rw         CPO guest register 16/1           guestconfig2         64         8000ca00         rw         CPO guest register 16/1           guestconfig3         64         dc003161         rw         CPO guest register 16/2           guestconfig3         64         dcf00227         rw         CPO guest register 16/3           guestconfig6         64         498         rw         CPO guest register 16/3           guestconfig6         64         498         rw         CPO guest register 16/3           guestconfig7         64         0         rw         CPO guest register 16/5           guestfaddr         64         0         rw         CPO guest register 16/5           guestmaar         64         0 <t< td=""><td></td><td>64</td><td>0</td><td>rw</td><td></td></t<>		64	0	rw	
guesteprid			0	rw	
guestprid         64         ffffffff         rw         CP0 guest register 15/0           guestcmgcrbase         64         ffffffff         rw         CP0 guest register 15/1           guestconfig         64         8000ca02         rw         CP0 guest register 16/0           guestconfig1         64         9eab5593         rw         CP0 guest register 16/1           guestconfig2         64         80000000         rw         CP0 guest register 16/2           guestconfig3         64         de0603161         rw         CP0 guest register 16/3           guestconfig5         64         488         rw         CP0 guest register 16/5           guestconfig6         64         4060227         rw         CP0 guest register 16/6           guestconfig6         64         488         rw         CP0 guest register 16/6           guestconfig6         64         0         rw         CP0 guest register 17/0           guestladdr         64         0         rw         CP0 guest register 17/1           guestmaar         64         0         rw         CP0 guest register 23/0           guestfracecontrol         64         0         rw         CP0 guest register 23/1           guestfracecontrol		64		rw	
guestebase         64         fffffffffsom of the source of		64	0	rw	
guestcmgcrbase         64         0         rw         CP0 guest register 15/3           guestconfig         64         8000ca02         rw         CP0 guest register 16/0           guestconfig1         64         9eab5593         rw         CP0 guest register 16/1           guestconfig2         64         8000000         rw         CP0 guest register 16/2           guestconfig3         64         de003161         rw         CP0 guest register 16/3           guestconfig4         64         dof00227         rw         CP0 guest register 16/3           guestconfig5         64         498         rw         CP0 guest register 16/5           guestconfig7         64         0         rw         CP0 guest register 16/6           guesttonfig7         64         0         rw         CP0 guest register 17/0           guestmaar         64         0         rw         CP0 guest register 17/1           guestmaari         64         0         rw         CP0 guest register 20/0           guestdebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol         64					
guestconfig         64         8000ca02         rw         CP0 guest register 15/3           guestconfig1         64         8000ca02         rw         CP0 guest register 16/0           guestconfig2         64         80000000         rw         CP0 guest register 16/2           guestconfig3         64         dc003161         rw         CP0 guest register 16/3           guestconfig4         64         d0fc0227         rw         CP0 guest register 16/4           guestconfig5         64         498         rw         CP0 guest register 16/6           guestconfig6         64         0         rw         CP0 guest register 16/7           guestladdr         64         0         rw         CP0 guest register 17/0           guestmaar         64         0         rw         CP0 guest register 17/1           guestkacontext         64         0         rw         CP0 guest register 20/0           guesttracecontext         64         0         rw         CP0 guest register 23/0           guesttracecontrol2         64         0         rw         CP0 guest register 23/2           guesttraceibpc         64         0         rw         CP0 guest register 23/3           guesttraceibpc         64	0	-			0-0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
guestconfig         64         8000ca02         rw         CP0 guest register 16/0           guestconfig1         64         9eab5593         rw         CP0 guest register 16/1           guestconfig2         64         80000000         rw         CP0 guest register 16/2           guestconfig3         64         de003161         rw         CP0 guest register 16/3           guestconfig5         64         498         rw         CP0 guest register 16/5           guestconfig6         64         0         rw         CP0 guest register 16/6           guestconfig7         64         0         rw         CP0 guest register 16/7           guestladdr         64         0         rw         CP0 guest register 17/0           guestmaar         64         0         rw         CP0 guest register 17/1           guestmaari         64         0         rw         CP0 guest register 20/0           guestdebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol2         64         0         rw         CP0 guest register 23/2           guestusertracedata         64 <td< td=""><td>guestcmgcrbase</td><td>64</td><td></td><td>rw</td><td>CP0 guest register 15/3</td></td<>	guestcmgcrbase	64		rw	CP0 guest register 15/3
guestconfig1         64         9eab5593         rw         CP0 guest register 16/1           guestconfig2         64         80000000         rw         CP0 guest register 16/2           guestconfig3         64         d0060227         rw         CP0 guest register 16/3           guestconfig4         64         d0fc0227         rw         CP0 guest register 16/4           guestconfig5         64         498         rw         CP0 guest register 16/6           guestconfig6         64         0         rw         CP0 guest register 16/6           guestconfig7         64         0         rw         CP0 guest register 17/0           guestmaar         64         0         rw         CP0 guest register 17/1           guestmaar         64         0         rw         CP0 guest register 17/2           guestmaari         64         0         rw         CP0 guest register 20/0           guestdebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/2           guesttracedata         64         0         rw         CP0 guest register 23/2           guesttracedbpc         64         0				_	
guestconfig2         64         80000000         rw         CP0 guest register 16/2           guestconfig3         64         d0003161         rw         CP0 guest register 16/3           guestconfig4         64         d0fc0227         rw         CP0 guest register 16/4           guestconfig5         64         498         rw         CP0 guest register 16/5           guestconfig6         64         0         rw         CP0 guest register 16/7           guestladdr         64         0         rw         CP0 guest register 17/0           guestmaar         64         0         rw         CP0 guest register 17/1           guestmaari         64         0         rw         CP0 guest register 17/2           guestmaari         64         0         rw         CP0 guest register 23/0           guestrocontext         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol of 64         0         rw         CP0 guest register 23/2           guesttracedbpc         64         0         rw         CP0 guest register 23/3           guesttpb2_3_action         64         0         <					
guestconfig3         64         dc003161         rw         CP0 guest register 16/3           guestconfig4         64         d0fc0227         rw         CP0 guest register 16/4           guestconfig5         64         498         rw         CP0 guest register 16/6           guestconfig6         64         0         rw         CP0 guest register 16/6           guestconfig7         64         0         rw         CP0 guest register 16/7           guestmaar         64         0         rw         CP0 guest register 17/0           guestmaari         64         0         rw         CP0 guest register 17/2           guestxcontext         64         0         rw         CP0 guest register 20/0           guesttacecontrol         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol         64         0         rw         CP0 guest register 23/3           guesttracedata         64         0         rw         CP0 guest register 23/3           guesttracedbpc         64         0         rw         CP0 guest register 24/2           guesttbp2.3.action         64					
guestconfig4         64         d0fc0227         rw         CP0 guest register 16/4           guestconfig5         64         498         rw         CP0 guest register 16/5           guestconfig6         64         0         rw         CP0 guest register 16/6           guestconfig7         64         0         rw         CP0 guest register 17/0           guestmaar         64         0         rw         CP0 guest register 17/1           guestmaari         64         0         rw         CP0 guest register 20/0           guestkebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol2         64         0         rw         CP0 guest register 23/2           guesttracedbag         64         0         rw         CP0 guest register 23/3           guesttracedbpc         64         0         rw         CP0 guest register 23/4           guesttbp2.3_action         64         0         rw         CP0 guest register 24/0           guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2.3_action         64         0				_	
guestconfig5         64         498         rw         CP0 guest register 16/5           guestconfig6         64         0         rw         CP0 guest register 16/6           guestladdr         64         0         rw         CP0 guest register 16/7           guestladdr         64         0         rw         CP0 guest register 17/0           guestmaar         64         0         rw         CP0 guest register 17/1           guestmaari         64         0         rw         CP0 guest register 20/0           guestdebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol2         64         0         rw         CP0 guest register 23/2           guesttracedata         64         0         rw         CP0 guest register 23/3           guesttracedbpc         64         0         rw         CP0 guest register 23/4           guesttpp2.3_action         64         0         rw         CP0 guest register 24/0           guestdbp2.3_action         64         0         rw         CP0 guest register 24/0           guestdbp2.3_action         64         0					
guestconfig6         64         0         rw         CP0 guest register 16/6           guestladdr         64         0         rw         CP0 guest register 16/7           guestmaar         64         0         rw         CP0 guest register 17/0           guestmaar         64         0         rw         CP0 guest register 17/1           guestxcontext         64         0         rw         CP0 guest register 20/0           guestdebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol2         64         0         rw         CP0 guest register 23/2           guesttracetabec         64         0         rw         CP0 guest register 23/3           guesttracetabpc         64         0         rw         CP0 guest register 23/4           guesttip2_3_action         64         0         rw         CP0 guest register 24/2           guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2_3_action         64         0         rw         CP0 guest register 24/2           guesttracecontrol3         64         0					
guestconfig7         64         0         rw         CP0 guest register 16/7           guestlladdr         64         0         rw         CP0 guest register 17/0           guestmaar         64         0         rw         CP0 guest register 17/1           guestmaari         64         0         rw         CP0 guest register 17/2           guestxcontext         64         0         rw         CP0 guest register 23/0           guestdebug         64         0         rw         CP0 guest register 23/1           guesttracecontrol         64         0         rw         CP0 guest register 23/2           guesttracecontrol2         64         0         rw         CP0 guest register 23/3           guesttraceibpc         64         0         rw         CP0 guest register 23/4           guesttracedbpc         64         0         rw         CP0 guest register 23/5           guesttbp2_3_action         64         0         rw         CP0 guest register 24/0           guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2_3_action         64         0         rw         CP0 guest register 24/1           guestbp2_3_action         64         0					
guestladdr         64         0         rw         CP0 guest register 17/0           guestmaar         64         0         rw         CP0 guest register 17/1           guestmaari         64         0         rw         CP0 guest register 17/2           guestxcontext         64         0         rw         CP0 guest register 20/0           guestdebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol2         64         0         rw         CP0 guest register 23/2           guestusertracedata         64         0         rw         CP0 guest register 23/3           guesttraceibpc         64         0         rw         CP0 guest register 23/4           guesttp2_3_action         64         0         rw         CP0 guest register 23/5           guestdepc         64         0         rw         CP0 guest register 24/0           guestdp2_3_action         64         0         rw         CP0 guest register 24/0           guestdp2_3_action         64         0         rw         CP0 guest register 24/1           guestdp2_3_action         64         0				_	
guestmaar         64         0         rw         CP0 guest register 17/1           guestmaari         64         0         rw         CP0 guest register 17/2           guestxcontext         64         0         rw         CP0 guest register 20/0           guestdebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guestusertracedata         64         0         rw         CP0 guest register 23/2           guesttraceibpc         64         0         rw         CP0 guest register 23/3           guesttracedbpc         64         0         rw         CP0 guest register 23/4           guestibp2.3.action         64         0         rw         CP0 guest register 23/7           guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2.3.action         64         0         rw         CP0 guest register 24/1           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guestbp4.5.action         64					
guestmaari         64         0         rw         CP0 guest register 17/2           guestxcontext         64         0         rw         CP0 guest register 20/0           guestdebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol2         64         0         rw         CP0 guest register 23/2           guestusertracedata         64         0         rw         CP0 guest register 23/3           guesttracedbpc         64         0         rw         CP0 guest register 23/4           guestibp2.3 action         64         0         rw         CP0 guest register 23/5           guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2.3 action         64         0         rw         CP0 guest register 24/1           guestdbp2.3 action         64         0         rw         CP0 guest register 24/2           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestbconfig         64         0         rw         CP0 guest register 24/3           guestbp4.5 action         64					·
guestdebug         64         0         rw         CP0 guest register 20/0           guestdebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol         64         0         rw         CP0 guest register 23/2           guestusertracedata         64         0         rw         CP0 guest register 23/3           guesttracedbpc         64         0         rw         CP0 guest register 23/4           guestibp2.3_action         64         0         rw         CP0 guest register 23/7           guestdepc         64         0         rw         CP0 guest register 24/0           guestdp2.3_action         64         0         rw         CP0 guest register 24/1           guestdp2.3_action         64         0         rw         CP0 guest register 24/2           guestdp2.3_action         64         0         rw         CP0 guest register 24/2           guestdracecontrol3         64         0         rw         CP0 guest register 24/2           guestbcbconfig         64         0         rw         CP0 guest register 24/3           guestbcbcontrole         64				-	
guestdebug         64         0         rw         CP0 guest register 23/0           guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol2         64         0         rw         CP0 guest register 23/2           guestusertracedata         64         0         rw         CP0 guest register 23/3           guesttracedbpc         64         0         rw         CP0 guest register 23/4           guestibp2.3_action         64         0         rw         CP0 guest register 23/7           guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2.3_action         64         0         rw         CP0 guest register 24/1           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guestibp4.5_action         64         0         rw         CP0 guest register 24/5           guestibp6.7_action         64         0         rw         CP0 guest register 25/0           guestperfctl0         64					
guesttracecontrol         64         0         rw         CP0 guest register 23/1           guesttracecontrol2         64         0         rw         CP0 guest register 23/2           guestusertracedata         64         0         rw         CP0 guest register 23/3           guesttracedbpc         64         0         rw         CP0 guest register 23/4           guestibp2_3_action         64         0         rw         CP0 guest register 23/7           guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2_3_action         64         0         rw         CP0 guest register 24/1           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttbp4_5_action         64         0         rw         CP0 guest register 24/6           guestibp6_7_action         64         0         rw         CP0 guest register 25/0           guestperfctl0         64         80000000         rw         CP0 guest register 25/1           guestperfctl1					·
guesttracecontrol2         64         0         rw         CP0 guest register 23/2           guestusertracedata         64         0         rw         CP0 guest register 23/3           guesttraceibpc         64         0         rw         CP0 guest register 23/4           guestibp2.3.action         64         0         rw         CP0 guest register 23/7           guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2.3.action         64         0         rw         CP0 guest register 24/1           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4.5.action         64         0         rw         CP0 guest register 24/6           guestpefctl0         64         80000000         rw         CP0 guest register 25/0           guestperfctl1         64         0         rw         CP0 guest register 25/2					
guestusertracedata         64         0         rw         CP0 guest register 23/3           guesttraceibpc         64         0         rw         CP0 guest register 23/4           guestibp2_3_action         64         0         rw         CP0 guest register 23/7           guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2_3_action         64         0         rw         CP0 guest register 24/1           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4_5_action         64         0         rw         CP0 guest register 24/6           guestibp6_7_action         64         0         rw         CP0 guest register 25/0           guestperfctl0         64         80000000         rw         CP0 guest register 25/1           guestperfctl1         64         80000000         rw         CP0 guest register 25/2				-	
guesttraceibpc         64         0         rw         CP0 guest register 23/4           guesttracedbpc         64         0         rw         CP0 guest register 23/5           guestibp2_3_action         64         0         rw         CP0 guest register 24/0           guestdbp2_3_action         64         0         rw         CP0 guest register 24/1           guestdbp2_3_action         64         0         rw         CP0 guest register 24/2           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4_5_action         64         0         rw         CP0 guest register 24/6           guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfctl1         64         80000000         rw         CP0 guest register 25/2				_	
guestibp2_3_action         64         0         rw         CP0 guest register 23/5           guestibp2_3_action         64         0         rw         CP0 guest register 24/0           guestdbp2_3_action         64         0         rw         CP0 guest register 24/1           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4_5_action         64         0         rw         CP0 guest register 24/6           guestibp6_7_action         64         0         rw         CP0 guest register 24/7           guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfctl1         64         80000000         rw         CP0 guest register 25/2	0				
guestibp2_3_action         64         0         rw         CP0 guest register 23/7           guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2_3_action         64         0         rw         CP0 guest register 24/1           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4_5_action         64         0         rw         CP0 guest register 24/7           guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfctl1         64         80000000         rw         CP0 guest register 25/2					
guestdepc         64         0         rw         CP0 guest register 24/0           guestdbp2_3_action         64         0         rw         CP0 guest register 24/1           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4_5_action         64         0         rw         CP0 guest register 24/6           guestibp6_7_action         64         0         rw         CP0 guest register 25/0           guestperfctl0         64         80000000         rw         CP0 guest register 25/1           guestperfctl1         64         80000000         rw         CP0 guest register 25/2					
guestdbp2.3_action         64         0         rw         CP0 guest register 24/1           guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4_5_action         64         0         rw         CP0 guest register 24/6           guestibp6_7_action         64         0         rw         CP0 guest register 24/7           guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfctl1         64         80000000         rw         CP0 guest register 25/2					
guesttracecontrol3         64         0         rw         CP0 guest register 24/2           guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4_5_action         64         0         rw         CP0 guest register 24/6           guestibp6_7_action         64         0         rw         CP0 guest register 24/7           guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfctl1         64         80000000         rw         CP0 guest register 25/2					
guestusertracedata2         64         0         rw         CP0 guest register 24/3           guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4_5_action         64         0         rw         CP0 guest register 24/6           guestibp6_7_action         64         0         rw         CP0 guest register 24/7           guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfctl1         64         80000000         rw         CP0 guest register 25/1           guestperfctl1         64         80000000         rw         CP0 guest register 25/2				-	
guesttcbconfig         64         0         rw         CP0 guest register 24/4           guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4_5_action         64         0         rw         CP0 guest register 24/6           guestibp6_7_action         64         0         rw         CP0 guest register 24/7           guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfctl0         64         0         rw         CP0 guest register 25/1           guestperfctl1         64         80000000         rw         CP0 guest register 25/2	_				
guesttcbcontrole         64         0         rw         CP0 guest register 24/5           guestibp4_5_action         64         0         rw         CP0 guest register 24/6           guestibp6_7_action         64         0         rw         CP0 guest register 24/7           guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfcnt0         64         0         rw         CP0 guest register 25/1           guestperfctl1         64         80000000         rw         CP0 guest register 25/2	_				
guestibp4_5_action         64         0         rw         CP0 guest register 24/6           guestibp6_7_action         64         0         rw         CP0 guest register 24/7           guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfcnt0         64         0         rw         CP0 guest register 25/1           guestperfctl1         64         80000000         rw         CP0 guest register 25/2	_			rw	
guestibp6-7_action         64         0         rw         CP0 guest register 24/7           guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfcnt0         64         0         rw         CP0 guest register 25/1           guestperfctl1         64         80000000         rw         CP0 guest register 25/2				rw	
guestperfctl0         64         80000000         rw         CP0 guest register 25/0           guestperfcnt0         64         0         rw         CP0 guest register 25/1           guestperfctl1         64         80000000         rw         CP0 guest register 25/2				rw	
guestperfcnt0         64         0         rw         CP0 guest register 25/1           guestperfctl1         64         80000000         rw         CP0 guest register 25/2			_	rw	
guestperfctl1 64 80000000 rw CP0 guest register 25/2			80000000	rw	
			_	rw	
guestperfcnt1   64   0   rw   CP0 guest register 25/3			80000000	rw	
	guestperfcnt1	64	0	rw	CP0 guest register 25/3

guestperfctl2	64	80000000	rw	CP0 guest register 25/4
guestperfcnt2	64	0	rw	CP0 guest register 25/5
guestperfctl3	64	0	rw	CP0 guest register 25/6
guestperfcnt3	64	0	rw	CP0 guest register 25/7
guesterrctl	64	0	rw	CP0 guest register 26/0
guesttcbcontrold	64	0	rw	CP0 guest register 26/4
guestcacheerr	64	0	rw	CP0 guest register 27/0
guestitaglo	64	0	rw	CP0 guest register 28/0
guestidatalo	64	0	rw	CP0 guest register 28/1
guestdtaglo	64	0	rw	CP0 guest register 28/2
guestddatalo	64	0	rw	CP0 guest register 28/3
guestitaghi	64	0	rw	CP0 guest register 29/0
guestidatahi	64	0	rw	CP0 guest register 29/1
guestdtaghi	64	0	rw	CP0 guest register 29/2
guestddatahi	64	0	rw	CP0 guest register 29/3
guesterrorepc	64	0	rw	CP0 guest register 30/0
guestdesave	64	0	rw	CP0 guest register 31/0
guestkscratch1	64	0	rw	CP0 guest register 31/2
guestkscratch2	64	0	rw	CP0 guest register 31/3
guestkscratch3	64	0	rw	CP0 guest register 31/4
guestkscratch4	64	0	rw	CP0 guest register 31/5
guestkscratch5	64	0	rw	CP0 guest register 31/6
guestkscratch6	64	0	rw	CP0 guest register 31/7

Table 13.5: Registers at level 3, type:VP group:COP0

### 13.3.6 MSA

Registers at level:3, type:VP group:MSA

Name	Bits	Initial-Hex	RW	Description
w0	128	-	rw	
w1	128	-	rw	
w2	128	-	rw	
w3	128	-	rw	
w4	128	-	rw	
w5	128	-	rw	
w6	128	-	rw	
w7	128	-	rw	
w8	128	-	rw	
w9	128	-	rw	
w10	128	-	rw	
w11	128	-	rw	
w12	128	-	rw	
w13	128	-	rw	
w14	128	-	rw	
w15	128	-	rw	
w16	128	-	rw	
w17	128	-	rw	
w18	128	-	rw	
w19	128	-	rw	
w20	128	-	rw	
w21	128	-	rw	
w22	128	-	rw	
w23	128	-	rw	
w24	128	-	rw	

w25	128	_	rw	
w26	128	-	rw	
w27	128	-	rw	
w28	128	-	rw	
w29	128	-	rw	
w30	128	-	rw	
w31	128	-	rw	
msair	64	320	r-	MSA implementation
msacsr	64	0	rw	MSA control and status
msaaccess	64	-	r-	MSA access
msasave	64	-	r-	MSA save
msamodify	64	-	r-	MSA modify
msarequest	64	-	r-	MSA request
msamap	64	-	r-	MSA map
msaunmap	64	-	r-	MSA unmap

Table 13.6: Registers at level 3, type:VP group:MSA

# 13.3.7 CMP\_GCR

Registers at level:3, type: VP group: CMP\_GCR

Name	Bits	Initial-Hex	RW	Description
GCR_CONFIG	64	1	r-	-
GCR_BASE	64	1fbf8000	r-	
GCR_BASE_UPPER	64	0	rw	
GCR_CONTROL	64	40200000	rw	
GCR_REV	64	800	r-	
GCR_ERROR_CONTROL	64	13	rw	
GCR_ERROR_MASK	64	0	rw	
GCR_ERROR_CAUSE	64	0	r-	
GCR_ERROR_ADDR	64	0	r-	
GCR_ERROR_ADDR_UPPER	64	0	-	
GCR_ERROR_MULT	64	0	r-	
GCR_CUSTOM_BASE	64	0	rw	
GCR_CUSTOM_STATUS	64	0	r-	
GCR_GIC_BASE	64	0	rw	
GCR_GIC_BASE_UPPER	64	0	rw	
GCR_CPC_BASE	64	0	rw	
GCR_CPC_BASE_UPPER	64	0	rw	
GCR_GIC_STATUS	64	1	r-	
GCR_CACHE_REV	64	0	r-	
GCR_CPC_STATUS	64	1	r-	
GCR_ACCESS	64	3f	rw	
GCR_L2_CONFIG	64	0	rw	
GCR_SYS_CONFIG2	64	0	r-	
GCR_IOCU1_REV	64	400	r-	
GCR_BEV_BASE	64	bfc00000	rw	
GCR_MMIO_REQ_LIMIT	64	0	rw	
GCR_CL_COHERENCE	64	0	rw	
GCR_CL_CONFIG	64	3	r-	
GCR_CL_OTHER	64	0	rw	
GCR_CL_RESET_BASE	64	bfc00001	rw	
GCR_CL_ID	64	0	r-	
GCR_CO_COHERENCE	64	0	rw	
GCR_CO_CONFIG	64	3	r-	

GCR_CO_OTHER	64	0	rw	
GCR_CO_RESET_BASE	64	bfc00001	rw	
GCR_CO_ID	64	0	r-	

Table 13.7: Registers at level 3, type:VP group:CMP\_GCR

### 13.3.8 CMP\_CPC

Registers at level:3, type:VP group:CMP\_CPC

Name	Bits	Initial-Hex	RW	Description
CPC_SEQDEL	64	0	rw	
CPC_RAIL	64	0	rw	
CPC_RESETLEN	64	0	rw	
CPC_REVISION	64	0	r-	
CPC_CMD	64	3	rw	
CPC_STAT_CONF	64	b37203	rw	
CPC_CL_VP_STOP	64	0	rw	
CPC_CL_VP_RUN	64	1	rw	
CPC_CL_VP_RUNNING	64	1	r-	
CPC_CMD	64	3	rw	
CPC_STAT_CONF	64	b37203	rw	
CPC_CO_VP_STOP	64	0	rw	
CPC_CO_VP_RUN	64	1	rw	
CPC_CO_VP_RUNNING	64	1	r-	

Table 13.8: Registers at level 3, type:VP group:CMP\_CPC

#### 13.3.9 CMP\_GIC

Registers at level:3, type:VP group:CMP\_GIC

Name	Bits	Initial-Hex	RW	Description
GIC_SH_CONFIG	64	980f0007	rw	
GIC_Counter	64	0	rw	
GIC_SH_REVISION	64	500	r-	
GIC_SH_POL63_0	64	0	rw	
GIC_SH_POL127_64	64	0	rw	
GIC_SH_POL191_128	64	0	rw	
GIC_SH_POL255_192	64	0	rw	
GIC_SH_TRIG63_0	64	0	rw	
GIC_SH_TRIG127_64	64	0	rw	
GIC_SH_TRIG191_128	64	0	rw	
GIC_SH_TRIG255_192	64	0	rw	
GIC_SH_DUAL63_0	64	0	rw	
GIC_SH_DUAL127_64	64	0	rw	
GIC_SH_DUAL191_128	64	0	rw	
GIC_SH_DUAL255_192	64	0	rw	
GIC_SH_WEDGE	64	0	-w	
GIC_SH_RMASK63_0	64	0	-w	
GIC_SH_RMASK127_64	64	0	-w	
GIC_SH_RMASK191_128	64	0	-w	
GIC_SH_RMASK255_192	64	0	-w	
GIC_SH_SMASK63_0	64	0	-w	
GIC_SH_SMASK127_64	64	0	-W	

GIC_SH_SMASK191_128	64	0	-w	
GIC_SH_SMASK255_192	64	0	-w	
GIC_SH_MASK63_0	64	0	r-	
GIC_SH_MASK127_64	64	0	r-	
GIC_SH_MASK191_128	64	0	r-	
GIC_SH_MASK255_192	64	0	r-	
GIC_SH_PEND63_0	64	0	r-	
GIC_SH_PEND127_64	64	0	r-	
GIC_SH_PEND191_128	64	0	r-	
GIC_SH_PEND255_192	64	0	r-	
GIC_SH_MAP000_PIN	64	80000000	rw	
GIC_SH_MAP001_PIN	64	80000000	rw	
GIC_SH_MAP002_PIN	64	80000000	rw	
GIC_SH_MAP003_PIN	64	80000000	rw	
GIC_SH_MAP004_PIN	64	80000000	rw	
GIC_SH_MAP005_PIN	64	80000000	rw	
GIC_SH_MAP006_PIN	64	80000000	rw	
GIC_SH_MAP007_PIN	64	80000000	rw	
GIC_SH_MAP008_PIN	64	80000000	rw	
GIC_SH_MAP009_PIN	64	80000000	rw	
GIC_SH_MAP010_PIN	64	80000000	rw	
GIC_SH_MAP011_PIN	64	80000000	rw	
GIC_SH_MAP012_PIN	64	80000000	rw	
GIC_SH_MAP013_PIN	64	80000000	rw	
GIC_SH_MAP014_PIN	64	80000000	rw	
GIC_SH_MAP015_PIN	64	80000000	rw	
GIC_SH_MAP016_PIN	64	80000000	rw	
GIC_SH_MAP017_PIN	64	80000000	rw	
GIC_SH_MAP018_PIN	64	80000000	rw	
GIC_SH_MAP019_PIN	64	8000000	rw	
GIC_SH_MAP020_PIN	64	80000000	rw	
GIC_SH_MAP021_PIN	64	80000000		
GIC_SH_MAP022_PIN	64	8000000	rw	
GIC_SH_MAP023_PIN	64	80000000	rw	
GIC_SH_MAP023_FIN	64	8000000	rw	
GIC_SH_MAP024_PIN			rw	
GIC_SH_MAP025_PIN	64	80000000	rw	
GIC_SH_MAP026_PIN GIC_SH_MAP027_PIN	64	80000000	rw	
	-	80000000	rw	
GIC_SH_MAP028_PIN	64	80000000	rw	
GIC_SH_MAP029_PIN	64	80000000	rw	
GIC_SH_MAP030_PIN	64	80000000	rw	
GIC_SH_MAP031_PIN	64	80000000	rw	
GIC_SH_MAP032_PIN	64	80000000	rw	
GIC_SH_MAP033_PIN	64	80000000	rw	
GIC_SH_MAP034_PIN	64	80000000	rw	
GIC_SH_MAP035_PIN	64	80000000	rw	
GIC_SH_MAP036_PIN	64	80000000	rw	
GIC_SH_MAP037_PIN	64	80000000	rw	
GIC_SH_MAP038_PIN	64	80000000	rw	
GIC_SH_MAP039_PIN	64	80000000	rw	
GIC_SH_MAP040_PIN	64	80000000	rw	
GIC_SH_MAP041_PIN	64	80000000	rw	
GIC_SH_MAP042_PIN	64	80000000	rw	
GIC_SH_MAP043_PIN	64	80000000	rw	
GIC_SH_MAP044_PIN	64	80000000	rw	
GIC_SH_MAP045_PIN	64	80000000	rw	

GIC_SH_MAP046_PIN	64	80000000	rw	
GIC_SH_MAP047_PIN	64	80000000	rw	
GIC_SH_MAP048_PIN	64	80000000	rw	
GIC_SH_MAP049_PIN	64	80000000	rw	
GIC_SH_MAP050_PIN	64	80000000	rw	
GIC_SH_MAP051_PIN	64	80000000	rw	
GIC_SH_MAP052_PIN	64	80000000	rw	
GIC_SH_MAP053_PIN	64	80000000	rw	
GIC_SH_MAP054_PIN	64	80000000	rw	
GIC_SH_MAP055_PIN	64	80000000	rw	
GIC_SH_MAP056_PIN	64	80000000	rw	
GIC_SH_MAP057_PIN	64	80000000	rw	
GIC_SH_MAP058_PIN	64	80000000	rw	
GIC_SH_MAP059_PIN	64	80000000	rw	
GIC_SH_MAP060_PIN	64	80000000	rw	
GIC_SH_MAP061_PIN	64	80000000	rw	
GIC_SH_MAP062_PIN	64	80000000	rw	
GIC SH MAP063 PIN	64	80000000	rw	
GIC_SH_MAP064_PIN	64	80000000	rw	
GIC_SH_MAP065_PIN	64	80000000	rw	
GIC SH MAP066 PIN	64	80000000	rw	
GIC_SH_MAP067_PIN	64	80000000	rw	
GIC_SH_MAP068_PIN	64	80000000	rw	
GIC_SH_MAP069_PIN	64	80000000	rw	
GIC_SH_MAP070_PIN	64	80000000	rw	
GIC_SH_MAP071_PIN	64	80000000	rw	
GIC_SH_MAP072_PIN	64	80000000		
GIC_SH_MAP073_PIN	64	80000000	rw	
GIC_SH_MAP074_PIN	64	80000000	rw	
GIC_SH_MAP075_PIN	64	80000000	rw	
GIC_SH_MAP076_PIN	64	80000000	rw	
GIC_SH_MAP077_PIN	64	80000000	rw	
GIC_SH_MAP078_PIN	64	80000000	rw	
GIC_SH_MAP079_PIN	64	80000000	rw	
GIC_SH_MAP079_PIN	64		rw	
GIC_SH_MAP080_PIN		80000000	rw	
	64	80000000	rw	
GIC_SH_MAP082_PIN	64	80000000	rw	
GIC_SH_MAP083_PIN	64	80000000	rw	
GIC_SH_MAP084_PIN	64	80000000	rw	
GIC_SH_MAP085_PIN	64	80000000	rw	
GIC_SH_MAP086_PIN	64	80000000	rw	
GIC_SH_MAP087_PIN	64	80000000	rw	
GIC_SH_MAP088_PIN	64	80000000	rw	
GIC_SH_MAP089_PIN	64	80000000	rw	
GIC_SH_MAP090_PIN	64	80000000	rw	
GIC_SH_MAP091_PIN	64	80000000	rw	
GIC_SH_MAP092_PIN	64	80000000	rw	
GIC_SH_MAP093_PIN	64	80000000	rw	
GIC_SH_MAP094_PIN	64	80000000	rw	
GIC_SH_MAP095_PIN	64	80000000	rw	
GIC_SH_MAP096_PIN	64	80000000	rw	
GIC_SH_MAP097_PIN	64	80000000	rw	
GIC_SH_MAP098_PIN	64	80000000	rw	
GIC_SH_MAP099_PIN	64	80000000	rw	
GIC_SH_MAP100_PIN	64	80000000	rw	
GIC_SH_MAP101_PIN	64	80000000	rw	

GIC_SH_MAP102_PIN	64	80000000	rw	
GIC_SH_MAP103_PIN	64	80000000	rw	
GIC_SH_MAP104_PIN	64	80000000	rw	
GIC_SH_MAP105_PIN	64	80000000	rw	
GIC_SH_MAP106_PIN	64	80000000	rw	
GIC_SH_MAP107_PIN	64	80000000	rw	
GIC_SH_MAP108_PIN	64	80000000	rw	
GIC_SH_MAP109_PIN	64	80000000	rw	
GIC_SH_MAP110_PIN	64	80000000	rw	
GIC_SH_MAP111_PIN	64	80000000	rw	
GIC_SH_MAP112_PIN	64	80000000	rw	
GIC_SH_MAP113_PIN	64	80000000	rw	
GIC_SH_MAP114_PIN	64	80000000	rw	
GIC_SH_MAP115_PIN	64	80000000	rw	
GIC_SH_MAP116_PIN	64	80000000	rw	
GIC_SH_MAP117_PIN	64	80000000	rw	
GIC_SH_MAP118_PIN	64	80000000	rw	
GIC_SH_MAP119_PIN	64	80000000		
GIC_SH_MAP120_PIN	64	80000000	rw	
GIC_SH_MAP120_PIN GIC_SH_MAP121_PIN	64	80000000	rw	
GIC_SH_MAP121_FIN	64	80000000	rw	
GIC_SH_MAP122_PIN GIC_SH_MAP123_PIN	64	80000000	rw	
GIC_SH_MAP124_PIN	-		rw	
GIC SH MAP124 PIN	64	80000000 80000000	rw	
	64		rw	
GIC_SH_MAP126_PIN	64	80000000	rw	
GIC_SH_MAP127_PIN	64	80000000	rw	
GIC_SH_MAP128_PIN	64	0	rw	
GIC_SH_MAP129_PIN	64	0	rw	
GIC_SH_MAP130_PIN	64	0	rw	
GIC_SH_MAP131_PIN	64	0	rw	
GIC_SH_MAP132_PIN	64	0	rw	
GIC_SH_MAP133_PIN	64	0	rw	
GIC_SH_MAP134_PIN	64	0	rw	
GIC_SH_MAP135_PIN	64	0	rw	
GIC_SH_MAP136_PIN	64	0	rw	
GIC_SH_MAP137_PIN	64	0	rw	
GIC_SH_MAP138_PIN	64	0	rw	
GIC_SH_MAP139_PIN	64	0	rw	
GIC_SH_MAP140_PIN	64	0	rw	
GIC_SH_MAP141_PIN	64	0	rw	
GIC_SH_MAP142_PIN	64	0	rw	
GIC_SH_MAP143_PIN	64	0	rw	
GIC_SH_MAP144_PIN	64	0	rw	
GIC_SH_MAP145_PIN	64	0	rw	
GIC_SH_MAP146_PIN	64	0	rw	
GIC_SH_MAP147_PIN	64	0	rw	
GIC_SH_MAP148_PIN	64	0	rw	
GIC_SH_MAP149_PIN	64	0	rw	
GIC_SH_MAP150_PIN	64	0	rw	
GIC_SH_MAP151_PIN	64	0	rw	
GIC_SH_MAP152_PIN	64	0	rw	
GIC_SH_MAP153_PIN	64	0	rw	
GIC_SH_MAP154_PIN	64	0	rw	
GIC_SH_MAP155_PIN	64	0	rw	
GIC_SH_MAP156_PIN	64	0	rw	
	64	0	1	
GIC_SH_MAP157_PIN	1 ()4	U	rw	

GIC_SH_MAP158_PIN	64	0	rw	
GIC_SH_MAP159_PIN	64	0	rw	
GIC_SH_MAP160_PIN	64	0	rw	
GIC_SH_MAP161_PIN	64	0	rw	
GIC_SH_MAP162_PIN	64	0	rw	
GIC_SH_MAP163_PIN	64	0	rw	
GIC_SH_MAP164_PIN	64	0	rw	
GIC_SH_MAP165_PIN	64	0	rw	
GIC-SH_MAP166_PIN	64	0	rw	
GIC_SH_MAP167_PIN	64	0	rw	
GIC_SH_MAP168_PIN	64	0	rw	
GIC_SH_MAP169_PIN	64	0	rw	
GIC_SH_MAP170_PIN	64	0	rw	
GIC_SH_MAP171_PIN	64	0	rw	
GIC_SH_MAP172_PIN	64	0		
GIC_SH_MAP173_PIN	64	0	rw	
GIC_SH_MAP174_PIN	64	0	rw	
GIC_SH_MAP175_PIN	64	-	rw	
		0	rw	
GIC_SH_MAP176_PIN	64	0	rw	
GIC_SH_MAP177_PIN	64	0	rw	
GIC_SH_MAP178_PIN	64	0	rw	
GIC_SH_MAP179_PIN	64	0	rw	
GIC_SH_MAP180_PIN	64	0	rw	
GIC_SH_MAP181_PIN	64	0	rw	
GIC_SH_MAP182_PIN	64	0	rw	
GIC_SH_MAP183_PIN	64	0	rw	
GIC_SH_MAP184_PIN	64	0	rw	
GIC_SH_MAP185_PIN	64	0	rw	
GIC_SH_MAP186_PIN	64	0	rw	
GIC_SH_MAP187_PIN	64	0	rw	
GIC_SH_MAP188_PIN	64	0	rw	
GIC_SH_MAP189_PIN	64	0	rw	
GIC_SH_MAP190_PIN	64	0	rw	
GIC_SH_MAP191_PIN	64	0	rw	
GIC_SH_MAP192_PIN	64	0	rw	
GIC_SH_MAP193_PIN	64	0	rw	
GIC_SH_MAP194_PIN	64	0	rw	
GIC_SH_MAP195_PIN	64	0	rw	
GIC_SH_MAP196_PIN	64	0	rw	
GIC_SH_MAP197_PIN	64	0	rw	
GIC_SH_MAP198_PIN	64	0	rw	
GIC_SH_MAP199_PIN	64	0	rw	
GIC_SH_MAP200_PIN	64	0	rw	
GIC_SH_MAP201_PIN	64	0	-	
GIC_SH_MAP201_PIN	64	0	rw	
GIC_SH_MAP202_PIN GIC_SH_MAP203_PIN			rw	
	64	0	rw	
GIC_SH_MAP204_PIN	64	0	rw	
GIC_SH_MAP205_PIN	64	0	rw	
GIC_SH_MAP206_PIN	64	0	rw	
GIC_SH_MAP207_PIN	64	0	rw	
GIC_SH_MAP208_PIN	64	0	rw	
GIC_SH_MAP209_PIN	64	0	rw	
GIC_SH_MAP210_PIN	64	0	rw	
GIC_SH_MAP211_PIN	64	0	rw	
GIC_SH_MAP212_PIN	64	0	rw	
GIC_SH_MAP213_PIN	64	0	rw	

GIC_SH_MAP214_PIN	64	0	rw	
GIC_SH_MAP215_PIN	64	0	rw	
GIC_SH_MAP216_PIN	64	0	rw	
GIC_SH_MAP217_PIN	64	0	rw	
GIC_SH_MAP218_PIN	64	0	rw	
GIC_SH_MAP219_PIN	64	0	rw	
GIC_SH_MAP220_PIN	64	0	rw	
GIC_SH_MAP221_PIN	64	0	rw	
GIC_SH_MAP222_PIN	64	0	rw	
GIC_SH_MAP223_PIN	64	0	rw	
GIC_SH_MAP224_PIN	64	0	rw	
GIC_SH_MAP225_PIN	64	0	rw	
GIC_SH_MAP226_PIN	64	0	rw	
GIC_SH_MAP227_PIN	64	0	rw	
GIC_SH_MAP228_PIN	64	0		
GIC_SH_MAP229_PIN	64	0	rw	
	64	0	rw	
GIC_SH_MAP230_PIN		-	rw	
GIC_SH_MAP231_PIN	64	0	rw	
GIC_SH_MAP232_PIN	64	0	rw	
GIC_SH_MAP233_PIN	64	0	rw	
GIC_SH_MAP234_PIN	64	0	rw	
GIC_SH_MAP235_PIN	64	0	rw	
GIC_SH_MAP236_PIN	64	0	rw	
GIC_SH_MAP237_PIN	64	0	rw	
GIC_SH_MAP238_PIN	64	0	rw	
GIC_SH_MAP239_PIN	64	0	rw	
GIC_SH_MAP240_PIN	64	0	rw	
GIC_SH_MAP241_PIN	64	0	rw	
GIC_SH_MAP242_PIN	64	0	rw	
GIC_SH_MAP243_PIN	64	0	rw	
GIC_SH_MAP244_PIN	64	0	rw	
GIC_SH_MAP245_PIN	64	0	rw	
GIC_SH_MAP246_PIN	64	0	rw	
GIC_SH_MAP247_PIN	64	0	rw	
GIC_SH_MAP248_PIN	64	0	rw	
GIC_SH_MAP249_PIN	64	0	rw	
GIC_SH_MAP250_PIN	64	0	rw	
GIC_SH_MAP251_PIN	64	0	rw	
GIC_SH_MAP252_PIN	64	0		
GIC_SH_MAP253_PIN	64	0	rw	
GIC_SH_MAP253_PIN GIC_SH_MAP254_PIN	64	0	rw	
		_	rw	
GIC_SH_MAP255_PIN	64	0	rw	
GIC_SH_MAP000_VPE31_0	64	0	rw	
GIC_SH_MAP001_VPE31_0	64	0	rw	
GIC_SH_MAP002_VPE31_0	64	0	rw	
GIC_SH_MAP003_VPE31_0	64	0	rw	
GIC_SH_MAP004_VPE31_0	64	0	rw	
GIC_SH_MAP005_VPE31_0	64	0	rw	
GIC_SH_MAP006_VPE31_0	64	0	rw	
GIC_SH_MAP007_VPE31_0	64	0	rw	
GIC_SH_MAP008_VPE31_0	64	0	rw	
GIC_SH_MAP009_VPE31_0	64	0	rw	
GIC_SH_MAP010_VPE31_0	64	0	rw	
GIC_SH_MAP011_VPE31_0	64	0	rw	
GIC_SH_MAP012_VPE31_0	64	0	rw	
GIC_SH_MAP013_VPE31_0	64	0	rw	
	1 " -	1 -	1	

GIC_SH_MAP014_VPE31_0	64	0	rw	
GIC_SH_MAP015_VPE31_0	64	0	rw	
GIC_SH_MAP016_VPE31_0	64	0	rw	
GIC_SH_MAP017_VPE31_0	64	0	rw	
GIC_SH_MAP018_VPE31_0	64	0	rw	
GIC_SH_MAP019_VPE31_0	64	0	rw	
GIC_SH_MAP020_VPE31_0	64	0	rw	
GIC_SH_MAP021_VPE31_0	64	0	rw	
GIC_SH_MAP022_VPE31_0	64	0	rw	
GIC_SH_MAP023_VPE31_0	64	0	rw	
GIC_SH_MAP024_VPE31_0	64	0	rw	
GIC_SH_MAP025_VPE31_0	64	0	rw	
GIC_SH_MAP026_VPE31_0	64	0	rw	
GIC_SH_MAP027_VPE31_0	64	0	rw	
GIC_SH_MAP028_VPE31_0	64	0	rw	
GIC_SH_MAP029_VPE31_0	64	0	rw	
GIC_SH_MAP030_VPE31_0	64	0	rw	
GIC_SH_MAP031_VPE31_0	64	0	rw	
GIC_SH_MAP031_VPE31_0	64	0		
GIC_SH_MAP032_VPE31_0 GIC SH MAP033 VPE31_0	64	0	rw	
GIC_SH_MAP033_VPE31_0	64	0	rw	
GIC_SH_MAP034_VPE31_0	64	0	rw	
		-	rw	
GIC_SH_MAP036_VPE31_0	64	0	rw	
GIC_SH_MAP037_VPE31_0	64	0	rw	
GIC_SH_MAP038_VPE31_0	64	0	rw	
GIC_SH_MAP039_VPE31_0	64	0	rw	
GIC_SH_MAP040_VPE31_0	64	0	rw	
GIC_SH_MAP041_VPE31_0	64	0	rw	
GIC_SH_MAP042_VPE31_0	64	0	rw	
GIC_SH_MAP043_VPE31_0	64	0	rw	
GIC_SH_MAP044_VPE31_0	64	0	rw	
GIC_SH_MAP045_VPE31_0	64	0	rw	
GIC_SH_MAP046_VPE31_0	64	0	rw	
GIC_SH_MAP047_VPE31_0	64	0	rw	
GIC_SH_MAP048_VPE31_0	64	0	rw	
GIC_SH_MAP049_VPE31_0	64	0	rw	
GIC_SH_MAP050_VPE31_0	64	0	rw	
GIC_SH_MAP051_VPE31_0	64	0	rw	
GIC_SH_MAP052_VPE31_0	64	0	rw	
GIC_SH_MAP053_VPE31_0	64	0	rw	
GIC_SH_MAP054_VPE31_0	64	0	rw	
GIC_SH_MAP055_VPE31_0	64	0	rw	
GIC_SH_MAP056_VPE31_0	64	0	rw	
GIC_SH_MAP057_VPE31_0	64	0	rw	
GIC_SH_MAP058_VPE31_0	64	0	rw	
GIC_SH_MAP059_VPE31_0	64	0	rw	
GIC_SH_MAP060_VPE31_0	64	0	rw	
GIC_SH_MAP061_VPE31_0	64	0	rw	
GIC_SH_MAP062_VPE31_0	64	0	rw	
GIC_SH_MAP063_VPE31_0	64	0	rw	
GIC_SH_MAP064_VPE31_0	64	0	rw	
GIC_SH_MAP065_VPE31_0	64	0	rw	
GIC_SH_MAP066_VPE31_0	64	0		
GIC_SH_MAP060_VPE31_0	64	0	rw	
	-	_	rw	
GIC_SH_MAP068_VPE31_0	64	0	rw	
GIC_SH_MAP069_VPE31_0	64	0	rw	

GIC_SH_MAP070_VPE31_0	64	0	rw	
GIC_SH_MAP071_VPE31_0	64	0	rw	
GIC_SH_MAP072_VPE31_0	64	0	rw	
GIC_SH_MAP073_VPE31_0	64	0	rw	
GIC_SH_MAP074_VPE31_0	64	0	rw	
GIC_SH_MAP075_VPE31_0	64	0	rw	
GIC_SH_MAP076_VPE31_0	64	0	rw	
GIC_SH_MAP077_VPE31_0	64	0	rw	
GIC_SH_MAP078_VPE31_0	64	0	rw	
GIC SH MAP079 VPE31 0	64	0	rw	
GIC_SH_MAP080_VPE31_0	64	0	rw	
GIC_SH_MAP081_VPE31_0	64	0	rw	
GIC_SH_MAP082_VPE31_0	64	0	rw	
GIC_SH_MAP083_VPE31_0	64	0	rw	
GIC_SH_MAP084_VPE31_0	64	0		
GIC_SH_MAP085_VPE31_0	64	0	rw	
GIC_SH_MAP086_VPE31_0	64	0	rw	
GIC_SH_MAP087_VPE31_0	-	0	rw	
	64		rw	
GIC_SH_MAP088_VPE31_0	64	0	rw	
GIC_SH_MAP089_VPE31_0	-	0	rw	
GIC_SH_MAP090_VPE31_0	64	0	rw	
GIC_SH_MAP091_VPE31_0	64	0	rw	
GIC_SH_MAP092_VPE31_0	64	0	rw	
GIC_SH_MAP093_VPE31_0	64	0	rw	
GIC_SH_MAP094_VPE31_0	64	0	rw	
GIC_SH_MAP095_VPE31_0	64	0	rw	
GIC_SH_MAP096_VPE31_0	64	0	rw	
GIC_SH_MAP097_VPE31_0	64	0	rw	
GIC_SH_MAP098_VPE31_0	64	0	rw	
GIC_SH_MAP099_VPE31_0	64	0	rw	
GIC_SH_MAP100_VPE31_0	64	0	rw	
GIC_SH_MAP101_VPE31_0	64	0	rw	
GIC_SH_MAP102_VPE31_0	64	0	rw	
GIC_SH_MAP103_VPE31_0	64	0	rw	
GIC_SH_MAP104_VPE31_0	64	0	rw	
GIC_SH_MAP105_VPE31_0	64	0	rw	
GIC_SH_MAP106_VPE31_0	64	0	rw	
GIC_SH_MAP107_VPE31_0	64	0	rw	
GIC_SH_MAP108_VPE31_0	64	0	rw	
GIC_SH_MAP109_VPE31_0	64	0	rw	
GIC_SH_MAP110_VPE31_0	64	0	rw	
GIC_SH_MAP111_VPE31_0	64	0	rw	
GIC_SH_MAP112_VPE31_0	64	0	rw	
GIC_SH_MAP113_VPE31_0	64	0	rw	
GIC_SH_MAP114_VPE31_0	64	0	rw	
GIC_SH_MAP115_VPE31_0	64	0	rw	
GIC_SH_MAP116_VPE31_0	64	0	rw	
GIC_SH_MAP117_VPE31_0	64	0		
GIC_SH_MAP118_VPE31_0	64	0	rw	
GIC_SH_MAP119_VPE31_0	64	0	rw	
	-	0	rw	
GIC_SH_MAP120_VPE31_0	64	0	rw	
GIC_SH_MAP121_VPE31_0	64	-	rw	
GIC_SH_MAP122_VPE31_0	64	0	rw	
GIC_SH_MAP123_VPE31_0	64	0	rw	
GIC_SH_MAP124_VPE31_0	64	0	rw	
GIC_SH_MAP125_VPE31_0	64	0	rw	

GIC SH.MAP126.VPE31.0 64 0 rw GIC SH.MAP128.VPE31.0 64 0 rw GIC SH.MAP129.VPE31.0 64 0 rw GIC SH.MAP130.VPE31.0 64 0 rw GIC SH.MAP140.VPE31.0 64 0 rw GIC SH.MAP140.VPE31.0 64 0 rw GIC SH.MAP141.VPE31.0 64 0 rw GIC SH.MAP140.VPE31.0 64 0 rw GIC SH.MAP160.VPE31.0 64 0 rw GIC SH					
GIC SH MAP128, VPE31.0 64 0 rw GIC SH MAP130, VPE31.0 64 0 rw GIC SH MAP131, VPE31.0 64 0 rw GIC SH MAP132, VPE31.0 64 0 rw GIC SH MAP132, VPE31.0 64 0 rw GIC SH MAP132, VPE31.0 64 0 rw GIC SH MAP134, VPE31.0 64 0 rw GIC SH MAP136, VPE31.0 64 0 rw GIC SH MAP137, VPE31.0 64 0 rw GIC SH MAP138, VPE31.0 64 0 rw GIC SH MAP139, VPE31.0 64 0 rw GIC SH MAP139, VPE31.0 64 0 rw GIC SH MAP140, VPE31.0 64 0 rw GIC SH MAP140, VPE31.0 64 0 rw GIC SH MAP141, VPE31.0 64 0 rw GIC SH MAP140, VPE31.0 64 0 rw GIC SH MAP150, VPE31.0 64 0 rw GIC SH MAP160, VPE31.0 64 0 rw GIC SH MAP170, VPE31.0 64 0 rw GIC SH MAP170, VPE31.0 64 0 rw	GIC_SH_MAP126_VPE31_0	64	0	rw	
GIC SILMAP130, VPE31.0 64 0 rw GIC SILMAP131, VPE31.0 64 0 rw GIC SILMAP131, VPE31.0 64 0 rw GIC SILMAP133, VPE31.0 64 0 rw GIC SILMAP135, VPE31.0 64 0 rw GIC SILMAP135, VPE31.0 64 0 rw GIC SILMAP136, VPE31.0 64 0 rw GIC SILMAP136, VPE31.0 64 0 rw GIC SILMAP137, VPE31.0 64 0 rw GIC SILMAP139, VPE31.0 64 0 rw GIC SILMAP139, VPE31.0 64 0 rw GIC SILMAP139, VPE31.0 64 0 rw GIC SILMAP140, VPE31.0 64 0 rw GIC SILMAP141, VPE31.0 64 0 rw GIC SILMAP140, VPE31.0 64 0 rw GIC SILMAP151, VPE31.0 64 0 rw GIC SILMAP152, VPE31.0 64 0 rw GIC SILMAP153, VPE31.0 64 0 rw GIC SILMAP154, VPE31.0 64 0 rw GIC SILMAP164, VPE31.0 64 0 rw	GIC_SH_MAP127_VPE31_0	64	0	rw	
GIC.SH.MAP13.VPE31.0 64 0 rw GIC.SH.MAP14.VPE31.0 64 0 rw GIC.SH.MAP15.VPE31.0 64 0 rw GIC.SH.MAP16.VPE31.0 64 0 rw GIC.SH.MAP174.VPE31.0 64 0 rw GIC.SH.MAP174.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP	GIC_SH_MAP128_VPE31_0	64	0	rw	
GIC SH MAP131 VPE31.0 64 0 rw GIC.SH.MAP132.VPE31.0 64 0 rw GIC.SH.MAP133.VPE31.0 64 0 rw GIC.SH.MAP133.VPE31.0 64 0 rw GIC.SH.MAP135.VPE31.0 64 0 rw GIC.SH.MAP135.VPE31.0 64 0 rw GIC.SH.MAP135.VPE31.0 64 0 rw GIC.SH.MAP137.VPE31.0 64 0 rw GIC.SH.MAP137.VPE31.0 64 0 rw GIC.SH.MAP137.VPE31.0 64 0 rw GIC.SH.MAP138.VPE31.0 64 0 rw GIC.SH.MAP138.VPE31.0 64 0 rw GIC.SH.MAP140.VPE31.0 64 0 rw GIC.SH.MAP140.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH	GIC_SH_MAP129_VPE31_0	64	0	rw	
GIC.SH.MAP133.VPE31.0 64 0 rw GIC.SH.MAP133.VPE31.0 64 0 rw GIC.SH.MAP134.VPE31.0 64 0 rw GIC.SH.MAP134.VPE31.0 64 0 rw GIC.SH.MAP136.VPE31.0 64 0 rw GIC.SH.MAP136.VPE31.0 64 0 rw GIC.SH.MAP137.VPE31.0 64 0 rw GIC.SH.MAP138.VPE31.0 64 0 rw GIC.SH.MAP138.VPE31.0 64 0 rw GIC.SH.MAP138.VPE31.0 64 0 rw GIC.SH.MAP140.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP142.VPE31.0 64 0 rw GIC.SH.MAP143.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH	GIC_SH_MAP130_VPE31_0	64	0	rw	
GIC.SH.MAP133.VPE31.0 64 0 rw GIC.SH.MAP133.VPE31.0 64 0 rw GIC.SH.MAP134.VPE31.0 64 0 rw GIC.SH.MAP134.VPE31.0 64 0 rw GIC.SH.MAP136.VPE31.0 64 0 rw GIC.SH.MAP136.VPE31.0 64 0 rw GIC.SH.MAP137.VPE31.0 64 0 rw GIC.SH.MAP138.VPE31.0 64 0 rw GIC.SH.MAP138.VPE31.0 64 0 rw GIC.SH.MAP138.VPE31.0 64 0 rw GIC.SH.MAP140.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP142.VPE31.0 64 0 rw GIC.SH.MAP143.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH	GIC_SH_MAP131_VPE31_0	64	0	rw	
GIC.SH.MAP133.VPE31.0 64 0 rw GIC.SH.MAP134.VPE31.0 64 0 rw GIC.SH.MAP136.VPE31.0 64 0 rw GIC.SH.MAP136.VPE31.0 64 0 rw GIC.SH.MAP136.VPE31.0 64 0 rw GIC.SH.MAP137.VPE31.0 64 0 rw GIC.SH.MAP139.VPE31.0 64 0 rw GIC.SH.MAP139.VPE31.0 64 0 rw GIC.SH.MAP140.VPE31.0 64 0 rw GIC.SH.MAP140.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP142.VPE31.0 64 0 rw GIC.SH.MAP142.VPE31.0 64 0 rw GIC.SH.MAP143.VPE31.0 64 0 rw GIC.SH.MAP143.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP156.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH		64	0	rw	
GIC SH MAP134 VPF31 0		64	0	rw	
GIC SH MAP136 VPE31.0 64 0 rw GIC SH MAP137 VPE31.0 64 0 rw GIC SH MAP137 VPE31.0 64 0 rw GIC SH MAP137 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP142 VPE31.0 64 0 rw GIC SH MAP142 VPE31.0 64 0 rw GIC SH MAP143 VPE31.0 64 0 rw GIC SH MAP144 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP147 VPE31.0 64 0 rw GIC SH MAP149 VPE31.0 64 0 rw GIC SH MAP150 VPE31.0 64 0 rw GIC SH MAP160 VPE31.0 64 0 rw GIC SH MAP170 VPE31.0 64 0 rw		_	-		
GIC SIL MAP136 VPE31.0 64 0 rw GIC SIL MAP137 VPE31.0 64 0 rw GIC SIL MAP138 VPE31.0 64 0 rw GIC SIL MAP139 VPE31.0 64 0 rw GIC SIL MAP140 VPE31.0 64 0 rw GIC SIL MAP140 VPE31.0 64 0 rw GIC SIL MAP141 VPE31.0 64 0 rw GIC SIL MAP141 VPE31.0 64 0 rw GIC SIL MAP142 VPE31.0 64 0 rw GIC SIL MAP143 VPE31.0 64 0 rw GIC SIL MAP145 VPE31.0 64 0 rw GIC SIL MAP146 VPE31.0 64 0 rw GIC SIL MAP149 VPE31.0 64 0 rw GIC SIL MAP149 VPE31.0 64 0 rw GIC SIL MAP149 VPE31.0 64 0 rw GIC SIL MAP150 VPE31.0 64 0 rw GIC SIL MAP160 VPE31.0 64 0 rw GIC SIL MAP170 VPE31.0 64 0 rw		-			
GIC SH MAP138 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP139 VPE31.0 64 0 rw GIC SH MAP140 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP141 VPE31.0 64 0 rw GIC SH MAP143 VPE31.0 64 0 rw GIC SH MAP143 VPE31.0 64 0 rw GIC SH MAP144 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP146 VPE31.0 64 0 rw GIC SH MAP146 VPE31.0 64 0 rw GIC SH MAP147 VPE31.0 64 0 rw GIC SH MAP147 VPE31.0 64 0 rw GIC SH MAP147 VPE31.0 64 0 rw GIC SH MAP148 VPE31.0 64 0 rw GIC SH MAP149 VPE31.0 64 0 rw GIC SH MAP151 VPE31.0 64 0 rw GIC SH MAP152 VPE31.0 64 0 rw GIC SH MAP153 VPE31.0 64 0 rw GIC SH MAP154 VPE31.0 64 0 rw GIC SH MAP154 VPE31.0 64 0 rw GIC SH MAP155 VPE31.0 64 0 rw GIC SH MAP156 VPE31.0 64 0 rw GIC SH MAP157 VPE31.0 64 0 rw GIC SH MAP157 VPE31.0 64 0 rw GIC SH MAP157 VPE31.0 64 0 rw GIC SH MAP159 VPE31.0 64 0 rw GIC SH MAP159 VPE31.0 64 0 rw GIC SH MAP169 VPE31.0 64 0 rw GIC SH MAP160 VPE31.0 64 0 rw GIC SH MAP170 VPE31.0 64 0 rw		-	-		
GIC.SH.MAP139.VPE31.0 64 0 rw GIC.SH.MAP140.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP143.VPE31.0 64 0 rw GIC.SH.MAP143.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP147.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP154.VPE31.0 64 0 rw GIC.SH.MAP156.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH		_	-		
GIC SH.MAP130.VPE31.0 64 0 rw GIC SH.MAP141.VPE31.0 64 0 rw GIC SH.MAP141.VPE31.0 64 0 rw GIC SH.MAP142.VPE31.0 64 0 rw GIC SH.MAP143.VPE31.0 64 0 rw GIC SH.MAP144.VPE31.0 64 0 rw GIC SH.MAP144.VPE31.0 64 0 rw GIC SH.MAP145.VPE31.0 64 0 rw GIC SH.MAP145.VPE31.0 64 0 rw GIC SH.MAP147.VPE31.0 64 0 rw GIC SH.MAP147.VPE31.0 64 0 rw GIC SH.MAP147.VPE31.0 64 0 rw GIC SH.MAP149.VPE31.0 64 0 rw GIC SH.MAP149.VPE31.0 64 0 rw GIC SH.MAP150.VPE31.0 64 0 rw GIC SH.MAP160.VPE31.0 64 0 rw GIC SH.MAP170.VPE31.0 64 0 rw		-	-		
GIC SH.MAP141.VPE31.0 64 0 rw GIC SH.MAP141.VPE31.0 64 0 rw GIC SH.MAP142.VPE31.0 64 0 rw GIC SH.MAP143.VPE31.0 64 0 rw GIC SH.MAP143.VPE31.0 64 0 rw GIC SH.MAP145.VPE31.0 64 0 rw GIC SH.MAP147.VPE31.0 64 0 rw GIC SH.MAP148.VPE31.0 64 0 rw GIC SH.MAP148.VPE31.0 64 0 rw GIC SH.MAP150.VPE31.0 64 0 rw GIC SH.MAP160.VPE31.0 64 0 rw GIC SH.MAP170.VPE31.0 64 0 rw					
GIC.SH.MAP141.VPE31.0 64 0 rw GIC.SH.MAP142.VPE31.0 64 0 rw GIC.SH.MAP143.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw			_		
GIC.SH.MAP142.VPE31.0 64 0 rw GIC.SH.MAP143.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP147.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP171.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP174.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw		_	-	-	
GIC SH MAP143 VPE31.0 64 0 rw GIC SH MAP144 VPE31.0 64 0 rw GIC SH MAP145 VPE31.0 64 0 rw GIC SH MAP150 VPE31.0 64 0 rw GIC SH MAP150 VPE31.0 64 0 rw GIC SH MAP151 VPE31.0 64 0 rw GIC SH MAP151 VPE31.0 64 0 rw GIC SH MAP152 VPE31.0 64 0 rw GIC SH MAP153 VPE31.0 64 0 rw GIC SH MAP155 VPE31.0 64 0 rw GIC SH MAP159 VPE31.0 64 0 rw GIC SH MAP169 VPE31.0 64 0 rw GIC SH MAP174 VPE31.0 64 0 rw GIC SH MAP175 VPE31.0 64 0 rw GIC SH MAP177 VPE31.0 64 0 rw GIC SH MAP177 VPE31.0 64 0 rw GIC SH MAP179 VPE31.0 64 0 rw		-	-		
GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP147.VPE31.0 64 0 rw GIC.SH.MAP147.VPE31.0 64 0 rw GIC.SH.MAP148.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP154.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw		-	-		
GIC.SH.MAP145.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP144.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP154.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw			-		
GIC.SH.MAP146.VPE31.0 64 0 rw GIC.SH.MAP147.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP156.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP171.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw		_	-		
GIC.SH.MAP147.VPE31.0 64 0 rw GIC.SH.MAP148.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP154.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw	0:-0-0:	-	_		
GIC.SH.MAP148.VPE31.0 64 0 rw GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP177.VPE31.0 64 0 rw GIC.SH.MAP178.VPE31.0 64 0 rw GIC.SH.MAP178.VPE31.0 64 0 rw GIC.SH.MAP178.VPE31.0 64 0 rw		_		rw	
GIC.SH.MAP149.VPE31.0 64 0 rw GIC.SH.MAP150.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP162.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP177.VPE31.0 64 0 rw GIC.SH.MAP178.VPE31.0 64 0 rw GIC.SH.MAP178.VPE31.0 64 0 rw			-	-	
GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP171.VPE31.0 64 0 rw GIC.SH.MAP172.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP174.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw		_	-	rw	
GIC.SH.MAP151.VPE31.0 64 0 rw GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP156.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw		-	-	rw	
GIC.SH.MAP152.VPE31.0 64 0 rw GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP154.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP162.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP17.VPE31.0 64 0 rw		_		rw	
GIC.SH.MAP153.VPE31.0 64 0 rw GIC.SH.MAP154.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP177.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw	1	-	-	rw	
GIC.SH.MAP154.VPE31.0 64 0 rw GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP162.VPE31.0 64 0 rw GIC.SH.MAP162.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP171.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP174.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw		-		rw	
GIC.SH.MAP155.VPE31.0 64 0 rw GIC.SH.MAP156.VPE31.0 64 0 rw GIC.SH.MAP157.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP171.VPE31.0 64 0 rw GIC.SH.MAP171.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw		64	0	rw	
GIC_SH_MAP156_VPE31_0 64 0 rw GIC_SH_MAP157_VPE31_0 64 0 rw GIC_SH_MAP158_VPE31_0 64 0 rw GIC_SH_MAP159_VPE31_0 64 0 rw GIC_SH_MAP160_VPE31_0 64 0 rw GIC_SH_MAP160_VPE31_0 64 0 rw GIC_SH_MAP161_VPE31_0 64 0 rw GIC_SH_MAP161_VPE31_0 64 0 rw GIC_SH_MAP163_VPE31_0 64 0 rw GIC_SH_MAP163_VPE31_0 64 0 rw GIC_SH_MAP165_VPE31_0 64 0 rw GIC_SH_MAP166_VPE31_0 64 0 rw GIC_SH_MAP166_VPE31_0 64 0 rw GIC_SH_MAP166_VPE31_0 64 0 rw GIC_SH_MAP166_VPE31_0 64 0 rw GIC_SH_MAP168_VPE31_0 64 0 rw GIC_SH_MAP169_VPE31_0 64 0 rw GIC_SH_MAP169_VPE31_0 64 0 rw GIC_SH_MAP171_VPE31_0 64 0 rw GIC_SH_MAP171_VPE31_0 64 0 rw GIC_SH_MAP172_VPE31_0 64 0 rw GIC_SH_MAP172_VPE31_0 64 0 rw GIC_SH_MAP172_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP174_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw		-	0	rw	
GIC.SH_MAP157_VPE31_0 64 0 rw GIC.SH_MAP158_VPE31_0 64 0 rw GIC.SH_MAP159_VPE31_0 64 0 rw GIC.SH_MAP160_VPE31_0 64 0 rw GIC.SH_MAP161_VPE31_0 64 0 rw GIC.SH_MAP161_VPE31_0 64 0 rw GIC.SH_MAP161_VPE31_0 64 0 rw GIC.SH_MAP162_VPE31_0 64 0 rw GIC.SH_MAP164_VPE31_0 64 0 rw GIC.SH_MAP165_VPE31_0 64 0 rw GIC.SH_MAP165_VPE31_0 64 0 rw GIC.SH_MAP166_VPE31_0 64 0 rw GIC.SH_MAP166_VPE31_0 64 0 rw GIC.SH_MAP168_VPE31_0 64 0 rw GIC.SH_MAP169_VPE31_0 64 0 rw GIC.SH_MAP169_VPE31_0 64 0 rw GIC.SH_MAP169_VPE31_0 64 0 rw GIC.SH_MAP170_VPE31_0 64 0 rw GIC.SH_MAP171_VPE31_0 64 0 rw GIC.SH_MAP172_VPE31_0 64 0 rw GIC.SH_MAP172_VPE31_0 64 0 rw GIC.SH_MAP173_VPE31_0 64 0 rw GIC.SH_MAP173_VPE31_0 64 0 rw GIC.SH_MAP174_VPE31_0 64 0 rw GIC.SH_MAP174_VPE31_0 64 0 rw GIC.SH_MAP175_VPE31_0 64 0 rw GIC.SH_MAP175_VPE31_0 64 0 rw GIC.SH_MAP175_VPE31_0 64 0 rw GIC.SH_MAP175_VPE31_0 64 0 rw GIC.SH_MAP176_VPE31_0 64 0 rw	GIC_SH_MAP155_VPE31_0	64	0	rw	
GIC.SH.MAP158.VPE31.0 64 0 rw GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP162.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw	GIC_SH_MAP156_VPE31_0	64	0	rw	
GIC.SH.MAP159.VPE31.0 64 0 rw GIC.SH.MAP160.VPE31.0 64 0 rw GIC.SH.MAP161.VPE31.0 64 0 rw GIC.SH.MAP162.VPE31.0 64 0 rw GIC.SH.MAP162.VPE31.0 64 0 rw GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP171.VPE31.0 64 0 rw GIC.SH.MAP171.VPE31.0 64 0 rw GIC.SH.MAP172.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP174.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP176.VPE31.0 64 0 rw GIC.SH.MAP177.VPE31.0 64 0 rw GIC.SH.MAP178.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw	GIC_SH_MAP157_VPE31_0	64	0	rw	
GIC.SH_MAP160_VPE31_0 64 0 rw GIC.SH_MAP161_VPE31_0 64 0 rw GIC.SH_MAP162_VPE31_0 64 0 rw GIC.SH_MAP163_VPE31_0 64 0 rw GIC.SH_MAP163_VPE31_0 64 0 rw GIC.SH_MAP164_VPE31_0 64 0 rw GIC.SH_MAP165_VPE31_0 64 0 rw GIC.SH_MAP166_VPE31_0 64 0 rw GIC.SH_MAP167_VPE31_0 64 0 rw GIC.SH_MAP168_VPE31_0 64 0 rw GIC.SH_MAP168_VPE31_0 64 0 rw GIC.SH_MAP170_VPE31_0 64 0 rw GIC.SH_MAP170_VPE31_0 64 0 rw GIC.SH_MAP171_VPE31_0 64 0 rw GIC.SH_MAP171_VPE31_0 64 0 rw GIC.SH_MAP172_VPE31_0 64 0 rw GIC.SH_MAP173_VPE31_0 64 0 rw GIC.SH_MAP173_VPE31_0 64 0 rw GIC.SH_MAP173_VPE31_0 64 0 rw GIC.SH_MAP175_VPE31_0 64 0 rw	GIC_SH_MAP158_VPE31_0	64	0	rw	
GIC_SH_MAP161_VPE31_0 64 0 rw GIC_SH_MAP162_VPE31_0 64 0 rw GIC_SH_MAP163_VPE31_0 64 0 rw GIC_SH_MAP164_VPE31_0 64 0 rw GIC_SH_MAP165_VPE31_0 64 0 rw GIC_SH_MAP166_VPE31_0 64 0 rw GIC_SH_MAP166_VPE31_0 64 0 rw GIC_SH_MAP168_VPE31_0 64 0 rw GIC_SH_MAP168_VPE31_0 64 0 rw GIC_SH_MAP169_VPE31_0 64 0 rw GIC_SH_MAP170_VPE31_0 64 0 rw GIC_SH_MAP171_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP174_VPE31_0 64 0 rw GIC_SH_MAP174_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw	GIC_SH_MAP159_VPE31_0	64	0	rw	
GIC_SH_MAP162_VPE31_0 64 0 rw GIC_SH_MAP163_VPE31_0 64 0 rw GIC_SH_MAP164_VPE31_0 64 0 rw GIC_SH_MAP165_VPE31_0 64 0 rw GIC_SH_MAP166_VPE31_0 64 0 rw GIC_SH_MAP166_VPE31_0 64 0 rw GIC_SH_MAP168_VPE31_0 64 0 rw GIC_SH_MAP168_VPE31_0 64 0 rw GIC_SH_MAP169_VPE31_0 64 0 rw GIC_SH_MAP170_VPE31_0 64 0 rw GIC_SH_MAP171_VPE31_0 64 0 rw GIC_SH_MAP171_VPE31_0 64 0 rw GIC_SH_MAP172_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP174_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw	GIC_SH_MAP160_VPE31_0	64	0	rw	
GIC.SH.MAP163.VPE31.0 64 0 rw GIC.SH.MAP164.VPE31.0 64 0 rw GIC.SH.MAP165.VPE31.0 64 0 rw GIC.SH.MAP166.VPE31.0 64 0 rw GIC.SH.MAP167.VPE31.0 64 0 rw GIC.SH.MAP168.VPE31.0 64 0 rw GIC.SH.MAP169.VPE31.0 64 0 rw GIC.SH.MAP170.VPE31.0 64 0 rw GIC.SH.MAP171.VPE31.0 64 0 rw GIC.SH.MAP172.VPE31.0 64 0 rw GIC.SH.MAP173.VPE31.0 64 0 rw GIC.SH.MAP174.VPE31.0 64 0 rw GIC.SH.MAP174.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP175.VPE31.0 64 0 rw GIC.SH.MAP176.VPE31.0 64 0 rw GIC.SH.MAP177.VPE31.0 64 0 rw GIC.SH.MAP178.VPE31.0 64 0 rw GIC.SH.MAP178.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw GIC.SH.MAP179.VPE31.0 64 0 rw	GIC_SH_MAP161_VPE31_0	64	0	rw	
GIC_SH_MAP164_VPE31_0 64 0 rw  GIC_SH_MAP165_VPE31_0 64 0 rw  GIC_SH_MAP166_VPE31_0 64 0 rw  GIC_SH_MAP167_VPE31_0 64 0 rw  GIC_SH_MAP168_VPE31_0 64 0 rw  GIC_SH_MAP169_VPE31_0 64 0 rw  GIC_SH_MAP170_VPE31_0 64 0 rw  GIC_SH_MAP171_VPE31_0 64 0 rw  GIC_SH_MAP172_VPE31_0 64 0 rw  GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP174_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP180_VPE31_0 64 0 rw	GIC_SH_MAP162_VPE31_0	64	0	rw	
GIC_SH_MAP164_VPE31_0 64 0 rw  GIC_SH_MAP165_VPE31_0 64 0 rw  GIC_SH_MAP166_VPE31_0 64 0 rw  GIC_SH_MAP167_VPE31_0 64 0 rw  GIC_SH_MAP168_VPE31_0 64 0 rw  GIC_SH_MAP169_VPE31_0 64 0 rw  GIC_SH_MAP170_VPE31_0 64 0 rw  GIC_SH_MAP171_VPE31_0 64 0 rw  GIC_SH_MAP172_VPE31_0 64 0 rw  GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP174_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP180_VPE31_0 64 0 rw	GIC_SH_MAP163_VPE31_0	64	0		
GIC_SH_MAP165_VPE31_0 64 0 rw GIC_SH_MAP166_VPE31_0 64 0 rw GIC_SH_MAP168_VPE31_0 64 0 rw GIC_SH_MAP168_VPE31_0 64 0 rw GIC_SH_MAP169_VPE31_0 64 0 rw GIC_SH_MAP170_VPE31_0 64 0 rw GIC_SH_MAP171_VPE31_0 64 0 rw GIC_SH_MAP171_VPE31_0 64 0 rw GIC_SH_MAP172_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP174_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP176_VPE31_0 64 0 rw GIC_SH_MAP176_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw		-	_		
GIC_SH_MAP166_VPE31_0 64 0 rw GIC_SH_MAP167_VPE31_0 64 0 rw GIC_SH_MAP168_VPE31_0 64 0 rw GIC_SH_MAP169_VPE31_0 64 0 rw GIC_SH_MAP170_VPE31_0 64 0 rw GIC_SH_MAP171_VPE31_0 64 0 rw GIC_SH_MAP171_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP173_VPE31_0 64 0 rw GIC_SH_MAP174_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP175_VPE31_0 64 0 rw GIC_SH_MAP176_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP180_VPE31_0 64 0 rw		_			
GIC_SH_MAP167_VPE31_0 64 0 rw  GIC_SH_MAP168_VPE31_0 64 0 rw  GIC_SH_MAP169_VPE31_0 64 0 rw  GIC_SH_MAP170_VPE31_0 64 0 rw  GIC_SH_MAP171_VPE31_0 64 0 rw  GIC_SH_MAP172_VPE31_0 64 0 rw  GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP174_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP18_VPE31_0 64 0 rw		_	ŭ.		
GIC_SH_MAP168_VPE31_0 64 0 rw  GIC_SH_MAP169_VPE31_0 64 0 rw  GIC_SH_MAP170_VPE31_0 64 0 rw  GIC_SH_MAP171_VPE31_0 64 0 rw  GIC_SH_MAP172_VPE31_0 64 0 rw  GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP174_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw			-		
GIC_SH_MAP169_VPE31_0 64 0 rw  GIC_SH_MAP170_VPE31_0 64 0 rw  GIC_SH_MAP171_VPE31_0 64 0 rw  GIC_SH_MAP172_VPE31_0 64 0 rw  GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP174_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw			_		
GIC_SH_MAP170_VPE31_0 64 0 rw  GIC_SH_MAP171_VPE31_0 64 0 rw  GIC_SH_MAP172_VPE31_0 64 0 rw  GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP174_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw		-		-	
GIC_SH_MAP171_VPE31_0 64 0 rw  GIC_SH_MAP172_VPE31_0 64 0 rw  GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP174_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw			-		
GIC_SH_MAP172_VPE31_0 64 0 rw  GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP174_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw		_			
GIC_SH_MAP173_VPE31_0 64 0 rw  GIC_SH_MAP174_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw					
GIC_SH_MAP174_VPE31_0 64 0 rw  GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw		-	-		
GIC_SH_MAP175_VPE31_0 64 0 rw  GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP180_VPE31_0 64 0 rw			_		
GIC_SH_MAP176_VPE31_0 64 0 rw  GIC_SH_MAP177_VPE31_0 64 0 rw  GIC_SH_MAP178_VPE31_0 64 0 rw  GIC_SH_MAP179_VPE31_0 64 0 rw  GIC_SH_MAP180_VPE31_0 64 0 rw		_	-		
GIC_SH_MAP177_VPE31_0 64 0 rw GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP180_VPE31_0 64 0 rw				-	
GIC_SH_MAP178_VPE31_0 64 0 rw GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP180_VPE31_0 64 0 rw					
GIC_SH_MAP179_VPE31_0 64 0 rw GIC_SH_MAP180_VPE31_0 64 0 rw			-		
GIC_SH_MAP180_VPE31_0 64 0 rw					
		-			
GIC_SH_MAP181_VPE31_0   64   0   rw				rw	
	GIC_SH_MAP181_VPE31_0	64	0	rw	

GIC_SH_MAP182_VPE31_0	64	0	rw	
GIC_SH_MAP183_VPE31_0	64	0	rw	
GIC_SH_MAP184_VPE31_0	64	0	rw	
GIC_SH_MAP185_VPE31_0	64	0	rw	
GIC_SH_MAP186_VPE31_0	64	0	rw	
GIC_SH_MAP187_VPE31_0	64	0	rw	
GIC_SH_MAP188_VPE31_0	64	0	rw	
GIC_SH_MAP189_VPE31_0	64	0	rw	
GIC_SH_MAP190_VPE31_0	64	0	rw	
GIC_SH_MAP191_VPE31_0	64	0	rw	
GIC SH MAP192 VPE31 0	64	0	rw	
GIC_SH_MAP193_VPE31_0	64	0	rw	
GIC_SH_MAP194_VPE31_0	64	0	rw	
GIC_SH_MAP195_VPE31_0	64	0	rw	
GIC_SH_MAP196_VPE31_0	64	0	rw	
GIC_SH_MAP197_VPE31_0	64	0	rw	
GIC_SH_MAP198_VPE31_0	64	0	rw	
GIC_SH_MAP199_VPE31_0	64	0		
GIC_SH_MAP200_VPE31_0	64	0	rw	
GIC_SH_MAP200_VPE31_0	64	0	rw	
GIC SH MAP201 VPE31 0	64		rw	
0.1 0 20 112111		0	rw	
GIC_SH_MAP203_VPE31_0	64	0	rw	
GIC_SH_MAP204_VPE31_0	64	0	rw	
GIC_SH_MAP205_VPE31_0	64	0	rw	
GIC_SH_MAP206_VPE31_0	64	0	rw	
GIC_SH_MAP207_VPE31_0	64	0	rw	
GIC_SH_MAP208_VPE31_0	64	0	rw	
GIC_SH_MAP209_VPE31_0	64	0	rw	
GIC_SH_MAP210_VPE31_0	64	0	rw	
GIC_SH_MAP211_VPE31_0	64	0	rw	
GIC_SH_MAP212_VPE31_0	64	0	rw	
GIC_SH_MAP213_VPE31_0	64	0	rw	
GIC_SH_MAP214_VPE31_0	64	0	rw	
GIC_SH_MAP215_VPE31_0	64	0	rw	
GIC_SH_MAP216_VPE31_0	64	0	rw	
GIC_SH_MAP217_VPE31_0	64	0	rw	
GIC_SH_MAP218_VPE31_0	64	0	rw	
GIC_SH_MAP219_VPE31_0	64	0	rw	
GIC_SH_MAP220_VPE31_0	64	0	rw	
GIC_SH_MAP221_VPE31_0	64	0	rw	
GIC_SH_MAP222_VPE31_0	64	0	rw	
GIC_SH_MAP223_VPE31_0	64	0	rw	
GIC_SH_MAP224_VPE31_0	64	0	rw	
GIC_SH_MAP225_VPE31_0	64	0	rw	
GIC_SH_MAP226_VPE31_0	64	0	rw	
GIC_SH_MAP227_VPE31_0	64	0	rw	
GIC_SH_MAP228_VPE31_0	64	0	rw	
GIC_SH_MAP229_VPE31_0	64	0	rw	
GIC_SH_MAP230_VPE31_0	64	0	rw	
GIC_SH_MAP231_VPE31_0	64	0	rw	
GIC_SH_MAP232_VPE31_0	64	0	rw	
GIC_SH_MAP233_VPE31_0	64	0	rw	
GIC_SH_MAP234_VPE31_0	64	0	rw	
GIC_SH_MAP235_VPE31_0	64	0	rw	
GIC_SH_MAP236_VPE31_0	64	0	rw	
GIC_SH_MAP237_VPE31_0	64	0	rw	
515_511_1111 201_V1 L01_0	01		1 44	

GIC_SH_MAP238_VPE31_0	64	0	rw	
GIC_SH_MAP239_VPE31_0	64	0	rw	
GIC_SH_MAP240_VPE31_0	64	0	rw	
GIC_SH_MAP241_VPE31_0	64	0	rw	
GIC_SH_MAP242_VPE31_0	64	0	rw	
GIC_SH_MAP243_VPE31_0	64	0	rw	
GIC_SH_MAP244_VPE31_0	64	0	rw	
GIC_SH_MAP245_VPE31_0	64	0	rw	
GIC_SH_MAP246_VPE31_0	64	0	rw	
GIC_SH_MAP247_VPE31_0	64	0	rw	
GIC_SH_MAP248_VPE31_0	64	0	rw	
GIC_SH_MAP249_VPE31_0	64	0	rw	
GIC_SH_MAP250_VPE31_0	64	0	rw	
GIC_SH_MAP251_VPE31_0	64	0	rw	
GIC_SH_MAP252_VPE31_0	64	0	rw	
GIC_SH_MAP253_VPE31_0	64	0	rw	
GIC_SH_MAP254_VPE31_0	64	0	rw	
GIC_SH_MAP255_VPE31_0	64	0	rw	
GIC_SH_EJTAG_BRK	64	0	rw	
GIC_SH_TEAMID_LO	64	0	rw	
GIC_SH_TEAMID_HI	64	0	rw	
GIC_SH_TEAMID_EXT	64	0	rw	
GIC_SH_DBG_CONFIG	64	70	rw	
GIC_SH_DINT_PART	64	0		
GIC_SH_DEBUGM_STATUS	64	0	rw r-	
GIC_VPE_CTL	64	0		
GIC_VPE_PEND	64	0	rw	
GIC_VPE_MASK	64	7f	r-	
GIC_VPE_MASK GIC_VPE_RMASK	-	-	r-	
GIC_VPE_RMASK GIC_VPE_SMASK	64	0	-W	
GIC_VPE_SMASK GIC_VPE_WD_MAP	64	0	-W	
GIC_VPE_WD_MAP GIC_VPE_COMPARE_MAP	-	40000000	rw	
	64	80000000	rw	
GIC_VPE_TIMER_MAP	64	80000005	rw	
GIC_VPE_FDC_MAP	64	80000005	rw	
GIC_VPE_PERFCTR_MAP	64	80000005	rw	
GIC_VPE_SWInt0_MAP	64	80000000	rw	
GIC_VPE_SWInt1_MAP	64	80000000	rw	
GIC_VPE_OTHER_ADDRESS	64	0	rw	
GIC_VPE_IDENT	64	0	r-	
GIC_VPE_WD_CONFIG	64	0	rw	
GIC_VPE_WD_COUNT	64	0	r-	
GIC_VPE_WD_INITIAL	64	0	rw	
GIC_VPE_Compare	64	mmm mmm	rw	
GIC_VPE_EICSS00	64	0	rw	
GIC_VPE_EICSS01	64	0	rw	
GIC_VPE_EICSS02	64	0	rw	
GIC_VPE_EICSS03	64	0	rw	
GIC_VPE_EICSS04	64	0	rw	
GIC_VPE_EICSS05	64	0	rw	
GIC_VPE_EICSS06	64	0	rw	
GIC_VPE_EICSS07	64	0	rw	
GIC_VPE_EICSS08	64	0	rw	
GIC_VPE_EICSS09	64	0	rw	
GIC_VPE_EICSS10	64	0	rw	
GIC_VPE_EICSS11	64	0	rw	
GIC_VPE_EICSS12	64	0	rw	
•		*	•	

GIC_VPE_EICSS13	64	0	rw	
GIC_VPE_EICSS14	64	0	rw	
GIC_VPE_EICSS15	64	0	rw	
GIC_VPE_EICSS16	64	0	rw	
GIC_VPE_EICSS17	64	0	rw	
GIC_VPE_EICSS18	64	0	rw	
GIC_VPE_EICSS19	64	0	rw	
GIC_VPE_EICSS20	64	0	rw	
GIC_VPE_EICSS21	64	0	rw	
GIC_VPE_EICSS22	64	0	rw	
GIC_VPE_EICSS23	64	0	rw	
GIC_VPE_EICSS24	64	0	rw	
GIC_VPE_EICSS25	64	0	rw	
GIC_VPE_EICSS26	64	0	rw	
GIC-VPE-EICSS27	64	0	rw	
GIC_VPE_EICSS28	64	0		
GIC_VPE_EICSS29	64	0	rw	
GIC_VPE_EICSS29 GIC_VPE_EICSS30		-	rw	
	64	0	rw	
GIC_VPE_EICSS31	64	0	rw	
GIC_VPE_EICSS32	64	0	rw	
GIC_VPE_EICSS33	64	0	rw	
GIC_VPE_EICSS34	64	1	rw	
GIC_VPE_EICSS35	64	0	rw	
GIC_VPE_EICSS36	64	0	rw	
GIC_VPE_EICSS37	64	0	rw	
GIC_VPE_EICSS38	64	0	rw	
GIC_VPE_EICSS39	64	0	rw	
GIC_VPE_EICSS40	64	0	rw	
GIC_VPE_EICSS41	64	0	rw	
GIC_VPE_EICSS42	64	0	rw	
GIC_VPE_EICSS43	64	0	rw	
GIC_VPE_EICSS44	64	0	rw	
GIC_VPE_EICSS45	64	0	rw	
GIC_VPE_EICSS46	64	0	rw	
GIC_VPE_EICSS47	64	0	rw	
GIC_VPE_EICSS48	64	0	rw	
GIC_VPE_EICSS49	64	0	rw	
GIC_VPE_EICSS50	64	0	rw	
GIC_VPE_EICSS51	64	0	rw	
GIC_VPE_EICSS51	64	0	rw	
GIC_VFE_EICSS32 GIC_VPE_EICSS33	64	0	rw	
GIC_VPE_EICSS33	64	0		
GIC_VPE_EICSS54 GIC_VPE_EICSS55	64	0	rw	
GIC_VPE_EICSS55 GIC_VPE_EICSS56			rw	
	64	0	rw	
GIC_VPE_EICSS57	64	0	rw	
GIC_VPE_EICSS58	64	0	rw	
GIC_VPE_EICSS59	64	0	rw	
GIC_VPE_EICSS60	64	0	rw	
GIC_VPE_EICSS61	64	0	rw	
GIC_VPE_EICSS62	64	0	rw	
GIC_VPE_EICSS63	64	0	rw	
GIC_VL_COFFSET	64	0	rw	
GIC_VL_VIRTUAL_VP_NUM	64	0	rw	
GIC_VPE_CTL	64	0	rw	
GIC_VPE_PEND	64	0	r-	
GIC_VPE_MASK	64	7f	r-	
		I	1	1

GIC_VPE_RMASK	64	0	-w	
GIC_VPE_SMASK	64	0	-w	
GIC_VPE_WD_MAP	64	40000000	rw	
GIC_VPE_COMPARE_MAP	64	80000000	rw	
GIC_VPE_TIMER_MAP	64	80000005	rw	
GIC_VPE_FDC_MAP	64	80000005	rw	
GIC_VPE_PERFCTR_MAP	64	80000005	rw	
GIC_VPE_SWInt0_MAP	64	80000000	rw	
GIC_VPE_SWInt1_MAP	64	80000000	rw	
GIC_VPE_OTHER_ADDRESS	64	0	rw	
GIC_VPE_IDENT	64	0	r-	
GIC_VPE_WD_CONFIG	64	0	rw	
GIC_VPE_WD_COUNT	64	0	r-	
GIC_VPE_WD_INITIAL	64	0	rw	
GIC_VPE_Compare	64	fiffiff fiffiff	rw	
GIC_VPE_EICSS00	64	0	rw	
GIC_VPE_EICSS01	64	0	rw	
GIC_VPE_EICSS02	64	0	rw	
GIC-VPE-EICSS03	64	0	rw	
GIC-VPE-EICSS04	64	0	rw	
GIC_VPE_EICSS05	64	0	rw	
GIC_VPE_EICSS06	64	0	rw	
GIC-VPE-EICSS07	64	0	rw	
GIC_VPE_EICSS08	64	0	rw	
GIC_VPE_EICSS09	64	0	rw	
GIC_VPE_EICSS10	64	0	rw	
GIC-VPE-EICSS10	64	0	rw	
GIC_VPE_EICSS11	64	0	rw	
GIC-VPE-EICSS13	64	0	rw	
GIC-VPE-EICSS14	64	0	rw	
GIC_VPE_EICSS14	64	0	rw	
GIC_VPE_EICSS16	64	0	rw	
GIC_VPE_EICSS10	64	0		
GIC_VFE_EICSS17 GIC_VPE_EICSS18	64	0	rw	
GIC_VPE_EICSS18	64	0	rw	
GIC_VFE_EICSS19 GIC_VPE_EICSS20	64	0	rw	
GIC_VPE_EICSS21			rw	
GIC_VPE_EICSS21	64	0	rw	
	-	0	rw	
GIC_VPE_EICSS23	64	0	rw	
GIC_VPE_EICSS24	64	0	rw	
GIC_VPE_EICSS25	64	0	rw	
GIC_VPE_EICSS26	64	0	rw	
GIC_VPE_EICSS27	64	0	rw	
GIC_VPE_EICSS28	64	0	rw	
GIC_VPE_EICSS29	64	0	rw	
GIC_VPE_EICSS30	64	0	rw	
GIC_VPE_EICSS31	64	0	rw	
GIC_VPE_EICSS32	64	0	rw	
GIC_VPE_EICSS33	64	0	rw	
GIC_VPE_EICSS34	64	1	rw	
GIC_VPE_EICSS35	64	0	rw	
GIC_VPE_EICSS36	64	0	rw	
GIC_VPE_EICSS37	64	0	rw	
GIC_VPE_EICSS38	64	0	rw	
GIC_VPE_EICSS39	64	0	rw	
GIC_VPE_EICSS40	64	0	rw	

GIC_VPE_EICSS41	64	0	rw	
GIC_VPE_EICSS42	64	0	rw	
GIC_VPE_EICSS43	64	0	rw	
GIC_VPE_EICSS44	64	0	rw	
GIC_VPE_EICSS45	64	0	rw	
GIC_VPE_EICSS46	64	0	rw	
GIC_VPE_EICSS47	64	0	rw	
GIC_VPE_EICSS48	64	0	rw	
GIC_VPE_EICSS49	64	0	rw	
GIC_VPE_EICSS50	64	0	rw	
GIC_VPE_EICSS51	64	0	rw	
GIC_VPE_EICSS52	64	0	rw	
GIC_VPE_EICSS53	64	0	rw	
GIC_VPE_EICSS54	64	0	rw	
GIC_VPE_EICSS55	64	0	rw	
GIC_VPE_EICSS56	64	0	rw	
GIC_VPE_EICSS57	64	0	rw	
GIC_VPE_EICSS58	64	0	rw	
GIC_VPE_EICSS59	64	0	rw	
GIC_VPE_EICSS60	64	0	rw	
GIC_VPE_EICSS61	64	0	rw	
GIC_VPE_EICSS62	64	0	rw	
GIC_VPE_EICSS63	64	0	rw	
GIC_VL_COFFSET	64	0	rw	
GIC_VL_VIRTUAL_VP_NUM	64	0	rw	
GIC_CounterLoUser	64	0	r-	
GIC_CounterHiUser	64	0	r-	

Table 13.9: Registers at level 3, type:VP group:CMP\_GIC

# 13.3.10 Integration\_support

Registers at level:3, type:VP group:Integration\_support

Name	Bits	Initial-Hex	RW	Description
stop	32	0	rw	write with non-zero to stop processor

Table 13.10: Registers at level 3, type:VP group:Integration\_support