CSCI/CMPE 2333 Fall 2016 Homework #2 Due date: Tue. 9/27/2016

A hard copy must be turned in at the beginning of class. **Note that work must be shown for all computations or no credit will be received, even if the correct answer is given**. Please word process your work.

Chapter 3:

1. What general categories of functions are specified by computer instructions? [5 pts]
2. List and briefly define the possible states that define an instruction execution. [5 pts]
3. List and briefly define two approaches to dealing with multiple interrupts. [5 pts]
4. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.
    a. What is the maximum directly addressable memory capacity (in bytes)? [5 pts]
    b. Discuss the impact on the system speed if the microprocessor bus has
        i. A 32-bit local address bus and a 16-bit local data bus, or [5 pts]
        ii. A 16-bit local address bus and a 16-bit local data bus. [5 pts]
    c. How many bits are needed for the program counter and the instruction register? [5 pts]

Chapter 4:

5. What is the general relationship among access time, memory cost, and capacity? [5 pts]
6. For a direct-mapped cache, a main memory address is viewed as consisting of three fields. List and define the three fields. [10 pts]
7. For an associative cache, a main memory address is viewed as consisting of two fields. List and define the two fields. [10 pts]
8. For a set-associative cache, a main memory address is viewed as consisting of three fields. List and define the three fields. [10 pts]
9. What is the distinction between spatial locality and temporal locality? [5 pts]
10. A set-associative cache consists of 128 lines, or slots, divided into four-line sets, with each line holding 128 bytes. If main memory contains 512 M bytes, show the format of the main memory address. [10 pts]
11. A two-way set-associative cache has lines of 32 bytes and a total size of 16 Kbytes. The 256-Mbyte main memory is byte addressable. Show the format of main memory addresses. [10 pts]
12. Show the format of main memory addresses for a system with the same parameters as in question 11 EXCEPT that the cache is direct-mapped rather than two-way set-associative. [5 pts]