Curriculum Vitae (CV)

Gudmundur Bogason
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PROFILE

Personality
Innovative, creative and analytical person that enjoys to acquire new knowledge and experience and to work with challenging tasks. Approaches problem solving in a systematic and organized way. Has the ability to work at a very detailed level while still maintaining overview and orientation. Is focused and responsible and prefers to deliver high quality work in a professional way.

Enjoys a flexible working environment based on freedom and personal responsibility and to have influence on the decision process. Good at working independently and also as a part of a competent and stimulating team.

Experience
More than 30 years of professional experience from working with innovative and cutting edge companies such as ams-OSRAM, AceZone, NXP / Retune-DSP, EPOS / Sennheiser Communications, Harman/Becker Automotive Systems, Knowles and Oticon in the development of Software, Firmware, DSP algorithms and mixed-signal ASIC's for ultra low-power, high-performance embedded real-time digital audio signal processing systems.

Has worked extensively with all phases of the project development process from planning, specification, architecture, design, implementation, testing and documentation.

Customer contact and interaction with world leading manufacturers of mobile communication chip-sets and producers of mobile devices regarding discussion of requirements and presentation of ideas and solutions. Business knowledge from working within the field of Microelectronics, Consumer Electronics and Hearing Instruments.

Competences
Possesses extensive technical skills and a thorough theoretical background in the following areas:

- Software development of tools for simulation, verification and automation of embedded systems and DSP algorithms.
- Firmware and Embedded Software development for Microcontrollers and DSP’s.
- DSP algorithm development for real-time digital audio signal processing.
- Development of ANC solutions for audio systems.
- System architecture and design of mixed-signal ASIC's for high-performance audio signal processing.
- Mapping of DSP algorithm to optimized hardware architectures on ASIC’s.
- Digital RTL design for ASIC and FPGA.
- Analog CMOS ASIC design of mixed-signal, ultra low-power audio circuits and data converters.

Education
PhD in Discrete Time Analog Signal Processing and ASIC Design and MSc in Electrical Engineering and ASIC Design.

EXPERIENCE: embed-dsp (Self-Employed, 11 years)

Contractor (ams-OSRAM)
May 2023 – May 2024 (1 year)

Technical Project Lead, System Architecture and Design, System Modeling, System Simulation, Digital Signal Processing and Algorithms, Mixed Signal ASIC Design, Performance Assessments, Specifications.

Consultant (AceZone)
Oct 2022 – Mar 2023 (6 months)

Handover of ANC activities and Firmware / Software activities to other resources in AceZone.

Contractor (Spottune / AceZone)
Jun 2019 – Jul 2019 (2 months)

Bring up of firmware on a custom hardware platform and software for communication with a PC. Initial implementation of acoustic measurements techniques for a digital feed-back ANC algorithm running on custom hardware platform.

Contractor (Retune-DSP)
May 2017 – Nov 2017 (7 months)

Implementation of multi-channel Acoustic Echo Canceler (AEC) algorithm in Assembler on CSR8670 / CSR8675 Kalimba and integration with SBC audio codec and Voice trigger detector system.

Contractor (EPOS / Sennheiser Communications)
Feb 2016 – Aug 2016 (7 months)

Porting of an Open-source high performance low latency audio codec from floating-point to 24-bit fixed-point. Optimization of instructions count and memory usage and of performance due to fixed-point quantization effects.

Implementation in assembler and C code on the CSR 8670 Bluetooth SoC.

Freelancer (Retune-DSP)
Aug 2015 – Sep 2015 (2 months)

Feasibility study of how to implement DSP algorithms on the Qualcomm Snapdragon 810 processor, using CAPIV2, that can be tuned in real-time from a Java App running on the application processor.

Development performed using the Intrinsyc DragonBoard Development Kit (APQ8094).

Contractor (GreenGo Energy Group)
Jan 2015 – Sep 2017 (2 years, 9 months)

Development of embedded software and server side software for enabling intelligent system monitoring and analysis of the next generation of Photovoltaic / Solar-Power – systems …

Bare metal implementation in C on a dsPIC33 Microcontroller of Modbus RTU communication, FLASH memory data buffer and system scheduling.

Design and implementation of a Data-Manager (Data-Logger and Modbus TCP Gateway) on an industrial Embedded Linux system using C++ and Pthreads. Modbus RTU communication and TCP network communication using built in Mobile radio and LAN.

Design and implementation of server side software in Java and Python for control of Data-Managers and for collecting data from Data-Managers. TCP network communication in Java and feeding of data to SQL Database systems.

Contractor (Harman/Becker Automotive Systems)
Oct 2013 – Apr 2014 (7 months)

Porting and testing of a multi-channel (4 mic x 5 spkr) Engine Order Cancellation (EOC) ANC system from floating-point on Analog-Devices TigerSHARC DSP to 24-bit fixed-point on Tensilica HiFi2 DSP.

Implementation on the NXP Dirana3 Multi-Tuner Car Radio SoC.

PhD Project Examiner (DTU)
Sep 2013

Examiner on a DTU PhD project:

Peter Pracný, *“Design considerations for a digital audio Class D output stage with emphasis on hearing aid application”*, PhD thesis, June 2013, DTU Orbit

Owner, Principal Engineer (embed-dsp)
May 2013 – May 2024 (11 years)

Started own company working as an independent professional.

Design and implementation of embedded real-time digital audio signal processing systems targeting DSP, FPGA and ASIC technology. Freelancing / Contracting / Consulting within the areas of Digital Signal Processing, Firmware, Embedded Software and Digital Design.

EXPERIENCE: AceZone

Co-Owner, Senior Audio DSP and Firmware / Embedded Software Engineer
Aug 2019 – Sep 2022 (3 years, 2 months)

Worked on development of world-class high performance Gaming Headsets for professional and commercial markets. Design and implementation of digital hybrid ANC algorithms and optimization of ANC filters. Development and implementation of techniques and tools for measuring and characterizing headset acoustics and frequency responses. Design and implementation of firmware / embedded software for gaming headset platforms and audio DSP algorithms on DSP's and Microcontrollers. Design and implementation of protocols for communication using USB and Bluetooth for controlling headsets from production test equipment and mobile App's.

– Responsible for digital hybrid ANC design and implementation.

– Responsible for Firmware / Embedded Software design and implementation.

EXPERIENCE: Knowles Electronics Denmark – ASIC Design Center (3 years and 6 months)

Principal Engineer, ASIC Design & System Integration
Dec 2010 – Apr 2013 (2 years and 5 months)

System architect on the world's first digital MEMS microphone optimized for multiple performance modes and ultrasonic processing:

Knowles Enables Touch-less Gesture Recognition for Smartphones and Tablets
Knowles Engineers Dramatically Reduce Power Consumption in Microphones

Worked on the development of a high-performance digital MEMS microphone ASIC. Definition of system concepts, architecture and design. Customer contact and interaction and writing of ASIC requirement and design specifications. Design of high-performance A/D data conversion architecture. DSP algorithm design and simulation and mapping of DSP algorithms to optimized hardware blocks. Digital microarchitecture design and RTL implementation. RTL and Gate-Level verification. Development of mixed-signal simulation setup for full ASIC verification.

– Responsible for system architecture and design of a high-performance digital MEMS microphone ASIC

Acting Manager, ASIC Design & Engineering
Feb 2010 – Nov 2010 (9 months)

Took over full responsibility of ASIC Design Center for a predefined period of time. Performed daily management including people management, management of expenses, project planning and project management, coordination with and reporting to head office. Initial ASIC roadmap and technology roadmap. Identification and selection of ASIC foundry. Specification and implementation of design flow. Buildup of lab facilities. Worked on the development of a low-cost analog MEMS microphone ASIC. Definition of system architecture and writing of specifications. Analog ASIC design, tapeout and interaction with foundry services.

– Responsible for ASIC Design Center

– Responsible for system architecture and design of a low-cost analog MEMS microphone ASIC

Senior ASIC and DSP Development Engineer
Nov 2009 – Feb 2010 (4 months)

Worked on starting an ASIC Design Center in Denmark. Identification of ASIC designers for hire-ring and performed job interviews. Specification of Linux servers and Windows clients that are used for ASIC and DSP development including hardware requirements and applications. Installation and administration of EDA tools and related applications on Linux servers. Installation and management of PDK's.

– Responsible for specification of hardware and applications for Linux servers and Windows clients.

– Responsible for installation and administration of PDK's, EDA tools and related applications.

EXPERIENCE: Oticon – DSP Development Engineer (7 years and 9 months)

Jun 2006 – Sep 2009 (3 years and 5 months) : DSP Design Flow and Embedded Software
Worked on starting a new DSP group with focus on implementation of algorithms in hardware and embedded software and functioned as a group coordinator in the beginning. Worked on developing a DSP design flow on Linux for use in implementation of complex algorithms and systems as embedded software for multiprocessor SoC ASIC designs. Implemented a SCons based build flow for building tools and embedded DSP software. Implemented a Java tool for automation and code generation of embedded software from XML meta descriptions. Implemented a SystemC based Virtual System Prototype (VSP) for functional system level simulations of embedded DSP software in floating and fixed – point and for cycle accurate and bit-true simulation of embedded DSP software on a single processor including models of peripheral units and memories and with embedding of Instruction Set Simulator (ISS) for the DSP processor. Performed initial porting of a sub-band directional microphone system from a floating point Simulink model to fixed point C++ firmware for guiding the design of a custom SIMD DSP processor.

– Responsible for DSP group planning and coordination.

– Responsible for DSP design flow implementation.

Sep 2005 – Jun 2006 (10 months) : DSP Design Flow
Worked on developing a DSP design flow for use in concept development of complex DSP algorithms and systems on

Windows and Linux. Specified and implemented the work-flow process for the design flow including component based design and version control strategy. The design flow was implemented in the corporate Quality system. Performed an exhaustive investigation of MathWorks Simulink and Real-Time Workshop for DSP concept development and rapid prototyping. Implemented a Java tool for supporting and automating the management of component based designs.

– Responsible for DSP design flow implementation.

Jun 2004 – Sep 2005 (1 year and 4 months) : DSP Design
Worked on planning and redesigning a Digital Feedback Cancellation (DFC) system and on implementing a frequency domain Transform Processor for use in a hearing instrument platform. Worked on DSP algorithm design and implementation of Matlab and C++ / SystemC DSP simulation models in floating and fixed – point for use in verification against RTL hardware implementation.

– Responsible for system architecture and design.

– Responsible for DSP algorithm design and verification.

Jan 2002 – Oct 2004 (2 years and 10 months) : DSP Design Flow
Worked on developing a DSP design flow for use in all phases in the development of complex DSP algorithms and systems on Windows and Linux. Developed and described the work-flow process for the design flow. Implemented a dataflow driven simulation system in C++, SystemC, Java and Matlab. The simulation system supported real-time simulation and performance evaluation in floating and fixed – point and generation of test-vectors for verification against RTL implementation. Real-time visualization and control was implemented using a multi-threaded Java Swing GUI.

– Responsible for DSP design flow implementation.

Apr 2003 – Jun 2004 (1 year and 3 months) : DSP Design and Digital ASIC Design
Worked on developing an audio codec ASIC in CMOS technology together with a well known IC vendor. The codec is used with a Bluetooth baseband controller in Headset applications. The chipset has been used in several commercial designs from known Headset producing companies. Designed a digital fractional clock system to support vast number of standard audio sampling frequencies without using a PLL. Redesigned decimation and interpolation systems and a sigma-delta D/A converter to work with the clock system. Implemented Matlab and C++ / SystemC DSP simulation models in floating and fixed – point for use in verification against RTL hardware implementation.

– Responsible for system architecture and design.

– Responsible for DSP algorithm design and verification

– Responsible for RTL implementation.

Apr 2003 – Jun 2003 (3 months) : DSP Design and Digital ASIC Design
Worked on developing a digital Squelch for use in the base-band part of a FM receiver IC. Worked on DSP algorithm design and Verilog RTL implementation. Implemented Matlab and C++ / SystemC DSP simulation models in floating and fixed – point for use in verification against RTL hardware implementation.

– Responsible for DSP algorithm design and verification

– Responsible for RTL implementation.

Aug 2002 – Apr 2003 (9 months) : DSP Design
Worked on developing DSP algorithms for a new hearing instrument platform. Implemented Matlab and C++ / SystemC DSP simulation models in floating and fixed – point for Filter-Bank, Compressor and AGC systems based on Verilog RTL implementation. Implemented real-time Java Swing GUI's for visualizing operation and performance of a directional microphone and automatics system.

– Responsible for DSP team planning and coordination.

– Responsible for DSP algorithm development and verification.

Jul 2001 – Jan 2002 (7 months) : DSP Design
Worked on developing DSP algorithm concepts for implementing automatic fading between omni and directional modes for a directional microphone system in a hearing instrument.

– Responsible for DSP algorithm design

EXPERIENCE: Oticon – ASIC Development Engineer (6 years and 11 months)

Jan 2001 – Aug 2001 : Digital Communication
Worked on initial development of a short range Near Field Communication (NFC) system based on magnetic transmission. The system is intended for enabling communication between hearing instruments and external units. Worked on specifying communication protocol and radio architecture and low voltage and current circuit design for implementation in CMOS technology. Implemented Matlab and C++ DSP simulation models in floating – point for architecture exploration and performance evaluation.

– Responsible for system architecture and design.

Apr 2001 – Jul 2001 (4 months) : DSP Simulation using Hard Real-Time Linux
Worked on investigating the possibilities of using RTLinux for implementing a hard real-time low latency DSP simulation system for system level verification of DSP algorithms. Collected requirements for the system and implemented several RTLinux kernel modules and a parallel port driver.

Aug 1999 – Jan 2001 (1 year and 6 months) : Analog RF ASIC Design and DSP Design
Worked on specifying the design and implementation of a low voltage and low current FM receiver in CMOS technology. The receiver is used as an external add-on for hearing instruments. Worked on system design of a digital frequency synthesis system and on electrical design of a phase/frequency detector, charge pump and SCL prescaler. Worked on DSP algorithm design and Verilog RTL implementation of digital FM demodulation and digital decimation and filtering. Looked at different implementations for IF filtering.

– Responsible for system architecture and design.

– Responsible for electrical design.

– Responsible for DSP algorithm design, verification and RTL implementation.

Apr 1999 – Aug 1999 (5 months) : Analog ASIC Design
Worked on developing initial system specification for a new hearing instrument platform. Worked on developing DSP concept for a high-order single-bit Switched-Capacitor Sigma-Delta A/D converter and a high-order multi-bit/PWM digital Sigma-Delta D/A converter with low jitter sensitivity. Worked on developing concept for an oscillator for generating the system clock.

– Responsible for system design.

– Responsible for DSP algorithm design.

Apr 1996 – Apr 1999 (3 years and 1 month) : Analog ASIC Design
Worked on developing low voltage and low current analog circuits in CMOS technology for a new hearing instrument platform: biasing circuit, voltage reference circuit, capacitive microphone amplifier, high-order single-bit switched-capacitor sigma-delta A/D converter, low jitter RC oscillator. Worked on developing ISO9000 work procedures and checklists for analog IC development.

– Responsible for electrical design and physical layout.

– Responsible for analog test specifications for wafer testing.

– Responsible for PCB design and analog test implementation in LabView for verification and characterization of packaged IC's.

Mar 1995 – Apr 1996 (1 year and 2 months) : Analog ASIC Design
Worked on developing and redesigning low voltage and low current analog circuits in BiCMOS technology for the world's first digital hearing instrument: voltage monitoring and reset circuit, high-order single-bit switched-capacitor sigma-delta A/D converter, high-order single-bit digital sigma-delta D/A converter.

– Responsible for electrical design and physical layout.

– Responsible for analog test specifications for wafer testing.

– Responsible for PCB design and analog test implementation in LabView for verification and characterization of packaged IC's.

COURSES

Jun 2006 – Jun 2006 : ECSI User experience with SystemC TLM
Workshop where users of TLM presented how they use SystemC and the TLM standard, and what they recommended as best practice. The workshop focused on both timed and un-timed modeling abstraction levels.

May 2002 – May 2002 : SuperUsers SU-0204 C++ Programming Advanced
Advanced C++ concepts and constructs and how to apply these in large programming projects.

May 2002 – May 2002 : SuperUsers SU-0203 C++ Programming Fundamentals
Basic object oriented programming in C++ with focus on how OOA/OOD is used in the implementation.

Mar 1995 – Mar 1995 : Cadence Analog Artist
Training course describing how to design integrated circuits using Composer for schematic capture and Analog Artist for simulation.

EDUCATION

Sep 1992 – Apr 1996 : PhD in Discrete Time Analog Signal Processing and ASIC Design
Technical University of Denmark (DTU), Department of Information Technology

Supervisor: Erik Bruun, Professor
Examiner: Tor Sverre Lande, Professor

Wrote a thesis on the subject of "*Design, Optimization and Applications of CMOS Switched Current circuits*".

Work experience during Ph.D study:

- Was hired by DANAVOX for a period of 2 months during which I was working at DELTA
- Involved in project work with MICROTRONIC

Sep 1987 – Aug 1992 : MSc in Electrical Engineering and ASIC Design
Technical University of Denmark (DTU), Electronics Institute

Supervisor: Erik Bruun, Professor

Implemented a working CMOS chip containing a 4th Order Switched Current low-pass and high-pass filter as part of the graduate project.

Aug 1984 – Jun 1987 : Math and Physics High School Graduate
Stenhus High School

LANGUAGES

- Danish: Speaks, reads and writes fluently.
- English: Speaks, reads and writes fluently.
- Swedish: Reads and understands.
- Norwegian: Reads and understands.
- Icelandic: Speaks, reads and understands to some degree (mother tongue).

LEISURE INTERESTS

- Travel, exercise.
- Good wine, beer and food.

PATENTS

[1] Patent: US20040096076, US6975739 (US7058191), *"Hearing aid with a radio frequency receiver"*, Gudmundur Bogason, Bjarne Klemmensen, Oct 4, 2001

[2] Patent: US20040161120, US7340068, *"Device and method for detecting wind noise"*, Gudmundur Bogason, Thomas Bo Elmedyb, Ulrik Kjems, Kim Spetzler Petersen, Feb 19, 2003

[3] Patent: US20130058495, *"System and A Method For Streaming PDM Data From Or To At Least One Audio Component"*, Claus Erdmann Furst, Gudmundur Bogason, Michael Deruginsky, Sep 1, 2011

[4] Patent: US20140177874, *"Digital Microphone with Frequency Booster"*, Gudmundur Bogason, Henrik Thomsen, Dec 18, 2013

PUBLICATIONS

[1] G. Bogason, *"Switched Current Micropower 4th Order Lowpass/Highpass Filter"*, ESSCIRC`93 Proceedings, 19th European Solid-State Circuits Conference, pp. 170, September 1993
ieeexplore.ieee.org

[2] G. Bogason, *"Generation of a Neuron transfer Function and its Derivatives"*, Electronics Letters, Volume 29 Issue 21, pp. 1867-1869, October 1993
ieeexplore.ieee.org :: digital-library.theiet.org

[3] T. Kaulberg and G. Bogason, *"An Angle Detector based on Magnetic Sensing"*, ISCAS`94 Proceedings, Volume 5, pp. 329-332, May/June 1994
ieeexplore.ieee.org

[4] T. Kaulberg and G. Bogason, *"A Digital Volume Control for Hearing Aid Applications"*, NORCHIP Proceedings, pp. 144-151, November 1994

[5] G. Bogason, *"Switched Current 3rd order Sigma-Delta A/D Converter for Digital Audio"*, Submittet to ISCAS`95, April 1995

[6] T. Kaulberg and G. Bogason, *"Position detection with the use of MAGFETs"*, Instrumentation and Measurement Technology Conference, pp. 158-???, April 1995
ieeexplore.ieee.org

[7] Ivan H. H. Jørgensen, G. Bogason, and Erik Bruun, *"A Neural Micro-Flow Estimator"*, Instrumentation and Measurement Technology Conference, pp. 385-389, April 1995
ieeexplore.ieee.org

[8] T. Kaulberg and G. Bogason, *"A silicon potentiometer for hearing aids"*, Analog Integrated Circuits and Signal Processing, Volume 9 , Issue 1, pp. 31-38, January 1996
link.springer.com :: dl.acm.org

[9] Ivan H. H. Jørgensen and G. Bogason, *"Design of a 3rd Order Micro Power Switched Current ΣΔ-Modulator"*, ICECS '96, Volume 2, pp. 948-951, October 1996
ieeexplore.ieee.org

[10] Ivan H. H. Jørgensen and G. Bogason, *"A 3rd Order Low Power SI ΣΔ- A/D Converter for Voice Band Applications"*, ISCAS '97, Volume 1, pp. 69-72, June 1997
ieeexplore.ieee.org

[11] Ivan H. H. Jørgensen and G. Bogason, *"Optimization and Design of a Low Power Switched Current A/D-ΣΔ-Modulator for Voice Band Applications"*, Analog Integrated Circuits and Signal Processing, Volume 17 , Issue 3, pp. 221-247, November 1998
link.springer.com :: dl.acm.org

[12] Ivan H. H. Jørgensen and G. Bogason, *"Noise Analysis of Switched-Current Circuits"*, Analog Integrated Circuits and Signal Processing, Volume 18 , Issue 1, pp. 69-77, January 1999
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