Bachelor in Electronic Engineering

Hardware Engineering:

Hardware Engineering Lab

Exercise 6

09.06.2022

Prof. Dr.-Ing. Ali Hayek

University of Applied Sciences Hamm-Lippstadt (HSHL)

Tel.: + 49 (2381) 8789 - 924

Room: L4.2-E02-370

E-mail: ali.hayek@hshl.de

Exercise 1 – FPGA Design Intro

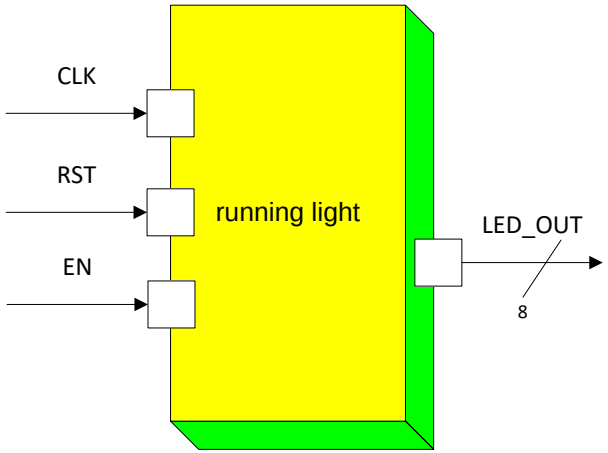
HOCHSCHULE
HAMM-LIPPSTADT

- Install the Xilinx ISE Design Suite and work through the Xilinx ISE tutorial (see lecture slides).

- Load the test programm on your FPGA board.

Exercise 2 – Running light on FPGA

- Design a an 8-bit running light in VHDL and implement it on your FPGA board. The running light model should have the following inputs and outputs:

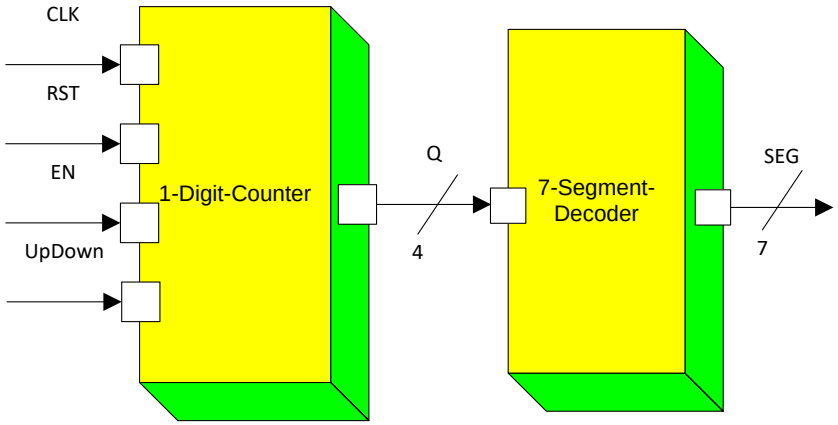


Note: use the clock divider module from Lab 4 Exercise 2 to be able to see a noticable running light

Use the LEDs and the push buttons on the FPGA board to realize your module

Exercise 3 – Counter on FPGA

- Design a 1-digit counter on your FPGA board. Use the 7-segment display to display the outputs and push buttons to realize your inputs.



Note: Use the clock divider module from Lab 4 Exercise 2 to be able to see a noticable running light.

Use the counter module and the 7-segment display decoder from Lab 4 Exercise 5

Thank you for your attention.

Prof. Dr.-Ing. Ali Hayek

University of Applied Sciences Hamm-Lippstadt (HSHL)

Tel.: **+ 49 (2381) 8789 - 924**

Room: **L4.2-E02-370**

E-mail: **ali.hayek@hshl.de**