Bachelor in Electronic Engineering

Hardware Engineering:

Hardware Engineering Lab

Exercise 2

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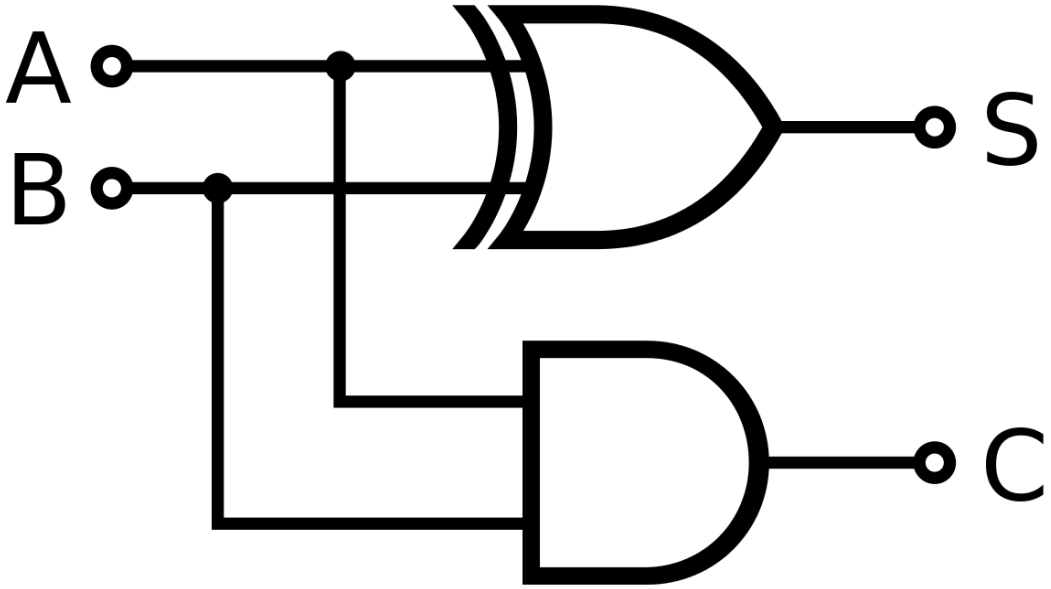
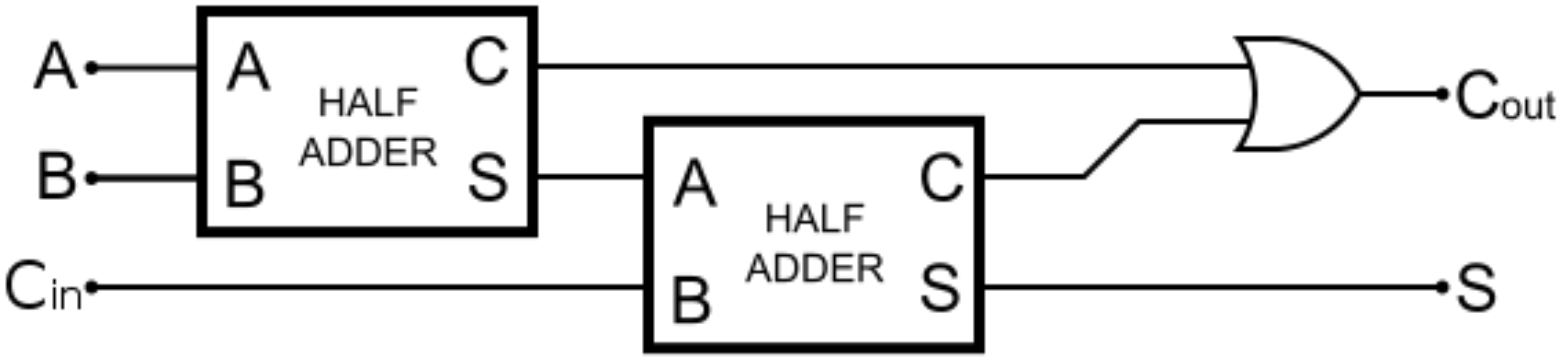
Exercise 1

- Design a VHDL model to implement the behavior of a 1 bit half adder (HA). Verify your model using a suitable testbench.



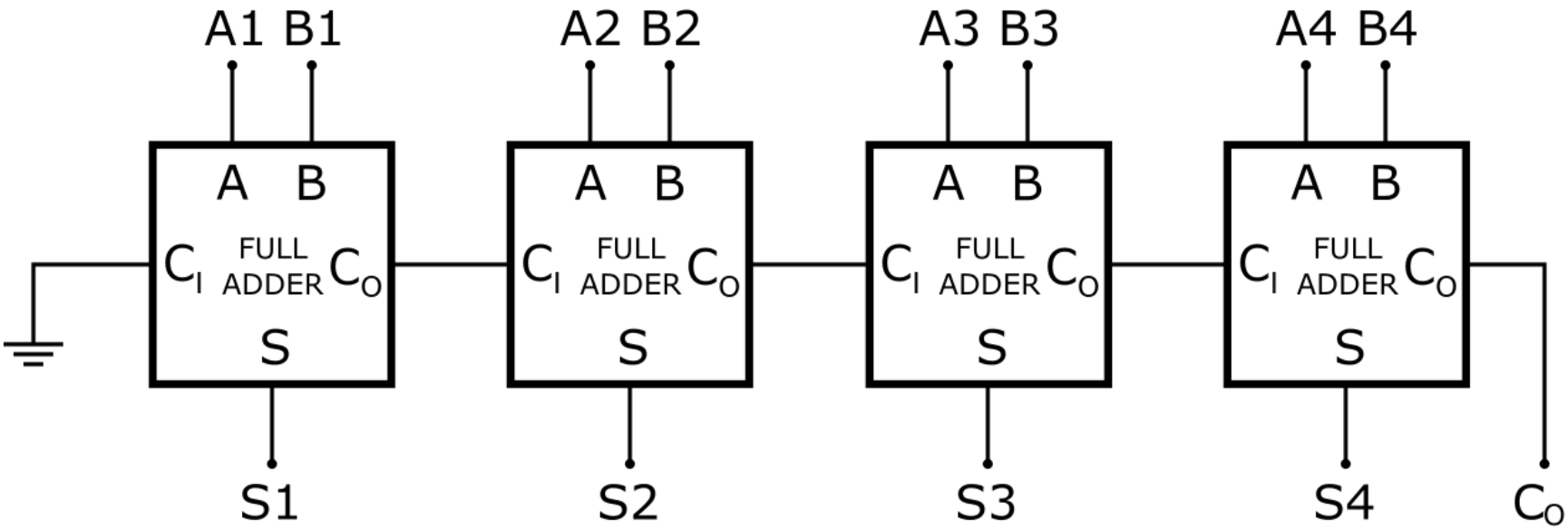
Exercise 2

- Design a VHDL model to implement the structure of a 1 bit full adder (FA) using the model of the designed half adder as a component. Verify your model using a suitable testbench.



Exercise 3

- Design a VHDL model to implement the structure of a 4 bit Ripple Cary Adder using the model of the designed full adder as a component. Verify your model using a suitable testbench.
- How you can enhance your model to implement different bit width Adder?



Exercise 4

- Design a VHDL model to implement the structure of a 4 bit Adder/Subtractor using the model of the designed 4 bit Ripple Carry Adder as a component. Verify your model using a suitable testbench.

Exercise 5

- Design a PCB Schematic of a 1 bit full adder circuit using Autodesk Eagle.

HOCHSCHULE
HAMM-LIPPSTADT

Thank you for your attention.

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