Bachelor in Electronic Engineering

Hardware Engineering:

Hardware Engineering Lab

Exercise 4

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Exercise 1 – D-Flip-Flop in VHDL

- Write a VHDL model that implements a D-Flip-Flop.
- Write a VHDL testbench for simulating the D-Flip-Flop.
- Use the D-Flip-flop model to design an 8 bit register in VHDL (structure description).
- Use the D-Flip-flop model to design an 8 bit shift register in VHDL (structure description).

Exercise 2 – Clock Divider in VHDL

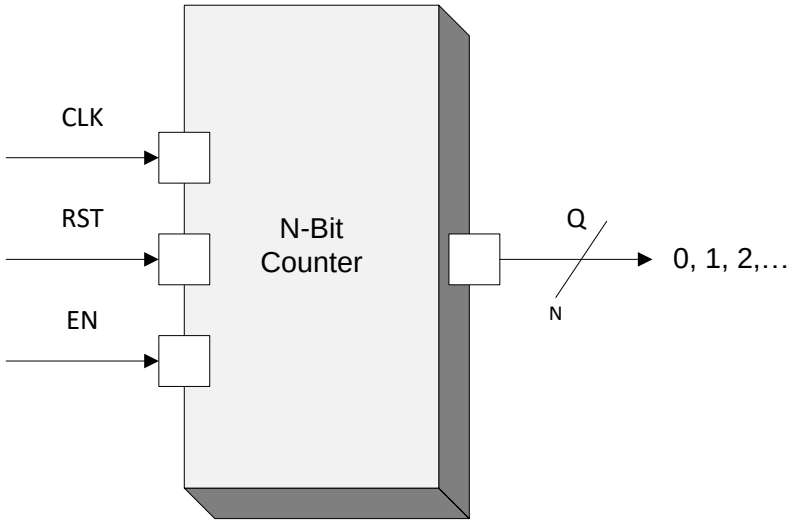
- In digital circuits different clocks are often required by different components. Usually only one frequency generated by an internal oscillator is available for this purpose. In order to have different internal synchronized clocks, all clocks are derived by dividing the main clock generated by the oscillator.
  - Design a VHDL model that generates the clock signal CLK_N from a main clock CLK, the frequency of which is lower by a factor of 2^N than the frequency of the basic clock.
  - Write a suitable for a testbench that verifies the behavior of the circuit.

Exercise 3 – Multiplexer in VHDL

- Write a VHDL program that models the behavior of a 4:1 multiplexer. For this, a model with concurrent statements and a model with sequential statements should be written.
- Write a suitable testbench to simulate the behavior of the circuit.

Exercise 4 – Counter in VHDL

- Design a VHDL model to implement the behavior of an N bit counter. The counter has an asynchronous input reset (RST) and synchronous input enable (EN). The counter start counting when EN = “1” on the rising edge of clock (CLK). Write a test bench to verify your model.



Exercise 5 – Counter and Display in VHDL

HOCHSCHULE HAMM-LIPPSTADT

- In this exercise, a 1-digit Up/Down counter will be modeled. This should now have the following inputs and outputs:
  - CLK: clock input
  - RST: reset input
  - EN: Start input (starts the counting process)
  - UpDown: Select signal (selects the counting direction)
  - Q: counter output
- Write a VHDL program that implements this counter. Write a suitable testbench for this.
- In order to be able to show the results of the counter on a display, enhance your model using the 7-segment display decoder model from Lab 3.

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Thank you for your attention.

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