Bachelor in Electronic Engineering

Hardware Engineering:

Hardware Engineering Lab

Exercise 3

05.05.2022

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Exercise 1 – Combinational Circuits in VHDL

HOCHSCHULE
HAMM-LIPPSTADT

- Design a VHDL model to implement the behavior of a BCD to 7-segment-LED decoder using concurrent statements. Verify your model using a suitable testbench

Exercise 2 – Combinational Circuits in VHDL

HOCHSCHULE HAMM-LIPPSTADT

- Design the VHDL model to implement a 4 bit BCD Adder displaying the results on 7-segment-dsiplays. Use the VHDL model of your Adder design from Lab 2. Verify your model using a suitable testbench.

Exercise 3 – Sequential Circuits

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- Design the circuit of a 3 bit synchronous down counter using JK-Flipflops.
- Repeat the same exercise designing the same circuit using D-Flipflops.

Exercise 4 – PCB-Design

- Add the Component CC2640R2F to your Eagle libraries conforming to the instructions in Chapter 5.
- Create the footprint and symbol of the component CC2640R2F conforming to the instructions in Chapter 5.

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Thank you for your attention.

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