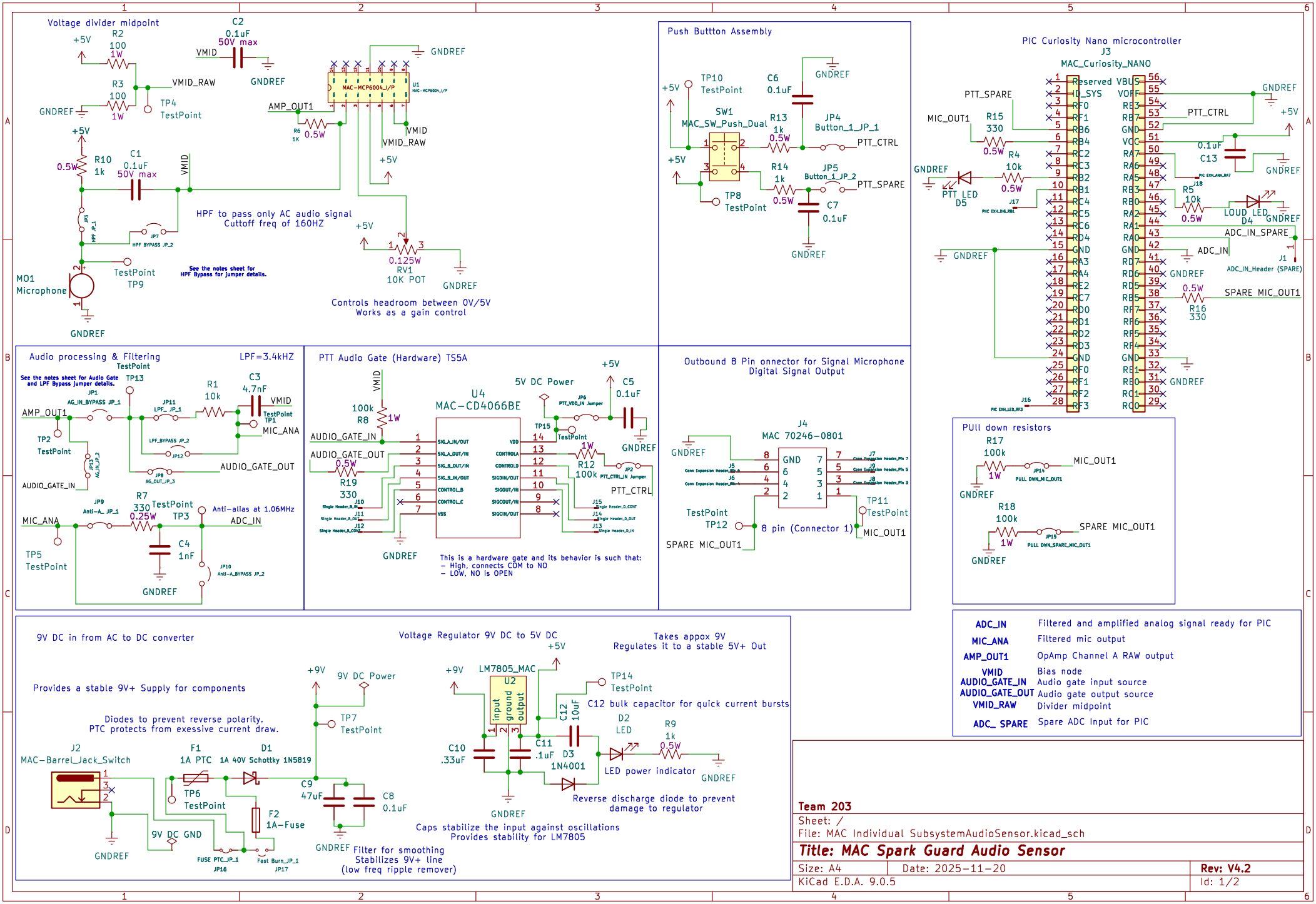
Voltage divider midpoint
+5V
R2
100
1W
R3
100
1W
GNDREF
VMID_RAW
TP4
TestPoint
C2
0.1uF
50V max
VMID
GNDREF
MAC-MCP6004_I/P
U1
AMP_OUT1
R6
1K
0.5W
VMID
VMID_RAW
+5V
0.5W
R10
1k
C1
0.1uF
50V max
VMID
HPF to pass only AC audio signal
Cuttoff freq of 160HZ
JP3
HPF JP_1
JP7
HPF BYPASS JP_2
MO1
Microphone
TestPoint
TP9
See the notes sheet for
HPF Bypass for jumper details.
+5V
0.125W
RV1
10K POT
GNDREF
Controls headroom between 0V/5V
Works as a gain control
Push Buttton Assembly
TP10
TestPoint
+5V
SW1
MAC_SW_Push_Dual
TP8
TestPoint
C6
0.1uF
GNDREF
R13
1k
0.5W
JP4
Button_1_JP_1
PTT_CTRL
R14
1k
0.5W
JP5
Button_1_JP_2
PTT_SPARE
C7
0.1uF
GNDREF
PIC Curiosity Nano microcontroller
J3
MAC_Curiosity_NANO
PTT_SPARE
MIC_OUT1
R15
330
0.5W
R4
10k
0.5W
GNDREF
PTT LED
D5
J17
PIC EXH_DIG_RB1
Reserved
ID_SYS
RF0
RF1
RB6
RB4
RC2
RC3
RB2
RB1
RC4
RC5
RC6
RD4
GND
RA3
RA4
RE2
RC7
RD0
RD1
RD2
RD3
GND
RF0
RF1
RF2
RF3
VBUS
VOFF
RE3
RE7
GND
VCC
RA7
RA6
RA5
RE3
RE0
RA2
RA1
RA0
GND
RD7
RD6
RD5
RB5
RF7
RF6
RF5
RF4
GND
RB1
RB0
RC1
RC0
PTT_CTRL
+5V
0.1uF
C13
GNDREF
J18
PIC EXH_ANA_RA7
R5
10k
0.5W
LOUD LED
D4
GNDREF
ADC_IN_SPARE
ADC_IN
J1
ADC_IN_Header (SPARE)
0.5W
R16
330
SPARE MIC_OUT1
J16
PIC EXH_LED_RF3
PUll down resistors
R17
100k
1W
JP14
PULL DWN_MIC_OUT1
MIC_OUT1
GNDREF
R18
100k
1W
JP15
PULL DWN_SPARE_MIC_OUT1
SPARE MIC_OUT1
GNDREF
Audio processing & Filtering
LPF=3.4kHZ
See the notes sheet for Audio Gate
and LPF Bypass jumper details.
TestPoint
TP13
JP1
AG_IN_BYPASS JP_1
AMP_OUT1
TP2
TestPoint
JP13
AG_IN_JP_2
AUDIO_GATE_IN
JP11
LPF_ JP_1
R1
10k
C3
4.7nF
VMID
TestPoint
TP1
MIC_ANA
LPF_BYPASS JP_2
JP12
JP8
AG_OUT_JP_3
AUDIO_GATE_OUT
R7
330
0.25W
TestPoint
TP3
Anti-alias at 1.06MHz
ADC_IN
JP9
Anti-A_ JP_1
MIC_ANA
TP5
TestPoint
C4
1nF
JP10
Anti-A_BYPASS JP_2
GNDREF
PTT Audio Gate (Hardware) TS5A
VMID
100k
R8
1W
AUDIO_GATE_IN
AUDIO_GATE_OUT
0.5W
R19
330
U4
MAC-CD4066BE
5V DC Power
JP6
PTT_VDD_IN Jumper
+5V
C5
0.1uF
GNDREF
TP15
TestPoint
1W
R12
100k
JP2
PTT_CTRL_IN Jumper
PTT_CTRL
SIG_A_IN/OUT
SIG_A_OUT/IN
SIG_B_OUT/IN
SIG_B_IN/OUT
CONTROL_B
CONTROL_C
VSS
VDD
CONTROLA
CONTROLB
SIGDIN/OUT
SIGOUT/IN
SIGCOUT/IN
SIGCIN/OUT
J10
J11
J12
J15
J14
J13
GNDREF
This is a hardware gate and its behavior is such that:
– High, connects COM to NO
– LOW, NO is OPEN
Outbound 8 Pin onnector for Signal Microphone
Digital Signal Output
J4
MAC 70246-0801
GNDREF
J5
J6
GND
TestPoint
TP12
SPARE MIC_OUT1
8 pin (Connector 1)
J7
J9
J8
TP11
TestPoint
MIC_OUT1
9V DC in from AC to DC converter
Provides a stable 9V+ Supply for components
Diodes to prevent reverse polarity.
PTC protects from exessive current draw.
J2
MAC-Barrel_Jack_Switch
F1
1A PTC
D1
1A 40V Schottky 1N5819
TP6
TestPoint
F2
1A-Fuse
9V DC GND
GNDREF
FUSE PTC_JP_1
JP16
Fast Burn_JP_1
JP17
+9V
9V DC Power
TP7
TestPoint
C9
47uF
C8
0.1uF
GNDREF
Filter for smoothing
Stabilizes 9V+ line
(low freq ripple remover)
Voltage Regulator 9V DC to 5V DC
Takes appox 9V
Regulates it to a stable 5V+ Out
+9V
LM7805_MAC
U2
input
ground
output
+5V
TP14
TestPoint
C12
10uF
C12 bulk capacitor for quick current bursts
C10
.33uF
C11
.1uF
D3
1N4001
D2
LED
R9
1k
0.5W
LED power indicator
GNDREF
Reverse discharge diode to prevent
damage to regulator
Caps stabilize the input against oscillations
Provides stability for LM7805
ADC_IN Filtered and amplified analog signal ready for PIC
MIC_ANA Filtered mic output
AMP_OUT1 OpAmp Channel A RAW output
VMID Bias node
AUDIO_GATE_IN Audio gate input source
AUDIO_GATE_OUT Audio gate output source
VMID_RAW Divider midpoint
ADC_ SPARE Spare ADC Input for PIC
Team 203
Sheet: /
File: MAC Individual SubsystemAudioSensor.kicad_sch
Title: MAC Spark Guard Audio Sensor
Size: A4
Date: 2025-11-20
Rev: V4.2
KiCad E.D.A. 9.0.5
Id: 1/2

Additional Schematic Notes

HPF BYPASS JP_1 & JP_2

–Condition 1 is where the JP_1 jumper connects pins 1, 2, and 3. With 2 sending the signal to JP_2 while this is left open to prevent a bypass. This is the "NORMAL HPF" condition.

–Condition 2 is where the JP_1 jumper connects pins 1 and 2, leaving 3 open. In this condition the signal bypasses the HPF and it sends its signal via JP_2 to the rest of the circuit. This is the "BYPASS HPF" condition.
NOTE: These conditions were put in place for debugging purposes during hardware testing.

Audio Processing & Filtering AG_IN & OUT

–Condition 1 is where the AG_IN_BYPASS JP_1 jumper connects pins 1 and 2 with a closed jumper, while the jumper to pin 3 stays open. Pin 2 sends the signal to AUDIO_GATE_IN (for our logic controlled switch) via a closed AG_OUT_BYPASS JP_2 jumper. The ouput signal comes out of AUDIO_GATE_OUT and it passes through a closed the AG_OUT_BYPASS JP_3 jumper. The signal proceeds to the LPF downstream. This is the "NORMAL AG" condition.
NOTE: This serves as the base condition in which we can utilize the hardware audio gate to operate our push to talk.

–Condition 2 is where the audio gate is bypassed completely. In this condition AG_IN_BYPASS JP_1 jumpers connect pins 1 and 3 by being in the closed position. Pin 2 will remain open by having AG_OUT_BYPASS JP_2 and AG_OUT_BYPASS JP_3 jumpers in the open position. In this condition the signal bypasses the hardware audio gate and it sends its signal via AG_IN_BYPASS JP_1 pin 3 to the LPF downstream. This is the "BYPASS AG" condition.

Audio Processing & Filtering LPF Bypass JP_1

–Condition 1 is where the LPF_BYPASS JP_1 jumper connects pins 1 and 3 with closed jumpers. Pin 2 stays open by having the LPF_BYPASS JP_2 jumper open. The signal flows from pin 3 through the LPF and the rest of our circuit. This is the "NORMAL LPF" condition.
NOTE: This serves as the base condition in which the LPF is utilized.

–Condition 2 is where the LPF_BYPASS JP_1 jumper connects pins 1 and 2 with a single closed jumper, while the jumper to pin 3 stays open. Pin 2 sends the signal to LPF_BYPASS JP_2 jumper that is closed, which then bypasses the LPF and send the signal out MIC_ANA. This is the "BYPASS LPF" condition.
NOTE: This serves as the bypass condition in which we skip over the LPT for testing purposes.

Anti Alias BYPASS Anti–A_Bypass JP_1 & JP_2

–Condition 1 is where the Anti–A_Bypass JP_1 jumper connects pins 1 and 3 with closed jumpers. Pin 2 stays open by having Anti–A_Bypass JP_2 jumper open. The signal flows from pin 3 through the anti alias signal conditioner as normal and then to ADC_IN. This is the "NORMAL AA" condition.
NOTE: This serves as the base condition in which the anti alias is utilized.

–Condition 2 is where the Anti–A_Bypass JP_1 jumper connects pins 1 and 2 with a single closed jumper, while the jumper to pin 3 stays open. Pin 2 sends the signal to Anti–A_Bypass JP_2 jumper that is closed, which then bypasses the anti alias circuit and send the signal directly to ADC_IN. This is the "BYPASS AA" condition.
NOTE: This serves as the bypass condition in which we skip over the anti alias for testing purposes.

PTT Audio Gate Jumpers

–Condition 1 is where the PTT_VDD_IN_JP1 and PTT_CTRL_IN_JP1 jumpers are closed. The power and control signal flow through both jumpers normally. This is the "NORMAL PTT" condition. It corresponds to Audio Processing & Filtering "Condition 1" or "NORMAL AG."
NOTE: This serves as the base condition in which the PTT audio gate is utilized.

–Condition 2 is where thePTT_VDD_IN_JP1 and PTT_CTRL_IN_JP1 jumpers are open. This the "PTT OFFLINE" condition. This corresponds Audio Processing & Filtering "Condition 2" or "BYPASS AG."
NOTE: This serves as an alternative condition in which the audio gate is not used for testing purposes.

Sheet: /Additional Notes/		
File: schematicnotes.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 9.0.5		Id: 2/2