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HW2
Embedded Systems
2/18/19

Exercise 1: RTL Schematic

clk

A[7:0]
B[7:0]
sel
lda

mux

muxOut_i

A[7:0]
B[7:0]
S=1'b1   I0[7:0]
S=1'b0   I1[7:0]
O[7:0]
muxOut[7:0]

S

RTL_MUX

sel

mux2to1

reg

reg_OUT_reg[7:0]

CLK
LD
reg_IN[7:0]
C
CE   Q
D

RTL_REG

Reg_A

reg_OUT[7:0]
F[7:0]
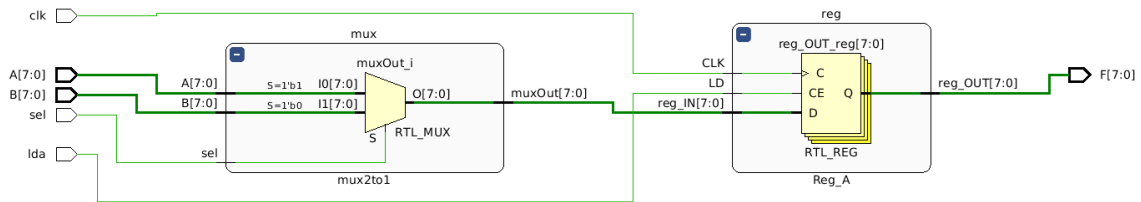
Exercise 2: RTL Schematic

CLK

DS

dec

output1_i

S=1'b0   I0
S=default I1
O
output0
output1

S   RTL_MUX

ds

decoder1to2

MS[1:0]
X[7:0]
Y[7:0]
Z[7:0]

mux

muxOut_i

MS[1:0]
RB_out[7:0]
x[7:0]
y[7:0]
z[7:0]
S=2'b00   I0[7:0]
S=2'b01   I1[7:0]
S=2'b10   I2[7:0]
S=2'b11   I3[7:0]
O[7:0]
muxOut[7:0]

S[1:0]   RTL_MUX

mux4to1

RegB

reg_OUT_reg[7:0]

CLK
LD
reg_IN[7:0]
C
CE   Q
D

RTL_REG

REG

reg_OUT[7:0]
RB[7:0]
RA[7:0]

RegA

reg_OUT_reg[7:0]

CLK
LD
reg_IN[7:0]
C
CE   Q
D

RTL_REG

REG

reg_OUT[7:0]
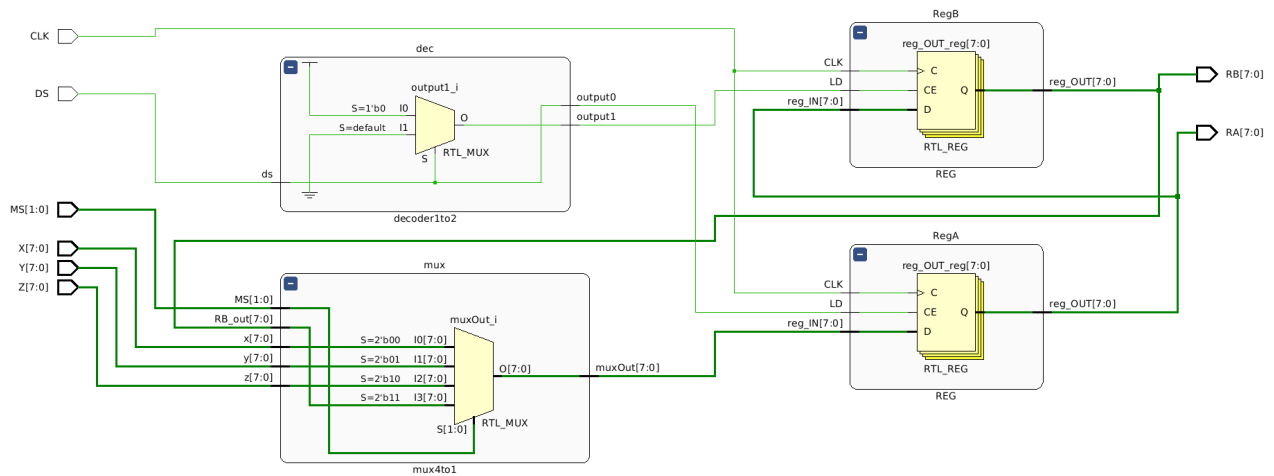
Exercise 3: RTL Schematic

CLK
X[7:0]
S1
IDA
LDB
Y[7:0]
S0

mux1
muxOut_i
input1[7:0]
input2[7:0]
S=1'b1 I0[7:0]
S=1'b0 I1[7:0]
O[7:0] muxOut[7:0]
sel
S
RTL_MUX
mux2to1

RegA
reg_OUT_reg[7:0]
CLK
LD
reg_IN[7:0]
C
CE Q
D
reg_OUT[7:0]
RTL_REG
REG

mux2
muxOut_i
input1[7:0]
input2[7:0]
S=1'b1 I0[7:0]
S=1'b0 I1[7:0]
O[7:0] muxOut[7:0]
sel
S
RTL_MUX
mux2to1

RegB
reg_OUT_reg[7:0]
CLK
LD
reg_IN[7:0]
C
CE Q
D
reg_OUT[7:0]
RTL_REG
REG
RB[7:0]
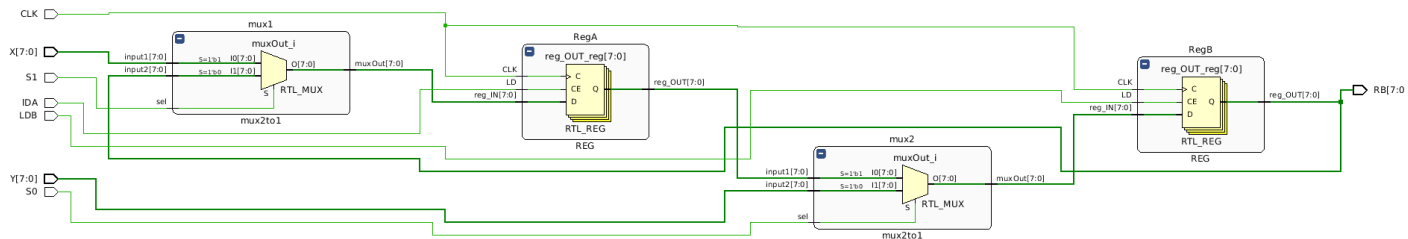
Exercise 4: RTL Schematic

CLK
X[7:0]
Y[7:0]
S1
S0
LDB
RD
IDA

mux1
muxOut_i
input1[7:0]
input2[7:0]
S=1'b1 I0[7:0]
S=1'b0 I1[7:0]
O[7:0] muxOut[7:0]
sel
S
RTL_MUX
mux2to1

RegB
reg_OUT_reg[7:0]
CLK
LD
reg_IN[7:0]
C
CE Q
D
reg_OUT[7:0]
RTL_REG
REG
RB[7:0]

mux2
muxOut_i
input1[7:0]
input2[7:0]
S=1'b1 I0[7:0]
S=1'b0 I1[7:0]
O[7:0] muxOut[7:0]
sel
S
RTL_MUX
mux2to1

RegA
reg_OUT_reg[7:0]
CLK
LD
reg_IN[7:0]
C
CE Q
D
reg_OUT[7:0]
RTL_REG
REG
RA[7:0]

inv
output0_i
input I0 O output
RTL_INV
inverter

and1
output0_i
inputA I0 O output
inputB I1
RTL_AND
andGate
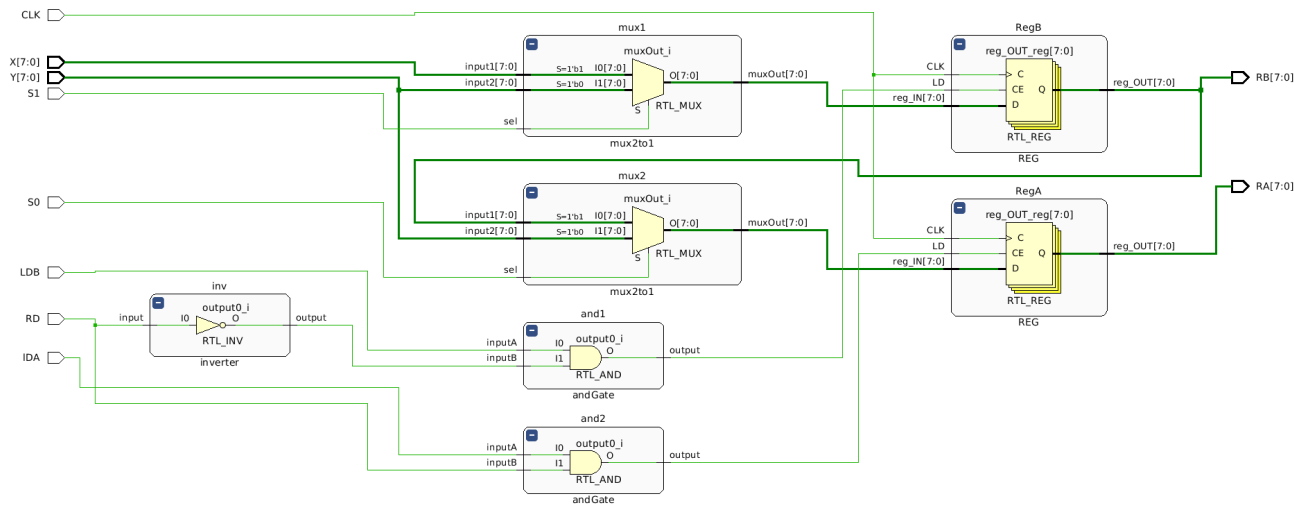
and2
output0_i
inputA I0 O output
inputB I1
RTL_AND
andGate

Exercise 5: RTL Schematic

CLK

B[7:0]
C[7:0]
SL2

mux

input1[7:0]
input2[7:0]

S=1'b1 I0[7:0]
S=1'b0 I1[7:0]

muxOut_i

O[7:0]

S

RTL_MUX

sel

mux2to1

muxOut[7:0]

RegB

reg_OUT_reg[7:0]

CLK
LD
reg_IN[7:0]

C
CE   Q
D

RTL_REG

REG

reg_OUT[7:0]

RBX[7:0]

SL1

A[7:0]

dec

S=1'b0   I0
S=default   I1

output1_i

O

S

RTL_MUX

ds

decoder1to2

output0
output1

RAX[7:0]

RegA

reg_OUT_reg[7:0]

CLK
LD
reg_IN[7:0]

C
CE   Q
D

RTL_REG

REG

reg_OUT[7:0]
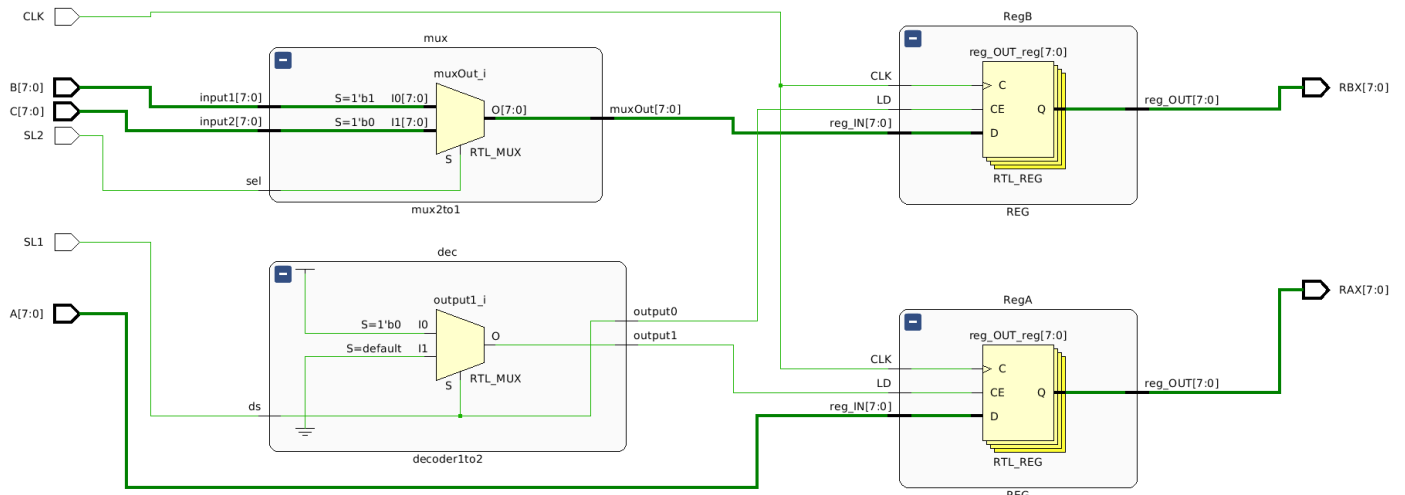
Exercise 6: RTL schematic

CLK

A[7:0]
B[7:0]
SEL1

mux

input1[7:0]
input2[7:0]

S=1'b1 I0[7:0]
S=1'b0 I1[7:0]

muxOut_i

O[7:0]

S

RTL_MUX

sel

mux2to1

muxOut[7:0]

RegA

reg_OUT_reg[7:0]

CLK
LD
reg_IN[7:0]

C
CE   Q
D

RTL_REG

REG

reg_OUT[7:0]

RAP[7:0]

SEL2

C[7:0]

dec

S=1'b0   I0
S=default   I1

output1_i

O

S

RTL_MUX

ds

decoder1to2

output0
output1

RBP[7:0]

RegB

reg_OUT_reg[7:0]

CLK
LD
reg_IN[7:0]

C
CE   Q
D

RTL_REG

REG

reg_OUT[7:0]