**ECE493 Lab 2 Report**

Shuyu Chen

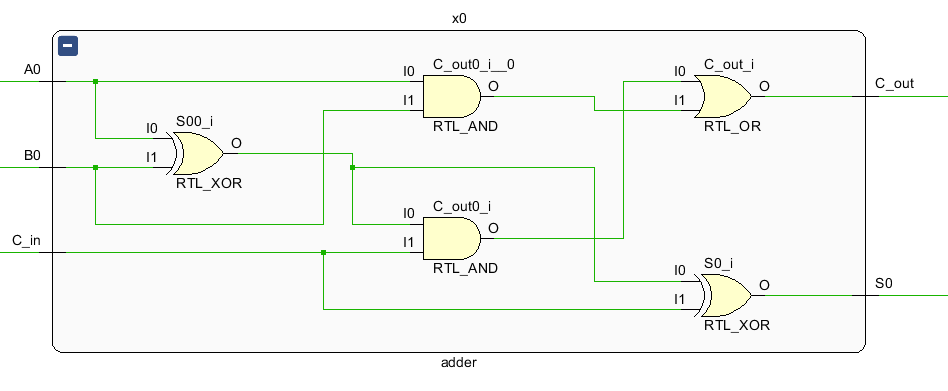
1. **4-bit full adder**

**Theory:**

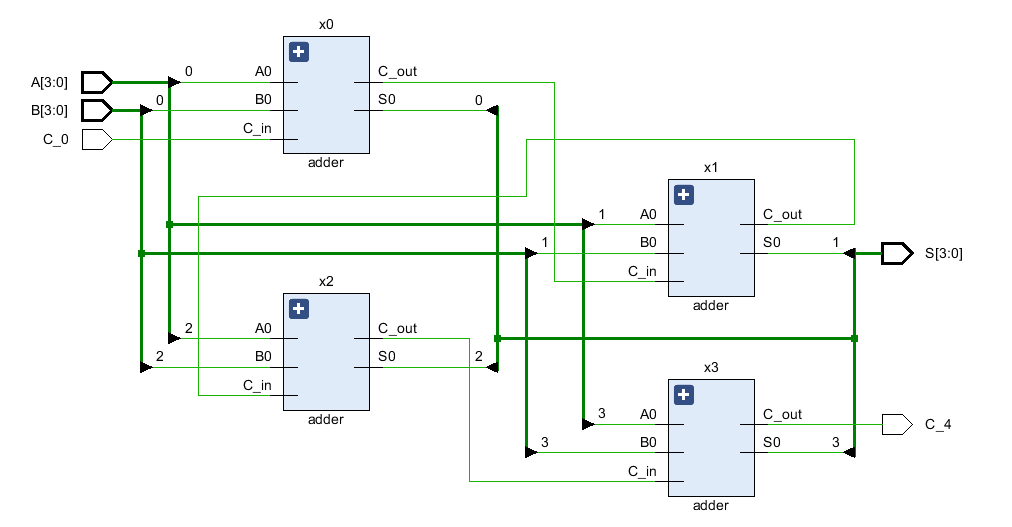
For a single full adder, we use combinational logic circuit to implement. Having single adder, we build the 4-bit adder with 4 single adder components. The input and output are 4-bit vectors, each of the 4 bits is distributed to one of the adders. The ripple adder is constructed by linking the carry\_in of an adder to the carry\_out of another adder.

**Schematics:**

Single Adder



4-bit Ripple Adder



**Simulation Result:**



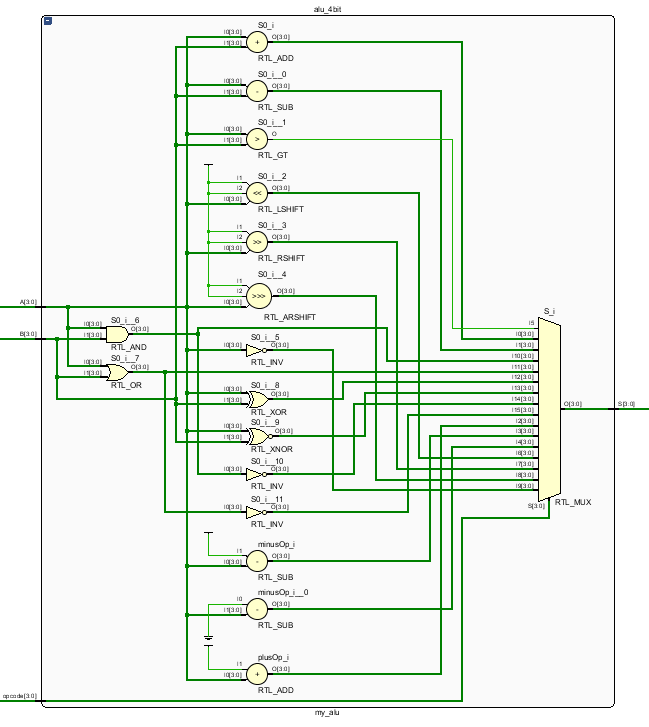
1. **4-bit, 16 function ALU**

**Theory:**

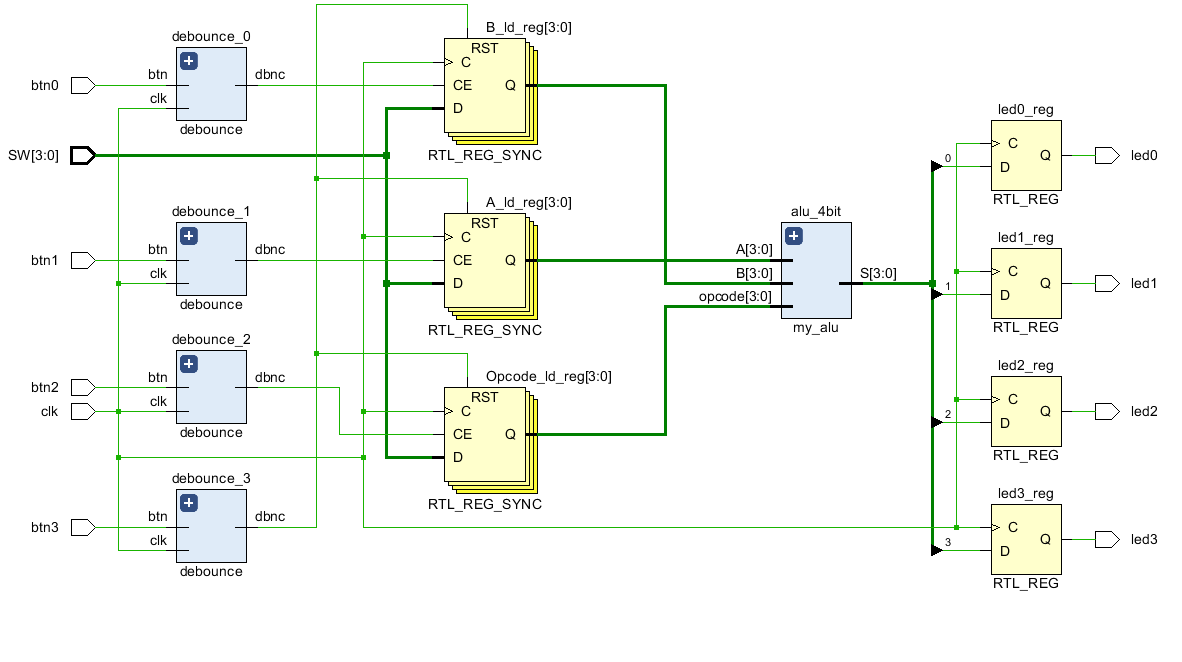
For ALU with 16 operations, we take advantage of pre-defined arithmetic operations defined in the IEEE numeric\_std library.

**Schematic**

“my\_alu” component:



ALU tester



Simulation results(without debouncing)

