

1

2

3

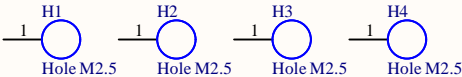
4

Revision History

1v0 Initial release.

Notes

See part description for case size.
All resistors are 1%.
All ceramic capacitors (non-polarized) are 50V (if possible) unless otherwise indicated.
Net names are global.



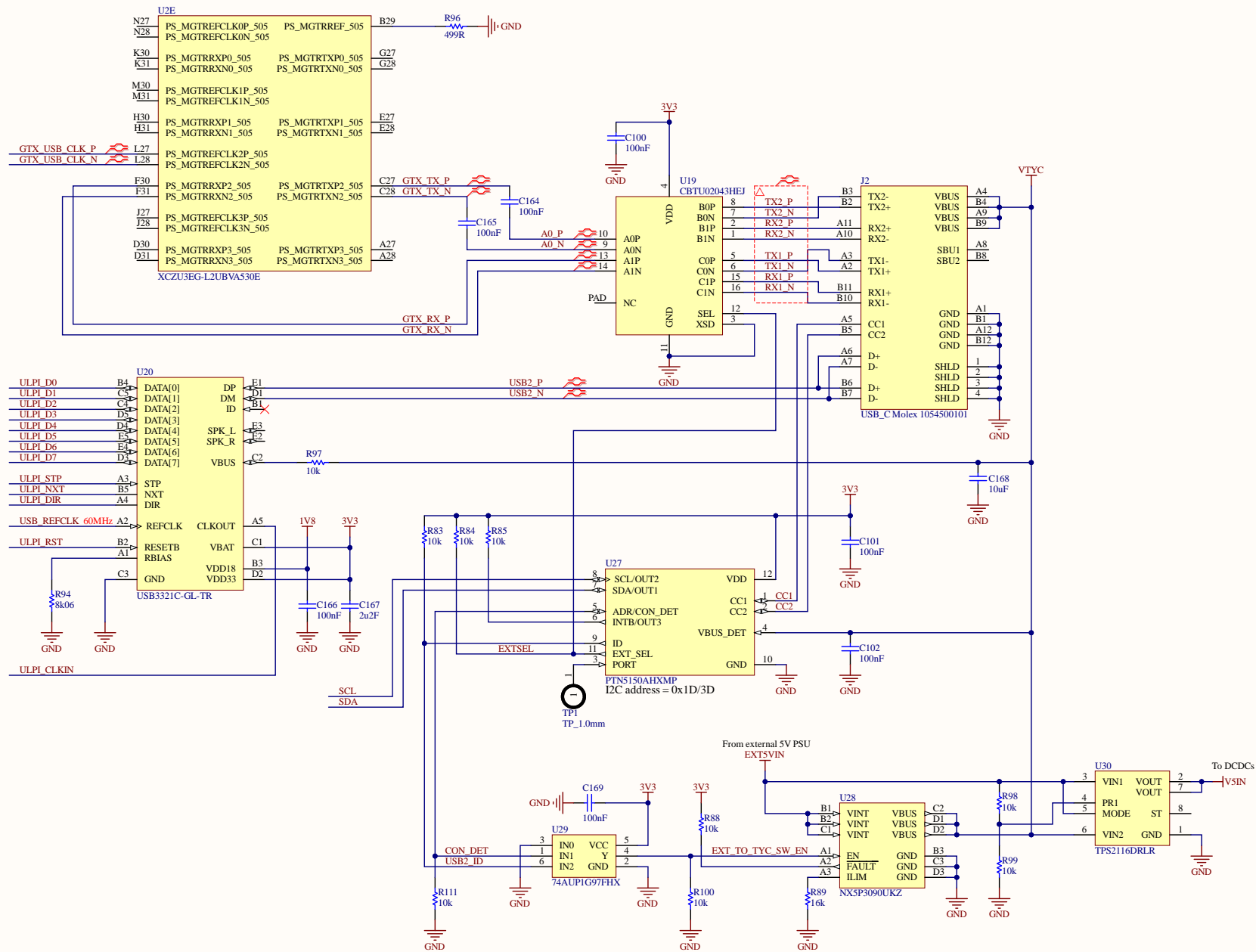
Company: Sundance / Opteran	Project: ODK v1
Title: Cover Sheet	Revision: 1v0
Date: 20/3/22	Sheet: 1 of 15
Filename: Cover Sheet.SchDoc	Drawn: GKP

1

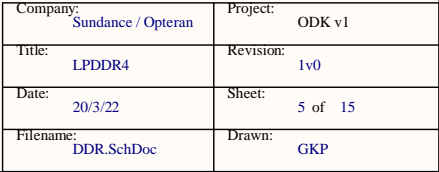
2

3

4



Company:	Sundance / Opteran	Project:	ODK v1
Title:	USB	Revision:	1v0
Date:	20/3/22	Sheet:	3 of 15
Filename:	USB.SchDoc	Drawn:	GKP



A

B

C

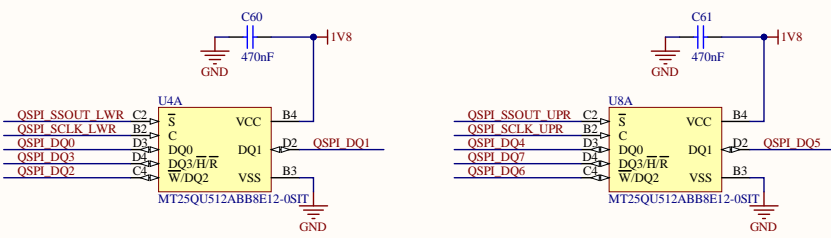
D

A

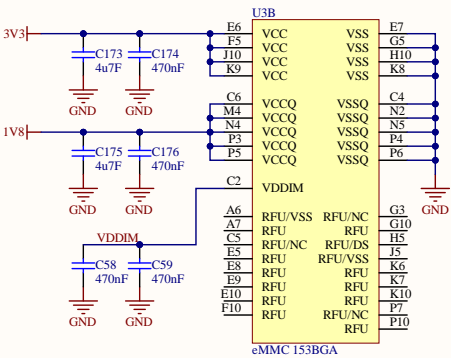
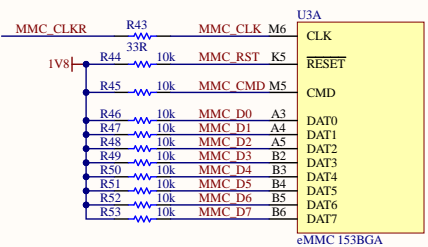
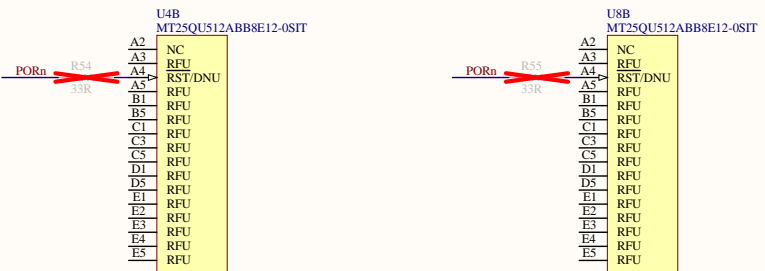
B

C

D

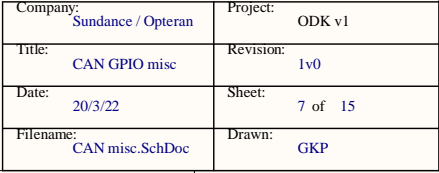


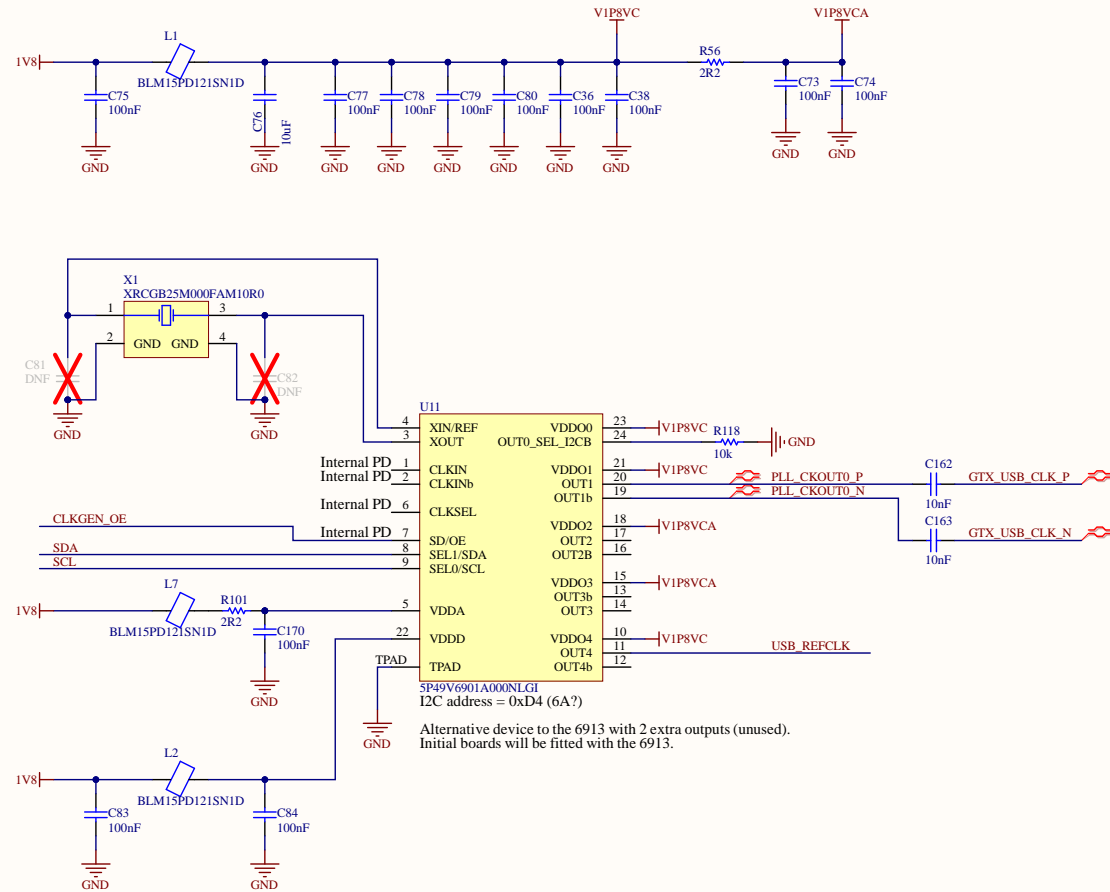
Alternative part MX25U51245GXD100 supported by Xilinx.



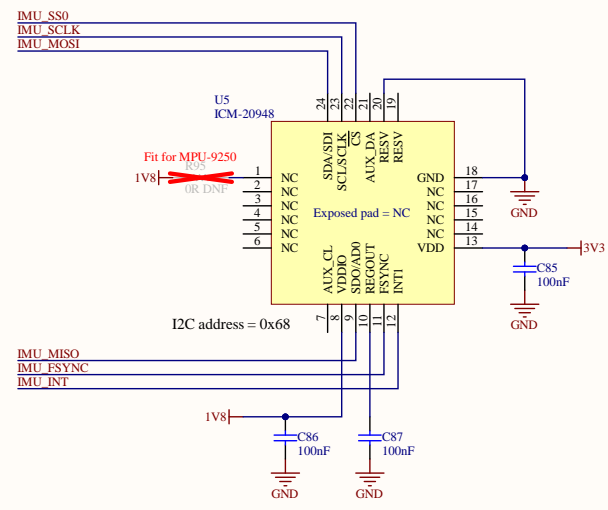
U3C		
A1	NC	H2
A2	NC	H3
A8	NC	H12
A9	NC	H13
A10	NC	H14
A11	NC	J1
A12	NC	J2
A13	NC	J3
A14	NC	J12
B1	NC	J13
B7	NC	J14
B8	NC	K1
B9	NC	K2
B10	NC	K3
B11	NC	K12
B12	NC	K13
B13	NC	K14
B14	NC	L1
C1	NC	L2
C3	NC	L3
C7	NC	L12
C8	NC	L13
C9	NC	L14
C10	NC	M1
C11	NC	M2
C12	NC	M3
C13	NC	M7
C14	NC	M8
D1	NC	M9
D2	NC	M10
D3	NC	M11
D4	NC	M12
D12	NC	M13
D13	NC	M14
D14	NC	N1
E1	NC	N3
E2	NC	N6
E3	NC	N7
E12	NC	N8
E13	NC	N9
E14	NC	N10
F1	NC	N11
F2	NC	N12
F3	NC	N13
F12	NC	N14
F13	NC	P1
F14	NC	P2
G1	NC	P8
G2	NC	P9
G12	NC	P11
G13	NC	P12
G14	NC	P13
H1	NC	P14

Company: Sundance / Opteran	Project: ODK v1
Title: Flash	Revision: 1v0
Date: 20/3/22	Sheet: 6 of 15
Filename: Flash.SchDoc	Drawn: GKP





Company: Sundance / Opteran	Project: ODK v1
Title: Clock PLL	Revision: 1v0
Date: 20/3/22	Sheet: 8 of 15
Filename: Clock PLL.SchDoc	Drawn: GKP



Company: Sundance / Opteran	Project: ODK v1
Title: IMU	Revision: 1v0
Date: 20/3/22	Sheet: 9 of 15
Filename: IMU.SchDoc	Drawn: GKP

A

B

C

D

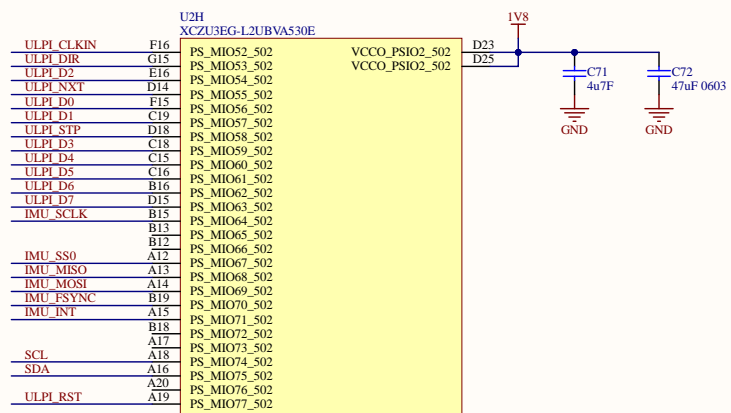
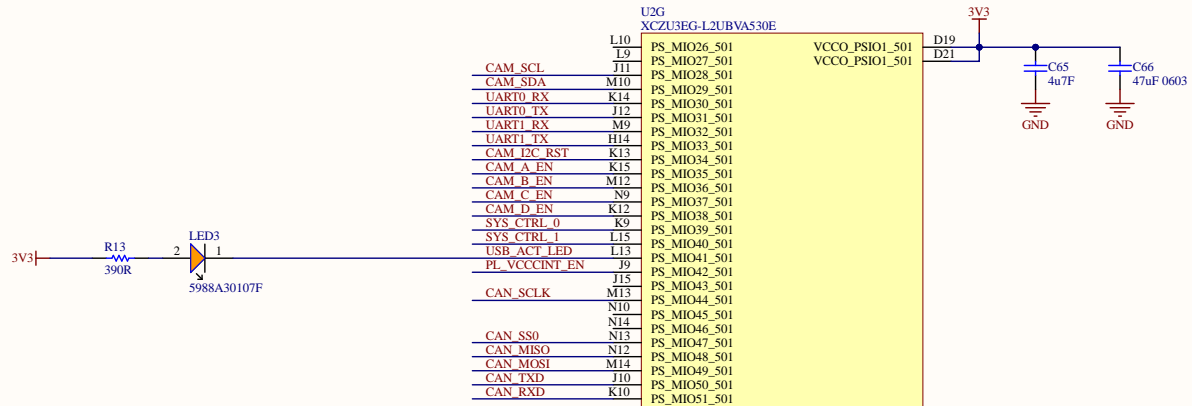
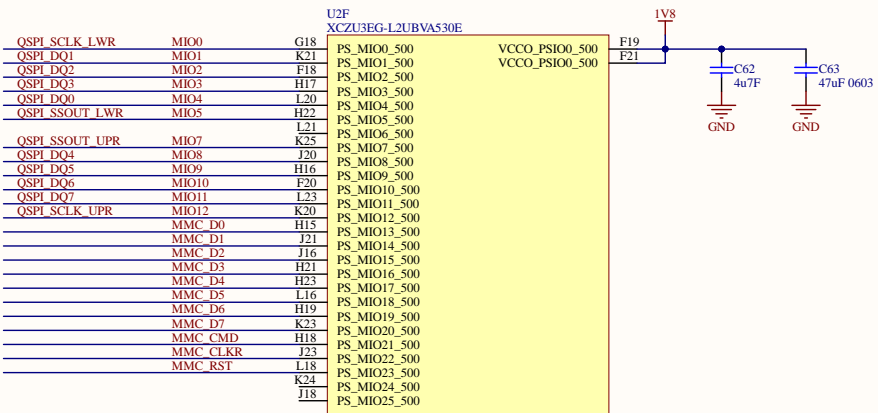
A

B

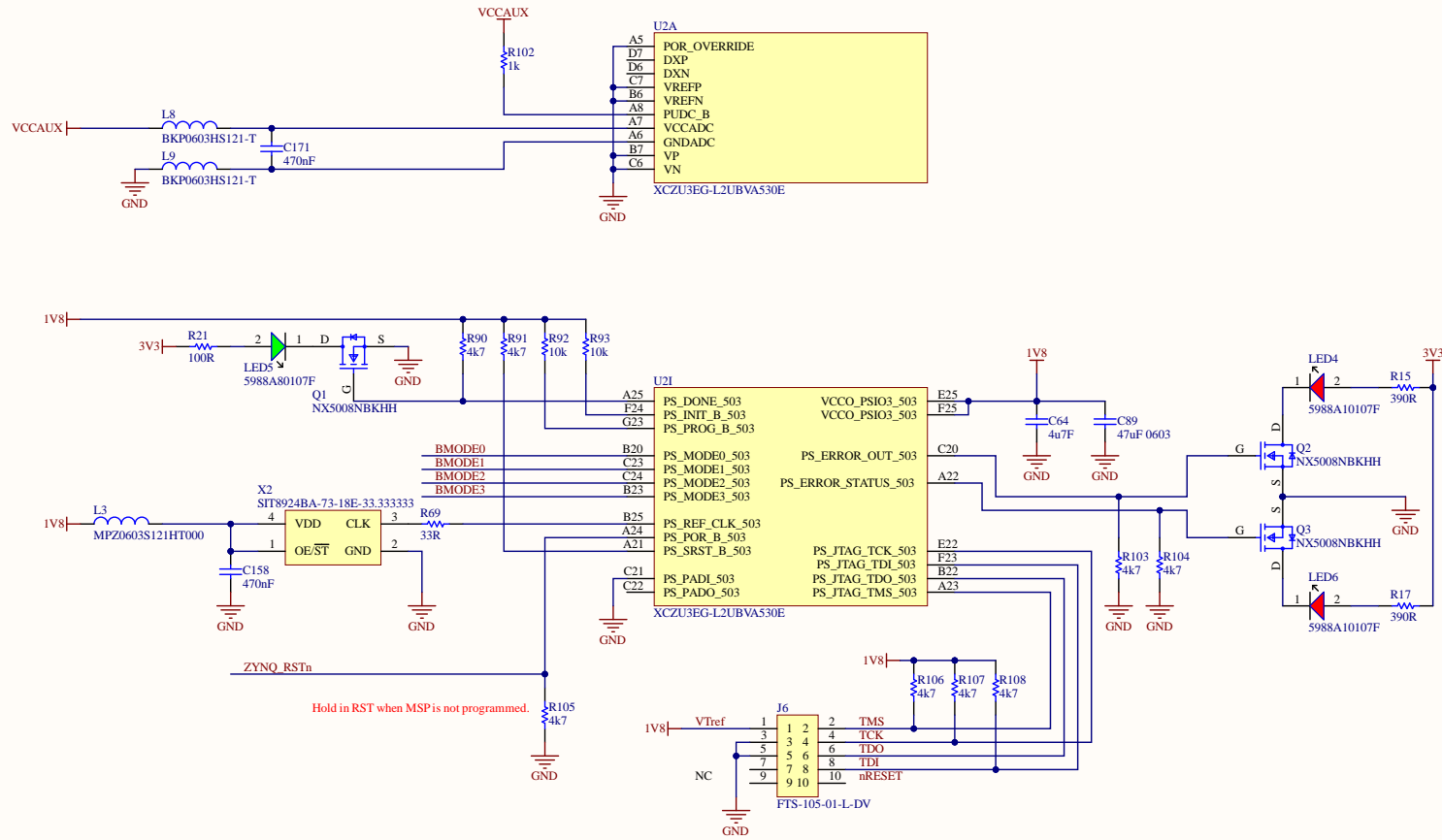
C

D

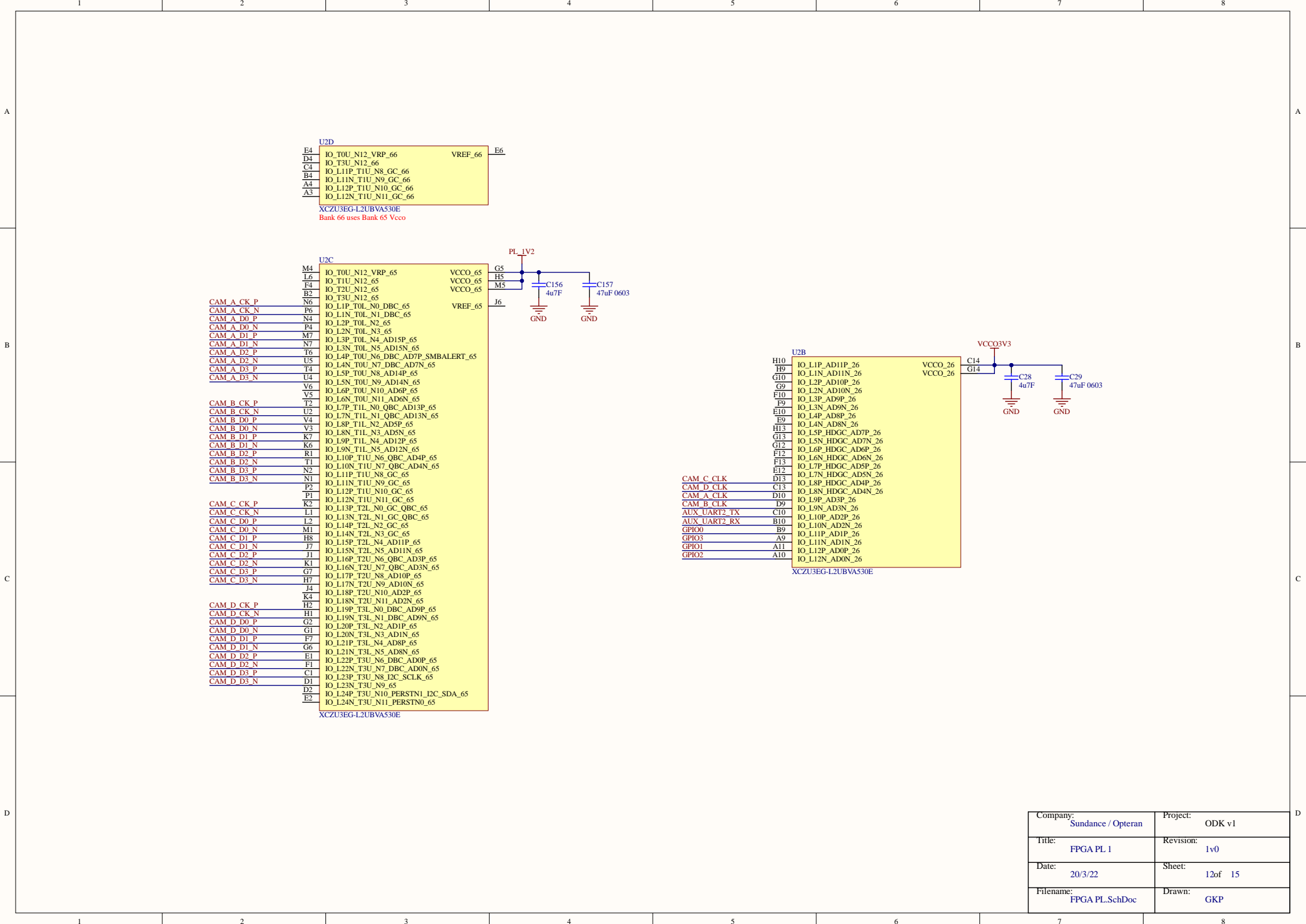
Flash and eMMC interfaces



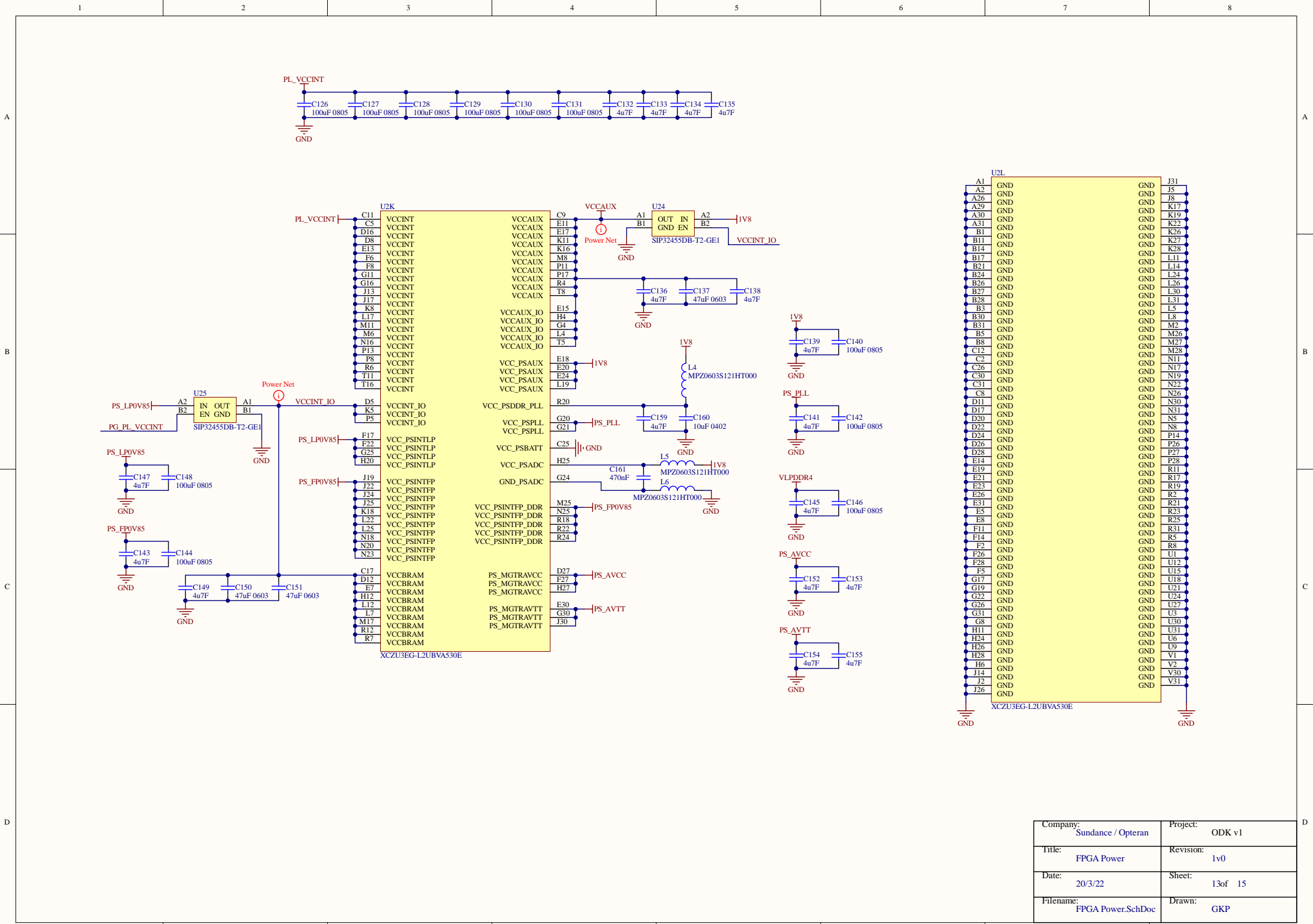
Company: Sundance / Opteran	Project: ODK v1
Title: MIO 1	Revision: 1v0
Date: 20/3/22	Sheet: 10of 15
Filename: MIO 500-502.SchDoc	Drawn: GKP



Company:	Sundance / Opteran	Project:	ODK v1
Title:	FPGA JTAG	Revision:	1v0
Date:	20/3/22	Sheet:	11 of 15
Filename:	FPGA JTAG.SchDoc	Drawn:	GKP



Company: Sundance / Opteran	Project: ODK v1
Title: FPGA PL 1	Revision: 1v0
Date: 20/3/22	Sheet: 12of 15
Filename: FPGA PL.SchDoc	Drawn: GKP



Company: Sundance / Opteran	Project: ODK v1
Title: FPGA Power	Revision: 1v0
Date: 20/3/22	Sheet: 13of 15
Filename: FPGA Power.SchDoc	Drawn: GKP

A

A

B

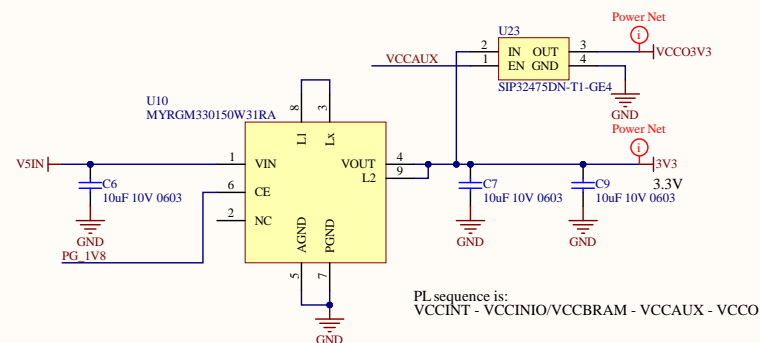
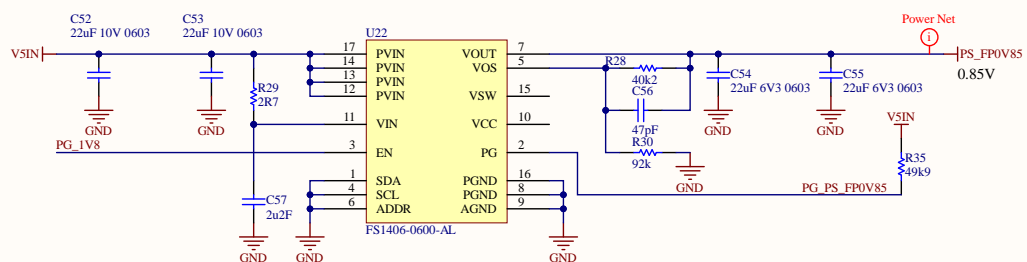
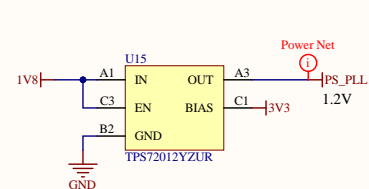
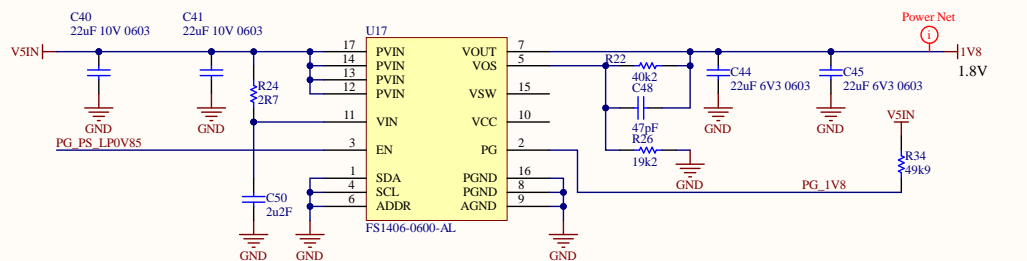
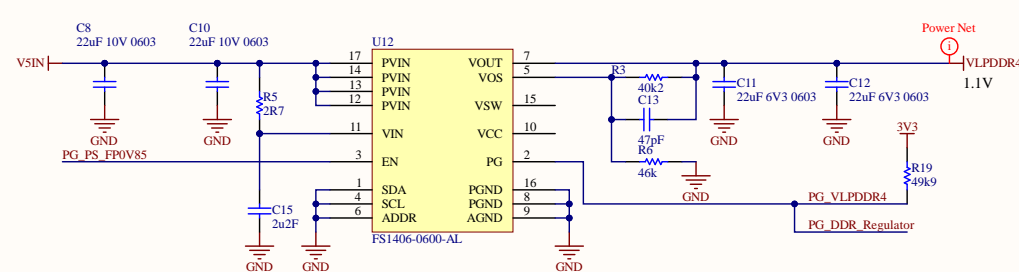
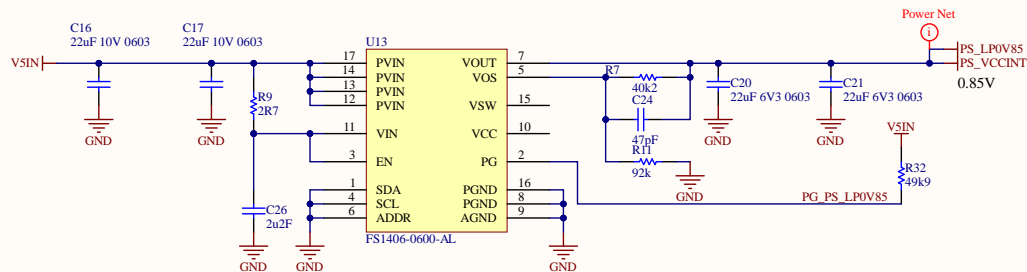
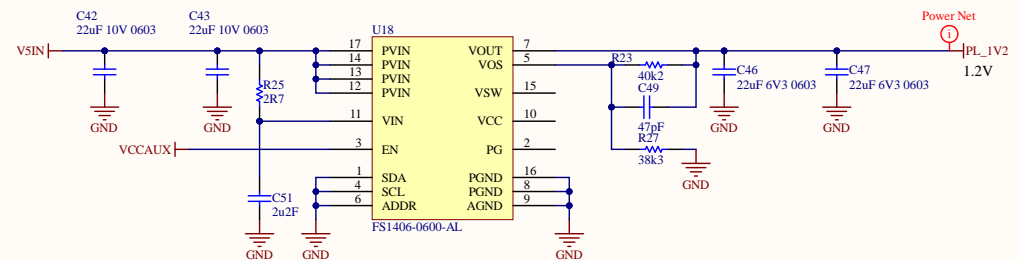
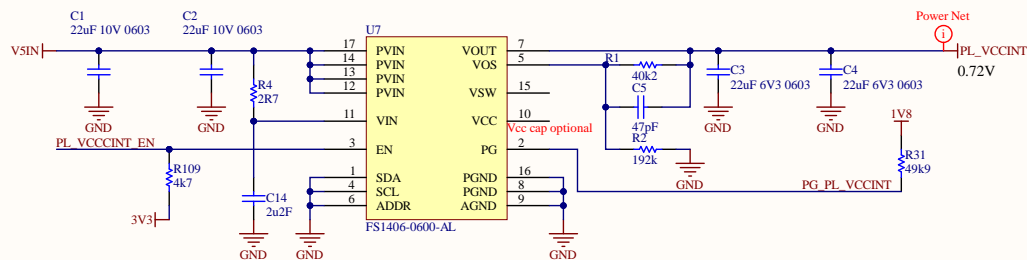
B

C

C

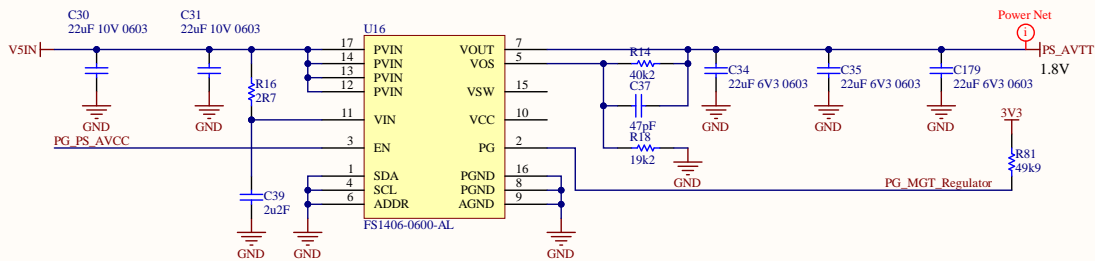
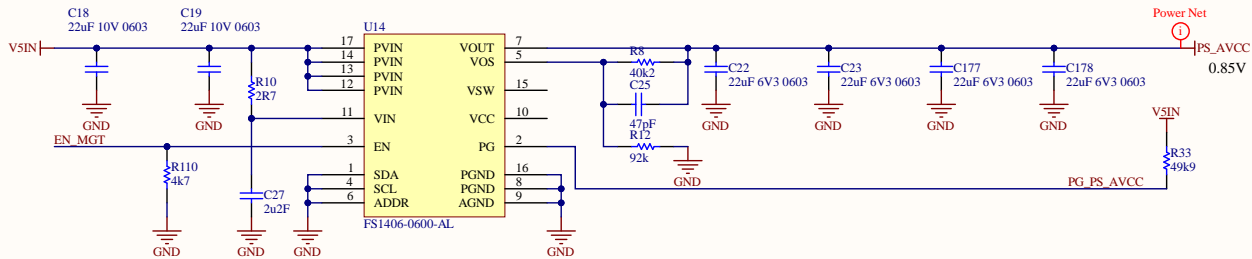
D

D



POWER ON V5IN > PS_VCCINT/PS_LP0V85 > 1V8 > PS_PLL/3V3 > PS_FP0V85 > PG_VLPDDR4
SIGNAL FROM PS PL_VCCINT_EN > PL_VCCINT > VCCINT_IO > VCCAUX > VCCO3V3
SIGNAL FORM MSP EN_MGT > PS_AVCC > PS_AVTT

Company: Sundance / Opteran	Project: ODK v1
Title: Power Supply	Revision: 1v0
Date: 20/3/22	Sheet: 14of 15
Filename: Power Supply.SchDoc	Drawn: GKP



Company: Sundance / Opteran	Project: ODK v1
Title: Power Supply 2	Revision: 1v0
Date: 20/3/22	Sheet: 15of 15
Filename: Power Supply 2.SchDoc	Drawn: GKP