TEST INSTRUCTIONS

SMT362 V1

Dual C6455 with FX60

SUNDANCE MULTIPROCESSOR TECHNOLOGY LTD.

Revision Record			
Revision.	Date	Change.	Initials
1	06 Dec. 06	Original Document First prototype with 1 DSP	J.V.
1.1	05 Feb. 07	Added test for SRIO and bottom RSL	J.V.
1.2	06 Feb. 07	RSL test described with loopback connectors	J.V.
1.3	08 Feb. 07	Rapidio test DSP <=> FPGA added	J.V.
1.4	14 Sep. 07	Ethernet ping test added	J.V.
1.5	22-7-2010	Updated to enable CPLD programming and how to set up Code Composer	CH
1.51	25-10-11	Added note about the batch file to make life easier.	CH

Comments

To make the reprogramming of the FLASH easier during the test of this board, there is a batch file in the "**SMT362 Batch file to make testing easier**" folder. Please read the README.txt file for any configuration changes.

Test Equipment.

An SMT310Q with the SMT362 plugged on the second TIM site with comport cable connections T2C0-T2C3, T2C1-T2C4, T2C2-T2C5.
SHB cable connected between SHBA and SHBB.

JTAG parallel cable and **JTAG adapter for the SMT362**.
This is the cable that looks like a SMT568, but has an extra pin coming off the VCC pin. Currently it's multi coloured.

For the RSL test, RSL loopback connector plugged on each connector and an SMT395_VP30 to drive the test.

How to set up Code Composer Studio V3 with the SMT362.

The Setup of code composer for the SMT362 is a bit of a black art.

To help with this, there are a couple of files that can be used to configure it for you.

If you are using an SMT310Q (Which is the standard), then you will be find the file "sample CCS setupfile.ccs" in the root of the SMT362 folder in SourceSafe.

If you are using an XDS510 USB module from SEED, then the link below will enable you download a zip file which contains the setup file.
http://www.sundance.com/drivers/cc3_3_smt362_xds510.zip

Get a copy of the CCS file, and unzip it if required.
Open Code Composer Setup, and remove any previous configuration.
From the "File" menu select "Import". Browse to the correct file and import it.

You now should see a full configuration in the left most pane of the setup program.

If you're using the SMT310Q (Or SMT310) now you need to right click the SMT310Q and check the properties. Chances are that you will have to change the address. The correct address can be found by looking in SMTBoardInfo (Part of SMT6300)

For the XDS510, no extra changes need to be made.

Close the Setup program and run Code Composer.

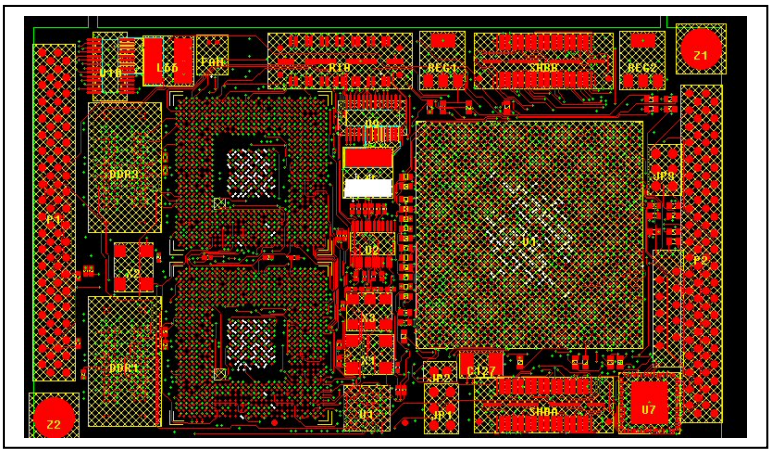
If it's all worked, you'll now see 2 DSPs connected Via the ice picks.

Test Procedure.

1. Voltages

Power up the board and swiftly verify the voltages on the following test points.

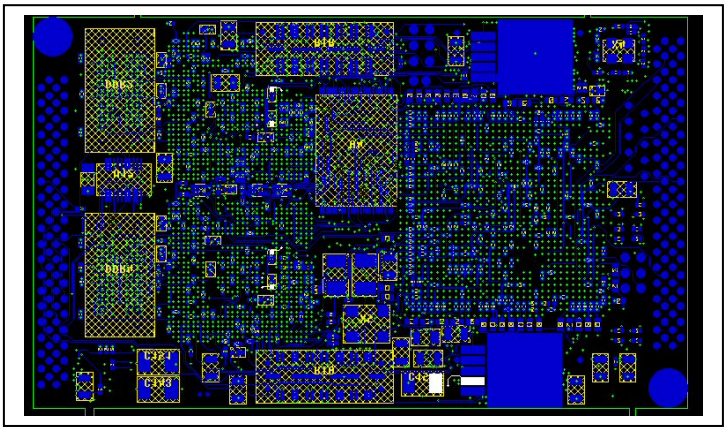
1.1 V1.2



The voltage should be 1.2V or 1.25V depending on the device speed.
For -1000 it should be 1.25V. (1.2125 V < 1.25 V < 1.2875 V)
For -800 / -600 it should be 1.2V. (1.1640 V < 1.20 V < 1.2360 V)

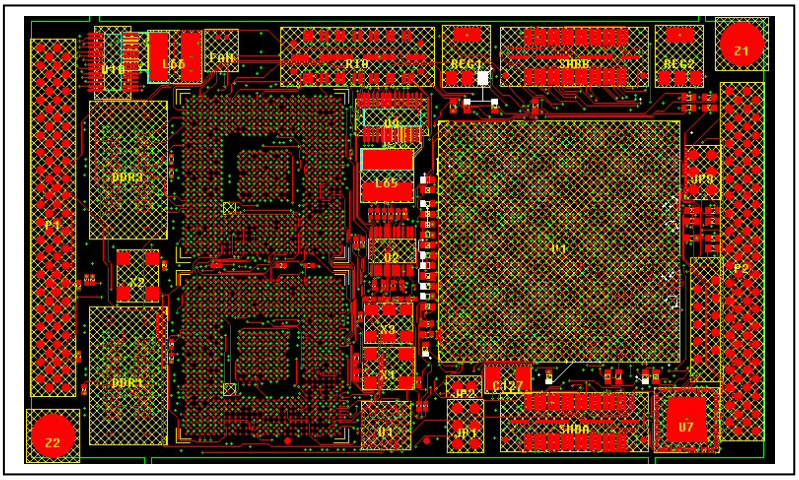
For the FPGA it is 1.2V. (1.14 V < 1.2 V < 1.26 V)

1.2 V1.2 LIN



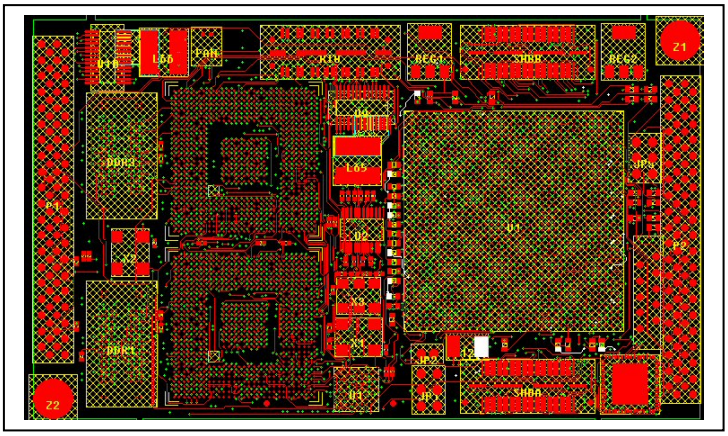
The voltage should be 1.2V or 1.25V depending on the device speed.
For -1000 it should be 1.25V. (1.2125 V < 1.25 V < 1.2875 V)
For -800 / -600 it should be 1.2V. (1.1640 V < 1.20 V < 1.2360 V)
It is only accessible from the bottom of the board.

1.3 V1.5



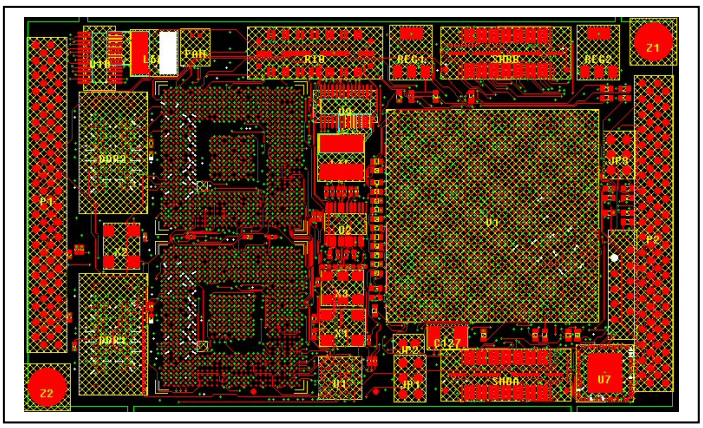
The voltage should be 1.5V. (1.14 V < 1.5 V < 1.575 V)

1.4 V1.2 RIO



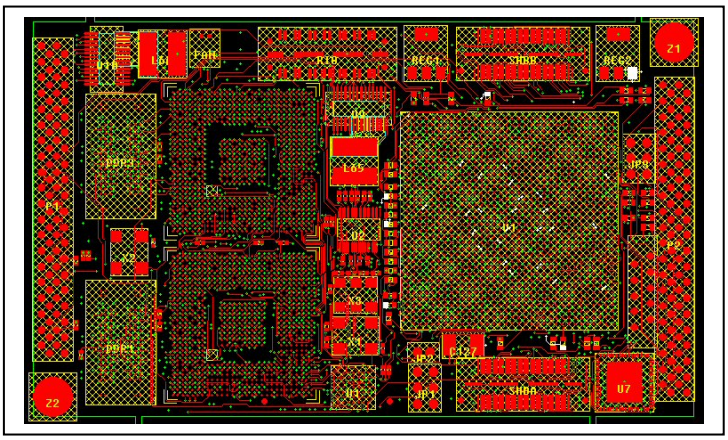
The voltage should be 1.2V. (1.14 V < 1.2 V < 1.26 V)

1.5 V1.8



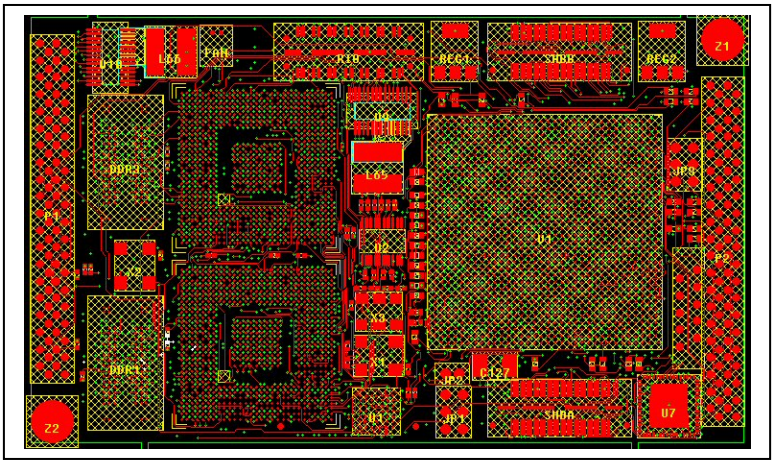
The voltage should be 1.8V. (1.71 V < 1.8 V < 1.89 V)

1.6 V2.5



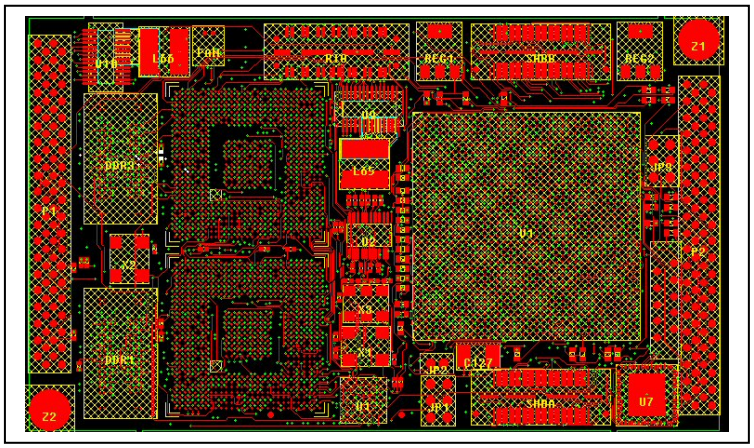
The voltage should be 2.5 V. (2.375 V < 2.5 V < 2.625 V)

1.7 VREFA



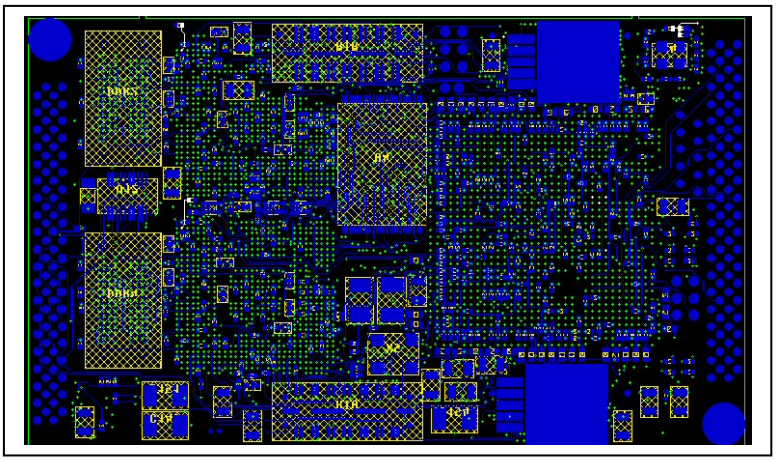
The voltage should be 0.9V. (0.855 V< 0.9 V < 0.945 V)

1.8 VREFB



The voltage should be 0.9V. (0.855 V< 0.9 V < 0.945 V)

1.9 VREFHSTL



The voltage should be 0.9V. (0.855 V< 0.9 V < 0.945 V)
It is only accessible from the bottom of the board.

CPLD programming

Connect the SPECIAL JTAG programming cable to JP1. VCC (the red wire) is pin 1. Connect the flying lead of this special cable to pin 1 of JP2 (The top pin of the two).

If this extra connection isn't made, you will only see the CPLD in the Xilinx JTAG chain, and even then you won't be able to program it.

Run iMPACT, and after doing a boundary scan, select the CPLD (9536XL). Program this with:
$/SMT362/Firmware/CPLD/cpld_readback_hpi.jed

JP1

TCK	GND	**VCC**
TDO	TDI	TMS

Remove the programming cable, and fit Jumper JP2.

GEL file

In order to initialise the peripherals load the following GEL file in CCS and reset the board under CCS.
SS\SMT362\Manufacture\Tests\Gel\ smt362.gel
If this fails it should be possible to load and run the boot code directly from the SMT6001 folder.

Memory test

Load the following application and run it. It will report any error.
Leave it to run until it displays “Memory test completed”.
SS:\SMT362\Manufacture\Tests\ MemoryTest\ddr2.out

Do this for both DSP1 and DSP2 to ensure that both banks of memory are tested.

Flash test

Load the following application and run it. It will report any error or hang if it can’t access the flash.
Leave it to run until it displays “Flash test completed”.
SS:\SMT362\Manufacture\Tests\Flash\testflash362.out

Board programming

The board can now be programmed using the SMT6001 with the default boot code and firmware using dspa only.

$/SMT362/Manufacture/Tests/Firmwares_for_test/smt362_dspa.bit
All the links are under control of DSPA to make it simpler to test.

At the end of the following tests the default boot code and firmware should be programmed.

LED test

Load and run the following application:
$/SMT362/Manufacture/Tests/LED/testled362.out

Comport tests

Load and run the following applications
SMT362\Manufacture\Tests\smt6400\cp03\cppolling.out
SMT362\Manufacture\Tests\smt6400\cp14\cppolling.out
SMT362\Manufacture\Tests\smt6400\cp25\cppolling.out

The application runs continuously but it can be stopped after it says
“Data bit tested and bus exchanged”
It will display an error message and hang if it finds any error.

SHB test

Load and run the following application
X:\SMT362\Manufacture\Tests\smt6400\sdb\ sdbpolling.out
The application runs continuously but it can be stopped after it says
“Data bit tested and bus exchanged”
It will display an error message and hang if it finds any error.

SRIO inter DSP Test

Program the FPGA with the firmware
$/SMT362/Manufacture/Tests/Firmwares_for_test/dsp_fpga_srio_loopback.bit

Test Lane 0:

On DSPB load and run $/SMT362/Manufacture/Tests/srio/srio_lane0/slave/Debug/srio_slave.out
On DSPA load and run $/SMT362/Manufacture/Tests/srio/srio_lane0/master/Debug/srio_master.out
It should display “SRIO transfers are successful” in a loop. If it doesn’t check the termination resistors have been fitted on the SRIO clocks.

Test Lane 1:

On DSPB load and run $/SMT362/Manufacture/Tests/srio/srio_lane1/slave/Debug/srio_slave.out
On DSPA load and run $/SMT362/Manufacture/Tests/srio/srio_lane1/master/Debug/srio_master.out
It should display “SRIO transfers are successful” in a loop. If it doesn’t check the termination resistors have been fitted on the SRIO clocks.

Test Lane2 DSPA:

On DSPA load and run $/SMT362/Manufacture/Tests/srio/srio_lane2/master/Debug/srio_master.out
It should display “SRIO transfers are successful” in a loop. If it doesn’t check the inductors L18 L21 L25 and L28 have been modified to be connected to V12LIN U11 pin4 instead of 1.5V.

Test Lane3 DSPA:

On DSPA load and run $/SMT362/Manufacture/Tests/srio/srio_lane3/master/Debug/srio_master.out
It should display “SRIO transfers are successful” in a loop. If it doesn’t check the inductors L18 L21 L25 and L28 have been modified to be connected to V12LIN U11 pin4 instead of 1.5V.

Test Lane2 DSPB:

On DSPB load and run $/SMT362/Manufacture/Tests/srio/srio_lane2/master/Debug/srio_master.out
It should display “SRIO transfers are successful” in a loop. If it doesn’t check the inductors L18 L21 L25 and L28 have been modified to be connected to V12LIN U11 pin4 instead of 1.5V.

Test Lane3 DSPB:

On DSPB load and run $/SMT362/Manufacture/Tests/srio/srio_lane3/master/Debug/srio_master.out
It should display “SRIO transfers are successful” in a loop. If it doesn’t check the inductors L18 L21 L25 and L28 have been modified to be connected to V12LIN U11 pin4 instead of 1.5V.

RSL Tests

SMT395_VP30 fitted in site 1, SMT362 fitted in site 2 with RSL loopback connector on each RSL connector. Comport connection T1C0 T2C3

Input clock test

Fit a cable between the bottom connectors to perform a loopback.
Program the SMT362 with the SMT6001 (SMT395 is added as a bypass of 38 bits) with the firmware
$/SMT362/Manufacture/Tests/rsl_clock_test/synthesis/clock_test.bit

Reset the board. 4 LEDs should flash synchronised. Each corresponds to a clock input.
If they don't flash or not at the same pace check the clock circuitry.

Bottom RSL test

Program using the SMT6001 the firmware with the following bitstream:
SS \SMT362\Manufacture\Tests\firmwares_for_test\rsl_bert_x4_refclk1_bot_362.bit
Run the following application
SS\SMT362\Manufacture\Tests\rsl_bert_test\short_test\ bert.app
It tests both direction of a link. A=>B and B=>A. Both results have to be checked.

The things to look for are:

1. Link detect is set to 1
2. BER is good i.e. Error =0 over large number of frames.

As it is a loopback B=>A test is connector A test (A is on the right i.e. connector RIR).
As it is a loopback A=>B test is connector B test (B is on the left i.e. connector RIQ)

Run the test for each lane, checking each direction. The test runs indefinitely.

Top RSL test

Program using the SMT6001 the firmware with the following bitstream:
SS \SMT362\Manufacture\Tests\firmwares_for_test\rsl_bert_x4_refclk1_top_362.bit
Run the following application
SS\SMT362\Manufacture\Tests\rsl_bert_test\short_test\ bert.app
It tests both direction of a link. A=>B and B=>A. Both results have to be checked.

The things to look for are:

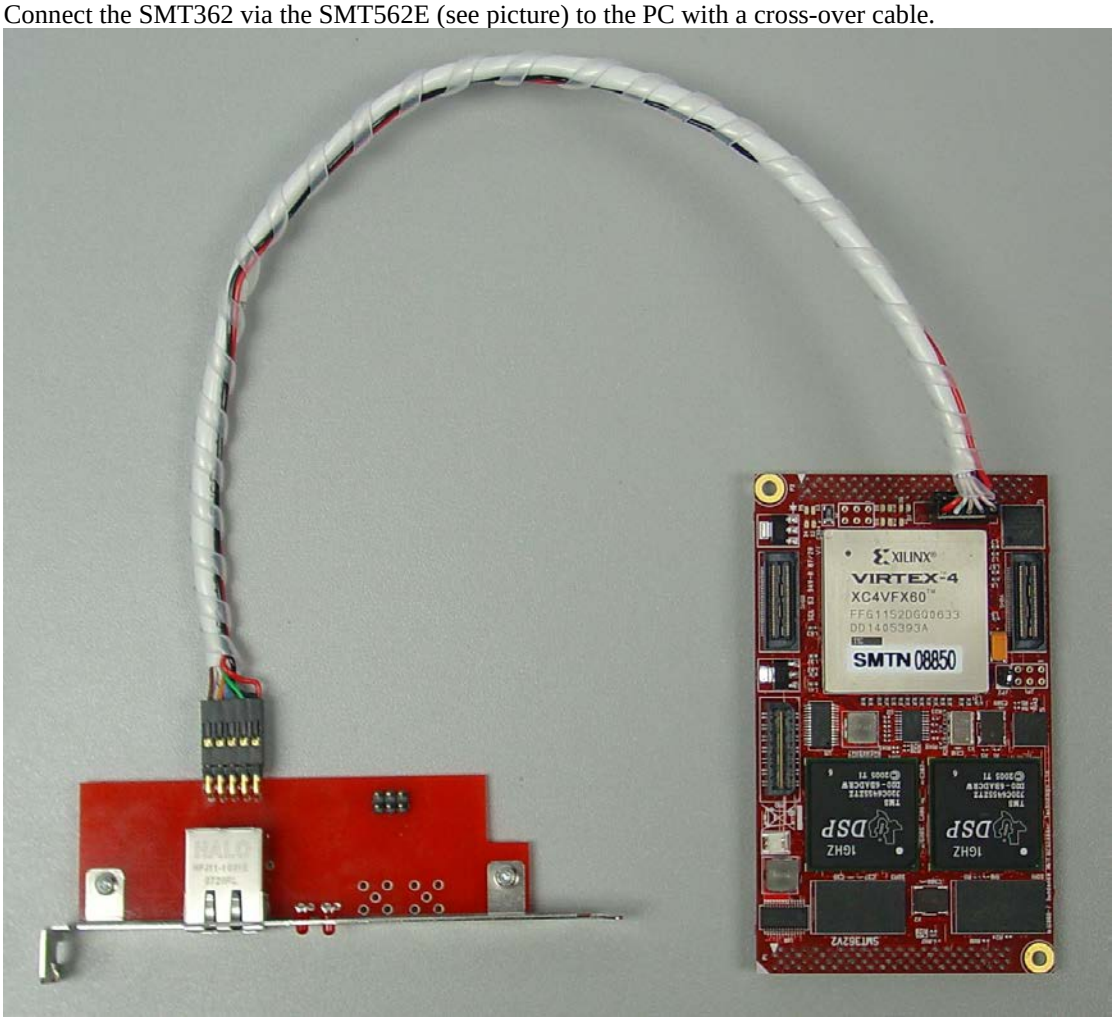
3. Link detect is set to 1
4. BER is good i.e. Error =0 over large number of frames.

As it is a loopback B=>A test is connector A test (A is on the right i.e. connector RIO).
As it is a loopback A=>B test is connector B test (B is on the left but on the bottom i.e. connector RIQ)

Run the test for each lane, checking each direction. The test runs indefinitely.

Ethernet ping test (For boards with RJ1 fitted)

Program the SMT362 with firmware 1.1 available in
$/Firmware/FPGA/synthesis/SMT362_FX60/smt362_fx60_V1_1.bit
In the control panel -> network connection list right click ans select properties of the pc ethernet card.
In the list of items highlight "Internet protocol (TCP/IP)" then click on properties.
Select the dot in front of "Use the following IP address"
In IP address type 192.168.0.12 and subnet mask should be 255.255.255.0
Press ok and exit.
Connect the SMT362 via the SMT562E (see picture) to the PC with a cross-over cable.



If you have the icon on the bottom right of the screen you should
already see that the local area connection gets detected and the speed should be 1Gbps if your PC supports it.
You can see that information in the control panel -> network connection -> status window too.
Then open the SMT362 with ccs and run the file
$/SMT362/Manufacture/Tests/emac/ping_test/debug/c6455_emac_echo.out
This should detect the link and wait for data to respond to.
Now on the PC run the application $/SMT362/Manufacture/Tests/emac/ping_test/ping_test.bat
For the test to be successful two things should be checked:
1. The dsp should now displayed that it has received 4 packets and responded to them. ("Packets echoed = 4")
2. The PC should have received replied to the ping request sent without loss.
("Packets: Sent = 4, Received = 4, Lost = 0 (0% loss)")

Interpretation of results

The test will display error message or hang if they fail.