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Product Specification for EMC^3

PC/104 Form-Factor Carrier for AMD's KRIA SoM

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Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	16/05/22	SM
1.1	Update to match last version	03/01/23	FC

Table of Contents

1 Introduction

The EMC³ is a carrier card designed to be populated with AMD's K26 SoM and is PCIe/104 *"OneBank"* compatible. The EMC³ is both a development platform and deployment solution for embedded AI and Vision applications targeted towards embedded HW & SW developers.

EMC³ can be used as a complete stand-alone solution or be part of a stack of PC/104 boards.

The image processing input available on the EMC³ includes x4 MIPI camera interfaces with an OnSemi Image Signal Processor per two MIPI cameras. In addition, there are x4 Raspberry Pi camera interfaces and x2 USB camera connectors.

Two 1Gb Ethernet ports provide high-speed connectivity, x1 PCIe Gen3 connections through the *"OneBank"* connector, x1 PCIe Gen3 available through the Samtec High-Speed connector and PCIe Gen2 connectivity through the mini PCIe connector.

Low-speed connections are available over the CAN interface and the GPIO. Wireless connectivity is available through the on-board WiFi module. Additional peripherals are available via the Mini-PCIe expansion socket, such as LoRaWAN, 5G or ADC/DAC modules.

Extensive data storage options are available through the connection of a SATA drive through the SATA connector on the EMC³.

The primary purpose of this document is to aid in the basic understanding of the EMC³ populated with the K26 SoM.

More details will be provided with the User Guide, BSP, etc. All will be provided on a GitHub of Sundance.

2 Related Documents

Ref #1

EMC³ compliance matrix:
Compliance Matrix Sundance v1.0 EMC3_HW Requirement Specification.xlsx

3 Acronyms, Abbreviations and Definitions

ADC	Analogue to Digital Converter
CAN	Controller Area Network
COTS	Commercial Off the Shelf
DAC	Digital to Analogue Converter
DH	Data Handling
ECC	Error-correcting code
EIA	Electronic Industries Alliance
EMC³	Carrier card only
EMC³-K26	Carrier card populated with the KRIA K26 SOM
FPGA	Field Programmable Gate Array
GigE	Gigabit Ethernet
GTH	Gigabit Transceiver up to 12.5Gb/s
GTR	Gigabit Transceiver up to 6Gb/s
HP	Zynq I/O bank, 1.8Vmax
HR	Zynq I/O bank, 3.3Vmax
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
ISO	International Organization for Standardisation
ISP	Image Signal Processor
JTAG	Joint Test Action Group
LVDS	Low Voltage Differential Serial
MDIO	Management Data Input/Output
MEM	Memory
MEMS	Micro Electro-mechanical Systems
MOBC	Main On-Board Computer
MPSoC	Multi-Processor System on Chip
MPU	Main Processor Unit
NRZ	Non-Return to Zero
NVMe	Non-volatile memory express
OneBank	Specific PC/104 format standard
PC/104	Industry Standard Stackable form-factor
PCB	Printed Circuit Board
PIU	Payload Interface Unit
PL	Programmable Logic
PS	Processor System
RF	Radio Frequency
RS	Recommended Standard
RS	Reed Solomon, error-correcting codes
RZ	Return to Zero
SATA	Serial AT Attachment
SDR	Shrunk Delta Ribbon
SGMII	Serial Gigabit Media Independent Interface
SPI	Serial Peripheral Interface
SSD	Solid State Drive
STO	Storage
SWaP	Size, Weight and Power
TBD	To Be Determined
TSN	Time Sensitive Networking
TTL	Transistor–Transistor logic
UART	Universal Asynchronous Receiver/Transmitter
uC	Microcontroller
USB	Universal Serial bus
Zynq	AMD Zynq Ultrascale+ FPGA

4 Requirements

4.1.1 EMC³ Board Interfaces

Table 1: EMC³ Board Interfaces

Interface	Description
External Data storage*	On board direct connection to external SATA drive. SATA (3.1) Drive connection 1.5, 3.0 and 6.0Gb/s rates supported
Video Output	External display connection via DisplayPort 1.2a (1 lane) resolution up to 1920 x1080 @ 60FPS
USB 3.0	x2 USB3.0 Type-C ports providing USB camera-capable inputs
Wired network connectivity	1Gb Ethernet over Harting ix Industrial ethernet connector connected to the PS 1Gb Ethernet over Harting ix Industrial ethernet connector connected to the PL
Wireless network connectivity	Microchip WiFi module, 802.11 b/g/n
JTAG / UART	Integrated JTAG and device UART interface via USB2.0. Micro-USB connector
Industrial Interface	ISO 11898-1 CAN 2.0A and CAN2.0B, CANBUS
Raspberry Pi Camera Interfaces	x4 Raspberry Pi (22 pin at 4 lane MIPI) connector
IAS Camera Interfaces with OnSemi ISP	x4 MIPI camera inputs (at 3 lanes MIPI) configured with x2 camera inputs per OnSemi ISP.
PCIe/104 connectivity	EMC³ is a CPU board with connectivity to one or more peripheral boards. Connectivity is through the “OneBank” connector
High density connector	SAMTEC SS4 - 60 pin high density connector with GPIO and x1 PCIe Gen3 interface. Compatible with SE50 (PolarFire MiniPCIe Module
Mini PCIe	x1 PCI Express (with SMBus), x1 USB 2.0
Form Factor	90mm x 96mm “SpaceCube” & PCIe/104 “OneBank” compatible
Power consumption	<20W, depending on KRIA performance
Operating voltage	Variable, from 12V
Total mass	<350g, excluding the KRIA Module and heat-sinks/fans

*high speed switch to select either option

4.1.2 KRIA SOM Interfaces

Table 2: SOM interfaces

Interface	Physical Location	Linked Subsystem	Functional description
QSPI	MIO bank 500 MIO[5..0]	PS	SOM QSPI memory
SD0	MIO bank 500 MIO[13..23]	PS	SOM eMMC memory, MIO[13..22] = eMMC, MIO[23] = reset
SD1	MIO bank 500 MIO[39..51]	PS	Micro SD card
I2C0	EMIO	PL	OneBank SMB
I2C1	MIO bank 500 [MIO 24..25]	PS	SOM power management, EEPROM
SPI0	EMIO	PL	WiFi module
SPI1	MIO bank 500 MIO[11..9], MIO[6]	PS	Isolated SPI interface for TPM 2.0 security module
Power management	MIO bank 501 MIO[34:32]	PS	Fixed PMU SOM based power management
	MIO bank 501 MIO[31]. MIO[35]	PS	MIO35_WD_OUT and MIO31_SHUTDOWN: Optional power management control signals for use by CC designer
MIO User Defined I/O	MIO bank 501 MIO[30:26], MIO[51:38]	PS	19 user-defined multiplexed CPU connected I/O pins
MIO User Defined I/O	MIO Bank 502 MIO[77:52]	PS	26 user-defined multiplexed CPU connected I/O pins
DDR memory controller	MIO bank 504	PS	SOM DDR4 memory
HDA	HDIO bank 45	PS	21 user-defined high-density input/output pins
HDB	HDIO bank 43	PS	24 user-defined high-density input/output pins
HDC	HDIO bank 44	PS	24 user-defined high-density input/output pins
HPA	HPIO bank 66 HPA[00..04]	PL	IAS MIPI interface HPA00_CC = MIPI clock, HPA[01..04] = MIPI data
	HPIO bank 66 HPA[05..09]	PL	IAS MIPI interface HPA05_CC = MIPI clock, HPA[06..09] = MIPI data
HPB	HPIO bank 64 HPC[00..04]	PL	Raspberry PI camera interface HPC00_CC = clock, HPC[01..04] = data
	HPIO bank 64 HPC[05..09]	PL	Raspberry PI camera interface HPC05_CC = clock, HPC[06..09] = data
	HPIO bank 64 HPC[10..14]	PL	Raspberry PI camera interface HPC10_CC = clock, HPC[11..14] = data

	HPIO bank 64 HPC[15..19]	PL	Raspberry PI camera interface HPC15_CC = clock, HPC[14..19] = data
HPC	HPIO bank 65	PL	21 user-defined high-performance input/output differential pin pairs
PS-GTR transceivers	PS GTR 505 GTR_0	PS	MINI PCIe 1 lane
PS-GTR transceiver	PS GTR 505 GTR_1	PS	USB 3.0
PS-GTR transceiver	PS GTR 505 GTR_2	PS	SATA
PS-GTR transceiver	PS GTR 505 GTR_3	PS	DisplayPort
GTH transceiver	GTH QUAD GTH_0	PL	Samtec 60 pin connector
GTH transceiver	GTH QUAD GTH_1	PL	PCIe/104 OneBank Top connector in Device mode.
GTH transceiver	GTH QUAD GTH_2	PL	PCIe/104 OneBank bottom connector in Device mode.
GTH transceiver	GTH QUAD GTH_3	PL	PCIe/104 OneBank selectable between Top and Bottom connector in Host mode.

4.1.3 MIO Banks

Pin location is fixed on Xilinx SOM

Pin location is defined on EMC3 carrier Board

Pin location is available to user

Bank Number	Interface Type	MIO	Pin label
500	QSPI	0	sclk_out
		1	miso_mo1
		2	mo2
		3	mo3
		4	mosi_mi0
		5	n_ss_out
	SPI1	6	sclk_out
	GPIO	7	LED_DS35
		8	LED_DS36
	SPI1	9	n_ss_out
		10	miso
		11	mosi
	GPIO	12	FW_UEn
	eMMC (SD0)	13	data[0]
		14	data[1]
		15	data[2]
		16	data[3]
		17	data[4]
		18	data[5]
		19	data[6]
		20	data[7]
		21	cmd_out
		22	clk_out
	GPIO	23	eMMC_Rst
	I2C1	24	scl
		25	sda
	mPCIE	26	MPCIE_WAKEN
	Display port	27	dp_aux_data_out
		28	dp_hot_plug_detect

501		29	dp_aux_data
		30	dp_aux_data_in
	PMU_GPI1	31	SHUTDOWN
	PMU_GPO2	32	FPD_Pwr_En
	PMU_GPO2	33	PL_Pwr_EN
	PMU_GPO2	34	PS_Pwr_En
	PMU_GPO1	35	WD_OUT
	UART1	36	txd
		37	rxd
	WIFI	38	EN_WIFI
	SD1	39	sdio1_data_out[4]
		40	sdio1_data_out[5]
		41	sdio1_data_out[6]
		42	
		43	SD_RESET_B
		44	
		45	
		46	sdio1_data_out[0]
		47	sdio1_data_out[1]
		48	sdio1_data_out[2]
		49	sdio1_data_out[3]
		50	sdio1_cmd_out
		51	sdio1clk_out
502	USB0	52	ulpi_clk_in
		53	ulpi_dir
		54	ulpi_tx_data[2]
		55	ulpi_nxt
		56	ulpi_tx_data[0]
		57	ulpi_tx_data[1]
		58	ulpi_stp
		59	ulpi_tx_data[3]
		60	ulpi_tx_data[4]
		61	ulpi_tx_data[5]
		62	ulpi_tx_data[6]
		63	ulpi_tx_data[7]

	PS Ethernet GEM3	64	rgmii_tx_clk
		65	rgmii_txd[0]
		66	rgmii_txd[1]
		67	rgmii_txd[2]
		68	rgmii_txd[3]
		69	rgmii_txd[0]
		70	rgmii_rx_clk
		71	rgmii_rxd[0]
		72	rgmii_rxd[1]
		73	rgmii_rxd[2]
		74	rgmii_rxd[3]
		75	rgmii_rxd_ctl
		76	USB_PHY_RESET_B
	CAN0	77	mioclk

4.1.4 Environmental

Operating temperature	-40 to +80ºC	
Survivable temperature	-45 to +80 ºC	
Sinusoidal Vibration Low	5-100Hz @ 2.5g	
Sinusoidal Vibration High	100-140 Hz @ 1.25g	
Vibration	8.03g RMS Vibration	
Shock Test	[30Hz@5g],[100Hz@100g],[700Hz@1500g],[1000Hz@2400g],[1500Hz@4000g],[5000Hz@4000g],[10000Hz@2000g] TBC	
Heated Vacuum Test	Pressurised to 1e-05 mbar, -→ 3.5e-03 mbar and heated to 60C for thermal hotspot verification TBC	

5 Board Description

The EMC³ carrier when populated with the KRIA SOM provides a completed embedded system targeted towards robotics and vison processing. The EMC³ carrier card allows up to eight cameras connected via MIPI interfaces in addition to two USB3.0 Type-C camera inputs. These consist of x4 IAS camera interfaces which incorporate an OnSemi image processor per two inputs and x4 Raspberry Pi (22 pin) camera inputs.

The Zynq Ultracscale+ MPSoC provides AI Inference at lower power with low latency, vision processing applications can be implemented within the FPGA fabric or within the processor.

The EMC³ is equipped with high-speed connectivity allowing fast transfer of raw data or the results of AI inference and vision processing. The SE50 interface incorporates a 60pin Samtec connector capable of PCIe Gen3 data transfers. The EMC³ carrier complies with PCIe/104 standards allowing interfacing to peripheral boards through the OneBank connector either Top mounting or bottom mounting utilising the x1 PCIe Gen3 lanes. Two wired ethernet connection at 1 Gb also facilitate in data transfer, with one connection to the PS and the other to the PL. The ethernet connection to the PL enables industrial ethernet control such Real-Time networking interfaces and Time Sensitive Networking (TSN).

Large data storage is available by using an external SSD via an onboard SATA connector.

Wireless connectivity is supplied via a 802.11 b/g/n WiFi module.

The mini PCIe connector allows the connection of additional peripheral cards.

The EMC³ is defined a PCIe/104 processor which can sit at either the Top or Bottom of the stack. When the EMC³ is configured as a HOST power is applied via the DC input with a range between 8.5V and 36V. Connections to peripheral boards are achieved through the OneBank connection either stacking up or down.

The EMC³ can also function as a peripheral board which requires external powering.

5.1 Clock Generator

The Texas Instruments SN65LVDS108DBTR clock generator can provide up to 8 clocks at 100MHz differential. The clocks are used the EMC³ in the following configuration.

5.1.1 Clock Generator: Differential Clock Outputs

The EMC3 provides 8 differential clock outputs at 100Mhz using the HCSL standard. The clocks are generated using the 9FGV0841 which uses a 25Mhz as the input frequency. The generator is configured to start generating the 100Mhz clocks on power-up and also has the ability for re-configuration via an I2C slave interface.

An addition differential clock is provided by a fixed frequency MEMS oscillator generating 125MHz for the SATA connection.

Table 3: 100Mhz Differential Clock Outputs

Clock Output	Speed	Connection
DIF0	100MHz	OneBank Top PCIe Slotclock
DIF1	100MHz	OneBank Bottom PCIe Slotclock
DIF2	100MHz	Razor Beam PCIe Slotclock
DIF3	100MHz	GTH0 reference clock
DIF4	100MHz	GTH1 reference clock
DIF5	100MHz	GTR0 reference clock
DIF6	100MHz	MPCIE reference clock
DIF7	100Mhz	N/C

5.1.2 Clock Generator: Single Ended Clock Outputs

The single ended clock outputs are provided by the factory programmable Skyworks Si5350A-B clock generator. The clock outputs are listed in the following table.

Table 4: Single Ended Clock Outputs

Clock Output	Speed	Connection
CLK0	24MHz	ISP0_EXTCLK
CLK1	24MHz	ISP1_EXTCLK
CLK2	25MHz	HPC_CLK0_P
CLK3	25MHz	PL_ETH_PHY_CLK
CLK4	25MHz	PL_ETH_PHY_CLK
CLK5	24MHz	USB_HUB_REFCLK_25MHZ
CLK6	100MHz	
CLK7	24MHz	

5.2 I2C Bus interface

The EMC³ utilises separate I2C for the platform management and camera control, the bus for platform management is connected to the PS while the I2C for camera control is connected to the PL.

5.2.1 I2C1: Platform management

The KRIA SOM hosts a SOM I2C platform management bus for interfacing with supporting peripherals. The devices are summarised in the following table. The I2C address are represented using 7-bit format.

Table 5: SOM I2C Platform Management Interface address

I2C 7-bit address	Device location	Description
0x50, 0x58	KRIA SOM	SOM EEPROM
0x30, 0x31	KRIA SOM	DA9062 PMIC
0x32	KRIA SOM	DA9130 PMIC
0x33	KRIA SOM	DA9131 PMIC
0x68	KRIA SOM	PL power domain monitor
0x70	KRIA SOM	PL power domain monitor
0x6A	EMC³	100MHz differential clock generator
0x51, 0x59	EMC³	EMC EEPROM
0x38	EMC³	Audio CODEC

5.2.2 I2C: Camera control and configuration

The x4 Raspberry Pi camera interfaces and the x2 OnSemi image processors are connected through the I2C MUX switch PCA9847PWJ. The switch is connected to an I2C core in the PL The 7-bit address I2C for the MUX switch is 0x71.

Table 6: Camera I2C MUX connections

KRIA SoM Signal	MUX Signal
HDA13	SCL
HDA14	SDA

5.3 Reset

5.3.1 Power-On-Reset

1. The SOM reset signal (PS_POR_L) is held in reset until the CC_PS_GOOD signal is asserted on the carrier.
2. All the PS and PL I/O device reset signals on the carrier are held in reset until 25ms after the PS and PL power domain are powered up and stable.
3. A hard reset is performed by momentarily connecting the power-on pin.

5.3.2 KRIA SoM reset pins

KRIA SoM Signal	Reset Signal
MIO43	SD_RESET_B
MIO76	USB_PHY_RESET_B
HPC11_P	USB_HUB_RESET_B
HPC11_N	PS_ETH_RESET_B
HPC12_P	MPCIE_RST_B
HPC12_N	USB_PHY_RESET_B
HPC13_P	PL_ETH_RESET_B
HPC13_N	ISP0_RESET_B
HPC14_P	ISP1_RESET_B
HPC14_N	RPI0_ENABLE
HPC15_P	RPI1_ENABLE
HPC15_N	RPI2_ENABLE
HPC16_P	RPI3_ENABLE
HPC16_N	N_RST_WIFI

6 User Configuration and settings

6.1 Power ON/OFF

The EMC³ can be configured to either start-up automatically when power is applied to the DC input or to start-up when a momentary contact switch is activated.

By selecting the Slide Switch position 1 to the ON position the EMC3 will always start-up when power is applied. When switch 1 is in the OFF position a momentary contact is required between the pins on J23. A short contact will power up the KRIA SOM, a longer contact of around 3 seconds will power down the KRIA SOM.

6.2 Host or Device configuration for PCIe/104

The EMC³ can be configured to function as either a Host or Device card while complying with PCIe/104 specification.

The ability to select between a Host or Device is accomplished by the setting switch 1 to either ON or OFF.

When the EMC³ is operating in Host mode power is required on the DC input, this power all regulators for the EMC3 and also supplies power the OneBank connections. While operating in master mode the EMC3 can either be placed at the top or bottom

of the stack. Switch position 6 specifies if the EMC³ is configured at the Top or Bottom of the stack.

When the EMC3 is selected as a Device power is not supplied through the DC input, power is taken from the OneBank connectors and used to power the regulators for the EMC3. The EMC³ will select the correct lanes for when stacking either above or below by utilising the Direction pin.

6.3 Switch Positions

Table 7: Configuration switch positions

Switch Number	Function when ON	Function when OFF
1	Auto Power-On enabled	Auto Power-On disabled
2	EMC³ functions as a HOST	EMC³ functions as a DEVICE
3	MODE 1 Enable[1]	MODE 1 Disable[1]
4	MODE 2 Enable[1]	MODE 2 Enable[1]
5	MODE 3 Enable[1]	MODE 3 Enable[1]
6	Host configured for TOP stack	Host configured for BOTTOM stack

[1] See JTAG Boot Mode Configuration for switch positions

6.4 JTAG Boot Mode Configurations

Table 8: Boot Mode Configurations

Boot Mode	MODE 1	MODE 2	MODE 3
JTAG	0	0	0
QSPI (32 bit)	0	0	1
eMMC	0	1	1
SD Card	1	1	1

7 Block Diagram

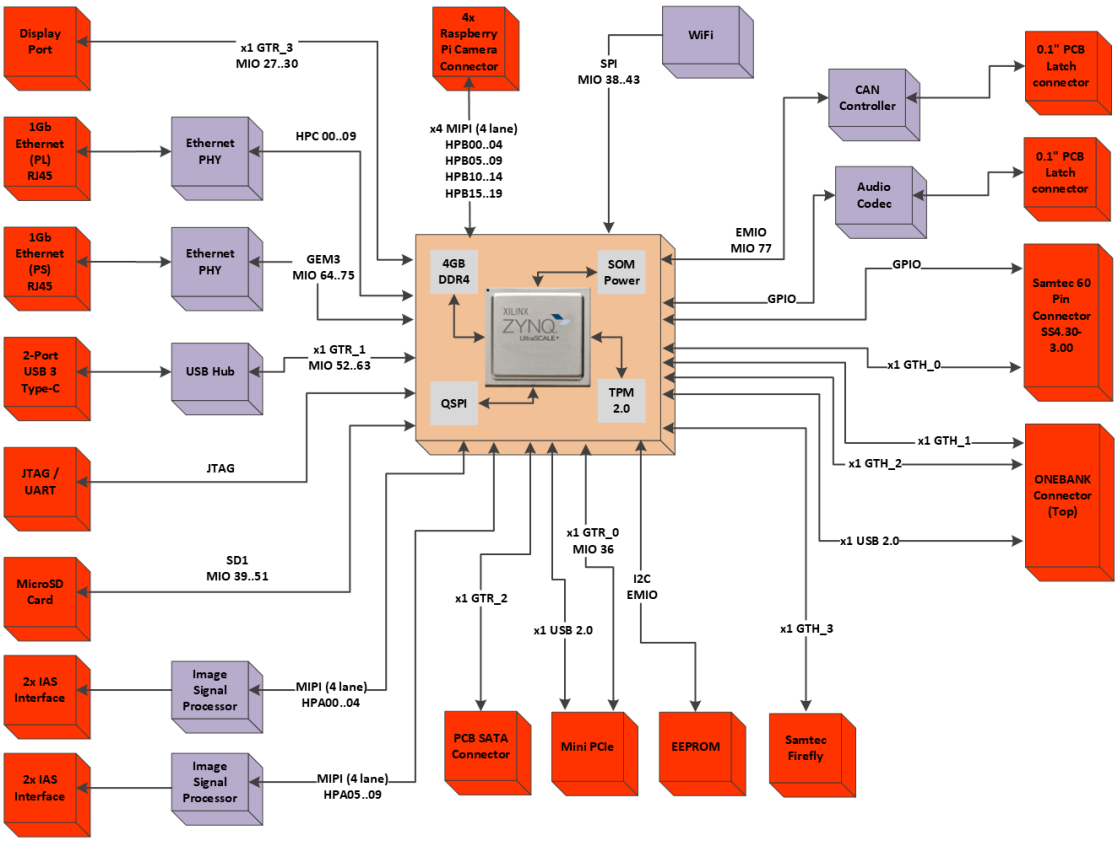

Figure 1: EMC³ Block Diagram

8 Circuit Description

When the EMC³ carrier card is populated with the KRIA K26 SOM the system is referred to the EMC³-K26.

The KRIA K26 SOM utilises the Zynq Ultrascale+ MPSoC which contains memory and an integrated power solution. High speed interfaces to the Zynq Ultrascale+ MPSoC are available through the carrier card.

The following interface descriptions are available on the EMC³-K26.

8.1 KRIA K26 System-on-Module

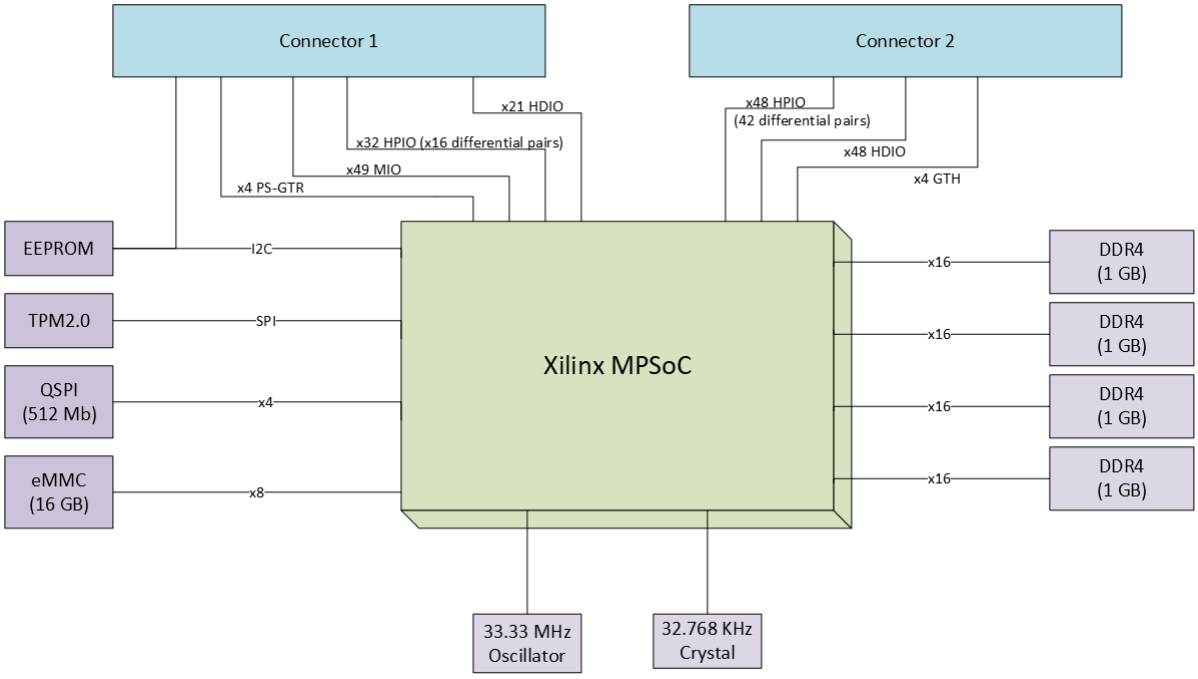

Figure 2: Block Diagram of the KRIA SOM

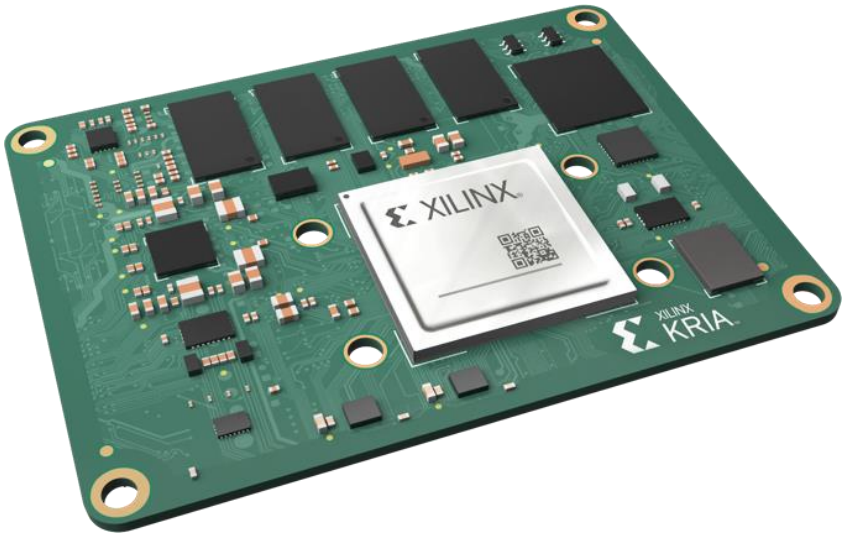

Figure 3: KRIA K26 SOM

8.1.1 DDR4 RAM

The Zynq PS is directly connected to DDR4 RAM. The capacity of each memory is 4GB and organised as 64-bit non-ECC.

8.1.2 Embedded Multimedia Card

Populated on the K26 SOM is a 16GB eMMC which provides sufficient storage for applications running on the MPSoC.

8.1.3 QSPI

The SOM contains a 512Mb QSPI devices which will run the fist stage bootloader, this insures fast configuration of the MPSoC and peripherals prior to the second stage bootloader provided by either the eMMC or SD Card.

8.1.4 Zynq MPSoC Local Clock

A 33.33 MHz oscillator is provided as a PS reference clock, this is a fixed frequency part.

8.2 EMC³ Power Supplies

The EMC³ is fitted with a 2.5mm DC jack connector with an input voltage range of 8.5V to 36V. The EMC³ input voltage rail in equipped with a voltage controller protecting against a variety of system faults such as reverse current, reverse voltage, overcurrent, overvoltage/undervoltage and overtemperature conditions.

A switching-step-down regulator supplies the KRIA SOM with a 5V supply (V_{CC_SOM}), once the 5V regulator is within the specified range a power-good is asserted and POWER_OFF_C2M_L signal is deserted.

The EMC³ provides voltage rails for the PS and PL with power good indication for each. After the KRIA SOM onboard power sequencing is complete the $V_{CCOEN\_PS\_M2C}$ and $V_{CCOEN\_PL\_M2C}$ signal are enabled by the SOM. The PS is supplied with 1.2V, 1.8V and 3.3V. The PL is supplied with 1.2V,1.8V, 3.3V and 2.75V. The Gigabit Ethernet PHY device is supplied with 1.0V and 2.5V.

8.3 Zynq Configuration

The KRIA SoM utilise both a primary and secondary boot device, this allows the isolation from the platform specific boot firmware and the application development. The primary boot device is the QSPI memory located on the KRIA SOM while the secondary boot device can be either the eMMC memory located on the KRIA SOM or the SD card located on the EMC³.

The primary boot device (QSPI) contains all necessary the elements packaged in a specific file format and file captured as BOOT.BIN, these elements are:

- FSBL: First-stage boot loader
- PMU: Platform management unit firmware
- ATF: Arm® trusted firmware
- U-boot: Second-stage boot loader

U-boot provides the functionality for the handoff between the first and second stage bootloader. U-boot will scan both the eMMC and SD card for second stage boot, if both are present the option to select either is presented to the user.

The second stage boot device contains the operating system and associated files which can written to either the eMMC or SD card.

The EMC³ provides different boot configurations set by switches on the board, the configurations are listed below.

8.4 External Storage Data

The EMC³ has the option of connecting a SATA drive.

Table 9: SATA drive pinouts

KRIA SOM PIN	SATA Drive / M.2 Signals
GTR_DP2_M2C_P	A+ (Transmit +)
GTR_DP2_M2C_N	A- (Transmit -)
GTR_DP2_C2M_P	B+ (Receive +)
GTR_DP2_C2M_N	B- (Receive -)

8.5 Video Output

Video output is available on the EMC³ though an onboard DisplayPort interface. The DisplayPort utilises a single GTR transceiver TX lines which provides resolution up to 1920 x 1080 at 60FPS.

Table 10: Video output pinouts

KRIA SOM PIN	Display data signals
GTR_DP3_M2C_P	ML_Lane 0 (p)
GTR_DP3_M2C_N	ML_Lane 0 (n)

8.6 USB3 Ports Type-C

There are two USB ports provided on the EMC[3] connected through a USB hub to one GTR transceiver pair. These USB3 ports allow the connection of USB3 devices to the KRIA SOM.

Table 11: USB3 pinouts

KRIA SOM PIN	SATA Drive / M.2 Signals
GTR_DP1_C2M_P	USB3UP_TXDM
GTR_DP1_C2M_N	USB3UP_TXDP
GTR_DP1_M2C_P	USB3UP_RXDM
GTR_DP1_M2C_N	USB3UP_RXDP

8.7 Wired network

Wired network connectivity of 1Gb is provided through a HPC pins on the KRIA SOM for the PL and MIO pins for the PS.

Table 12: PL Ethernet pinouts

KRIA SOM PIN	PL Ethernet PHY
HPC00_CCN	TX_EN/TX_CTL
HPC06P_CLK	GTX_CLK
HPC01P	TXD0
HPC01N	TXD1
HPC02P	TXD2
HPC02N	TXD3
HPC03P	MDC
HPC03N	MIO
HPC06N	RXD0
HPC07P	RXD1
HPC07N	RXD2

HPC08P	RXD3
HPC09P_CLK	RX_DV/RX_CTL
HPC08N	RX_CLK
HPC10_CCP	PL_FLF
HPC10_CCN	PS_FLF

Table 13: PS Ethernet pinouts

KRIA SOM PIN	PS Ethernet PHY
MIO69	TX_EN/TX_CTL
MIO64	GTX_CLK
MIO65	TXD0
MIO66	TXD1
MIO67	TXD2
MIO68	TXD3
MIO76	MDC
MIO77	MIO
MIO71	RXD0
MIO72	RXD1
MIO73	RXD2
MIO74	RXD3
MIO75	RX_DV/RX_CTL
MIO70	RX_CLK

8.8 Wireless network connectivity

The EMC³ is equipped with wireless capability via the onboard WiFi module, Microchip module ATWINC1500-MR210UB. A voltage level translator NXS0108BQX is required to interface with the KRIA SoMs 1.8V MIO pins.

Table 14: WiFi module pinouts

KRIA SOM PIN	Module Pin number	Module signal name
NC	1	GPIO_6
NC	2	I2C_SCL
NC	3	I2C_SDA
HDA04	4	RESET_N

HDB03	11	WAKE
HDB04	13	IRQN
NC	14	UART_TXD
HDA19	15	SPI_MOSI
HDA20	16	SPI_SSN
HDB02	17	SPI_MISO
HDB01	18	SPI_SCK
NC	19	UART_RXD
NC	21	GPIO_1
HDA18	22	CHIP_EN
NC	25	GPIO_3
NC	26	GPIO_4
NC	27	GPIO_5

8.9 JTAG / UART

A micro-USB connection to the EMC³ allows the UART serial communication to the KRIA SOM and JTAG programming/debugging.

Table 15: JTAG / UART pinouts

KRIA SOM PIN	JTAG Signal	JTAG connector pin	Description
JTAG_TMS_C2M	TMS	4	Test Mode Select
JTAG_TCK_C2M	TCK	2	Test Clock
JTAG_TDO_M2C	TDO	3	Test Data Out
JTAG_TDI_C2M	TDI	4	Test Data In

8.10 Industrial CAN interface

CAN-BUS connectivity is provided on the EMC³ via a two-pin screw terminal connector.

Table 16: CAN BUS connections to SOM

KRIA SOM PIN	CAN connections
HDA01	PHY_RX
HDA02	PHY_TX

8.11 Raspberry Pi 22-Interfaces

Up to four Raspberry Pi cameras can be connected to the EMC³ via the RPi camera 22-pin connector, Molex 0.5mm FFC/FPC. Each connector supports 4 MIPI lanes connecting directly to the Zynq Ultrascale+ MPSoC HPB bank. The alternative use of connectors will be as GPIO from the Zynq.

Table 17: Raspberry Pi camera connections to SOM

KRIA SOM PIN	Rpi camera connections	Description
HPB00_CC_P	CAM0_CK_P	Cam 0 Pixel Clock Output Form Sensor Positive
HPB00_CC_N	CAM0_CK_N	Cam 0 Pixel Clock Output Form Sensor Negaitive
HPB01_P	CAM0_D0_P	Cam 0 Pixel Data Lane0 Positive
HPB01_N	CAM0_D0_N	Cam 0 Pixel Data Lane0 Negative
HPB02_P	CAM0_D1_P	Cam 0 Pixel Data Lane1 Positive
HPB02_N	CAM0_D1_N	Cam 0 Pixel Data Lane1 Negative

HPB03_P	CAM0_D2_P	Cam 0 Pixel Data Lane2 Positive
HPB03_N	CAM0_D2_N	Cam 0 Pixel Data Lane2 Negative
HPB04_P	CAM0_D3_P	Cam 0 Pixel Data Lane3 Positive
HPB04_N	CAM0_D4_N	Cam 0 Pixel Data Lane3 Negative
HPB05_CC_P	CAM1_CK_P	Cam 1 Pixel Clock Output Form Sensor Positive
HPB05_CC_P	CAM1_CK_N	Cam 1 Pixel Clock Output Form Sensor Negaitive
HPB06_P	CAM1_D0_P	Cam 1 Pixel Data Lane0 Positive
HPB06_N	CAM1_D0_N	Cam 1 Pixel Data Lane0 Negative
HPB07_P	CAM1_D1_P	Cam 1 Pixel Data Lane1 Positive
HPB07_N	CAM1_D1_N	Cam 1 Pixel Data Lane1 Negative
HPB08_P	CAM1_D2_P	Cam 1 Pixel Data Lane2 Positive
HPB08_N	CAM1_D2_N	Cam 1 Pixel Data Lane2 Negative
HPB09_P	CAM1_D3_P	Cam 1 Pixel Data Lane3 Positive
HPB09_N	CAM1_D3_N	Cam 1 Pixel Data Lane3 Negative
HPB10_CC_P	CAM2_CK_P	Cam 2 Pixel Clock Output Form Sensor Positive
HPB10_CC_P	CAM2_CK_N	Cam 2 Pixel Clock Output Form Sensor Negaitive
HPB11_P	CAM2_D0_P	Cam 2 Pixel Data Lane0 Positive
HPB11_N	CAM2_D0_N	Cam 2 Pixel Data Lane0 Negative
HPB12_P	CAM2_D1_P	Cam 2 Pixel Data Lane1 Positive
HPB12_N	CAM2_D1_N	Cam 2 Pixel Data Lane1 Negative
HPB13_P	CAM2_D2_P	Cam 2 Pixel Data Lane2 Positive
HPB13_P	CAM2_D2_N	Cam 2 Pixel Data Lane2 Negative
HPB14_P	CAM2_D3_P	Cam 2 Pixel Data Lane3 Positive
HPB14_P	CAM2_D3_N	Cam 2 Pixel Data Lane3 Negative
HPB15_CC_P	CAM3_CK_P	Cam 3 Pixel Clock Output Form Sensor Positive
HPB15_CC_P	CAM3_CK_N	Cam 3 Pixel Clock Output Form Sensor Negaitive
HPB16_P	CAM3_D0_P	Cam 3 Pixel Data Lane0 Positive
HPB16_N	CAM3_D0_N	Cam 3 Pixel Data Lane0 Negative
HPB17_P	CAM3_D1_P	Cam 3 Pixel Data Lane1 Positive
HPB18_N	CAM3_D1_N	Cam 3 Pixel Data Lane1 Negative
HPB19_P	CAM3_D2_P	Cam 3 Pixel Data Lane2 Positive
HPB19_P	CAM3_D2_N	Cam 3 Pixel Data Lane2 Negative
HPB14_P	CAM3_D3_P	Cam 3 Pixel Data Lane3 Positive
HPB14_P	CAM2_D3_N	Cam 2 Pixel Data Lane3 Negative

8.12 IAS Camera Interfaces with ISP

The EMC³ provides two OnSemi ISPs each requiring 4-lane MIPI connections.

Table 18: OnSemi ISP connections to SOM

KRIA SOM PIN	IAS camera connections	Description
HPA00_CC_P	ISP0_CLK_DP	Clock positive
HPA00_CC_N	ISP0_CLK_DN	Clock negative
HPA01_P	ISP0_D0_DP	
HPA01_N	ISP0_D0_DN	
HPA02_P	ISP0_D1_DP	
HPA02_N	ISP0_D1_DN	
HPA03_P	ISP0_D2_DP	
HPA03_N	ISP0_D2_DN	
HPA04_P	ISP0_D3_DP	
HPA04_N	ISP0_D4_DN	
HPA05_CC_P	ISP1_CLK_DP	Clock positive
HPA05_CC_P	ISP1_CLK_DN	Clock negative
HPA06_P	ISP1_D0_DP	
HPA06_N	ISP1_D0_DN	
HPA07_P	ISP1_D1_DP	
HPA07_N	ISP1_D1_DN	
HPA08_P	IAS1_D2_DP	
HPA08_P	ISP1_D2_DN	
HPA09_P	ISP1_D3_DP	
HPA09_P	ISP1_D4_DN	

8.13 PCIe/104 connectivity via OneBank

The EMC³ is capable of configuration as either a CPU or peripheral board with connections available to other PCIe/104 boards. Connectivity is provided through the industry standard OneBank connector, which is equipped with an x1 Gen3 PCIe connection and USB2.0 connections to both the top and bottom OneBank connector, along with SMB, ATX control and power.

Top connections

KRIA SoM PIN	OneBank	Pin Description	OneBank PIn

	USB_OC	USB over-current	1
	USB_0p	USB 2.0 connection	6
	USB_0n	USB 2.0 connection	8
GTH_DP1_C2M_P	PEx1_0Tp	PCIe Transmitt positive	12
GTH_DP1_C2M_N	PEx1_0Tn	PCIe Transmitt negative	14
GTH_DP1_M2C_P	PEx1_0Rp	PCIe Receive positive	24
GTH_DP1_M2C_N	PEx1_0Rn	PCIe Receive negative	26
	PEx1_0Clkp	PCIe clock postive	36
	PEx1_0Clkn	PCIe clock neagtive	38
GPIO66	SMB_DAT	System Management Bus - Data	47
GPIO65	SMB_CLK	System Management Bus - Clock	49
GPIO64	SMB_ALERT	System Management Bus - Alert	51

Bottom connections

KRIA SoM PIN	OneBank	Pin Description	OneBank PIn
	USB_OC	USB over-current	1
	USB_0p	USB 2.0 connection	6
	USB_0n	USB 2.0 connection	8
GTH_DP2_C2M_P	PEx1_0Tp	PCIe Transmitt positive	12
GTH_DP2_C2M_N	PEx1_0Tn	PCIe Transmitt negative	14
GTH_DP2_M2C_P	PEx1_0Rp	PCIe Receive positive	24
GTH_DP2_M2C_N	PEx1_0Rn	PCIe Receive negative	26
	PEx1_0Clkp	PCIe clock postive	36
	PEx1_0Clkn	PCIe clock neagtive	38
GPIO66	SMB_DAT	System Management Bus - Data	47
GPIO65	SMB_CLK	System Management Bus - Clock	49
GPIO64	SMB_ALERT	System Management Bus - Alert	51

8.14 High density connector

A Samtec 60 pin high density connector allows a connectivity to a pair of Ultrascale+ GTH transceivers (16.3Gb/s) and GPIOs.

KRIA SoM PIN	Samtec 60-Pin extension connector	Description

GPIO67	7	GPIO0
GPIO68	9	GPIO1
GPIO69	11	GPIO2
GPIO70	13	GPIO3
GPIO71	15	GPIO4
GPIO72	17	GPIO5
GPIO73	23	GPIO6
GPIO74	25	GPIO7
HPA04_P	27	GCLK+/ GPIO8
HPA04_N	29	GCLK-/ GPIO9
GTH_DP0_M2C_P	12	PCIe_TX+
GTH_DP0_M2C_N	14	PCIe_TX-
GTH_DP0_C2M_P	18	PCIe_RX+
GTH_DP0_C2M_N	20	PCIe_RX-
GTH_REFCLK0_C2M_P	36	PCIe_REF_CLK+
GTH_REFCLK0_C2M_N	38	PCIe_ REF_CLK -

Mini PCIe connector

A PCIe edge connector on the carrier allows the connection mPCIe cards

KRIA SoM PIN	mPCIe pins	Pin name
GPIO67	1	mPCIe_WAKE
GPIO68	7	mPCIe_CLKREF
GTR_REFCLK0_C2M_N	11	mPCIe_CLK-
GTR_REFCLK0_C2M_P	13	mPCIe_CLK+
GTR_DP0_C2M_N	23	mPCIe_RX-
GTR_DP0_C2M_P	25	mPCIe_RX+
GTR_DP0_M2C_N	31	mPCIe_TX-
GTR_DP0_M2C_P	33	mPCIe_TX+
GPIO73	23	mPCIe_WDIS
GPIO74	25	mPCIe_RST
HPA04_P	30	mPCIe_SMB_CLK
HPA04_N	32	mPCIe_SMB_DAT
HDB05	20	mPCIe_W_DISSABLE1
HDB06	51	mPCIe_W_DISSABLE2N

8.15 Audio CODEC

Xilinx Audio IP core provides input and output audio.

KRIA SoM PIN	CODEC Pin	Description
HDA05	29	AUD_LRCLK
HDA06	26	AUD_ADC_SDATA
HDA07	27	AUD_DAC_SDATA
HDA08_CC	28	AUD_BCLK
HDA00_CC	2	AUD_MCLK

8.16 Fan Connector (ALT)

12V Fan Connector.

The fan is enabled by driving Zynq pin Y13 high. This connects to a DMG3406 N-channel MOSFET gate in a low-side configuration.

KRIA SoM PIN	Name	Description
HDA20	Fan Control Pin	Active high enable pin

8.17 Debug LEDs

Two green LEDs are connected to the PL and are provided as user debug indicators. They have a forward voltage of 1.9V and are driven from the 2.5V supply via a 120R resistor (giving a forward current of 5mA).

They can be disabled in the FPGA or alternatively not populated.

KRIA SOM PIN	Name	Description
HPC17_P	D11	Active high enable LED
HPC17_N	D15	Active high enable LED

8.18 PCIe

The EMC³ board can operate in both Host and Device board modes. The PCIe/104 OneBank connector provides power (+5V and +3V3), global reset and PCI express connections to the KRIA SOM. In device mode the top and bottom PCIe links are connected to separate GTH transceivers on the SOM. When in Host mode a SOM transceiver is switched between link0 and link3 determined whether mounted on the top or bottom of the stack. When either link is selected to connect the GTH line the other link is configured as pass-through.

The following diagram shows the connectivity for both Host and Device mode.

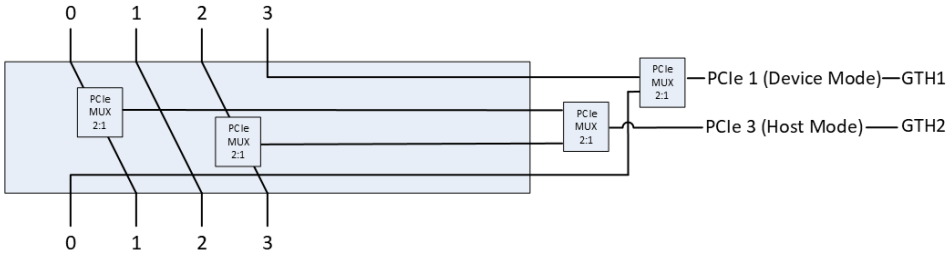

Figure 4: PCI Express Lanes in Host and Device Mode

When in Host mode the PCIe channel is switched to link0 (Top) link3 (Bottom) is configured as pass-through. When in Host mode the PCIe channel is switched to link3 (Bottom) link0 (Top) is configured as pass-through. Setting switch position 6 configures the Host for top or bottom configuration.

When in device mode the DIR (direction pin) will detect if the board is above or below the Host and switch the lanes accordingly.

8.18.1 USB

The EMC³ can provide USB in both Host and Device modes.

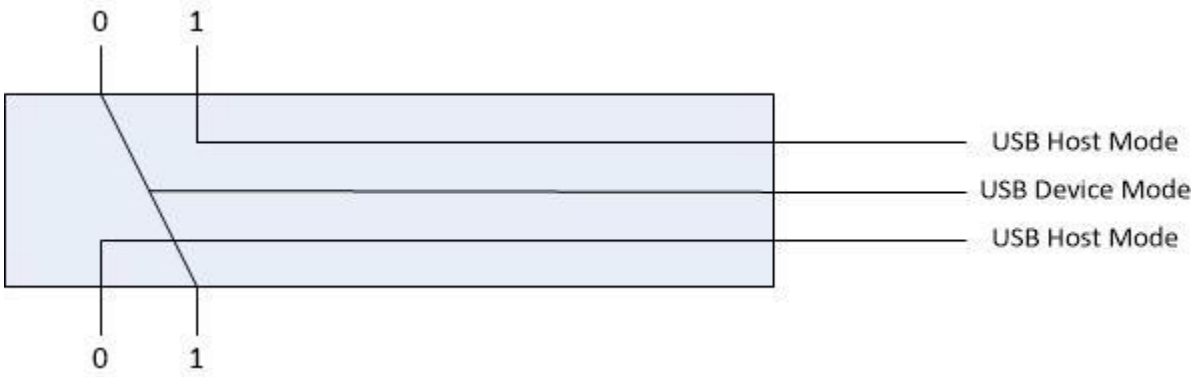

Figure 5: USB Lanes in Host and Device mode

When in Host mode the USB channels are connected to the centre channel via a USB hub, this places the USB signal lane 0 when the Host is mounted at the bottom and on lane 1 when the Host is mounted on the top.

When is device mode the DIR (direction pin) will detect if the board is above the Host and switch the lanes accordingly.

9 Samtec Razor Beam connector

The EMC³ is fitted with a 60-pin expansion connector which provides an additional PCIe to the SOM, audio connections and GPIOs.

Samtec Razor Beam Pin	Description
7	
9	
11	
13	
15	
17	
19	
23	
25	
27	UART_RXD
29	UART_TXD
31	ISP0_TRIG
33	ISP0_PWM
35	ISP1_TRIG
37	ISP1_PWM
43	RIGHT_LINE_IN
45	LEFT_LINE_IN
47	RIGHT_LINE_OUT
49	LEFT_LINE_OUT
51	
53	
55	
57	
59	
12	GTH0_TX+
14	GTH0_TX-
18	GTH0_RX+
20	GTH0_RX-
24	
26	

30	
32	
36	SAMTEC_100MHz_SLOTCLK_P
38	SAMTEC_100MHz_SLOTCLK_N
44	
46	
48	
50	
52	
54	
56	
58	

10 Verification, Review and Validation Procedures

See: https://www.sundance.com/about-sundance/iso9001-2015/

11 Board parts

11.1 EMC³ Top View

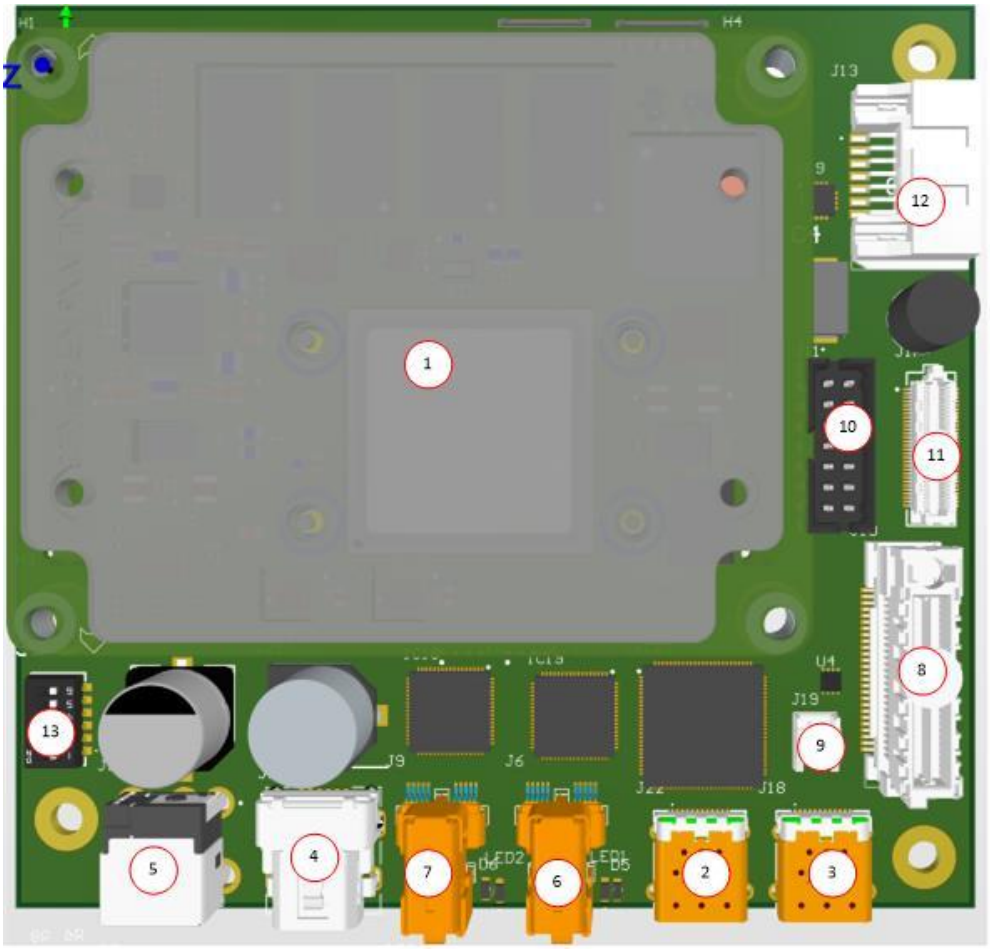

Figure 6: EMC³ PCB Top

Callout	Features / Components	Notes
1	KRIA SoM	
2	USB-C connector	
3	USB-C connector	
4	Mini HDMI	

5	2.5mm Power jack	
6	1G Ethernet connectors	Connected to the PS
7	1G Ethernet connectors	Connected to the PL
8	PCIe OneBank Top connector (22mm height)	
9	Industrial CAN connector	
10	Xilinx JTAG programmer	
11	Samtec 60-pin connector	
12	SATA connector	
13	6 position Switch	EMC³ board options

11.2 EMC³ Bottom View

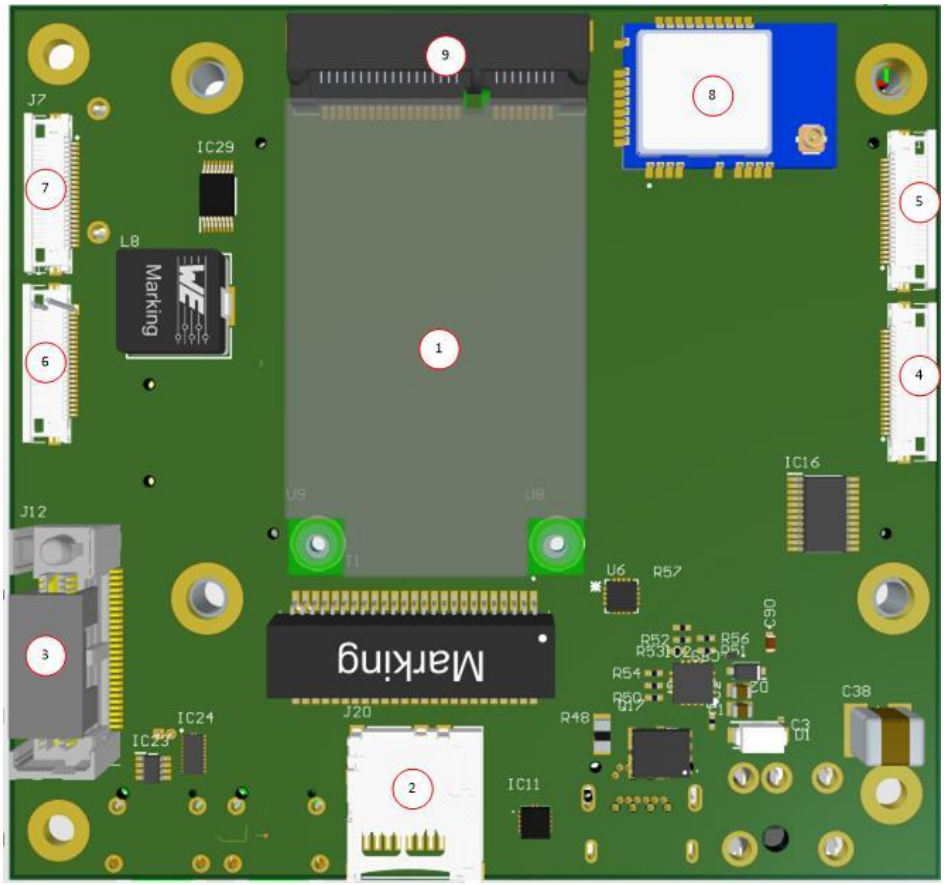

Figure 7: EMC³ PCB Bottom

Callout	Features / Components	Notes
1	Full size Mini-PCIe card	
2	SD Card	
3	OneBank bottom connector	
4	Raspberry Pi 22-pin connector	
5	Raspberry Pi 22-pin connector	
6	Raspberry Pi 22-pin connector	Connected to the PS
7	Raspberry Pi 22-pin connector	Connected to the PL
8	WiFi module	
9	Mini-PCIe connector	

12 Current & Voltage Measurement

Device	Voltage	Current (max)	Sensor	Switchable

The following table shows the power rails that are voltage monitored.

13 Physical Properties

Dimensions	90 x 96 mm	
Weight		
Supply Voltages	8.5V to 36V	
Supply Current	4 Amps	
MTBF		

14 Safety

This module presents no hazard to the user when in normal use.

15 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

16 Appendix

16.1 Host Logic selection

Table 19: Host Logic for PCIe switching

HOST_EN	DIR	SEL1	SEL2
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

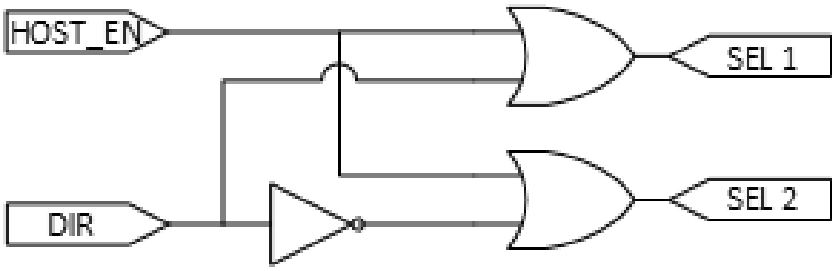

Figure 8: Logic to switch PCIe between Host and Device