AP1302_ICP3_120VFBGA_DEMO

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Rev	Who	Date	Description
Rev 0.0	Joe KK	02/14/12	Initial - Derive from AP1300_ICP2_Demo_Rev1 design
Rev 1.0	dmincinski	07/09/2013	Reassigned the Flash Pin to P20, S1_SDA to P24 and S1_SCL to P22. Added SP0 to P27 and Head_SSN to P34.
Rev 2.0	Sesha	02July2021	Based on Rev0, GPIO table in Page7 is updated with correct reset values

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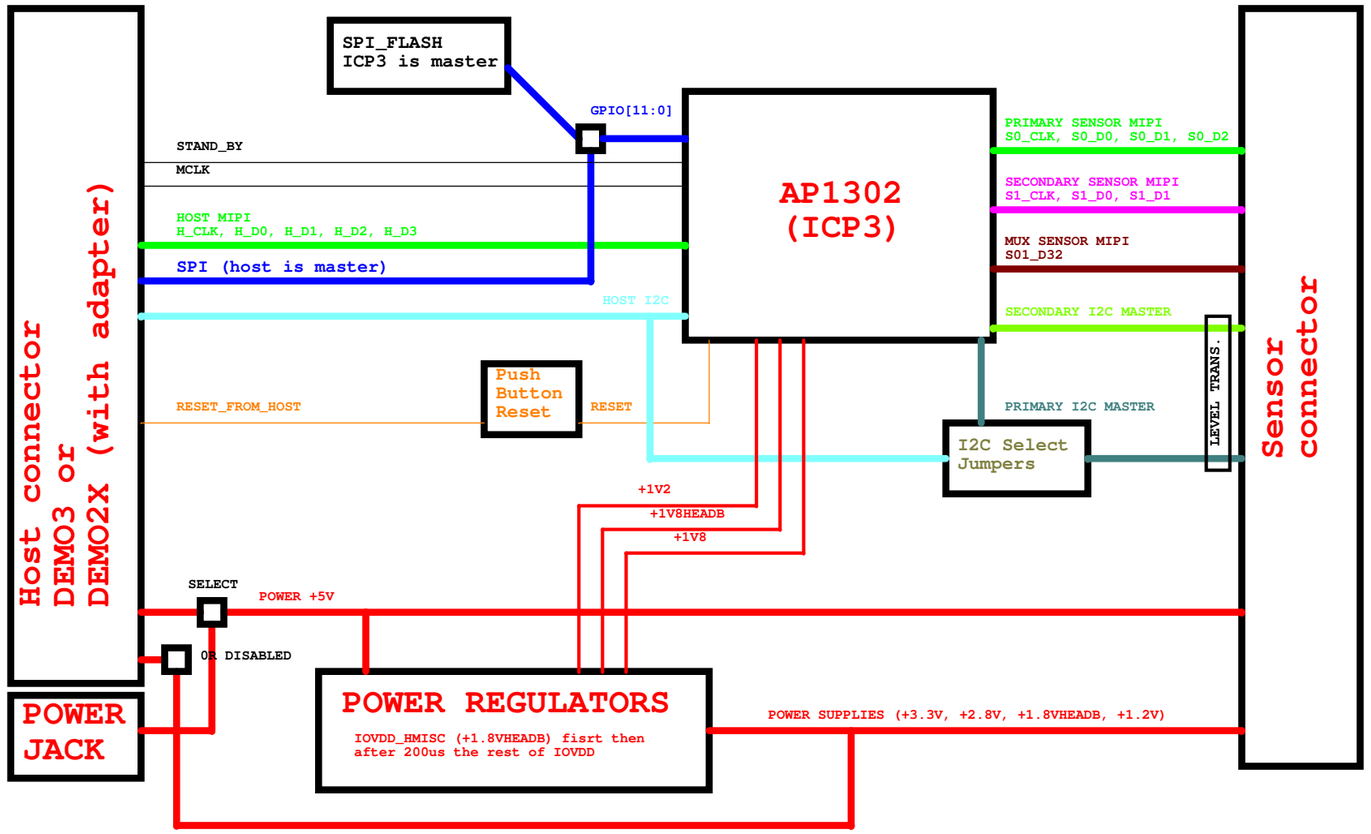
Block Diagram



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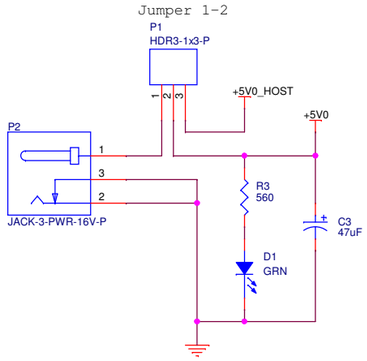
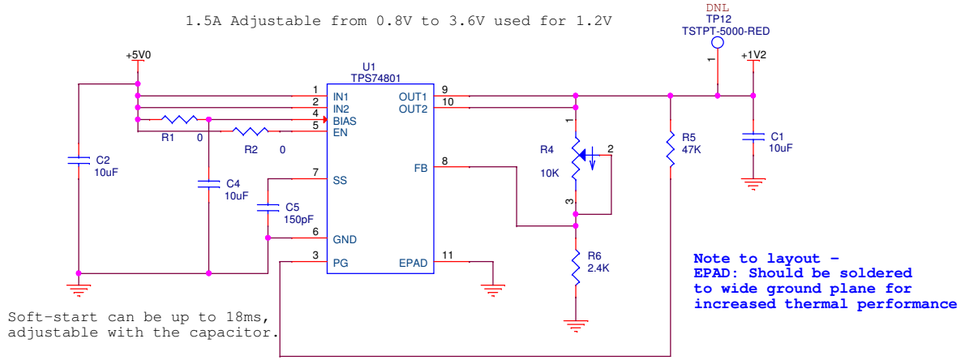
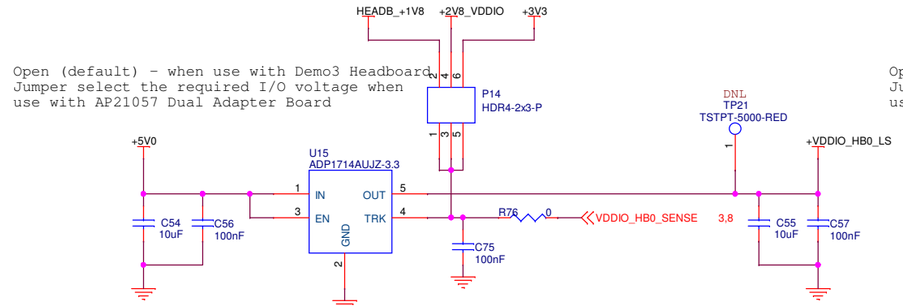
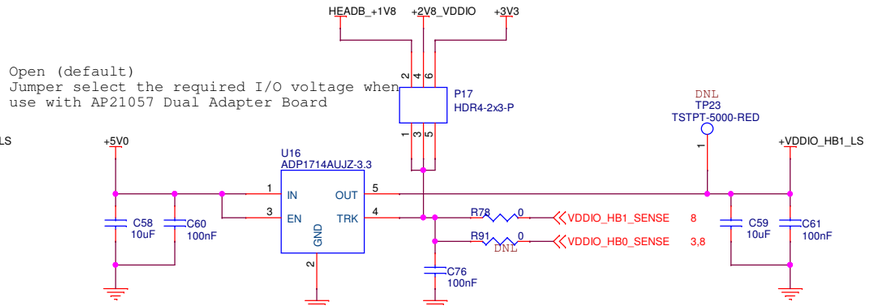
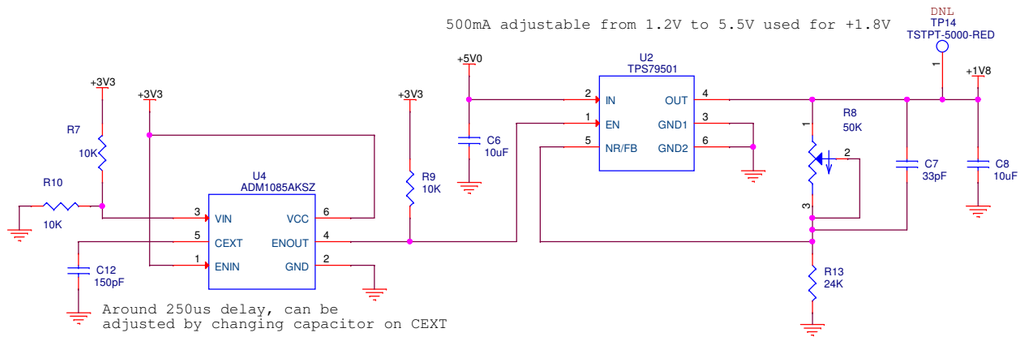
Power Supplies

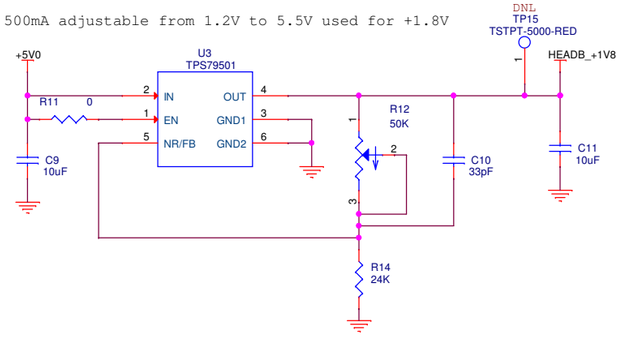


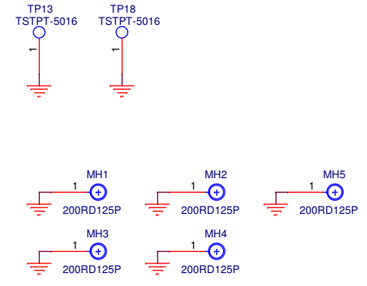


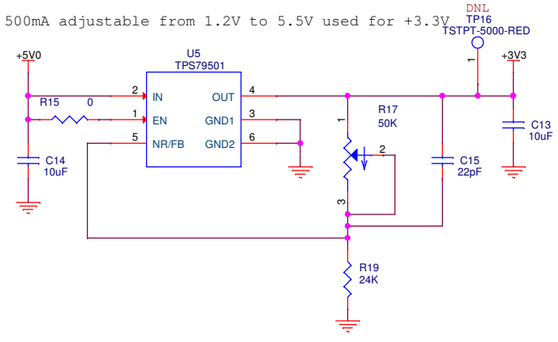


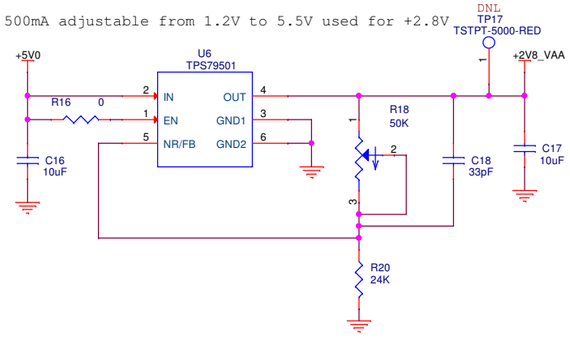


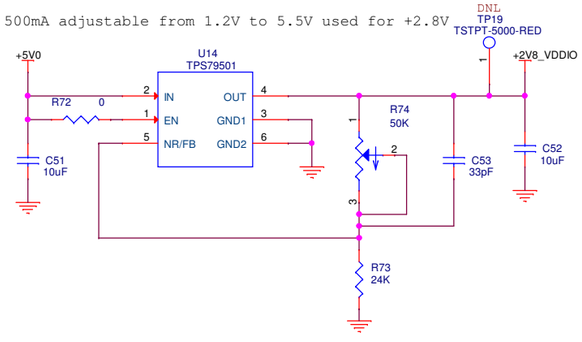


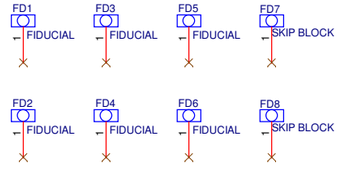


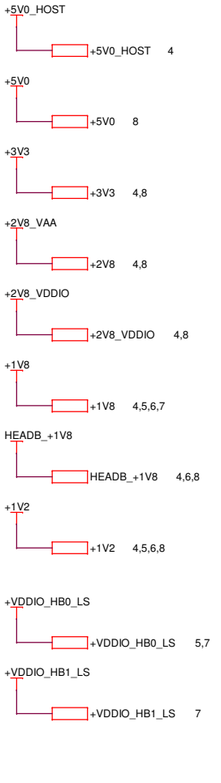












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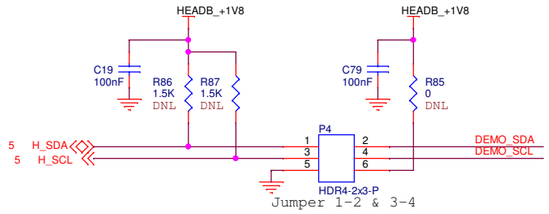
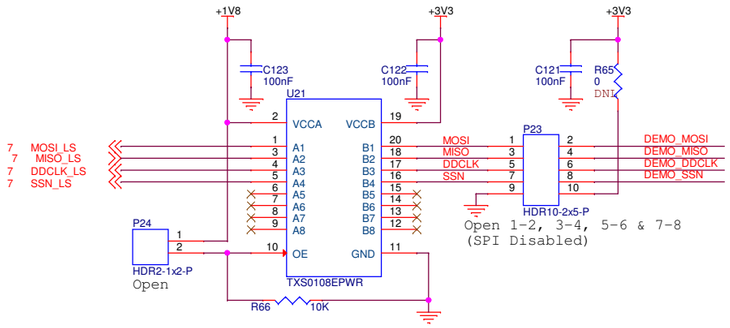
Connector to Host (Demo3 Baseboard)

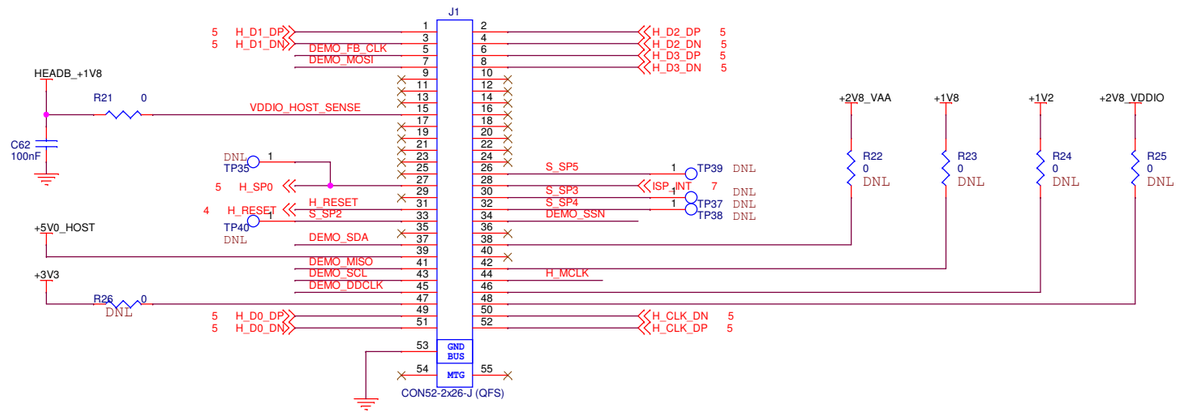
I2C DEBUG

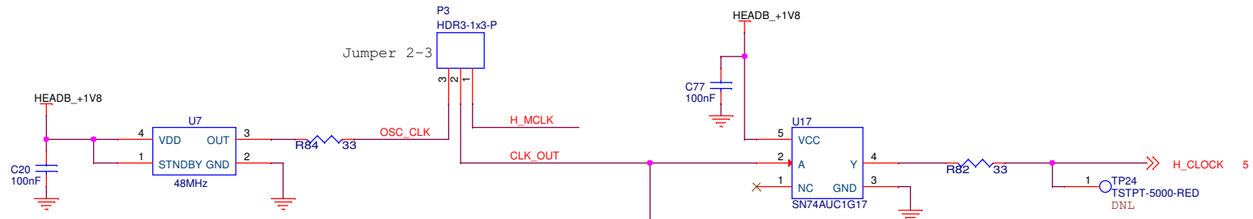


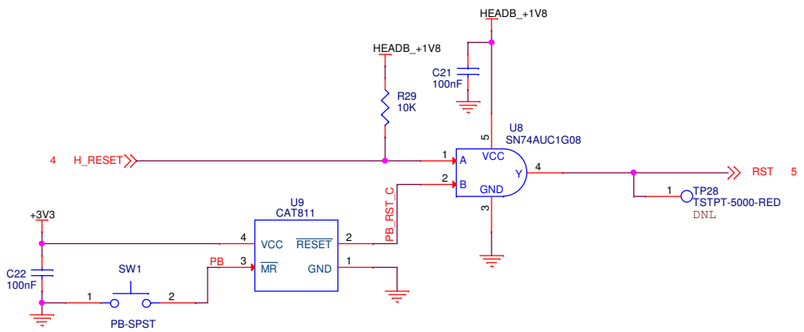
SPI DEBUG



from DEMO3 -> to ICP3







+5V0_HOST — +5V0_HOST 3

+5V0 — +5V0 3,8

+3V3 — +3V3 3,8

+2V8_VAA — +2V8 3,8

+2V8_VDDIO — +2V8_VDDIO 3,8

+1V8 — +1V8 3,5,6,7

HEADB_+1V8 — HEADB_+1V8 3,6,8

+1V2 — +1V2 3,5,6,8

+VDDIO_HB0_LS — +VDDIO_HB0_LS 3,5,7

+VDDIO_HB1_LS — +VDDIO_HB1_LS 3,7

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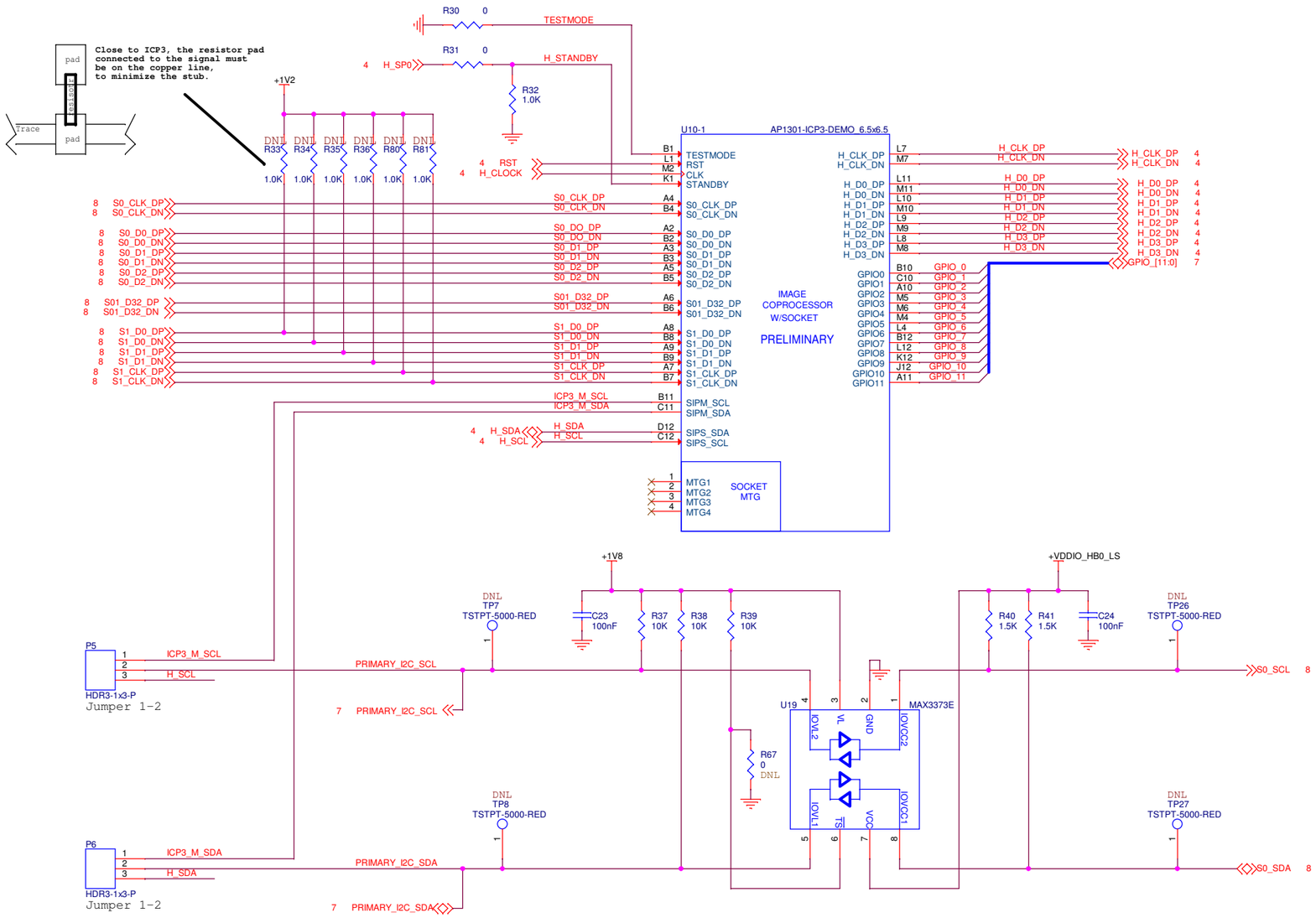
AP1302 Signals



+5V0_HOST
+5V0_HOST 3,4

+5V0
+5V0 3,8

+3V3
+3V3 3,4,8

+2V8_VAA
+2V8 3,4,8

+2V8_VDDIO
+2V8_VDDIO 3,4,8

+1V8
+1V8 3,4,6,7

HEADB_+1V8
HEADB_+1V8 3,4,6,8

+1V2
+1V2 3,4,6,8

+VDDIO_HB0_LS
+VDDIO_HB0_LS 3,7

+VDDIO_HB1_LS
+VDDIO_HB1_LS 3,7

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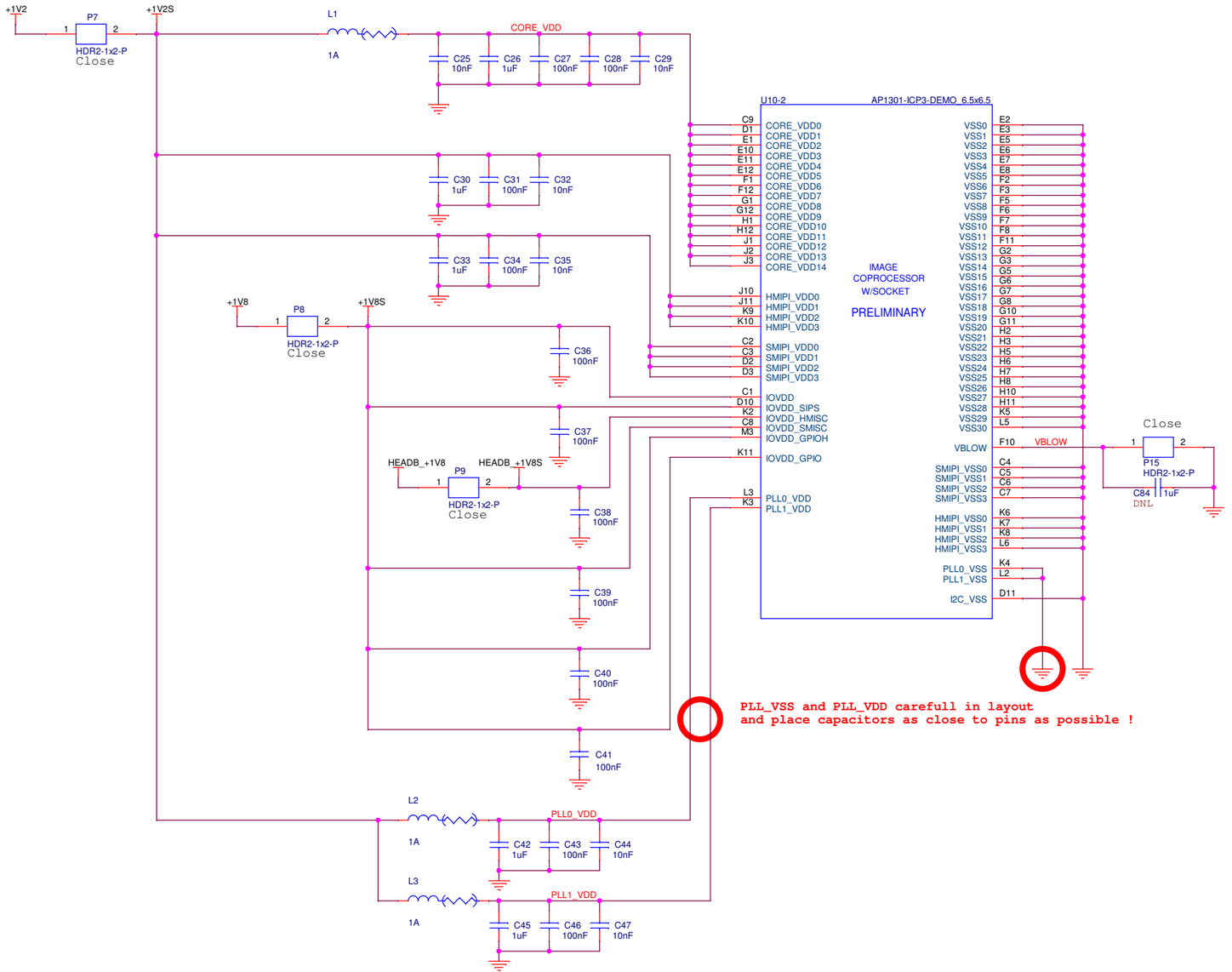
AP1302 Powers

Place the jumpers close to power supplys
and the capacitors as close to ICP2 as possible.



+5V0_HOST
+5V0_HOST 3,4

+5V0
+5V0 3,8

+3V3
+3V3 3,4,8

+2V8_VAA
+2V8 3,4,8

+2V8_VDDIO
+2V8_VDDIO 3,4,8

+1V8
+1V8 3,4,5,7

HEADB_+1V8
HEADB_+1V8 3,4,8

+1V2
+1V2 3,4,5,8

+VDDIO_HB0_LS
+VDDIO_HB0_LS 3,5,7

+VDDIO_HB1_LS
+VDDIO_HB1_LS 3,7

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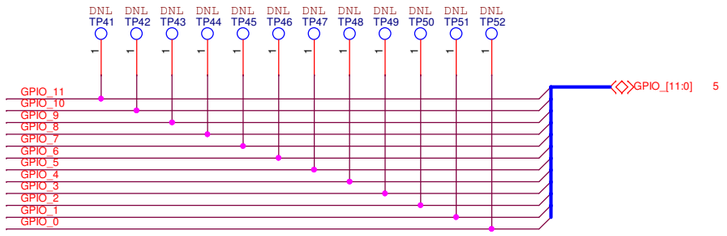
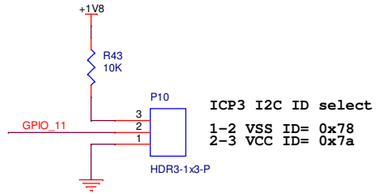
AP1302 GPIOs

ICP3 GPIO Function Mapping Table

GPIO	FUNCTION	RESET VALUE
0	SEN_CLK1	HIGH-Z
1	SHUTDOWN1	0
2	SEN_CLK2	HIGH-Z
3	SHUTDOWN2 / SPIS_CLK	HIGH-Z
4	SPIS_MISO	1
5	SPIS_MOSI / 2ND_I2C_SCL	HIGH-Z
6	SPIS_CS / 2ND_I2C_SDA	HIGH-Z
7	SPIM_CLK	1
8	SPIM_MISO	HIGH-Z
9	SPIM_MOSI	0
10	SPIM_CS	1
11	ICP3 I2C ID SELECT	HIGH-Z



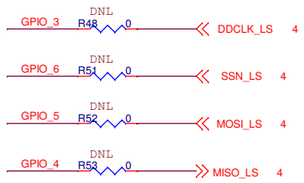
Note to layout:
Place all GPIOs 0R resistors close to ICP3

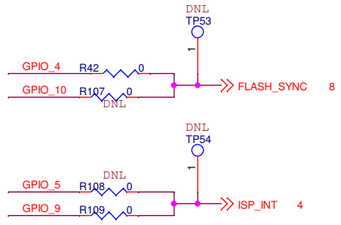


ICP3 I2C ID select

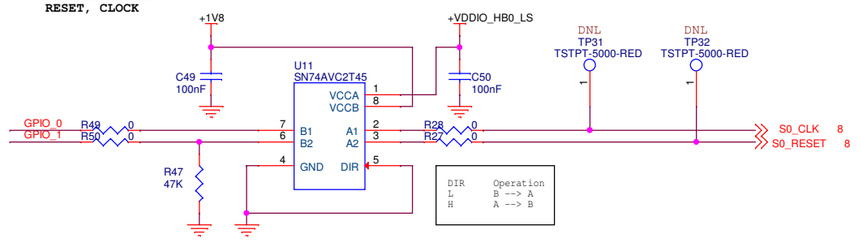
1-2 VSS ID= 0x78
2-3 VCC ID= 0x7a

SPI (ICP3 slave, host master)



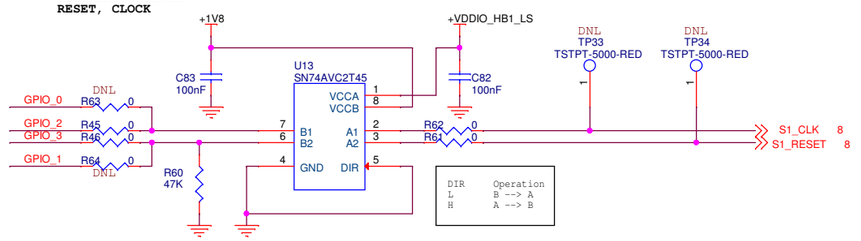


PRIMARY SENSOR
RESET, CLOCK



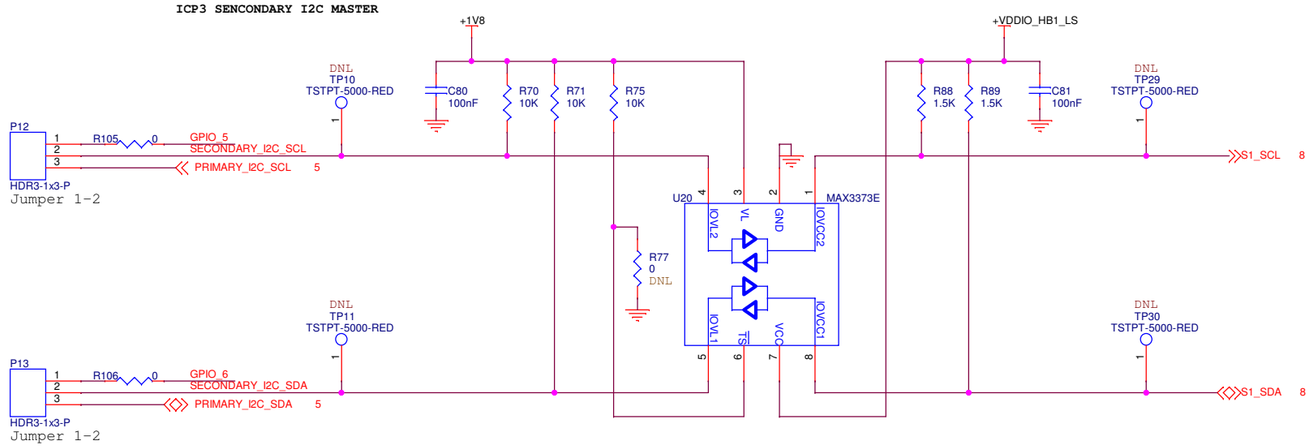
Note to layout: Place U11 and U13 close to each other to shorten GPIO_0 routing

SECONDARY SENSOR
RESET, CLOCK



ICP3 is SPI master

ICP3 SENCONDARY I2C MASTER



+5V0_HOST — +5V0_HOST 3,4
+5V0 — +5V0 3,8
+3V3 — +3V3 3,4,8
+2V8_VAA — +2V8 3,4,8
+2V8_VDDIO — +2V8_VDDIO 3,4,8
+1V8 — +1V8 3,4,5,6
HEADB_+1V8 — HEADB_+1V8 3,4,6,8
+1V2 — +1V2 3,4,5,6,8
+VDDIO_HB0_LS — +VDDIO_HB0_LS 3,5
+VDDIO_HB1_LS — +VDDIO_HB1_LS 3

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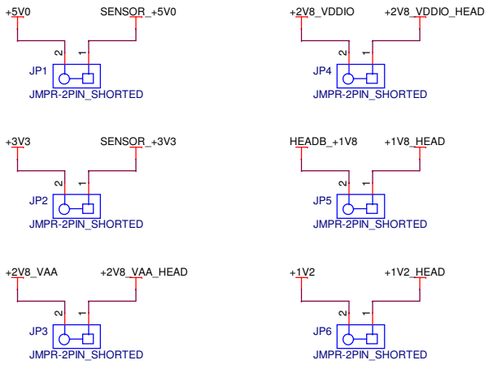
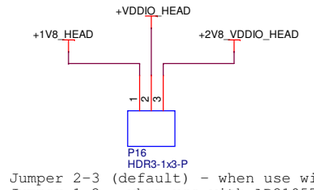
Connector to Sensors (Demo3 Headboards)



Power Debug Header: Cut away the shorted trace
and mount header for power debugging



Jumper 2-3 (default) - when use with Demo3 Headboard
Jumper 1-2 - when use with AP21057 Dual Adapter Board

+5V0_HOST — +5V0_HOST 3,4

+5V0 — +5V0 3

+3V3 — +3V3 3,4

+2V8_VAA — +2V8 3,4

+2V8_VDDIO — +2V8_VDDIO 3,4

+1V8 — +1V8 3,4,5,6,7

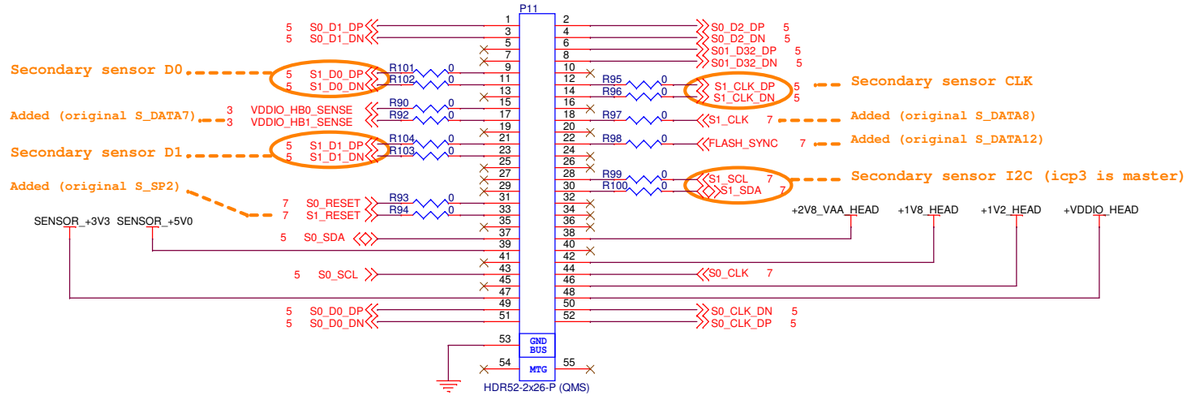
HEADB_+1V8 — HEADB_+1V8 3,4,6

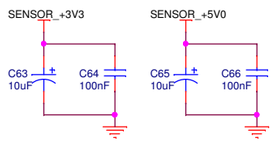
+1V2 — +1V2 3,4,5,6

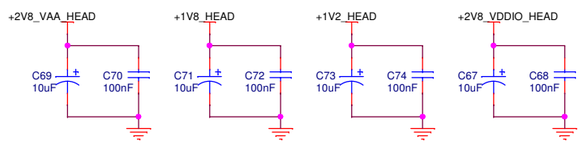
+VDDIO_HB0_LS — +VDDIO_HB0_LS 3,5,7

+VDDIO_HB1_LS — +VDDIO_HB1_LS 3,7

from ICP3 -> to Headboard or Dual Adapter Board







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