EMC3 Altium Circuit & PCB layout review

Date (start)	11/22/2022
Author	GKP

Title Page	Empty	Date	13/12/2022
		Author	SM
Block diagram page	Empty	Responses	

Always On Pwr

IC2 Maxim land pattern is a little off, but good enough.

Pad size 0.35x0.95mm

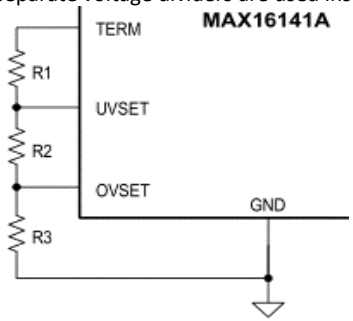
Central pad 2.23mm

Pin-2-pin 3.68mm

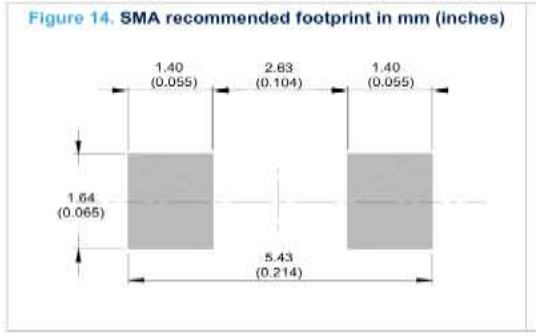
Why 39.2k on SLEEP pin?

Q17 land pattern close enough.

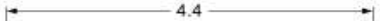
IC2 any reason two separate voltage dividers are used instead of this?

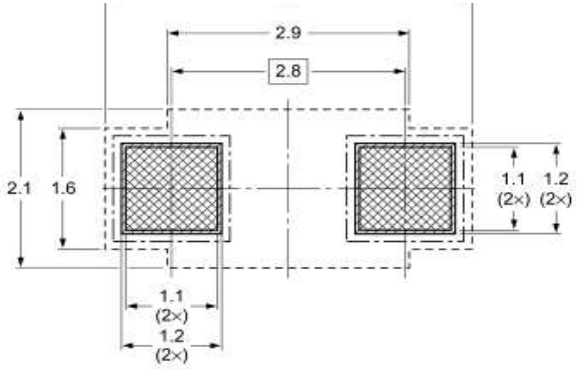


D1 This is the suggested footprint. But there are many alternatives.



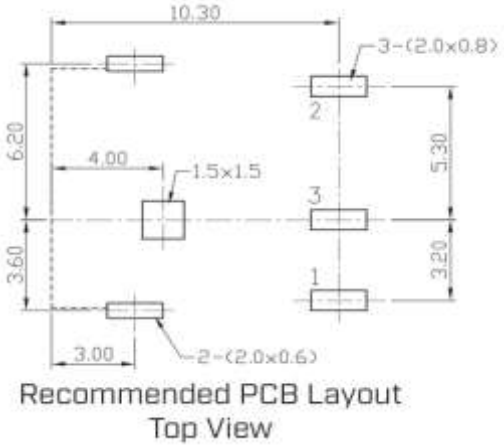
D2 This is the suggested footprint. But there are many alternatives.





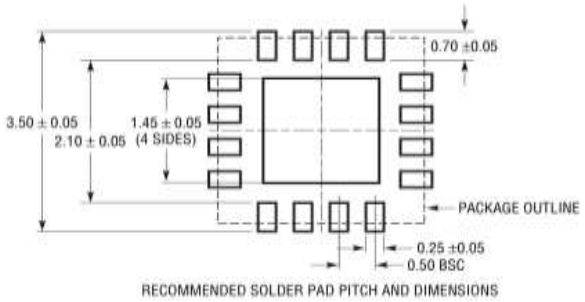
J3

Ignoring the holes instead of slots (this is normal) the footprint is the odd 0.1mm off from this

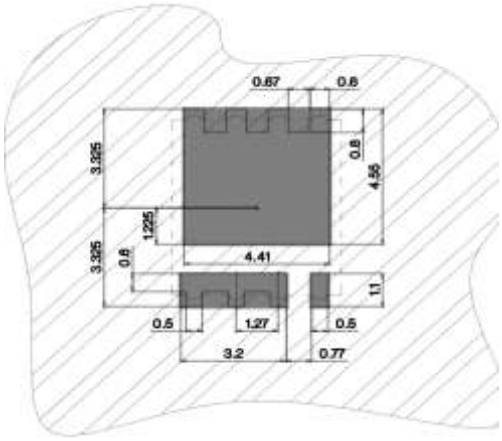


U6, LTC3851A

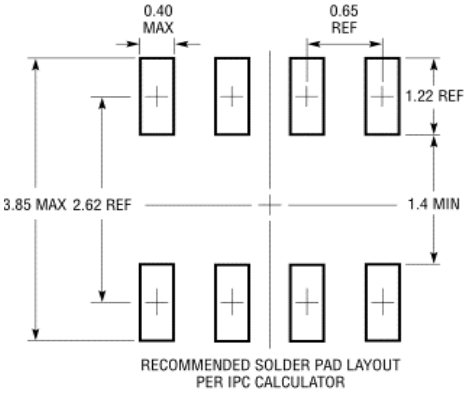
The datasheet says that pin 7 is Ilim. There is no PGOOD pin.
Footprint doesn't match the datasheet exactly.



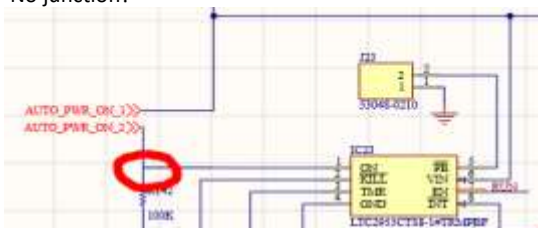
Q1 & Q2 Footprint doesn't exactly match datasheet.

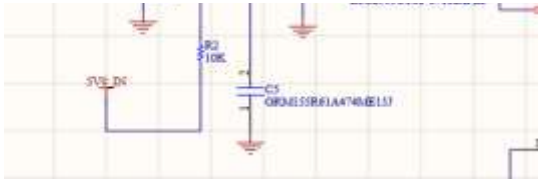


IC23 Don't know why, but the RUN signal (pin 7) doesn't seem to connect to U6 pin 1. Footprint?

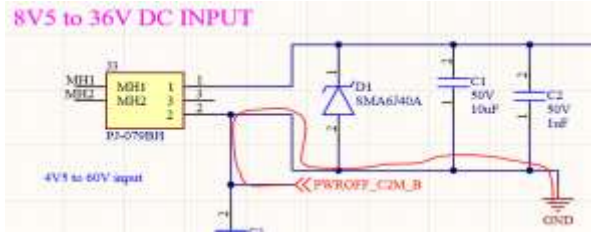


No junction?

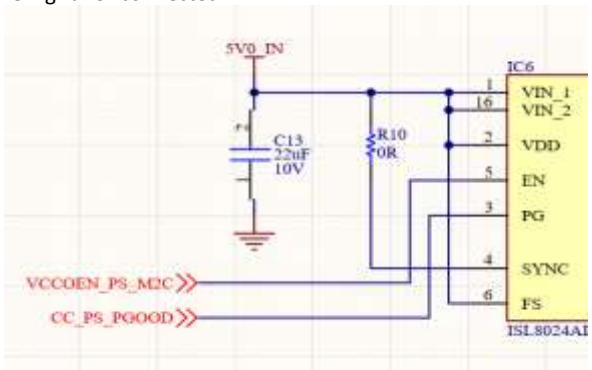




Signal PWROFF_C2M_B is connected to GND. That can't be right, can it?

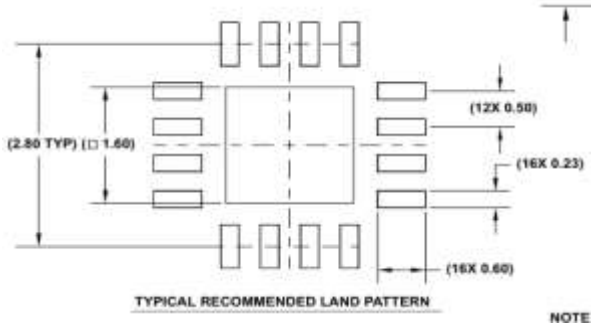


PS Power C13 Off grid. Unconnected.

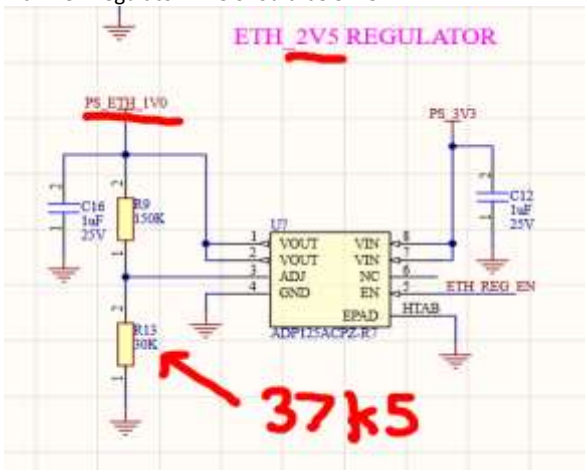


PG outputs need a pull-up.

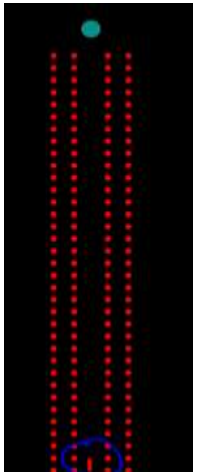
IC3, 6, 8 Footprint not as per datasheet.



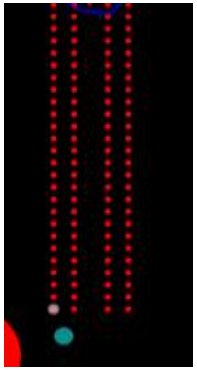
		Optional 4.7pF cap across FB resistor. Add a placeholder but do not fit.
	U7	Eth 2.5V regulator. R13 should be 37k5.



	IC1	Max recommended Vcc is 3.6V, not 5V.
PL Power	U10	Vout wrong name. Should be PS_ETH_2V5. R15 should be 37k5.
	U12	Vout wrong name. Should be PS_IAS_2V75? R23 should be 33k3. PG outputs need a pull-up.
SOM240_1 Connector	J1	What's that?

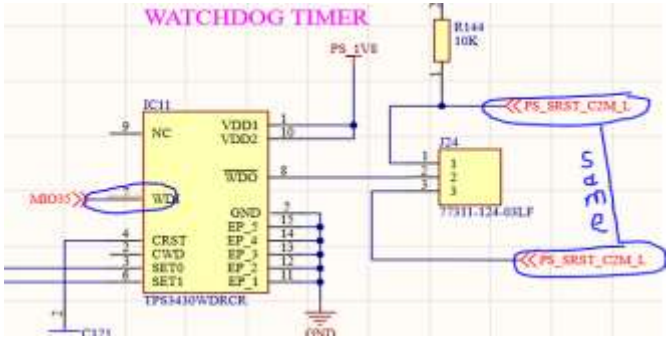


There's a few little track remnants on the board.

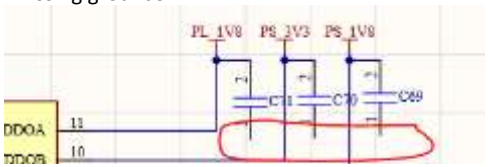


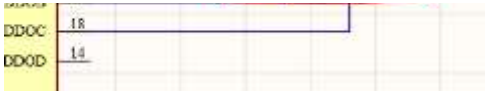
Several pins are not connected between J1 and U2. Not sure if pins on U2 are off grid, or where the termination point is for the pin.

SOM240_2 Connector	J2	Several pins are not connected between J2 and Rpi camera connector. I think the signal names are different.
EPROM, RTC, WD, LEDs		Where does UTIL_3V3 come from?
	IC12	I2C bus not connected. Not sure where it should go. A few of the LED driver FETs don't seem to have their gates connected. LEDs don't appear to have a pin 1 marker (or cathode/anode/polarity).
	IC11	WDI not connected.



Clock Gen	IC25	PCB footprint not identical to that in the datasheet, butclose enough. Do you need a 100 Ohm termination at the A&B inputs?
	IC15	Missing grounds

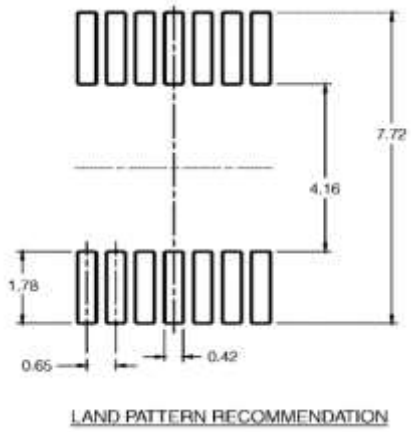




Is this Si part pre-programmed? What do the P0-4 inputs do?

JTAG UART J11 Pin 13 is normally GND. Pin 14 is usually JTG_RST.

Display Port IC30 Footprint not as per datasheet.

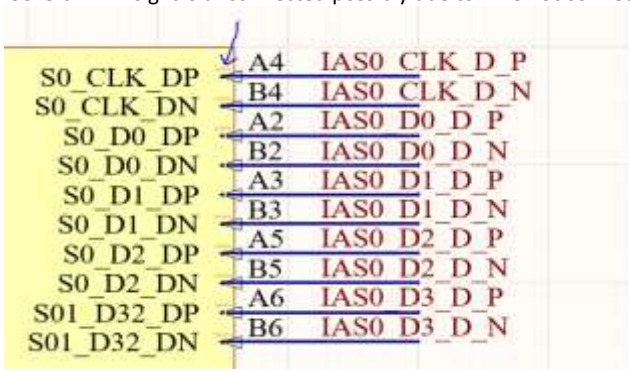


LAND PATTERN RECOMMENDATION

IAS MIPI Camera J4 Have you a link to the pinout?

U1 Pinout and footprint checked.

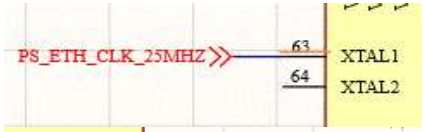
Several MIPI signals unconnected possibly due to wire not connecting with IC terminal/pin.



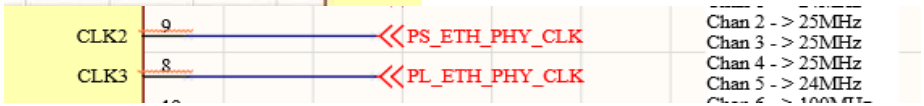
PS-PL Ethernet PHY IC19 Pinout checked. Footprint OK.

I wonder why Microsemi call TX pins inputs, and RX pins outputs. Seems the wrong way round to me.

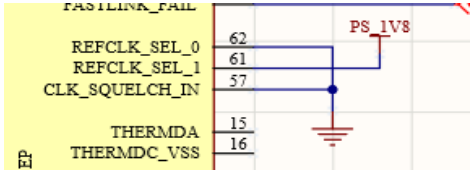
Eth clk is shown as:



But the clk gen is:

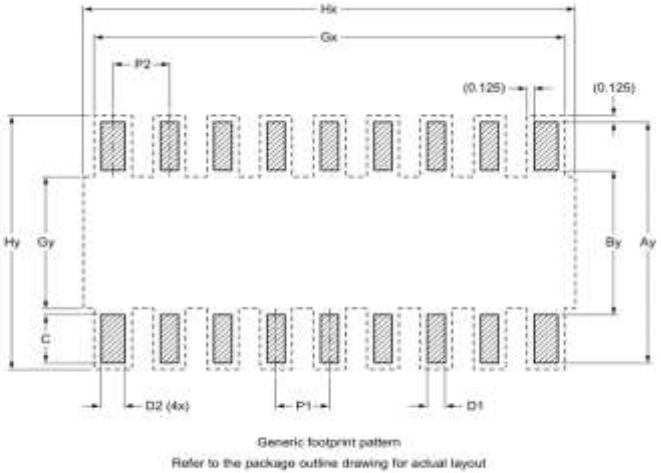


REFCLK_SEL is:



But 10 means 50MHz.

	IC18	As above.
	J6 & J9	I'll assume the footprint is correct as I'm having difficulties downloading data from Harting.
RPi Camera Connectors	IC16	Pinout not exactly as per datasheet, but close enough



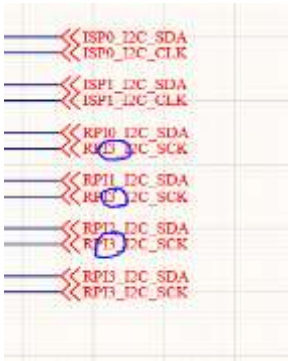
---- occupied area

DIMENSIONS in mm

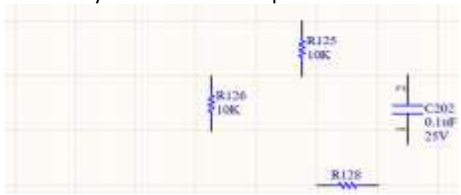
P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	8.200	5.300	8.600	7.450

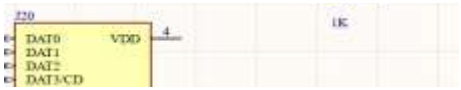
Circuits not yet finished

Same net names



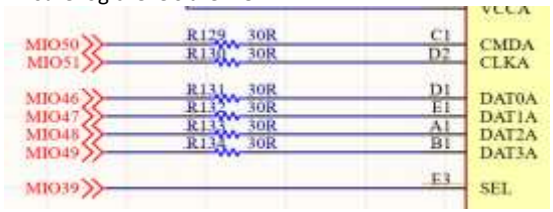
	J7 etc	A few unconnected pins probably due to net name inconsistencies across sheets. Connector has been replaced by 545482272. Footprint checked OK. Pinout matches what we've used before. We've always used capacitors of 10uF and 100nF on the supply pin. I seem to recall reading something about the max voltage on pin 18 (XCLK) being 2.8V. But this might be camera specific. Might be worth adding a resistor divider for pin 18 though.
SD Card PMOD	J20	Pinout and footprint checked OK. Obviously circuit is not complete





IC36

Recommended pad diameter is 0.23mm not 0.208mm.
Ensure logic levels are 1.8V



Samtec 30 pin

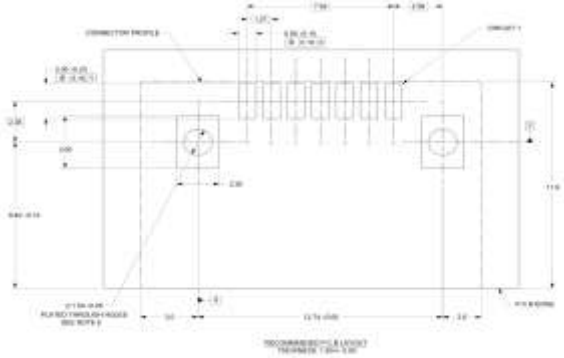
J17

Pin numbering and footprint checked OK.
What does this connector connect to?

SATA Connector

J13

Molex datasheet suggests rectangular pads for the mounting pins.



mPCIe

J21

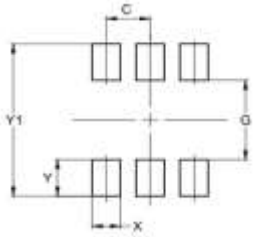
Footprint checked OK.
Normally the schematic symbol reflects the footprint which makes the connectivity easier to read.

1	WAKE#	2	3.3V
3	Reserved****	4	GND
5	Reserved****	6	1.5V
7	CLKREQ#	8	VCC***
9	GND	10	I/O***
11	REFCLK-	12	CLK***
13	REFCLK+	14	RST***
15	N/C or GND	16	VPP***
	Mechanical key		
17	Reserved	18	GND
19	Reserved	20	Reserved****
21	GND	22	PERST#
23	PERn0	24	+3.3Vaux

25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	Reserved*	38	USB_D+
39	Reserved*	40	GND
41	Reserved*	42	LED_WWAN#
43	Reserved*	44	LED_WLAN#
45	Reserved*	46	LED_WPAN#
47	Reserved*	48	+1.5V
49	Reserved*	50	GND
51	Reserved*	52	+3.3V

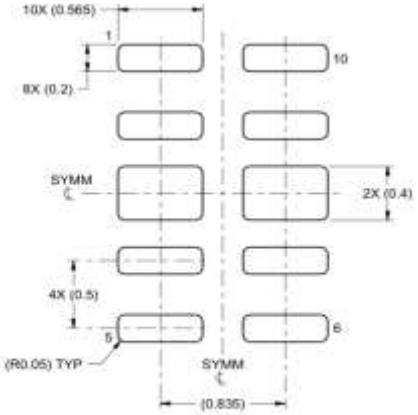
PCIE_PER P & N pins appear to be swapped.

Q21 Footprint not as per datasheet.



Dimensions	Value (in mm)
C	0.650
G	1.300
X	0.420
Y	0.600
Y1	2.500

D9 Footprint not as per datasheet.



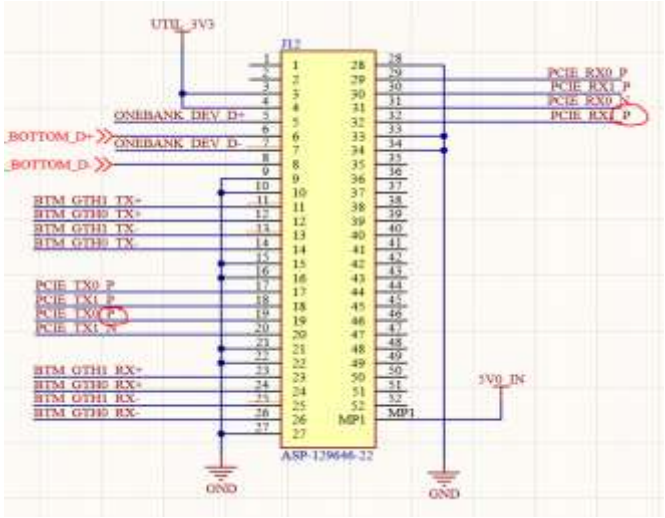
LAND PATTERN EXAMPLE
SCALE 30X

OneBank Connectors J10 Footprint checked OK.

J12

Too many Ps.

Footprint checked OK.



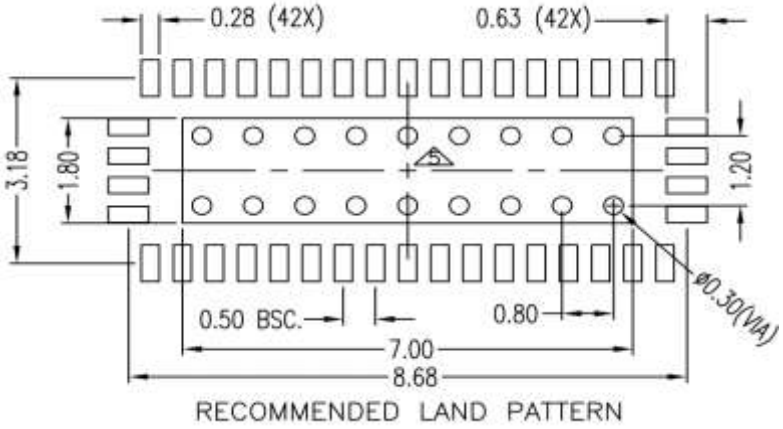
Easier to read if the schematic symbol matches the physical connector.

Top View Signal Assignment				
1	USB_OC#		PE_RST#	2
3	3.3V		3.3V	4
5	USB_1p		USB_0p	6
7	USB_1n		USB_0n	8
9	GND		GND	10
11	PEx1_1Tp		PEx1_0Tp	12
13	PEx1_1Tn		PEx1_0Tn	14
15	GND		GND	16
17	PEx1_2Tp		PEx1_3Tp	18
19	PEx1_2Tn		PEx1_3Tn	20
21	GND		GND	22
23	PEx1_1Rp		PEx1_0Rp	24
25	PEx1_1Rn		PEx1_0Rn	26
27	GND	+5 Volts	GND	28
29	PEx1_2Rp		PEx1_3Rp	30
31	PEx1_2Rn		PEx1_3Rn	32
33	GND		GND	34
35	PEx1_1Clkp		PEx1_0Clkp	36
37	PEx1_1Clkn		PEx1_0Clkn	38
39	+5V_SB		+5V_SB	40
41	PEx1_2Clkp		PEx1_3Clkp	42
43	PEx1_2Clkn		PEx1_3Clkn	44
45	DIR		PWRGOOD	46
47	SMB_DAT		Reserved	48
49	SMB_CLK		Reserved	50
51	SMB_ALERT		PSON#	52

Toward center of board

IC27

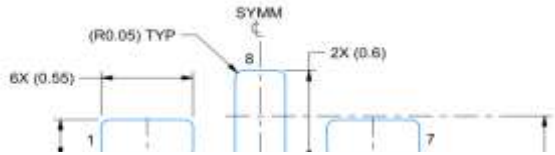
Footprint not as per datasheet.

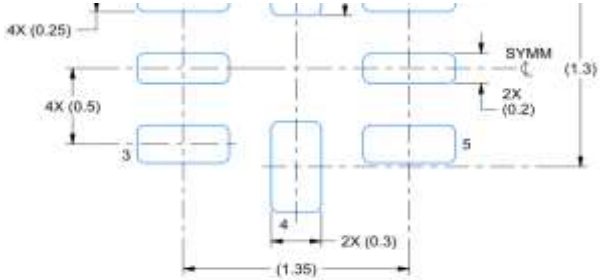


Don't forget the vias in the central pad.

IC28

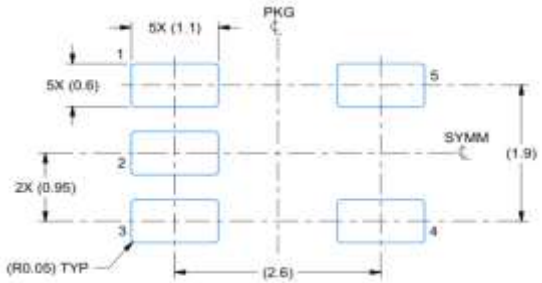
Footprint not as per datasheet.





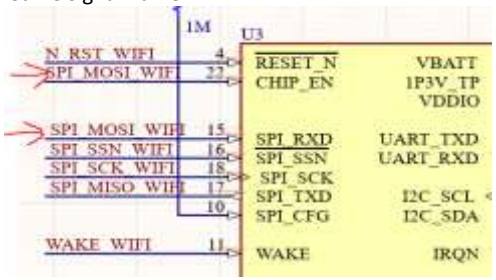
LAND PATTERN EXAMPLE
SCALE:30X

IC31 Pinout not exactly as per datasheet, but close enough



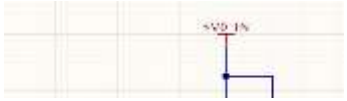
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

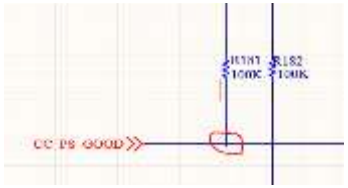
WiFi U3 Same signal name



Pinout and footprint checked OK.

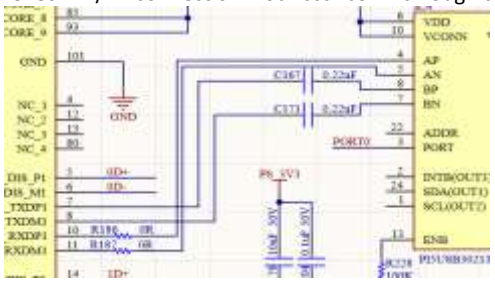
Reset Logic Not connected

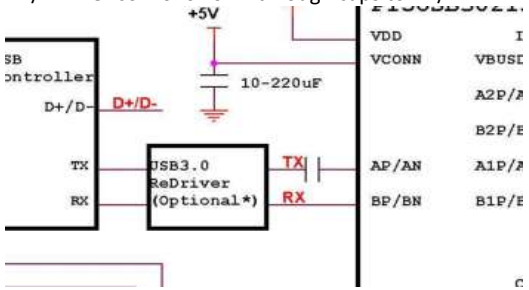




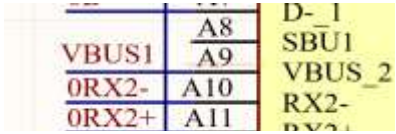
	IC7 & IC10	Pinout not exactly as per datasheet, but close enough RESET output is open drain for this device version. Needs a pull-up.
	74AUP1G09	Check footprint(s) Do the open-drain outputs need pull-ups? Plenty of Offsheet ports.
	IC26 & IC48	Vcc max is 3.6V not 5V.
	IC5	Output it open-drain and (possibly) needs a pull-up to 3.3V. Could power IC26&48 at 3.3V too. What a weird little footprint!
Fan Switches	S3	Footprint checked OK. 12V fan?

USB PHY and Connectors	IC22	Pinout and footprint checked OK. Check TX/RX connection. Your cct has TX through caps to BP/BN. Pericom shows TX through caps to AP/AN.



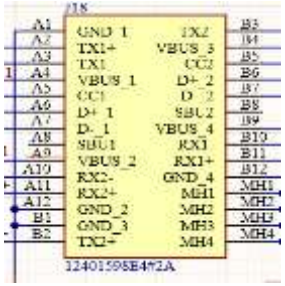


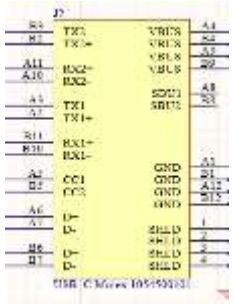
	J18	The wiggly red line is showing that pin A9 is not connected elsewhere. The wire is ok as this has an appropriate net name but the VBUS1 label is not attached to the wire. I've not seen this if the schematic grid is set to 100mil (0.1").



Pinout and footprint checked OK.

Personally, I'd use the sch symbol on the right. Easier to see the interfaces.

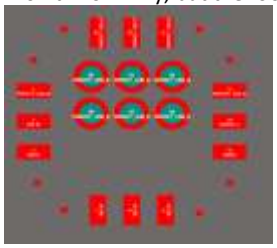




No ESD devices on the USB pins.

IC34 Pinout and footprint checked OK.

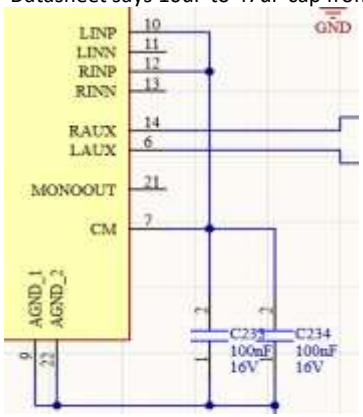
U5 Don't know why, but the footprint isn't showing properly



Active low power enable, maximum current limit.

Audio CODEC IC20 Pinout OK. Footprint looks OK but no suggested footprint in the datasheet.

Datasheet says 10uF to 47uF cap from CM to GND. Is LINP and RINP supposed to be conencted to CM? I guess it biases to AVDD/2.




GND