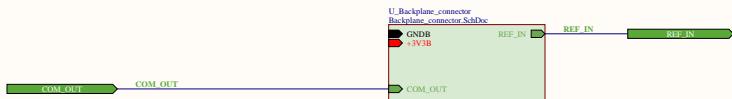


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BaseBoard to ADC board(s) signal connectors



ZONE B

NET analog signals A

NET analog signals B

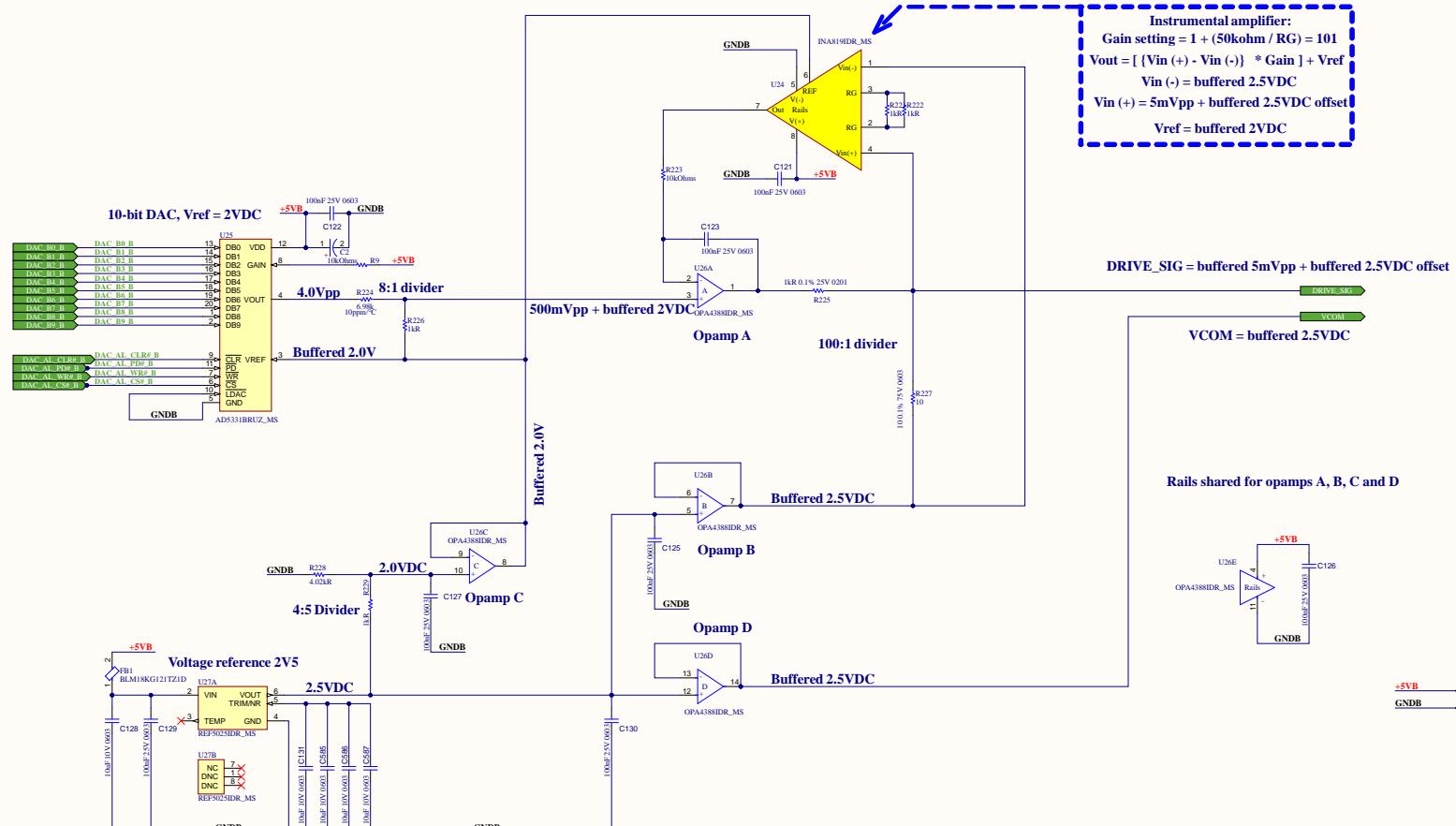
Power and control signals



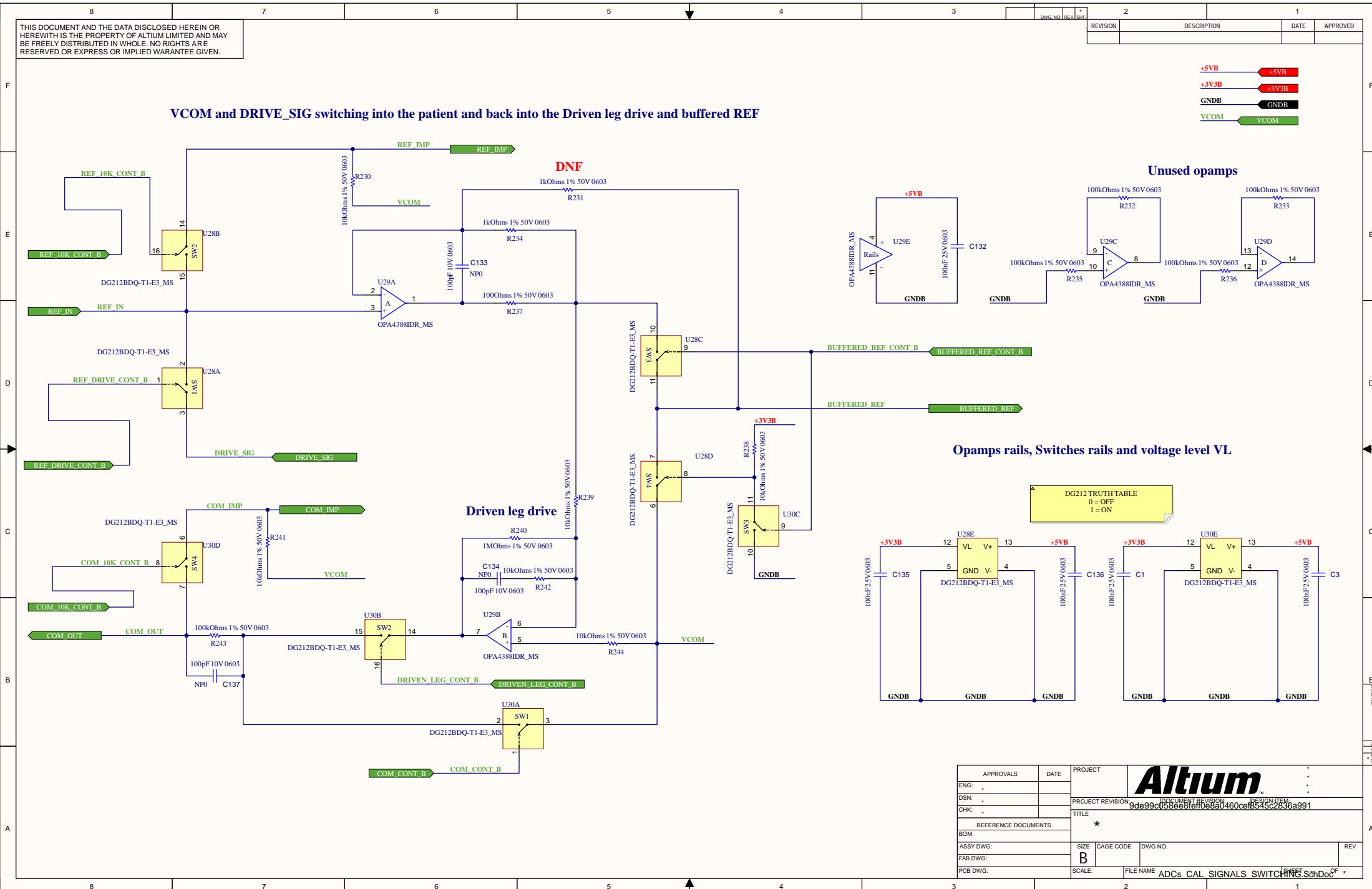
APPROVALS	DATE	PROJECT	<i>Altium</i>		
ENG:		PROJECT REVISION	0de99c1e02e99f1fb1e99d1460ceff-0cc233ba991		
DSN:		DOCUMENT Revision			
CHK:		TITLE	REVISIONS		
REFERENCE DOCUMENTS			*		
REF ID:					
ASSEMBLY:	SIZE	CAGE CODE	SWG NO.	REV	
PCB DNG:	C				
FRD DNG:					
PCB DNG:	SCALE	FILE NAME	ADCB_CONNECTORS.SchDoc	SHEET	OF

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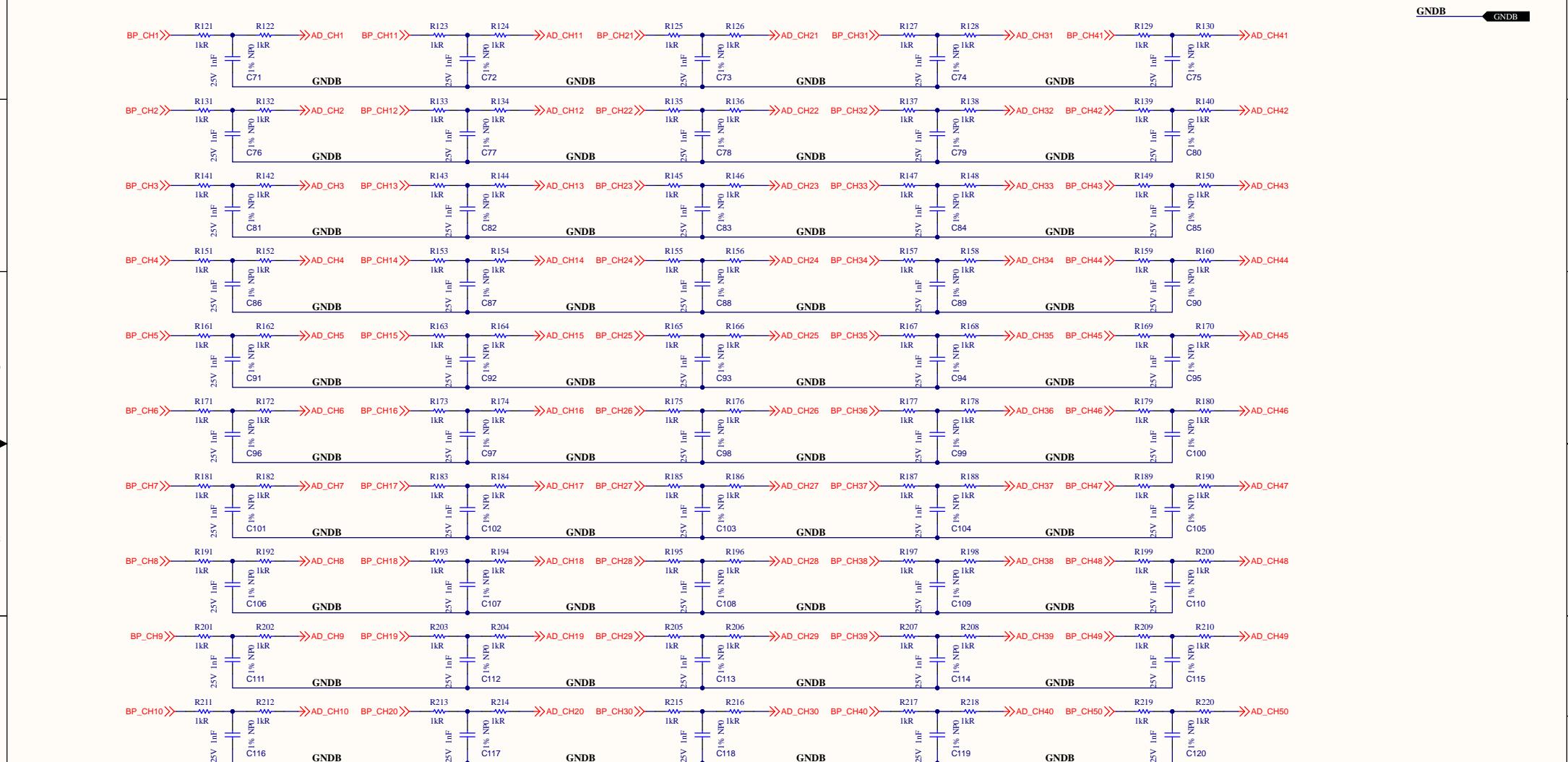
APPROVALS	DATE	PROJECT	Altium
ENG: .		PROJECT REVISION	90e99c158ae8f8f88bd460ccfb54c2336a991
DSN: .		DOCUMENT NUMBER	DS290183
CHK: .		TITLE	*
BCM:		REFERENCE DOCUMENTS	
ASSY DWG:		SIZE	CAGE CODE
FAB DWG:		C	DWG NO.
PCB DWG:		SCALE	FILENAME



APPROVALS		DATE	PROJECT	Altium	
ENG:	*		PROJECT REVISION	9de99cd5be8feff0e8a0460cef545c2836a991	
DSN:	*		DOCUMENT REVISION		
CHIC:	*		DESIGN ITEM		
REFERENCE DOCUMENTS	*		TITLE	*	
BOM:			ITEM		
ASSY DWG:			SIZE	B	
FAB DWG:			CAGE CODE		
PCB DWG:			DWG NO.		
			REV		
SCALE:			FILE NAME	ADCs_CAL_SIGNALS_SWITCHING.SchDoc	

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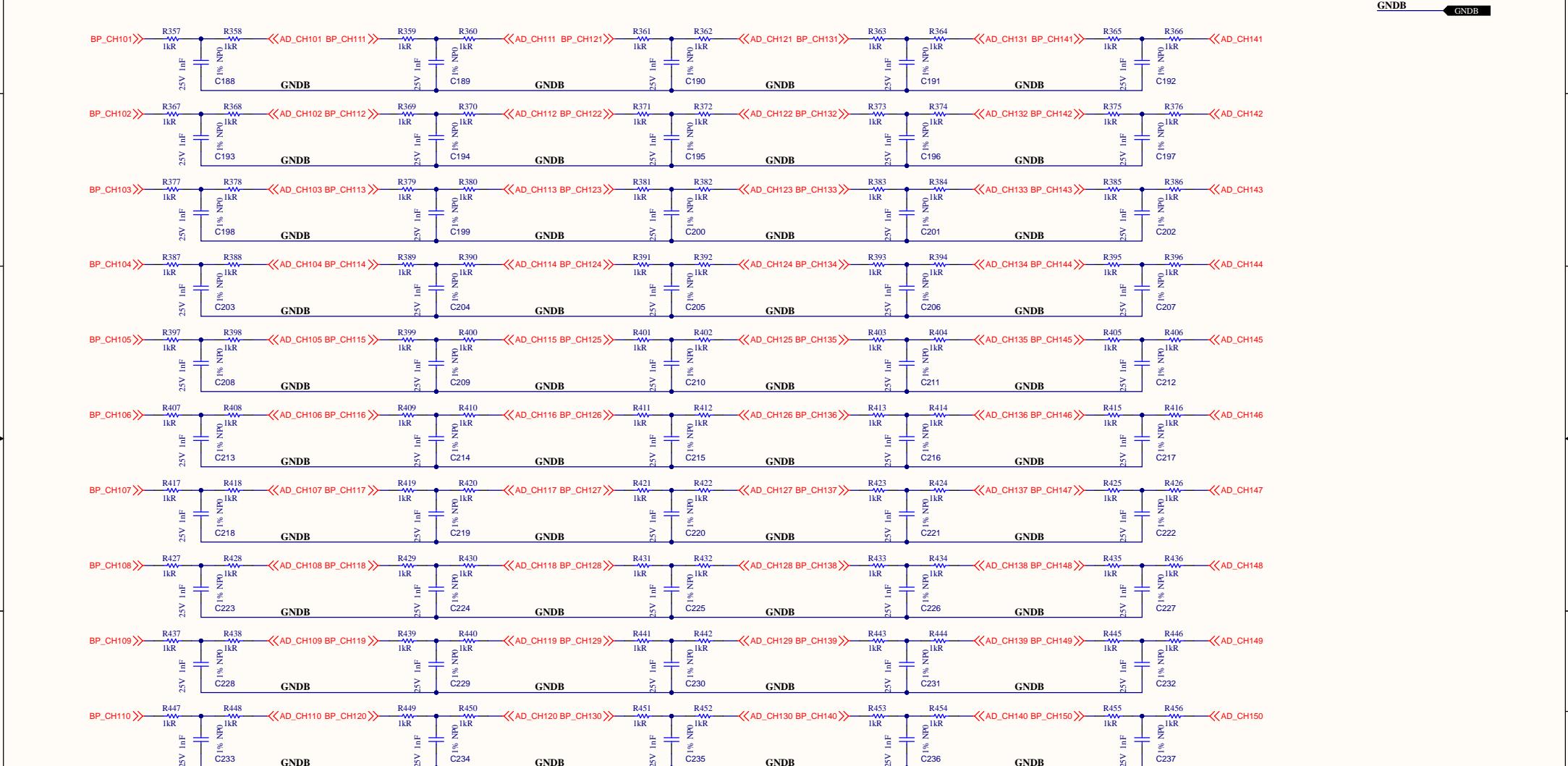
ZONE B



$$F(\text{cut-off}) \text{ or } f(-3\text{dB}) = 1 / (2 * \pi * R * C) = 159\text{Hz}$$

APPROVALS	DATE	PROJECT	Altium		
ENG:		PROJECT REVISION TITLE	DOCUMENT REVISION: 9de99c5b58ee8feff0e8a0460cef8545c2836a991		DESIGN ITEM:
DSN:			*		
CHK:					
REFERENCE DOCUMENTS					
BOM:					
ASSY DWG:		SIZE B	CAGE CODE	DWG NO.	REV
FAB DWG:					
PCB DWG:		SCALE:	FILE NAME	Backplane analog filters 1 to 50	SHEET OF *

ZONE B



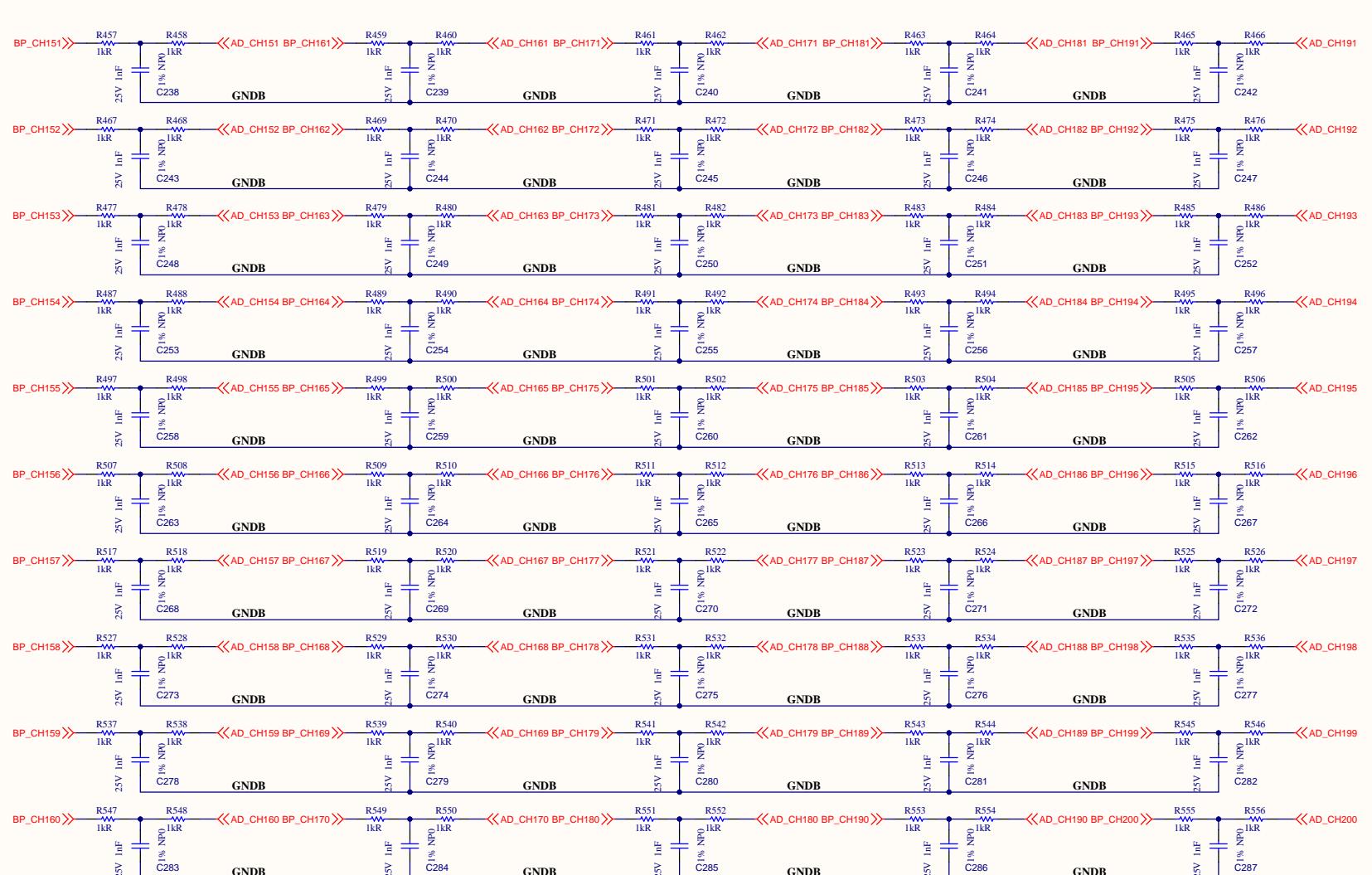
$$F(\text{cut-off}) \text{ or } f(-3\text{dB}) = 1 / (2 * \pi * R * C) = 885\text{Hz}$$

APPROVALS		DATE	PROJECT	Altium	
ENG:	*		PROJECT REVISION	9de99cd5be8feff0e8a0460cefb545c2836a991	
DSN:	*		DOCUMENT REVISION		
CHC:	*		DESIGN ITEM		
TITLE		*			
REFERENCE DOCUMENTS					
BOM:					
ASSY DWG:					
FAB DWG:					
PCB DWG:					
SCALE:			FILE NAME	Backplane analog filters 101	SHEET 10 of 150.SchDoc *
SIZE:	B	CAGE CODE	DWG NO.		REV

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ZONE B

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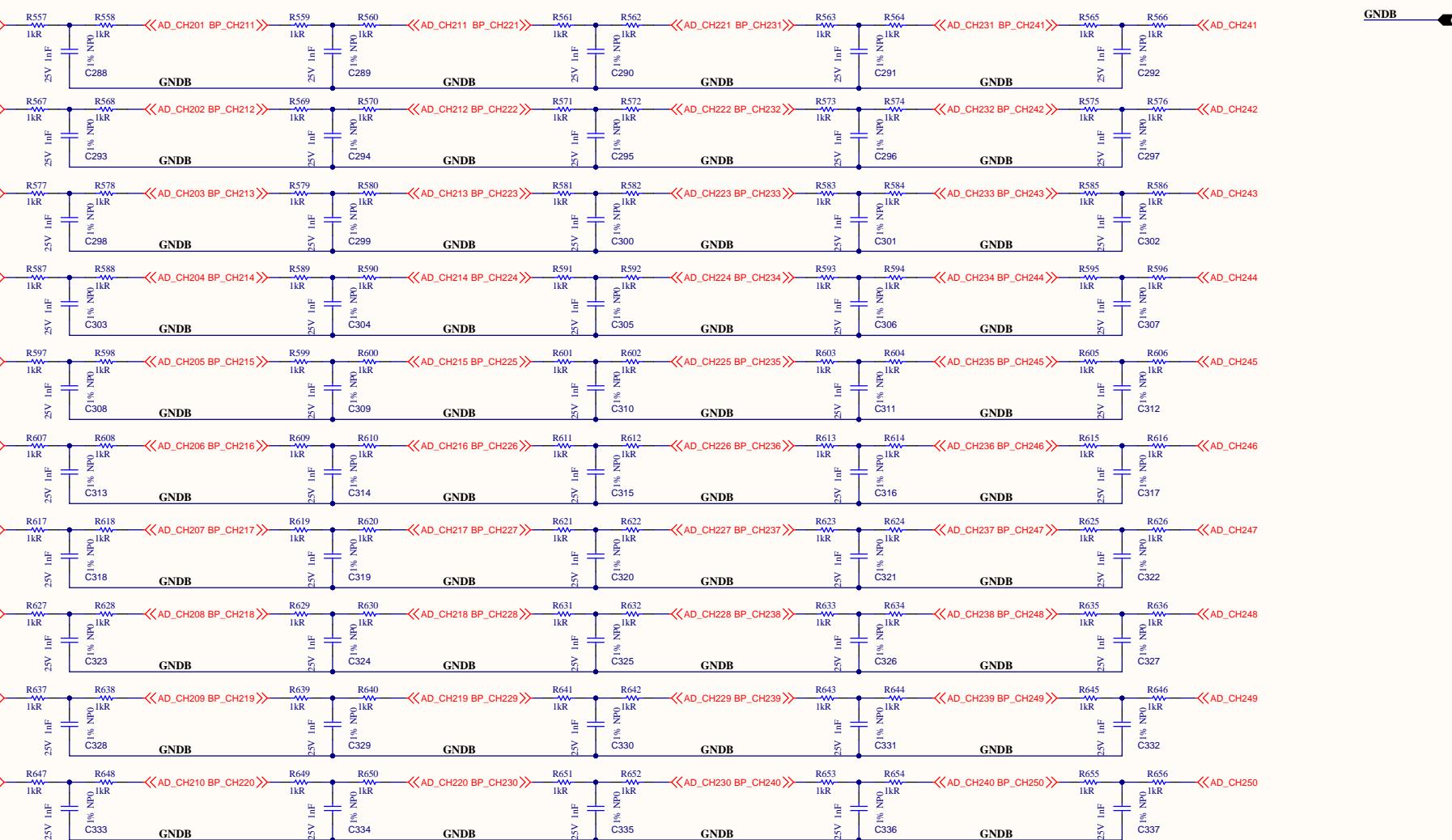


$$F(\text{cut-off}) \text{ or } f(-3\text{dB}) = 1 / (2 * \pi * R * C) = 885\text{Hz}$$

APPROVALS	DATE	PROJECT	Altium
ENG:	.	DOCUMENT REVISION	9de99cd58ee8feff0e8a0460cefb545c2836a991
DSN:	.	DESIGN ITEM	*
CHIC:	.	TITLE	*
BOM:	.	REFERENCE DOCUMENTS	
ASSY DWG:	.	SIZE	B
FAB DWG:	.	CAGE CODE	
PCB DWG:	.	DWG NO.	
	SCALE:	FILE NAME	Backplane analog filters 151 to 200.SchDoc

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ZONE B



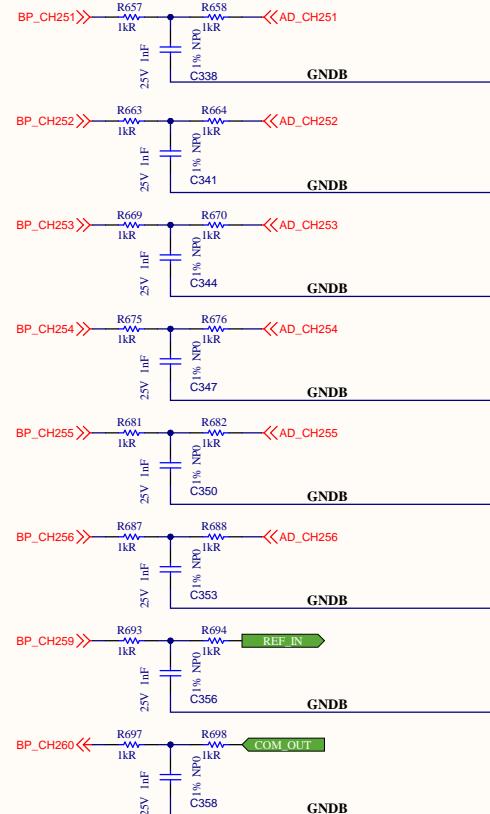
$$F(\text{cut-off}) \text{ or } f(-3\text{dB}) = 1 / (2 * \pi * R * C) = 885\text{Hz}$$

APPROVALS		DATE	PROJECT	Altium	
ENG:	*		PROJECT REVISION	9de99cd58ee8feff0e8a0460cefb545c2836a991	
DSN:	*		DOCUMENT REVISION		
CHC:	*		DESIGN ITEM		
TITLE *					
REFERENCE DOCUMENTS					
BOM:					
ASSY DWG:					
FAB DWG:					
PCB DWG:					
SCALE:			FILE NAME	Backplane analog filters 201	SHEET 1 OF 1
SIZE:	B	CAGE CODE	DWG NO.		REV:

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ZONE B

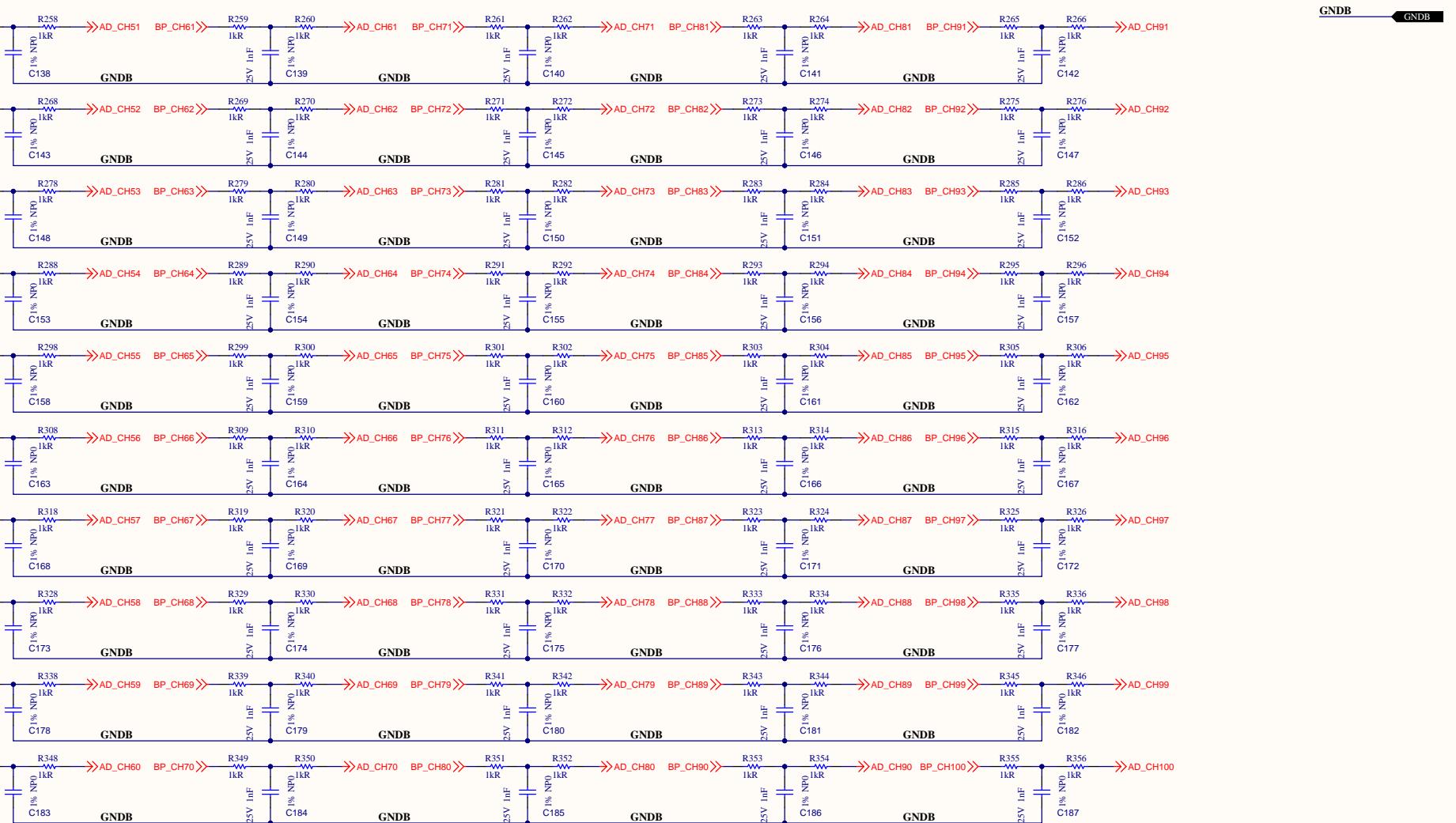
REVISION	DESCRIPTION	DATE	APPROVED



$$F(\text{cut-off}) \text{ or } f(-3\text{dB}) = 1 / (2 * \pi * R * C) = 885\text{Hz}$$

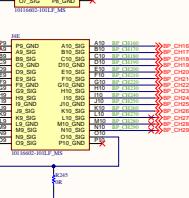
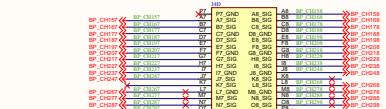
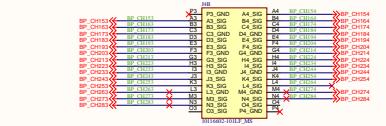
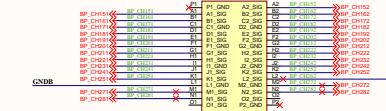
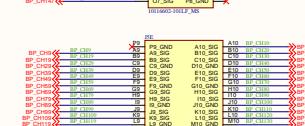
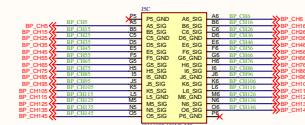
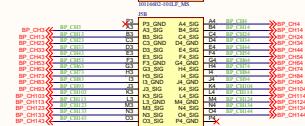
APPROVALS	DATE	PROJECT	Altium
ENG: *		PROJECT REVISION	DOCUMENT REVISION
DSN: *		9de99cd58ee8feff0e8a0460cef545c2836a991	DESIGN ITEM
CHG: *		TITLE	*
REFERENCE DOCUMENTS			
BOM:		SIZE	CAGE CODE DWG NO.
ASSY DWG:		B	REV
FAB DWG:			
PCB DWG:		SCALE:	FILE NAME Backplane analog filters 251
			SHEET 1 of 300.SchDoc *

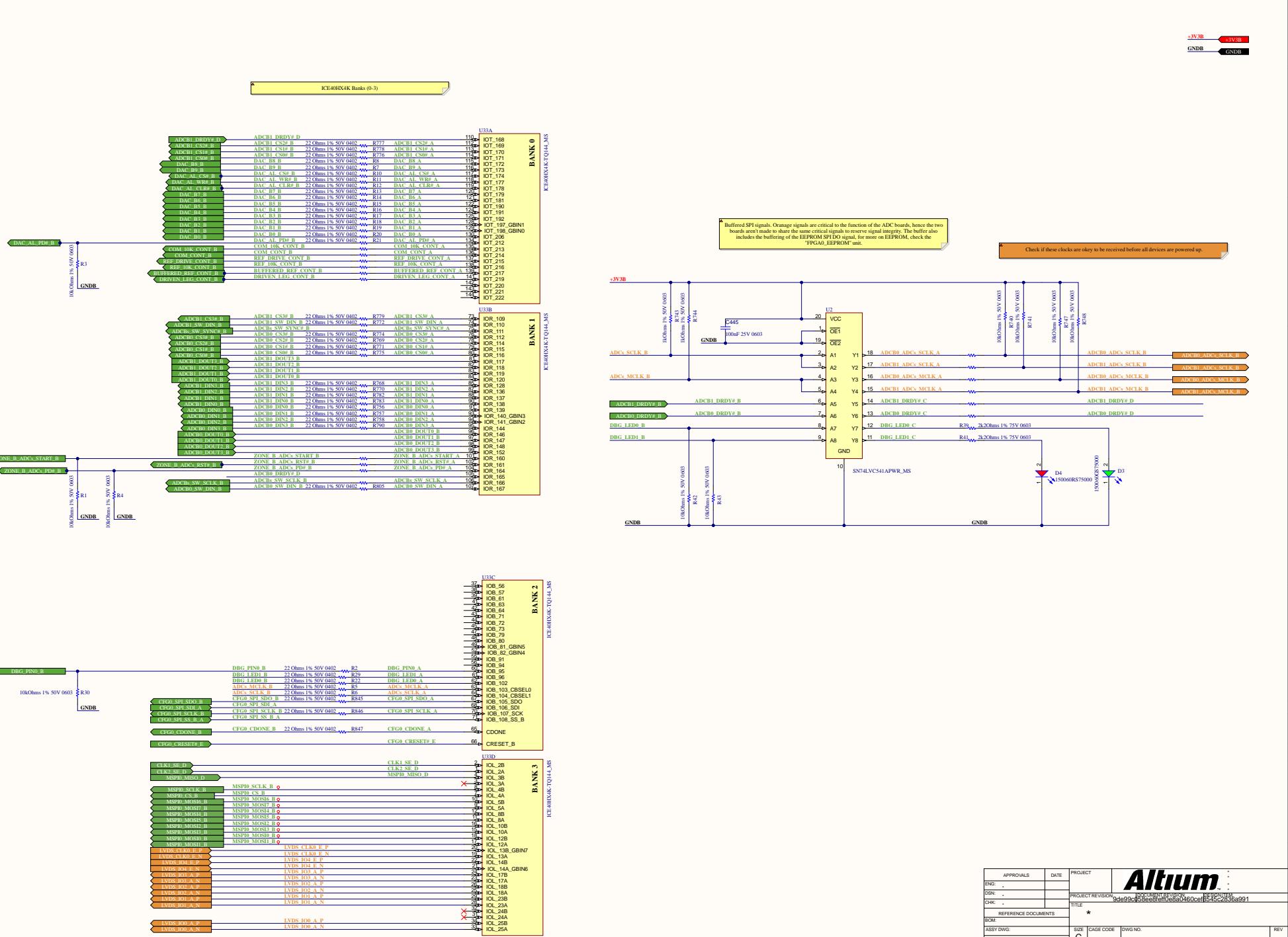
ZONE B



$$F(\text{cut-off}) \text{ or } f(-3\text{dB}) = 1 / (2 * \pi * R * C) = 885\text{Hz}$$

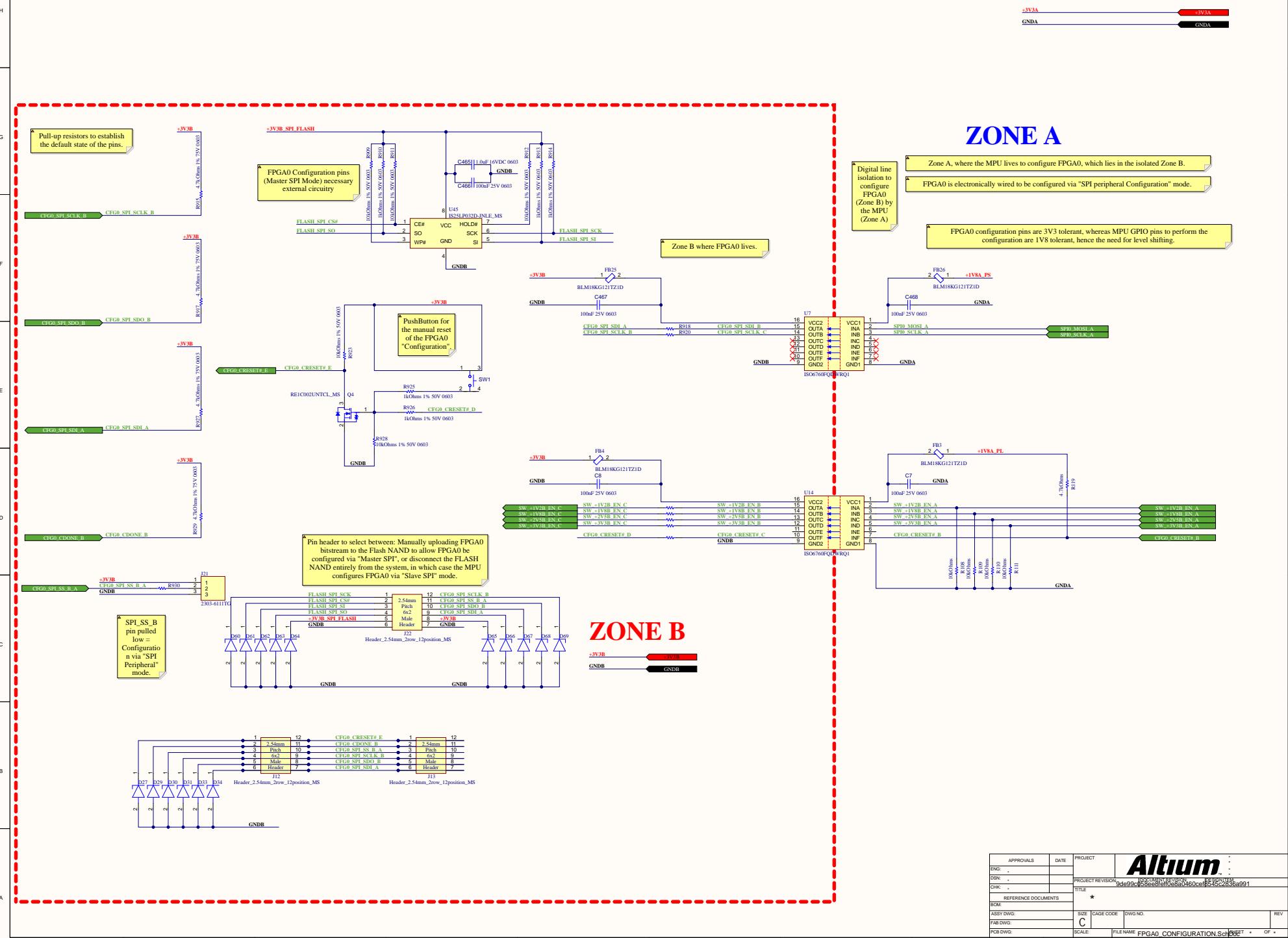
APPROVALS		DATE	PROJECT	Altium	
ENG:	*		PROJECT REVISION	9de99cd58ee8feff0e8a0460cefb545c2836a991	
DSN:	*		DOCUMENT REVISION		
CHC:	*		DESIGN ITEM		
TITLE		*			
REFERENCE DOCUMENTS					
BOM:					
ASSY DWG:					
FAB DWG:					
PCB DWG:					
SCALE:			FILE NAME	Backplane analog filters 51 to 100.SchDoc	REV: *
SHEET:					





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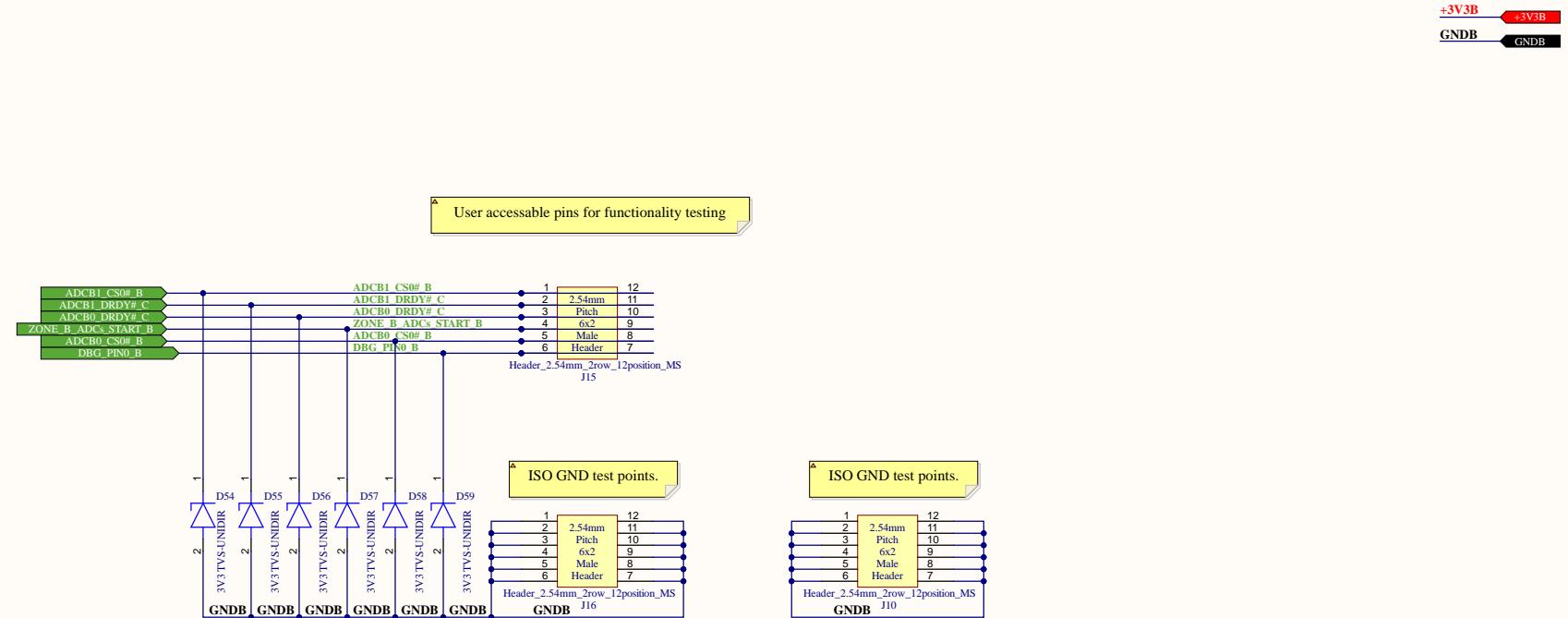
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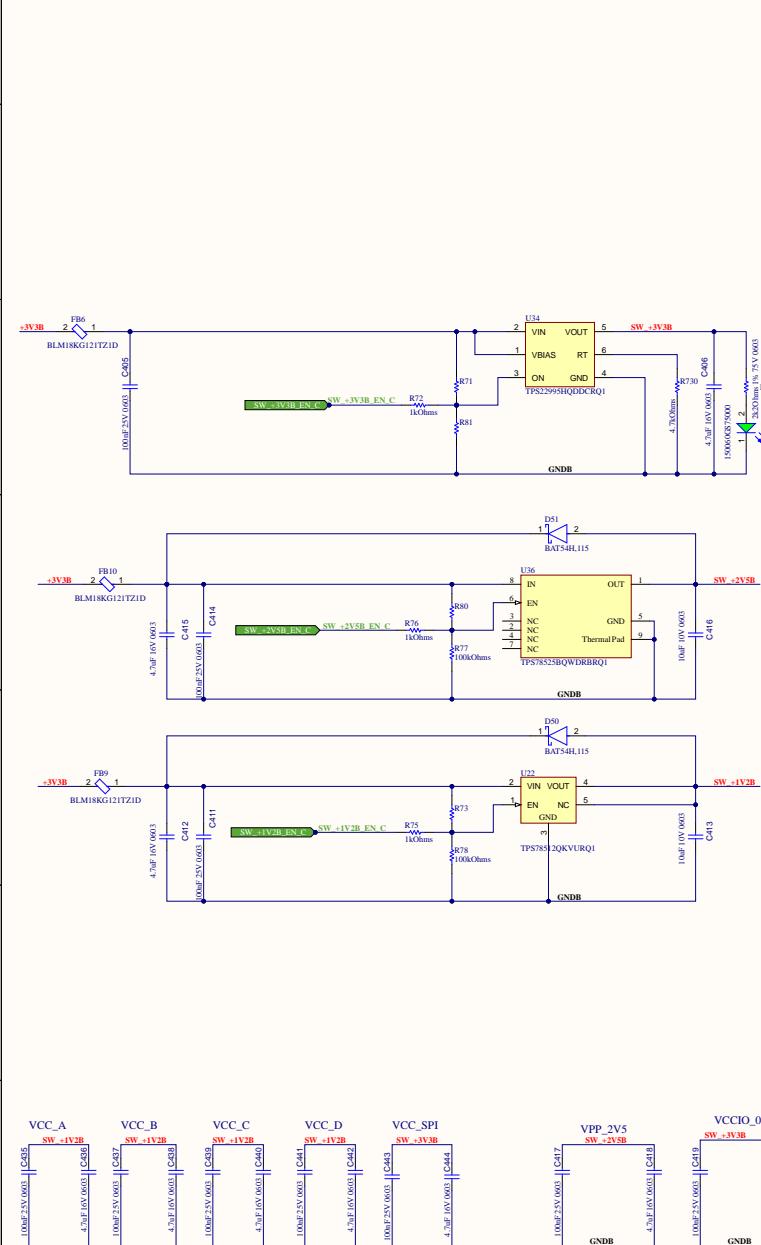
A



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ENG:	*	PROJECT REVISION	DOCUMENT REVISION 9de99cd58ee8feff0e8a0460cef545c2836a991		
DSN:	*	DESIGN ITEM			
CHIC:	*	TITLE	*		
REFERENCE DOCUMENTS					
BOM:					
ASSY DWG:	SIZE	CAGE CODE	DWG NO.	REV	
FAB DWG:	B				
PCB DWG:	SCALE:	FILE NAME FPGA0_DEBUG.SchDoc			SHEET * OF *

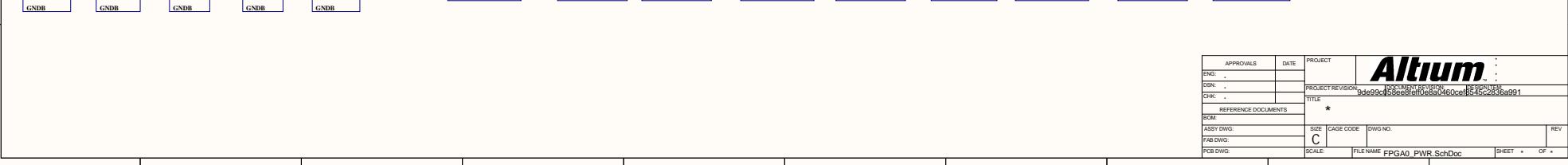
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REVISION: **U33E** DATE: **10/09/2018** APPROVED:



Switch to control ICE40 VPP_2V5 Power.
Only for Master SPI configuration, its
required to be powered 0.25ms after
VCC_SPI and VCC.

VCCIO_x — VCCIO - The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.



4.5. Power-up Supply Sequence

It is recommended to bring up the power supplies in the order below.

Note: There is no specified timing delay between the power supplies. There is, however, a requirement for each supply to reach a level of 0.5 V, or higher, before any subsequent power supplies in the sequence are applied.

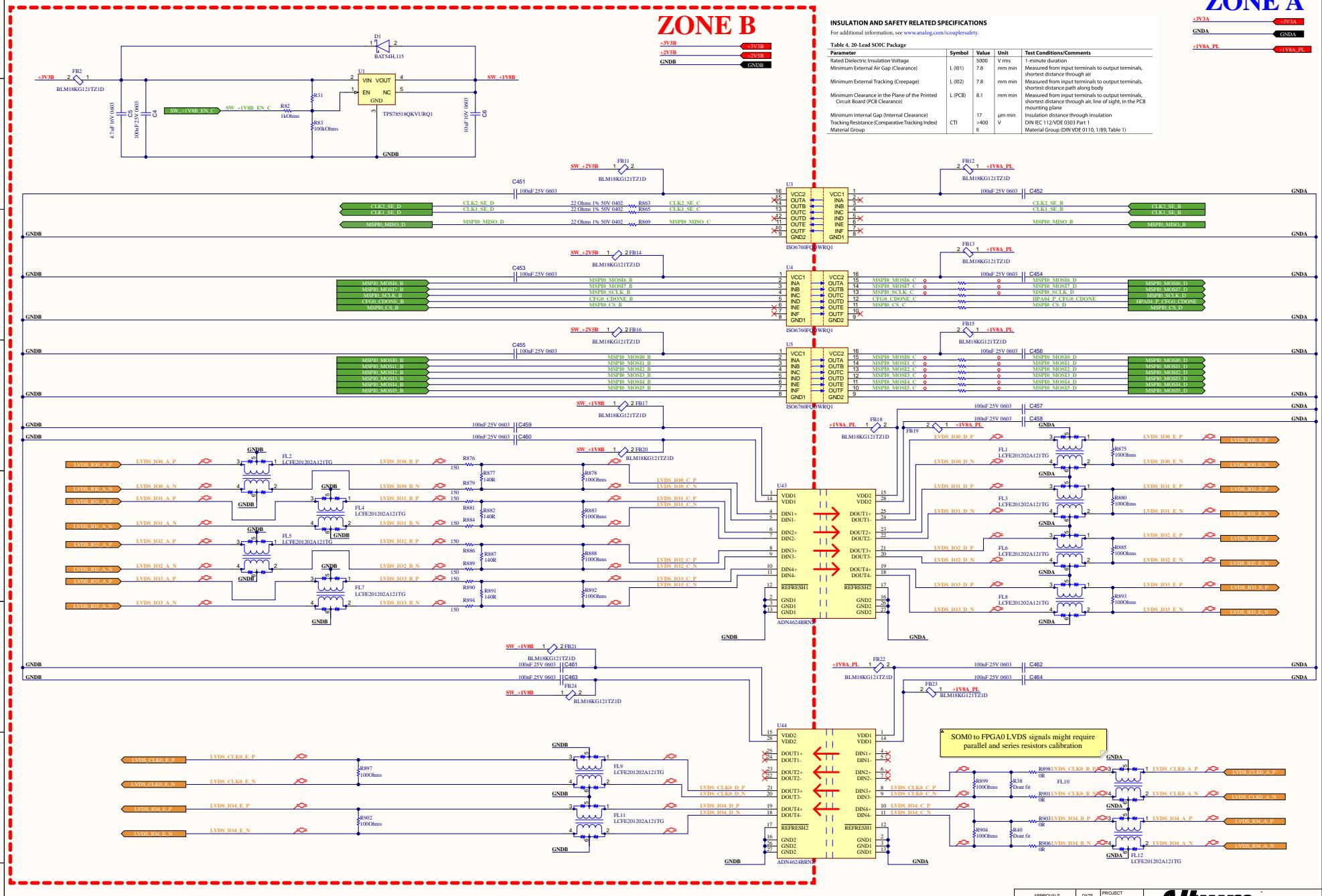
1. VCC and V_{CCPLL} should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the V_{CCPLL}. Refer to [ICE40 Hardware Checklist \(FPGA-TN-02006\)](#).
2. SPI_V_{CCIO1} should be the next supply, and can be applied any time after the previous supplies (VCC and V_{CCPLL}) have reached a level of 0.5 V or higher.
3. VPP_2V5 should be the next supply, and can be applied any time after previous supplies (VCC, V_{CCPLL} and SPI_V_{CCIO1}) have reached a level of 0.5 V or higher.
4. Other Supplies (V_{CCIO0} and V_{CCIO3}) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (VCC and V_{CCPLL}) have reached a level of 0.5 V or greater. There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are re-powered up again.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units	
V _{CC}	Core Supply Voltage	1.14	1.26	V	
V _{PP_2V5}	V _{PP_2V5} NVM Programming and Operating Supply Voltage	1.71	3.46	V	
	Slave SPI Configuration	2.30	3.46	V	
	Master SPI Configuration	2.30	3.46	V	
	Configure from NVM	2.30	3.46	V	
	NVM Programming	2.30	3.00	V	
V _{PP_FAST}	Optional fast NVMC programming supply. Leave unconnected.	N/A	N/A	V	
V _{CCPLL}	PLL Supply Voltage	1.14	1.26	V	
V _{CCIO^{1,2,3}}	I/O Driver Supply Voltage	V _{CCIO0-3} V _{CC_SPI}	1.71	3.46	V
T _{JIND}	Junction Temperature Industrial Operation	-40	100	°C	
T _{FPROG}	Junction Temperature NVMC Programming	10	30	°C	

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ENG: .		PROJECT REVISION	90e99c158ae98f8f8a0460ccfb54c235a991
DSN: .		DOCUMENT NUMBER	
CHK: .		FILE NUMBER	
REFERENCE DOCUMENTS *			
BCM:			
ASSY DWG:	C	CAGE CODE	DWG NO.
FAI DWG:			
PCB DWG:		SCALE	FILE NAME: FPGA0_PWR.SchDoc
			REV: *

ZONE A

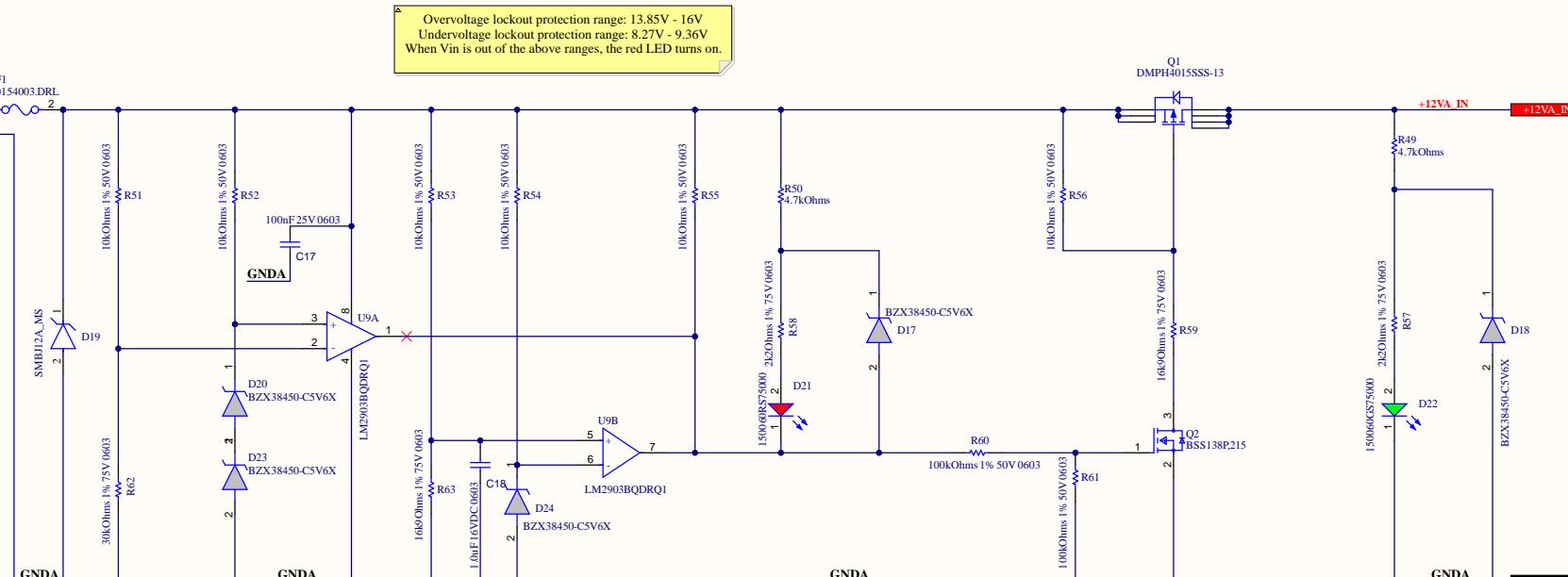


Altium

APPROVALS	DATE	PROJECT
ENG: .		
DSN: .		PROJECT REVISION: 90e99c1528eef7f8e0d460ccf8545c235a991
CHK: .		TITLE: *
RCM: .		REFERENCE DOCUMENTS
ASSY DWG: .		SIZE: CAGE CODE: DWG NO: REV: *
FAB DWG: .		PCB DWG: SCALE: FILE NAME: FPGA0_SOM0_ISO_BRIDGE_S910c OF *

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DWG. NO.	REV.	1	
REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS		DATE	PROJECT	Altium	
ENG:	*		PROJECT REVISION	9de99cd58ee8feff0e8au	DOCUMENT REVISION
DSN:	*		CHIC:	402036545628061008a0460cef8545c2836	DESIGN ITEM
CHIC:	*		TITLE	*	
REFERENCE DOCUMENTS					
BOM:					
ASSY DWG:			SIZE	CAGE CODE	DWG NO.
FAB DWG:			B		
PCB DWG:			SCALE:	FILE NAME	IN_PWR_Validation.SchDoc
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Title			Philips Neuro 500 E. 4th Ave. Eugene Oregon, 97401	
Size:	B	Number:	Revision:	
Date:	25/06/2024	Time:	11:06:46	Sheet of
File:	C:\Users\Public\Documents\Altium\EGL_Base_Board_PP1_4\Mechanical.SchDoc			

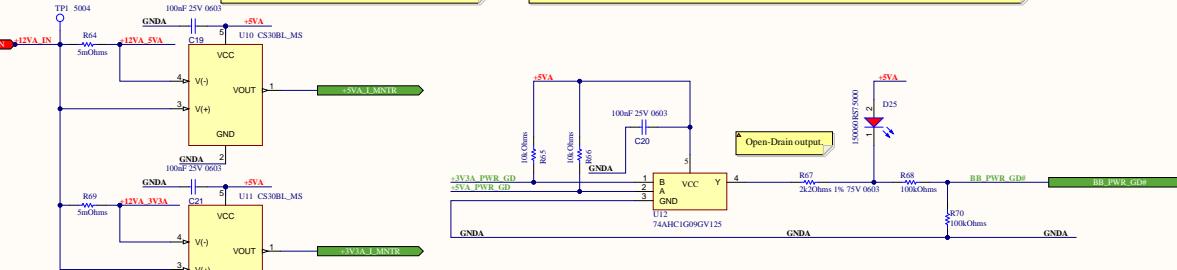
1 | 2 | 3 | 4 | 5 | 6

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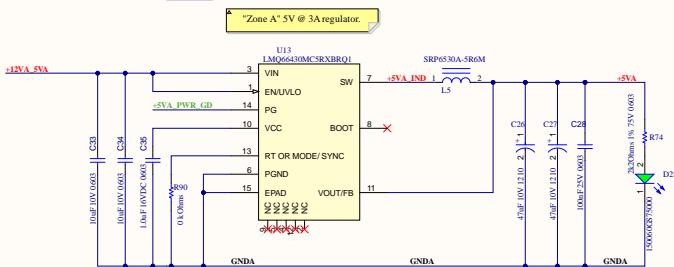
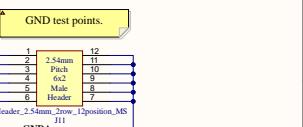
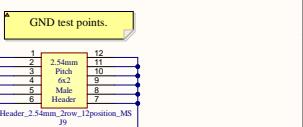
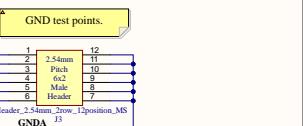
IN PSU current monitored by the non-isolated Physio ADC.

Mainboard 5V and 3V3 SMPS "Power good" flags combined in one output "MB_MPWR_GD" monitored by the SOM0

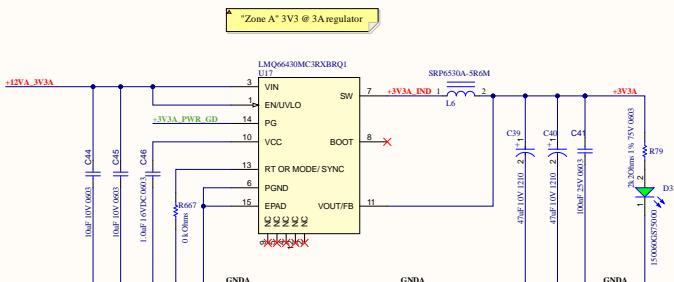
REVISION	DESCRIPTION	DATE	APPROVED
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ZONE A



"Zone A" 5V @ 3A regulator.

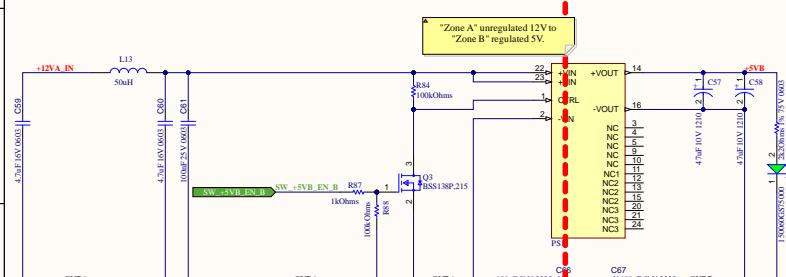
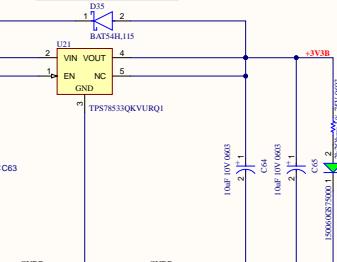


"Zone A" 3V3 @ 3A regulator.

ZONE B (Medical isolation)



"Zone B" Regulated 3V3 @ 1A.

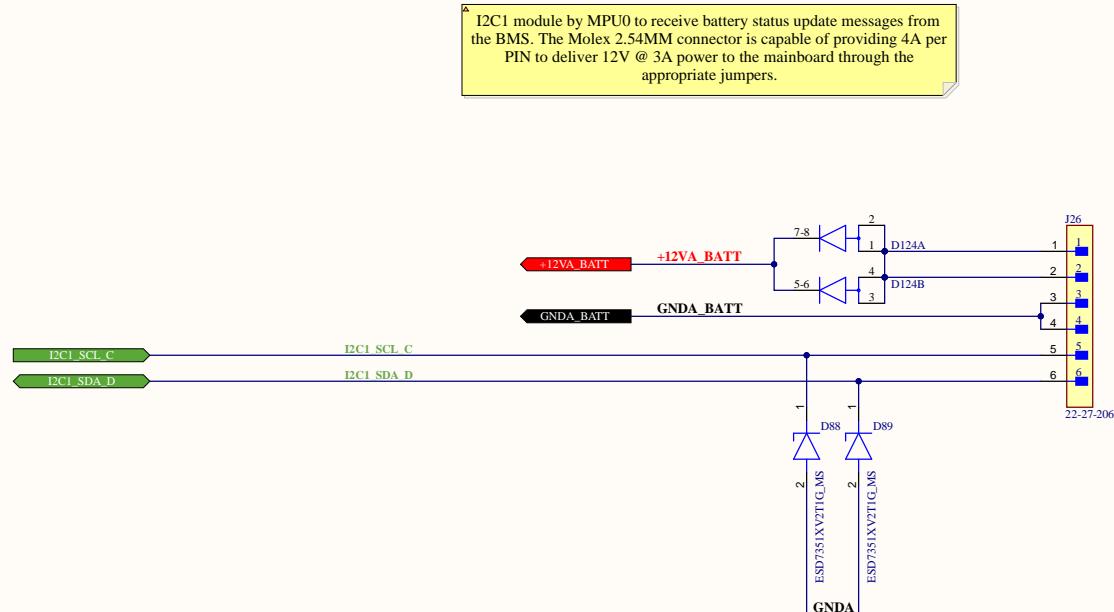
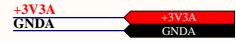


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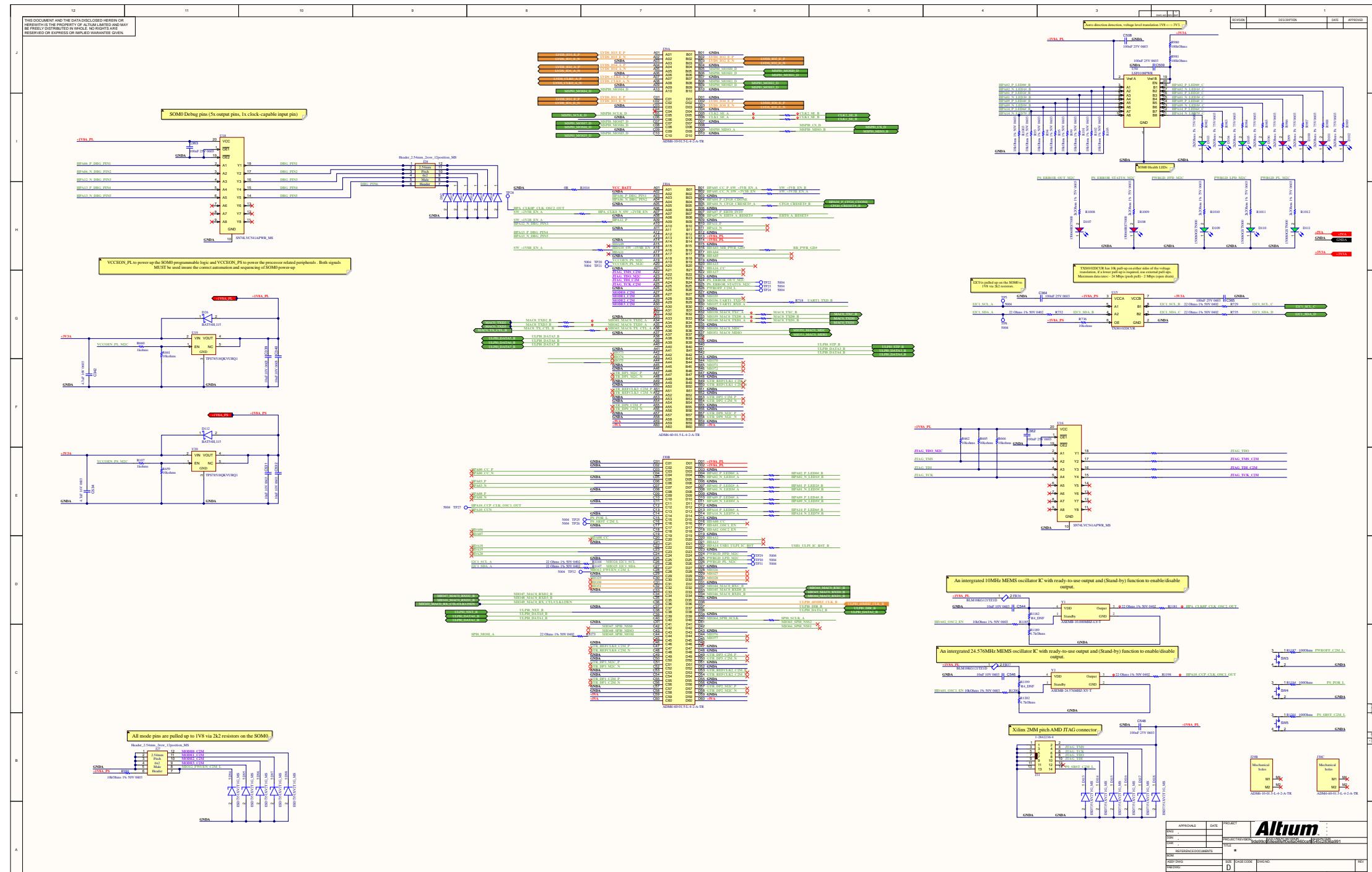
APPROVALS	DATE	PROJECT
ENG:		90e99c152ae9ef7f8a040ccfb54c2435a991
DSN:		DOCUMENT REVISED
CHK:		TITLE
REFERENCE DOCUMENTS	*	
BCM:		
ASSY DWG:		SIZE
FAB DWG:		CAGE CODE
PCB DWG:		DWG NO.
		REV
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		FILE NAME
		pWWR_management.SchDoc
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		* OF *

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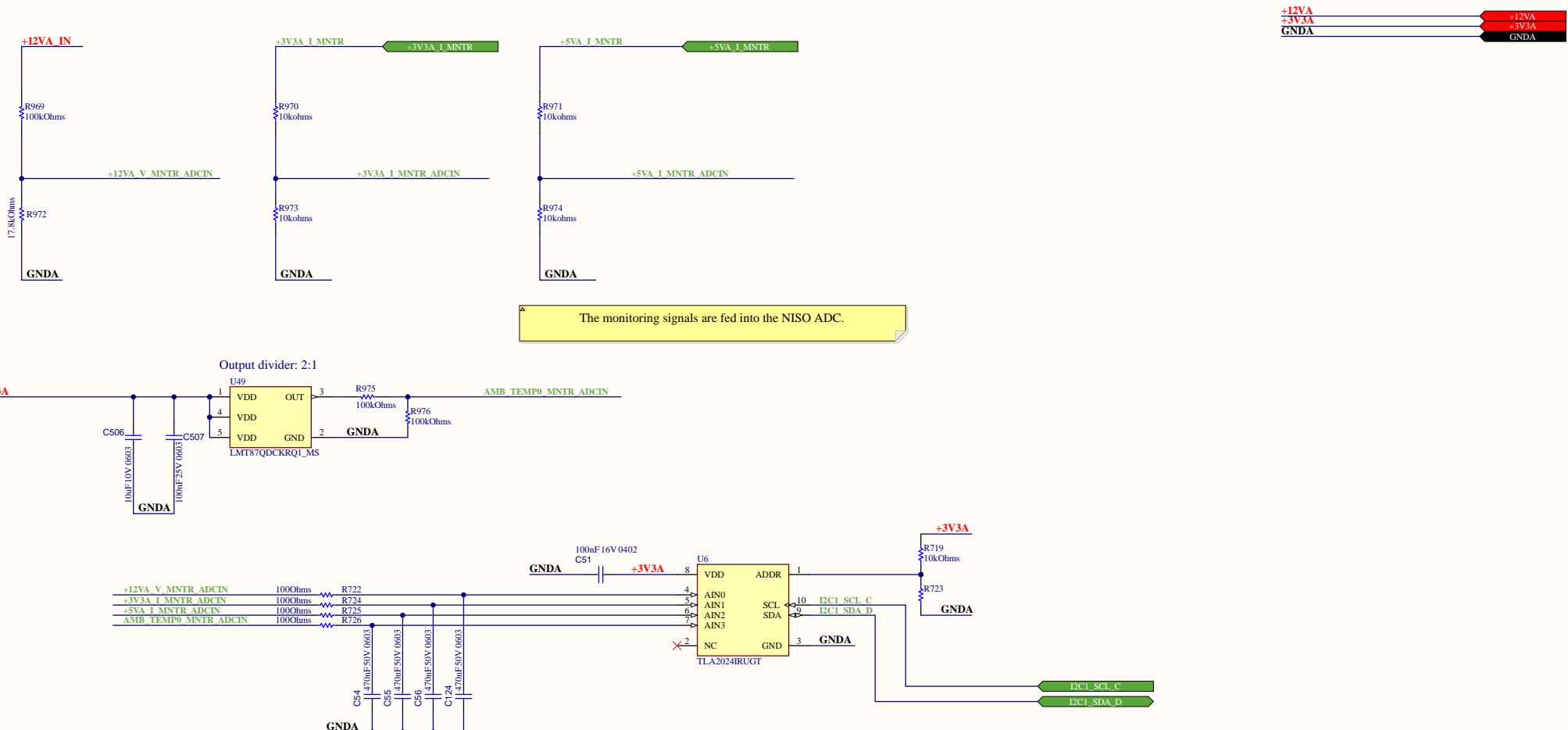
REVISION	DWG. NO.	REV.	ISHT	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT	Altium		
ENG: *		PROJECT REVISION	9de99c058ee8feff0e8a0460cef6545c2836a991		
DSN: *		DOCUMENT ITEM			
CHIC: *		TITLE	*		
REFERENCE DOCUMENTS					
BOM:		ASSY DWG:	SIZE	CAGE CODE	DWG NO.
		FAB DWG:	B		
		PCB DWG:	SCALE:	FILE NAME	SHEET * OF *
				SOM0_BATT_INTERFACE.SchDoc	



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APPROVALS	DATE	PROJECT	Altium
ENG: *		PROJECT REVISION	9de99cd58ee8feff0e8a0460cef545c2836a991
DSN: *		DOCUMENT ITEM	
CHIC: *		TITLE	*
REFERENCE DOCUMENTS			
BOM:		ASSY DWG:	SIZE: B
FAB DWG:		CAGE CODE	DWG NO.
PCB DWG:		SCALE: * OF *	FILE NAME: SOM0_MONITORING.SchDoc SHEET: * OF *

