Modifications for EMC3

Modifications List

Item 1: Modify resistors as per visit to Sundance office.

Item 2: Remove capacitor C2

Item 3: Remove capacitor C4

Item 4: Reconnect R175 to 5V0_REG_OUT instead of 5V0_IN.

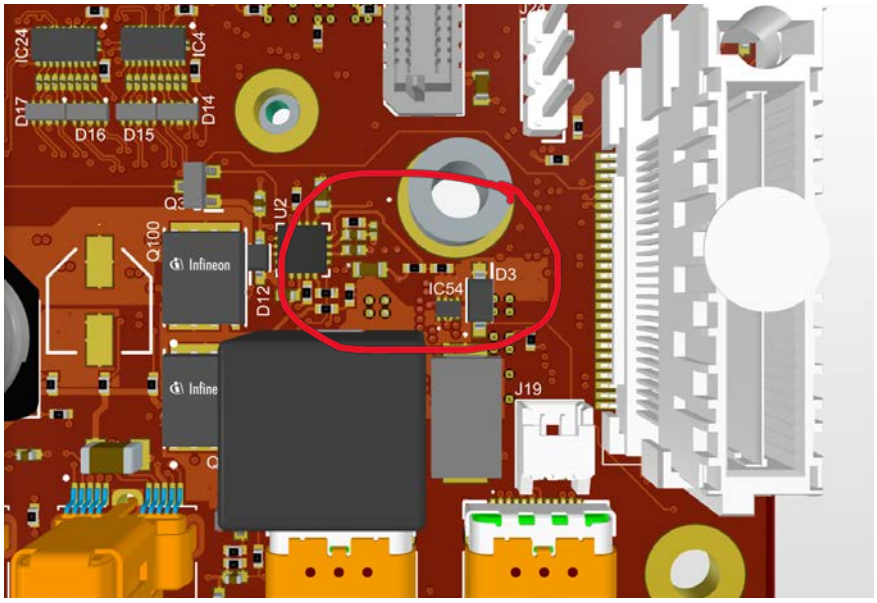


Figure 1: Modification area indicated in RED

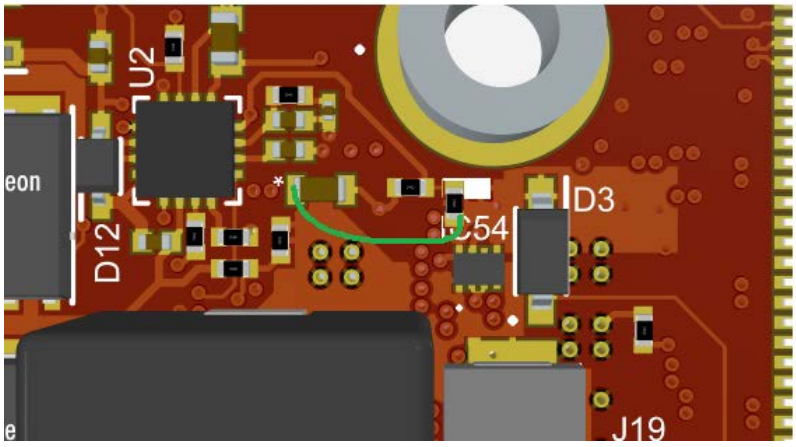


Figure 2: Modification procedure

Rotate R175 through 90 degrees then, keep one end of the resistor on the pad which connects to R 176. Use a piece of wire to connect the other to side of CAP C39.

Item 5: Reconnect R148 to 5V0_REG_OUT instead of 5V0_IN

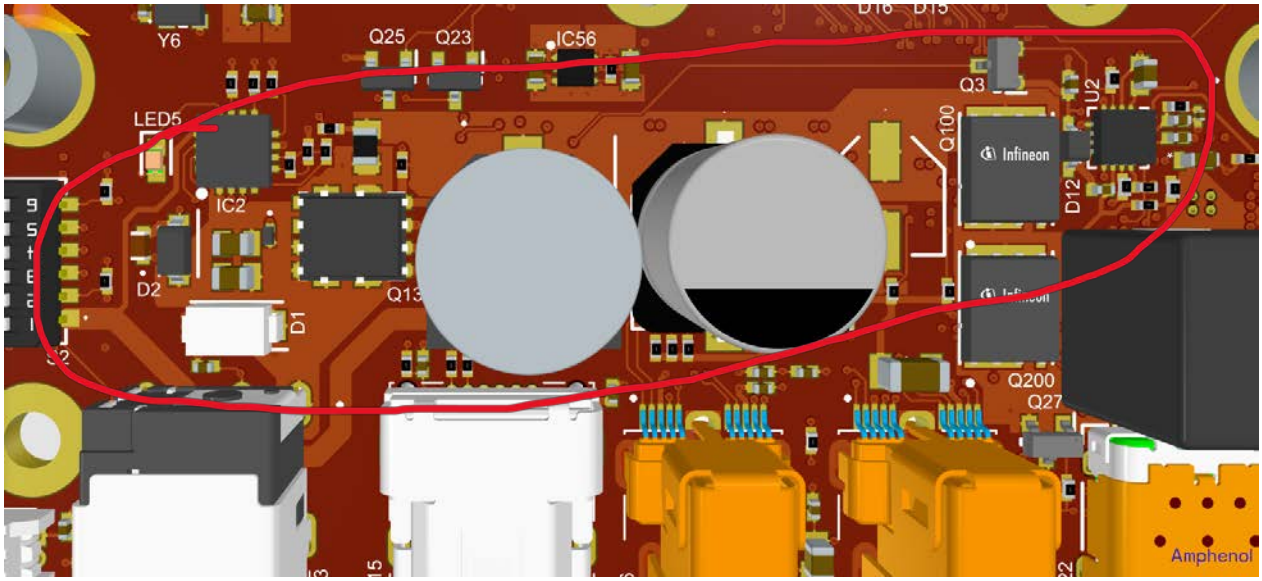


Figure 3: Modification area indicated in RED

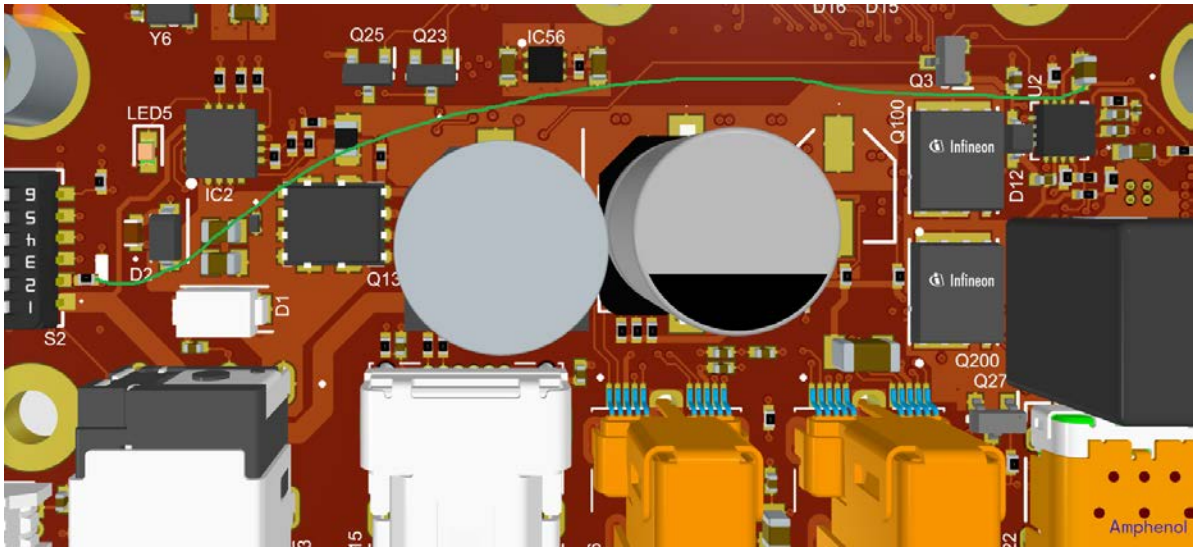
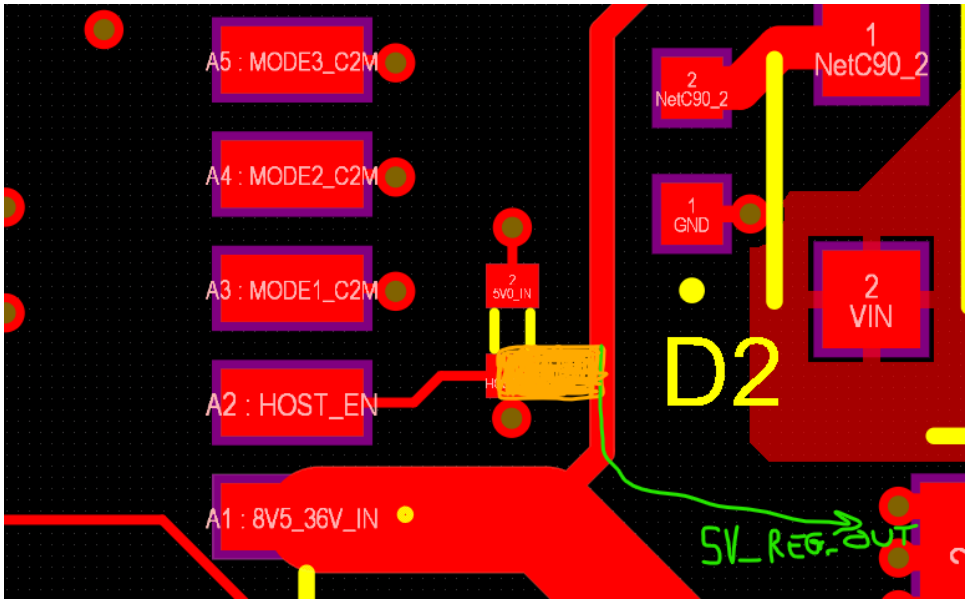


Figure 2: Modification procedure



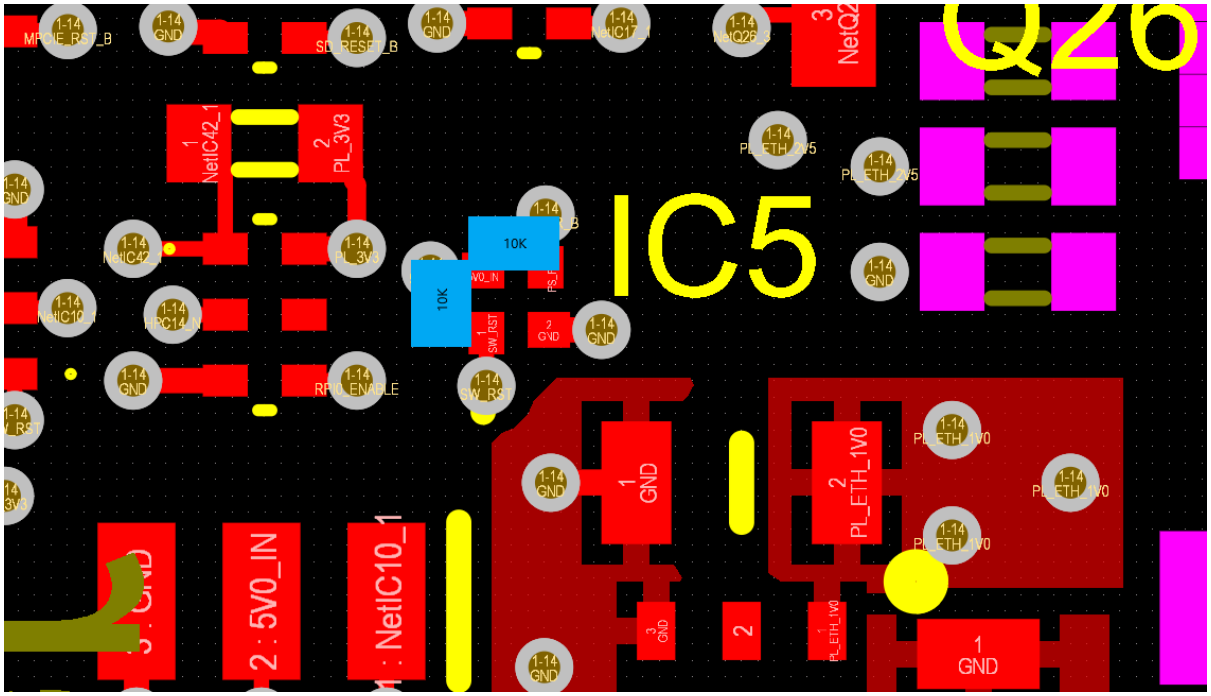
Rotate R148 90 degrees and connect to switch S2, connect the other end of the resistor using wire to CAP C46.

Item 6: Remove IC123

~~Item 7: Fit 10K resistor across pins 8 & 6 of IC123~~

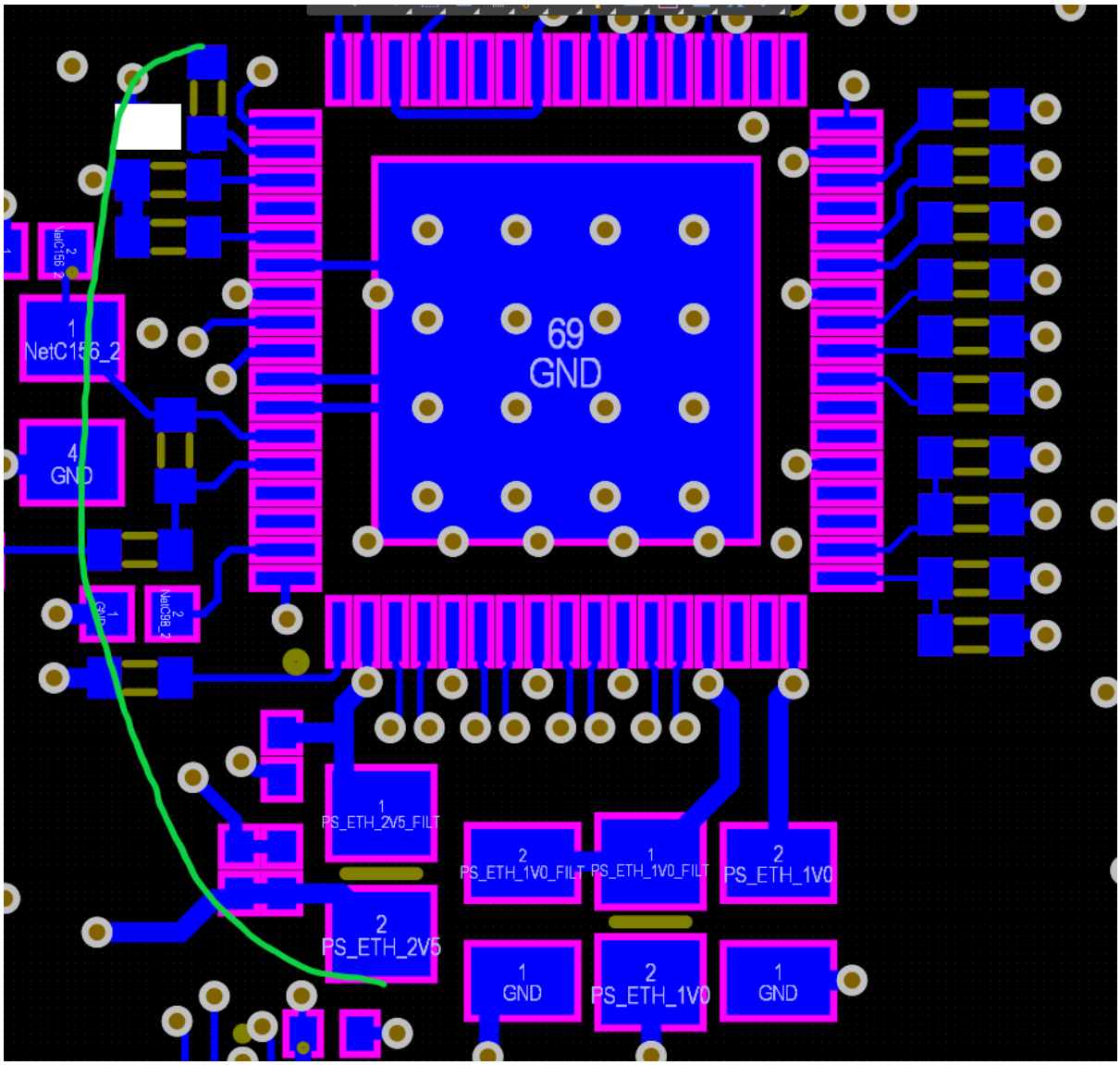
Item 8: Fit two 10K resistor across pins 4 –1 and 4-3 of IC5

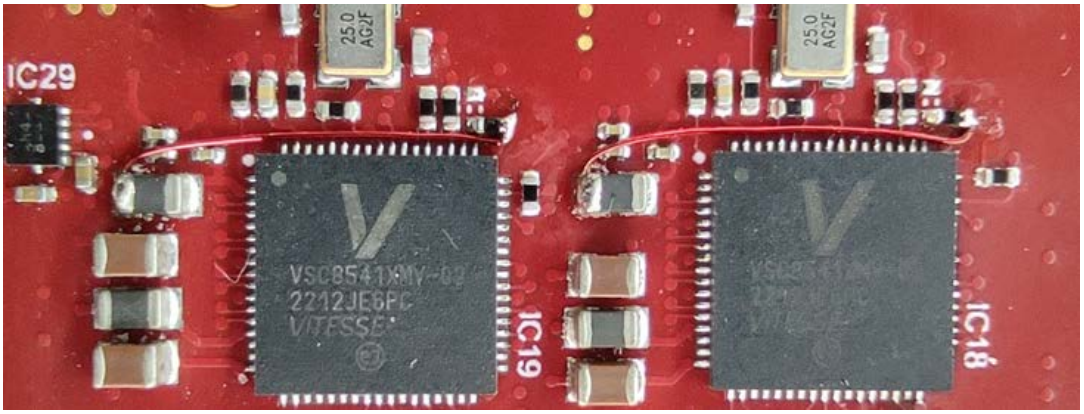
This will disable a global reset on the peripherals and allow individual hardware and software peripheral reset



Item 9: Ethernet PHY for PS & PL requires NRESET to be pulled to 2.5V

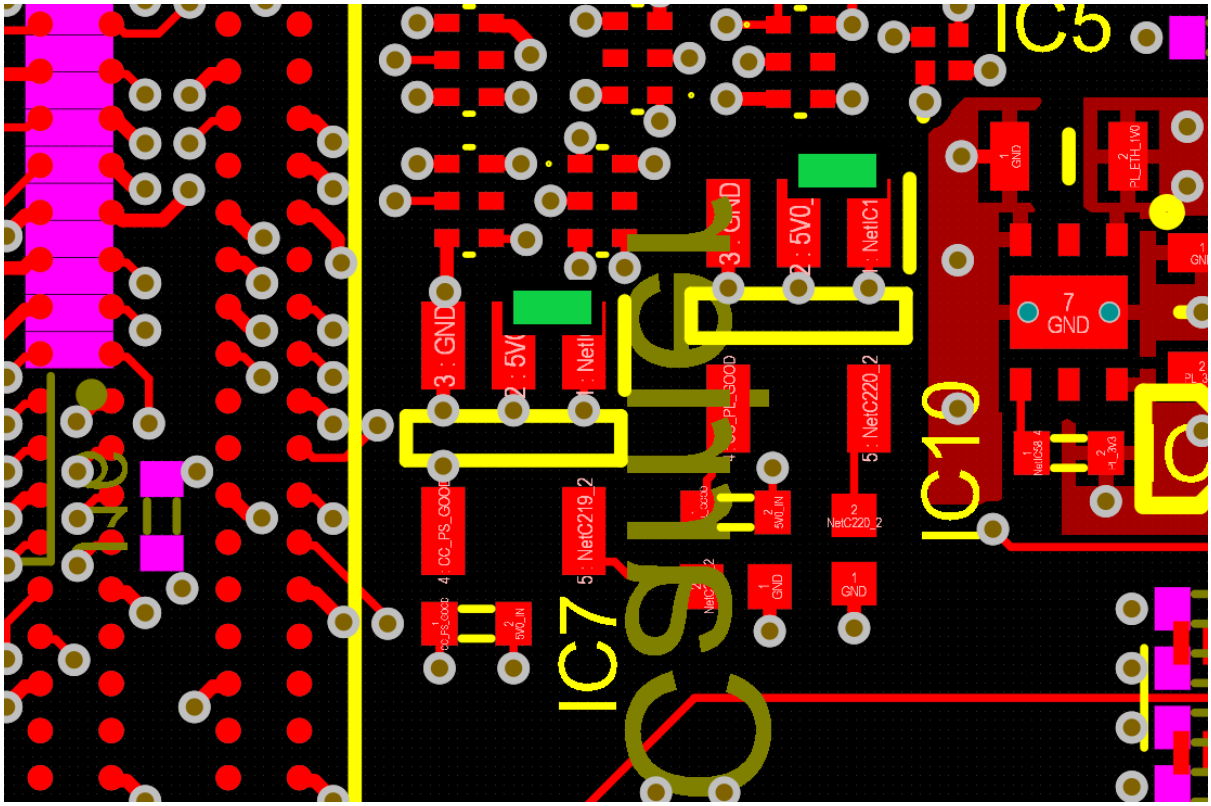
Currently the NRESET signal is tied to 1.8V, the I/O for the NRESET needs a voltage of 2.5V. Both PHY devices IC19 & IC18 require this mod. The modification requires rotating the R13 (PS) and R15 (PL) and connecting the end to a 2.5V supply using a wire. This is shown in the image below.

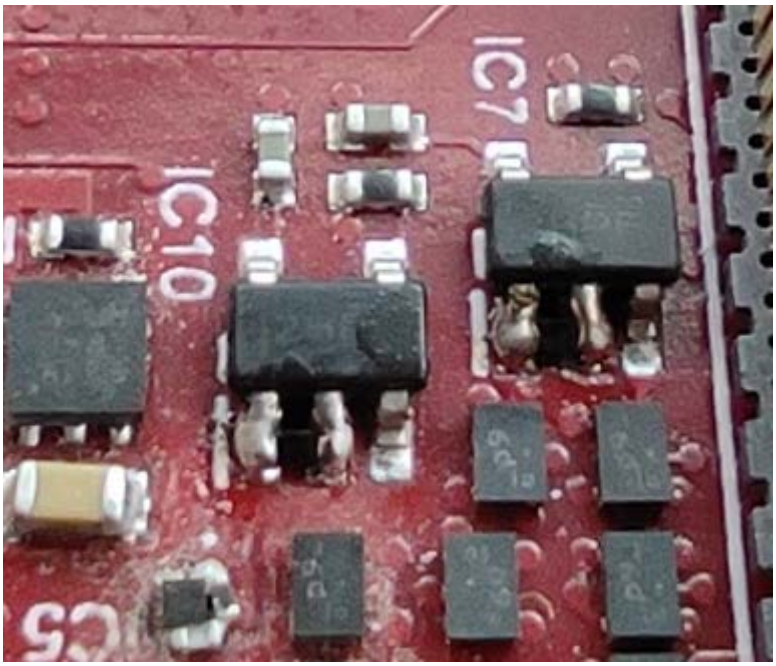




Item 10: Reset ICs require pull up resistor, on IC7 & IC10

The reset IC require a pull up resistor between pins 1 & 2 on both devices. I fitted a 10K 0402 which fits well across the pins.



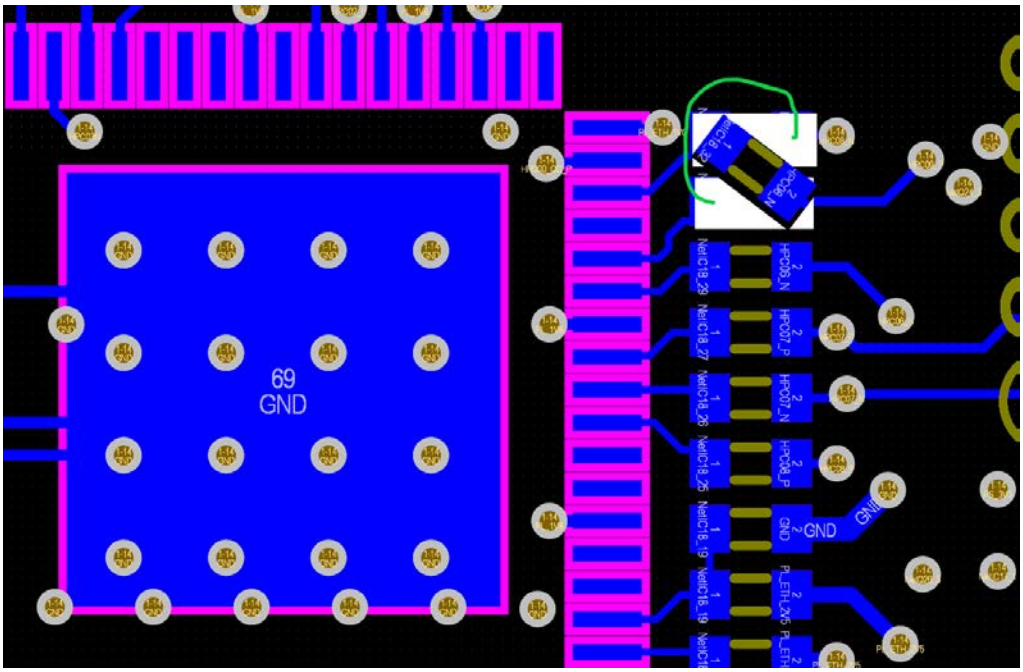


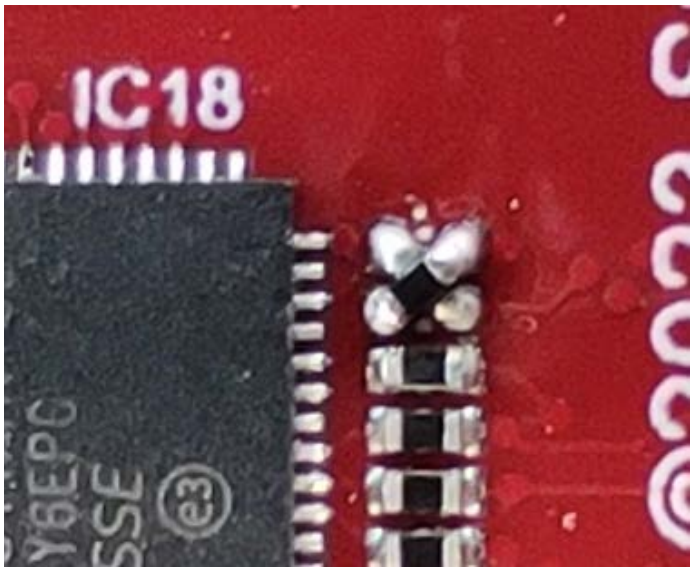
Item 11: RX_CLK to RGMII requires clock pin, swap with RX_CTRL

The RX clock from the PL PHY (IC18) is not on a clock capable pin for the FPGA and fails timing. The CLK and CTRL line can be swapped by;

a. Removing resistors R102 and R104
b. Placing a resistor “diagonally” on the pads between the RX CLK on the PHY and the clock pin of the FPGA
c. Attaching a wire on the pads between the CRTL pin of the PHY and the spare FPGA input

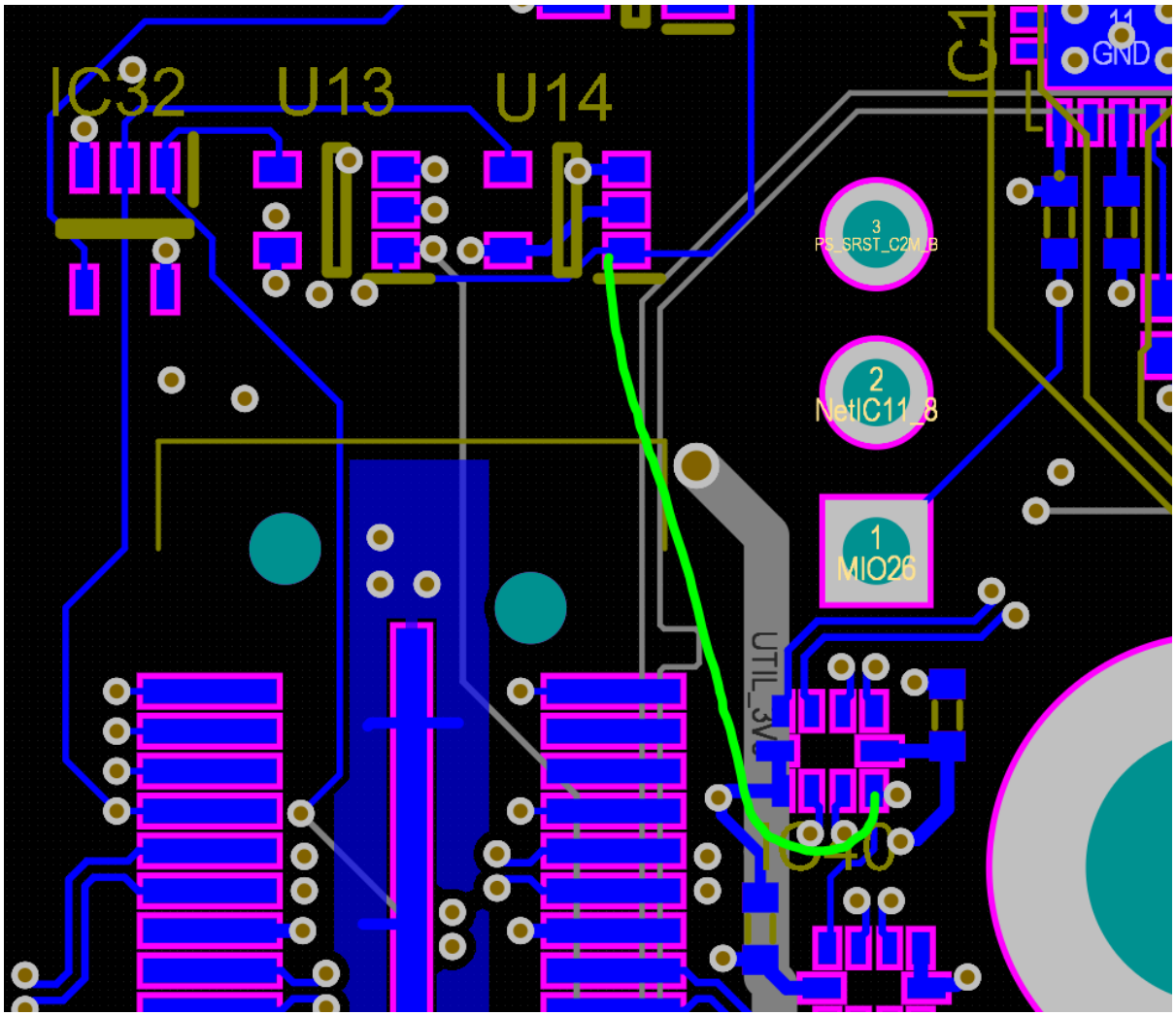
This is shown in the image below, a wire is used to connect the CRLT signal. I used an ~~OR~~ 33r(?) 0603 size part, but I think an 0402 may be better.





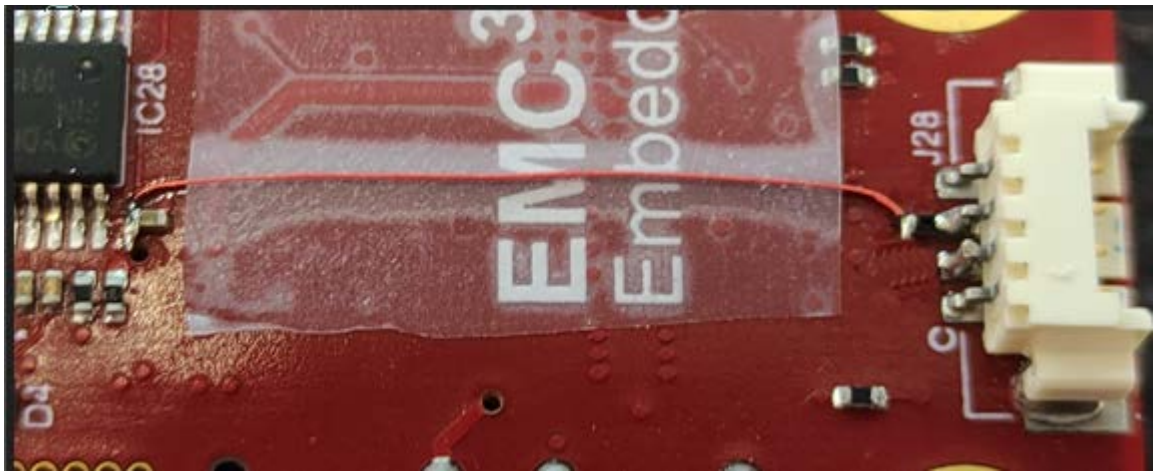
Item 12: Attach wire for PCIe HOST clocks

The switch signal for the PCIe clocks is floating, this needs to be attached by wire to a HOST_EN connection as indicted in the diagram below. Connection is from pin ‘1’ of U14 to pin ‘9’ of IC40.



Item 13: Pull ups for the UARTs.

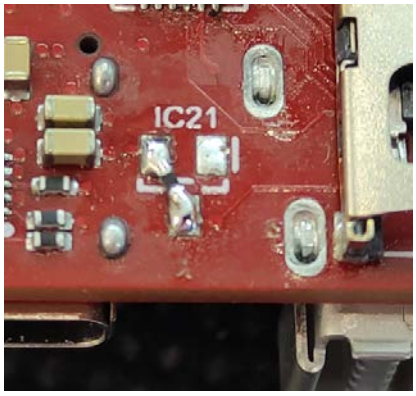
The UART needs a pull up on the TX line
So, pin 3 needs 250R pulling up to 3.3V.



It’s likely that the WIFI module will need it too. Again, a 250R to 3.3V:

Item 14: Make the SD Card work

To get the SD card working IC21 needs to be removed and a bypass 0R resistor need fitting:

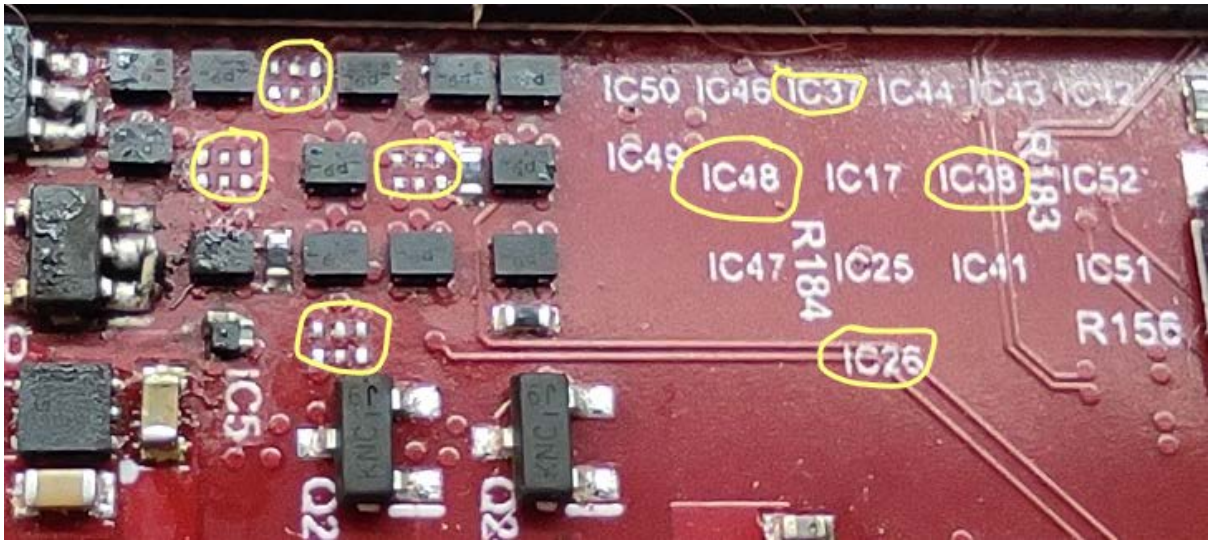


Item 15: Remove 4x AND gates

After more messing around, we (Emilie & myself) determined that the AND gates IC26, IC48, IC37 and IC38 were possibly bad and causing other problems.

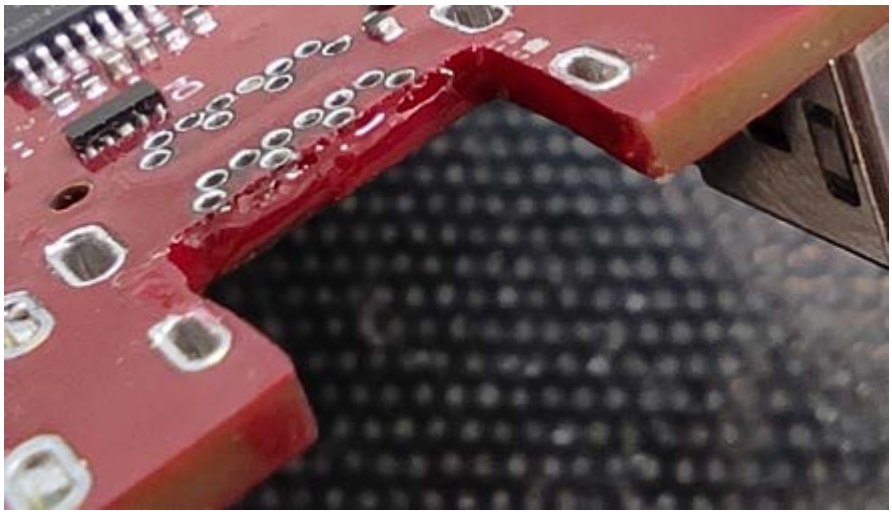
They have been removed as all the control circuits for these have already been disabled already.

It seems to have made things happier.

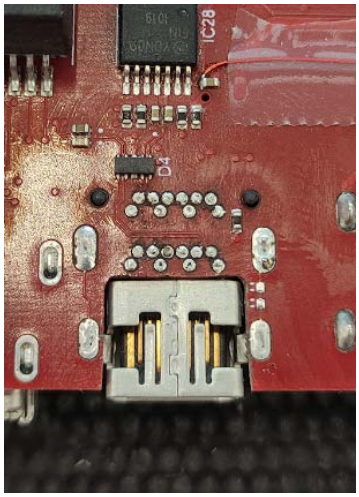


Item 16: File out a hole for the DP connector.

A slot needs filing for the DP connector to fit. There aren't any tracks in there but (after finding out the hard way), there are power planes, so its' best to make the hole slightly larger than needed and then coat the edge with some paint:



Let that dry, then fit the connector. Check the PL_3V3 power supply to ensure there are no shorts.

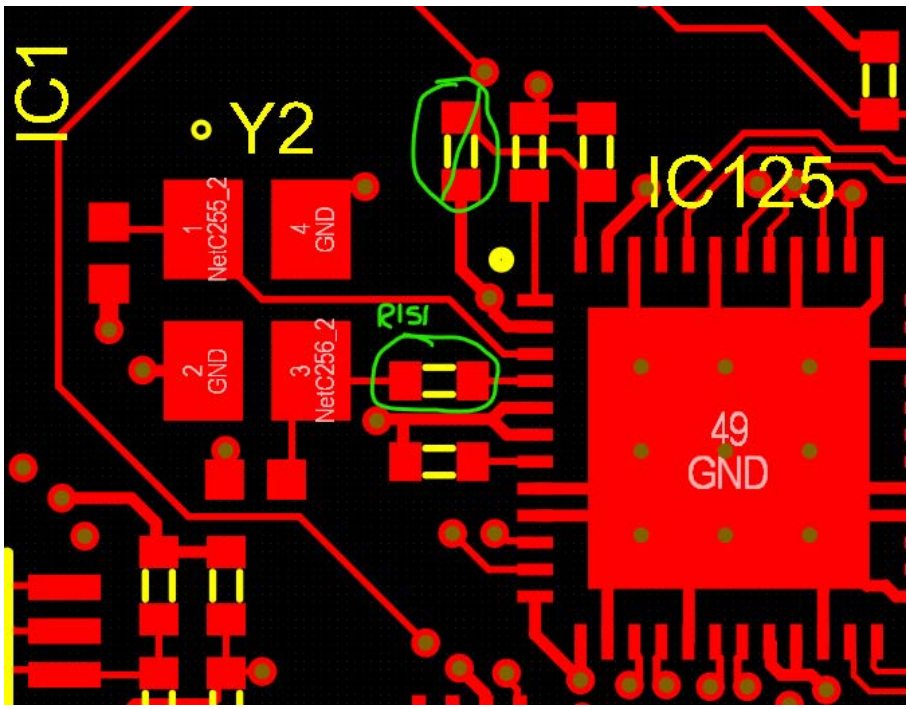


Item 17: Get the 100MHz clock generator working

Remove resistor R264. This should have been a DNF all along.

Change R151 to 33R.

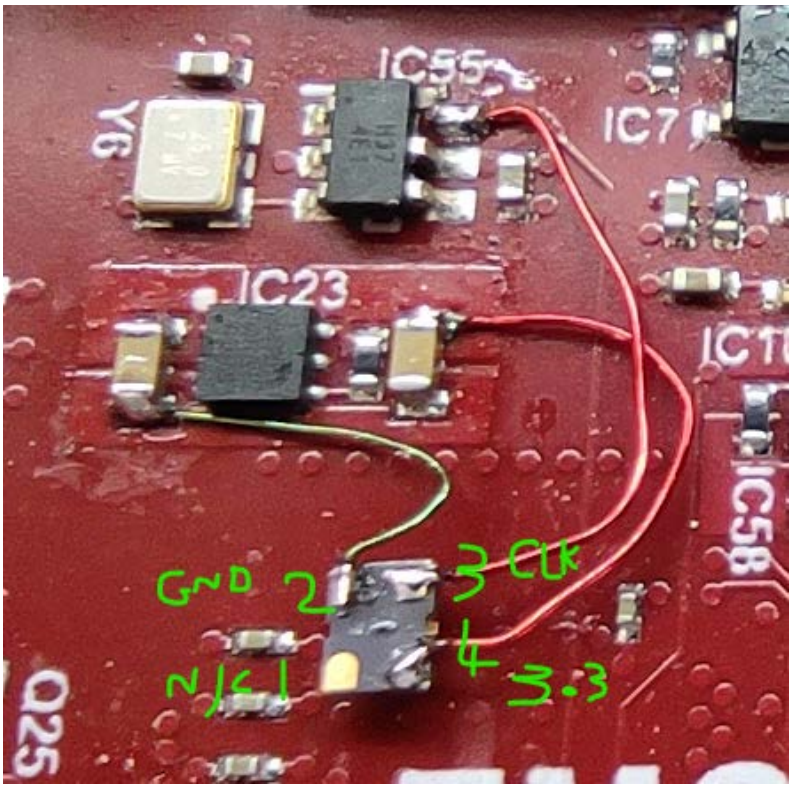
It's possible that C255 and 256 need to be changed to 18pf, but we're not 100% sure.



Item 18: Get a 3.3V clock for the USB hub.

The USB hub needs a 3.3V 25Mhz clock. The one that is currently routed is only 1.8V, so doesn't have enough power.

Lift pin 6 on IC55 and then wire up an oscillator so it outputs the right voltage:



Grab a ECS-2520MV-250-CN-TR osc from the kit (Y6) and wire it as below.

Pin 1 is not connected.

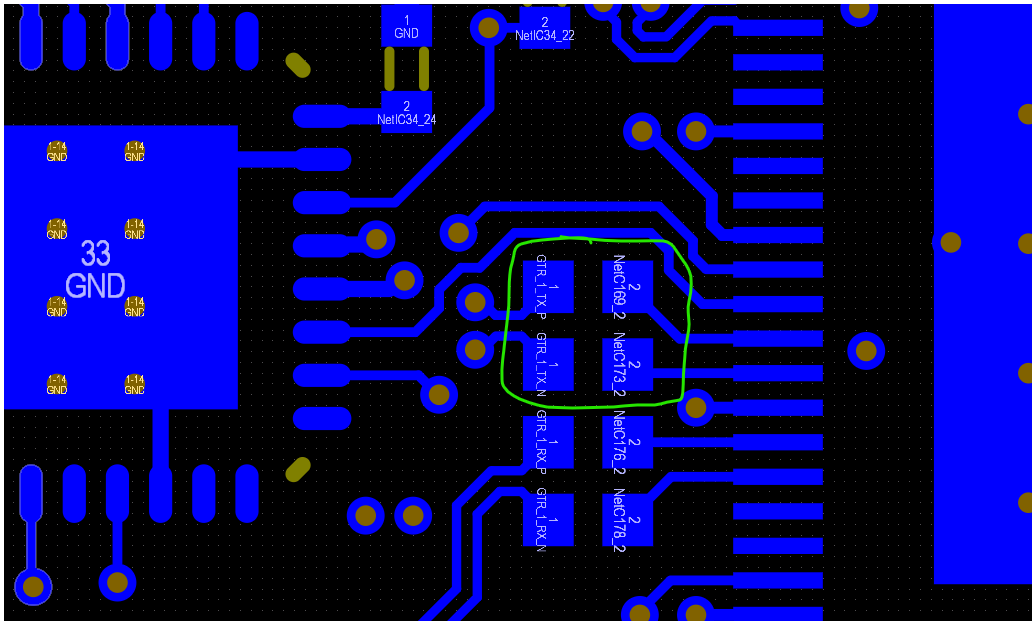
Pin 2 is ground.

Pin 3 is the clock output – Pad 6 of IC55.

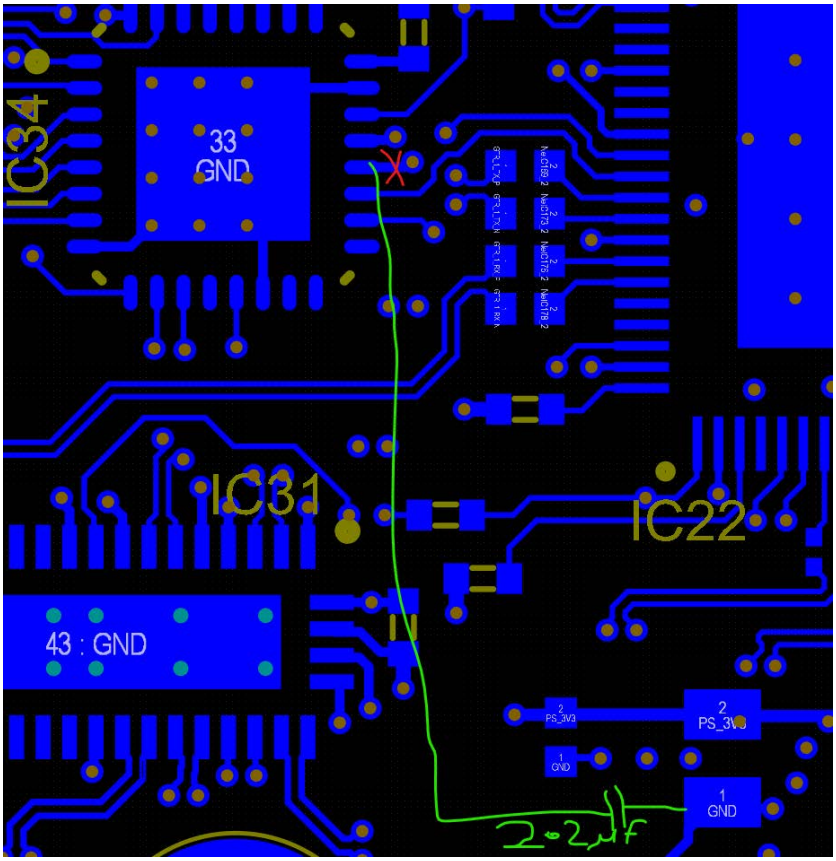
Pin 4 is 3.3V in.

Item 19: USB bits.

Change C169 and C173 to 0R resistors. These are between the USBPHY and the USB hub chip on the bottom.

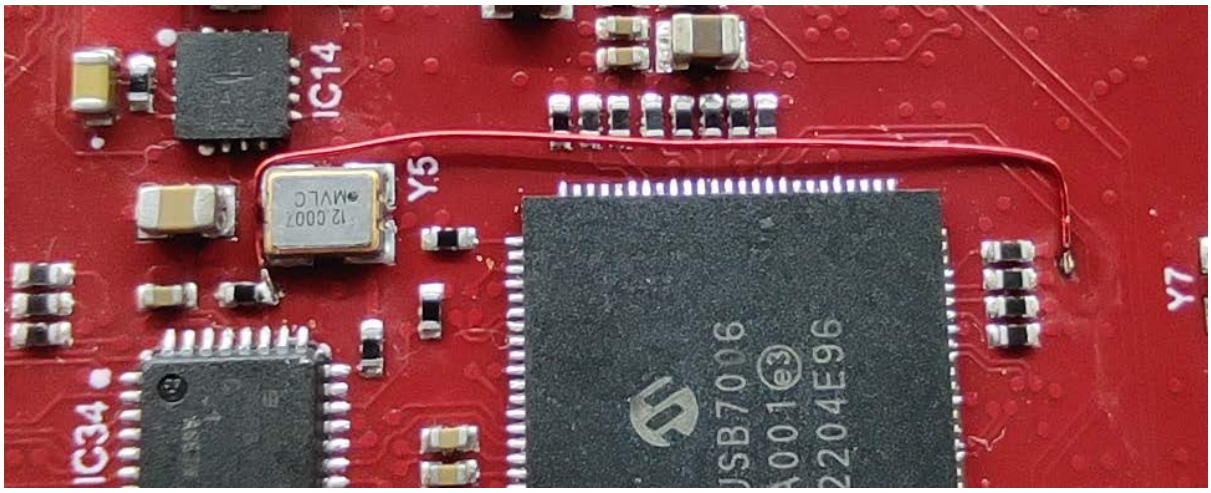


Disconnect pin 20 on IC34 and ground that through a 2.2Uf cap.

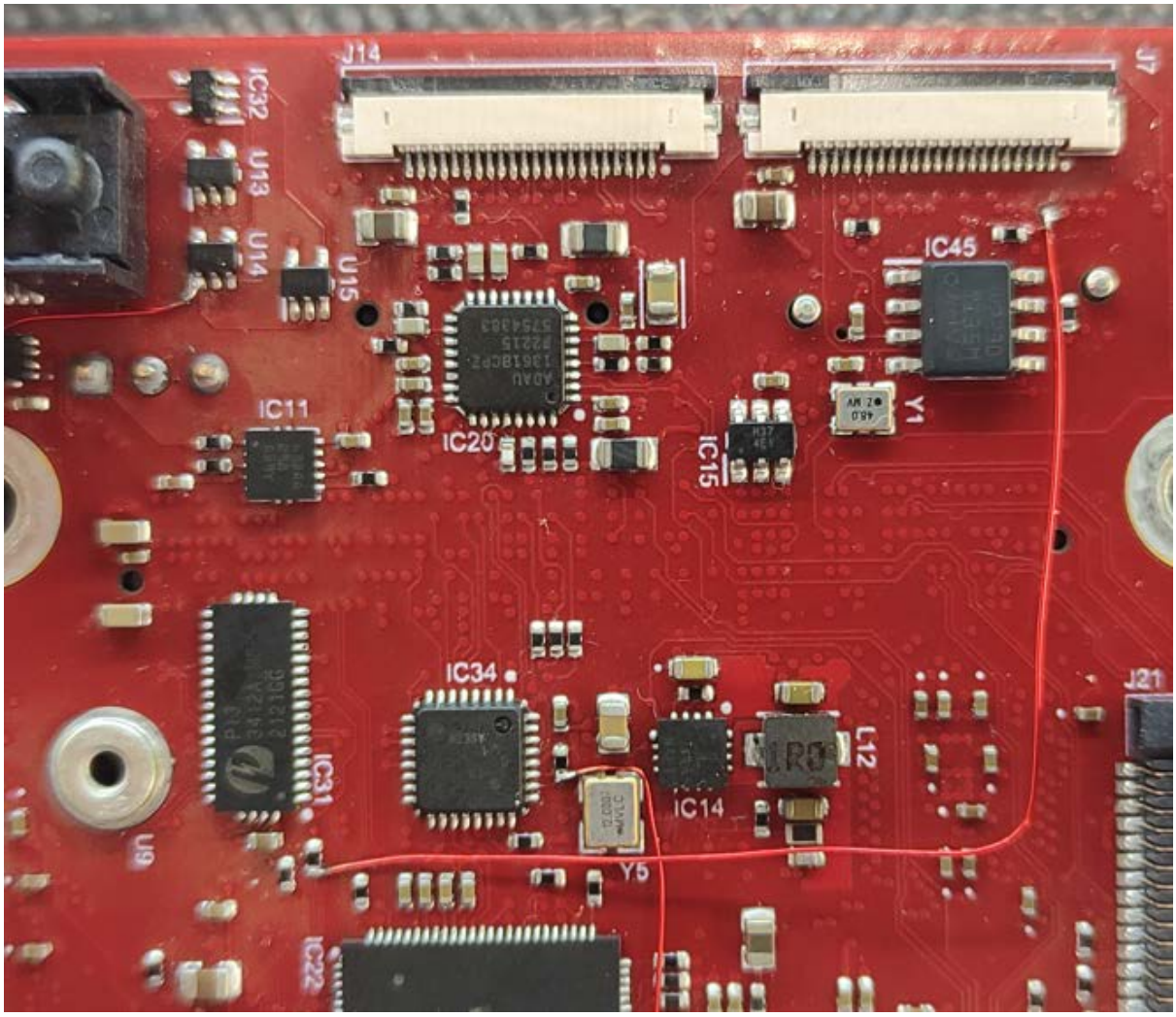


Link the USB PHY’s reset to MIO43:

There is a via to the right of the resistors there.



Link the USB Hub to HDA17:



Item 20: Display port clock

Once the SATA on the board has been tested, replace Y3 with a 135MHz clock

(XLL736135.000000X).

This is required for the display port.

Item 21: Other issues we have found / know of.

Other issues we have run into:

- Many of the AND gates (Page 22 of the schematics) have two different voltage levels (1.8 and 3.3).
  They don't work like that, so a new device / redesign is needed.
- Power supplies take a while to switch on, and sometimes the board needs a couple of goes to power on.
- MIO26 on the watchdog timer doesn't go anywhere
- HDA20 for the fan connector doesn't go anywhere