Memristor-Based Circuit Design for Neuron With Homeostatic Plasticity

Xinming Shi, Zhigang Zeng, *Senior Member, IEEE*, Le Yang, and Yi Huang

***Abstract*—The nonvolatility and resistance variability of memristor make it a candidate for emulating complex dynamic behaviors in the neural system. In this paper, the memristive neuron with homeostatic plasticity is implemented. The memristor is applied to the neuron circuit, and its memristance represents the membrane sensibility of neurons. Composed of a trigger module, a pulse generation module and a feedback module, the memristor-based neuron can adaptively adjust the firing rate of neuron and maintain it in the inherent firing rate range, which shows similarities to its biological counterpart. The proposed design can mimic firing rate behaviors of the electrophysiological experiment performed in rodent, where the homeostatic plasticity of neuron is inhibited by sleep signal and promoted by wake signal. Furthermore, all the simulations are conducted in Cadence PSPICE, and the functionality of the design is proved with the simulation.**

***Index Terms*—Memristor, neuron circuit, homeostatic plasticity, PSPICE.**

I. Introduction

A HUMAN brain has approximately 10^{11} neurons and 10^{14}–10^{15} synapses. A number of neurons and synapses interconnect with each other to transfer information, which is the foundation of different complex functions in the neural system [1], [2]. Neurons have the abilities of receiving, combining, and transferring information, while synapse is the junction between two neurons to transfer information. As one of the major forms of neural plasticity, homeostatic plasticity is the stabilizing activity that can maintain the firing frequency of neural system within a certain range, which stabilizes the brain function with respect to the external environment changes [3].

Several electrical and computer engineering researchers work at device level to study and simulate biological systems as well as their neural plasticities [4]. The majority of researches have used established analog and digital technologies with CMOS devices to implement a variety of characteristics of synapses [5], [6], and there have been many very large-scale integration (VLSI) neuromorphic approaches to emulate synaptic plasticities [7], [8]. Attempts have been made to mimic the dynamic behaviors of neuron by conventional CMOS devices [9] or analog integrated circuit [10], [11]. In addition, homeostasis mechanisms have also been encapsulated into the circuit to stabilize the network's activity in spiking neuromorphic systems [4]. For example, Liu *et al.* proposed silicon synaptic adaptation mechanisms to implement the homeostasis in a VLSI network of neurons [12]. Bartolozzi *et al.* designed an analog circuit to implement homeostatic plasticity mechanisms in VLSI spiking neural networks [13]. However, another homeostasis mechanism, the intrinsic homeostatic plasticity that reflects the neuron behavior, is scarcely implemented on hardware. Furthermore, since the complexity of CMOS synapses and neurons constrains their application in large scale integration, it is supposed to adopt another way into the implementation of homeostatic plasticity.

The invention of memristor is a milestone in the research of neural network circuit implementation. The memristor appeals numbers of researchers since its first theoretical postulation by Chua [14]. HP Labs first announced the realization of TiO_2 based memristor in 2008 [15], then the physical devices such as spintronic memristors [16], tantalum oxide memristors [17], ferroelectric memristors [18] etc, have become a major focus of research. Considering their special properties including non-volatility, nanoscale dimensions, low power consumption, and the ability to be programmed [19], the synaptic plasticity characteristics can be well implemented and mimicked by memristors. In spiking neural network, memristors were used to emulate synapse with different plasticities of neural system such as pair spike timing dependent plasticity (PSTDP), triplet spike timing dependent plasticity (TSTDP) and spike rate dependent plasticity (SRDP) [20]–[24] as well as other bio-inspired learning rules [25]. There have also been a variety of memristor-based synaptic implementations with crossbar for other neural networks and applications such as the Hamming distance comparator [26], the multilayer neural network [27], [28], winner-take-all [29], [30], and convolutional neural networks [31], [32]. Furthermore, memristor has also been used in implementing neurons, it can achieve the accumulative behavior that the neuron will fire after a certain number of received pulses [33]. Wright first suggested the use of phase change memory (PCM) devices for neuronal realization [34]. Tuma *et al.* recently proposed a PCM-based neuron that can integrate postsynaptic inputs [35]. Al-Shedivat *et al.* proposed stochastic artificial

Manuscript received October 23, 2017; revised January 20, 2018 and February 23, 2018; accepted April 1, 2018. Date of publication September 20, 2018; date of current version September 21, 2018. The work was supported in part by the Natural Science Foundation of China under Grants 61673188 and 61761130081, in part by the National Key Research and Development Program of China under Grant 2016YFB0800402, in part by the Foundation for Innovative Research Groups of Hubei Province of China under Grant 2017CFA005, and in part by the Fundamental Research Funds for the Central Universities under Grant 2017KFXKJC002. *(Corresponding author: Zhigang Zeng.)*

The authors are with the School of Automation, Huazhong University of Science and Technology, Wuhan 430074, China, and also with the Key Laboratory of Image Processing and Intelligent Control of Education Ministry of China, Wuhan 430074, China (e-mail: M201672506@hust.edu.cn; zgzeng@hust.edu.cn; yljiayou12@hust.edu.cn; huangyihust@hust.edu.cn).

Digital Object Identifier 10.1109/TETCI.2018.2829914

neurons using TiO_x-based resistive memory devices [36]. However, these memristor-based neurons did not act the behavior of homeostatic plasticity. In some related researches, the homeostasis-type rule of neuron has been implemented, in addition, these homeostasis-type rules of neuron have been confirmed extremely valuable in pattern recognition [37], [38]. However, these homeostasis-type rules were only realized by software which is carried out by serial computing with separated data storage and computation units. Therefore, a hardware implementation of the memristive neuron with homeostatic plasticity is valuable.

Compared to previous works, based on conventional CMOS devices, memristive realization of synapse and neuron is more biomimetic, which makes it easier to emulate biological functions. This paper proposes a memristor-based neuron circuit which consists of a trigger module, a pulse generator module and a feedback module, where the homeostatic plasticity mechanism of neuron is realized. Finally, the neuron can adaptively adjust the firing rate of the output pulse and maintain its inherent firing rate. The mathematic relation between the neuron's firing rate and memristance in the neuron is established quantitatively. Furthermore, the proposed memristor-based neuron circuit can emulate the firing behaviors of visual cortex neuron in the monocular deprivation experiment [39].

The rest of this paper is organized as follows. Section II introduces the mechanism of homeostatic plasticity. The memristive neuron with homeostatic plasticity is explained in Section III. Experimental results and circuit performance analysis are presented in Section IV, and the conclusions are drawn in Section V.

II. Homeostatic Plasticity

In the central neural system, the neural plasticity has a variety of forms, typically the Hebbian and homeostatic plasticity [40]. However, the positive-feedback nature of hebbian mechanism will destabilize the properties of neuronal networks. Hence, homeostatic plasticity, which can ensure the stabilization of neural networks, is indispensable in neural system [41].

Homeostatic plasticity has two forms reflected in synapse and neuron respectively as shown in Fig. 1. First, the strength of all of their synapses can be regulated to maintain a target firing level of neuron, it is called synaptic homeostasis. As shown in Fig. 1(a), if the input of excitatory synapse is so weak that the spike frequency of neuron cannot reach the target firing level, the excitatory inputs can be strengthened to approach the firing frequency to the target level, on the contrary, the excessive firing frequency also can be reduced to the target level. Second, the regulating sensitivity of a neuron, which can change both of excitatory and inhibitory inputs, is called intrinsic homeostasis [42]. As shown in Fig. 1(b), if the average firing rate is too low, the depolarizing channel that represents the input signal can be up-regulated and the hyperpolarizing channel that represents the output signal can be down-regulated to increase the firing frequency to an appropriate level. In order to realize the homeostatic plasticity of neuron, a memristor-based neuron circuit is designed in this paper.

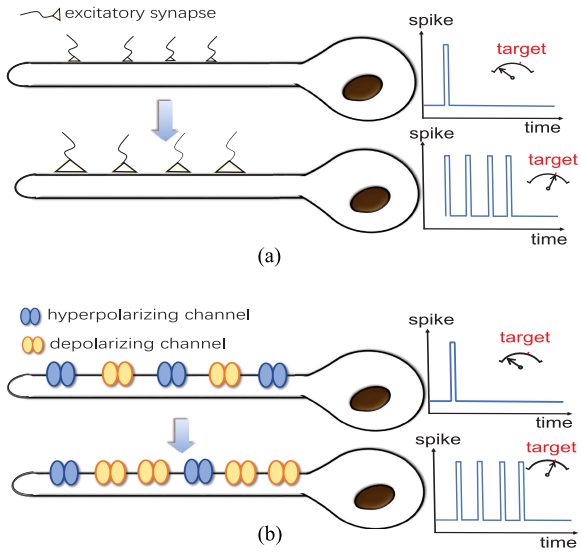

Fig. 1. Diagram of two homeostatic regulations. (a) Synaptic homeostatic regulation, the triangle represents excitatory synapse and its size defines the strength of excitation. (b) Intrinsic homeostatic regulation, the blue circle represents hyperpolarizing channel and yellow circle represents depolarizing channel. Its number defines the sensibility of neuron membrane.

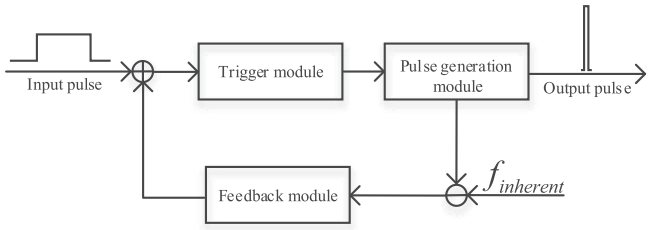

Fig. 2. Feedback control of the neuron circuit.

III. Memristive Neuron With Homeostatic Plasticity

In this paper, we propose a memristor-based neuron circuit to emulate homeostatic plasticity of neural system. Abstractly, homeostatic plasticity is an example of feedback control. In our design, the memristive neuron has three modules, the trigger module, pulse generation module and feedback module. The three modules, whose schematic representation is shown in Fig. 2, cooperate with each other acting as a feedback control model.

A. Memristor Model

To emulate the intrinsic homeostatic plasticity, the circuit configuration that can implement the sensibility of membrane must be designed. A voltage-driven memristor model such as the one proposed in the Vourkas' research in 2015 is chosen to realize this function, and it explains the nonlinear behaviors of quantum tunneling. In addition, this model also includes the consideration of programming thresholds, the low complexity of the equations of the model, and the support for high working frequencies of the applied signals [43]. These metrics totally meet our needs. The equivalent circuit of the memristor model is depicted in Fig. 3.

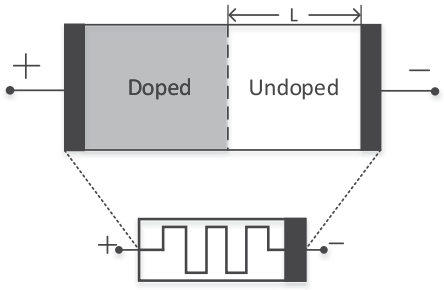

Fig. 3. The construction of the utilized memristor model and the device symbol of memristor used in this paper.

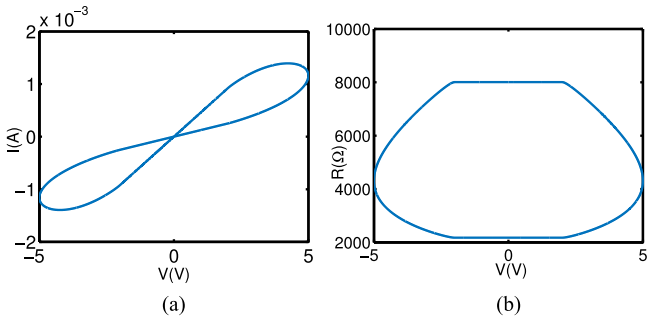

Fig. 4. (a) The current-voltage characteristics of the utilized memristor. (b) Memristance characteristics of the utilized memristor.

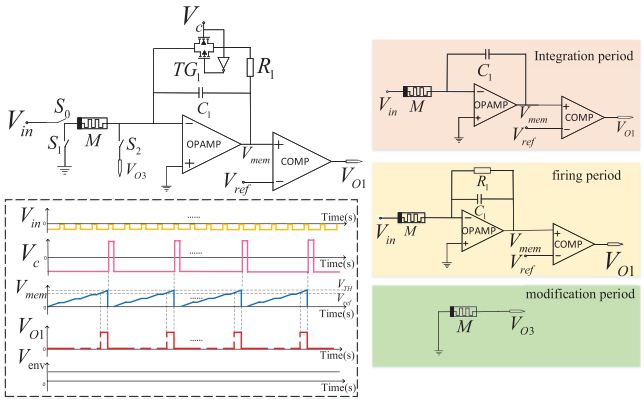

Fig. 5. Schematic diagram of trigger module and three equivalent circuits in integration period, firing period and modification period respectively, where C_1 is 250 nf and R_1 is 100 Ω. The chart shows the theoretical variation process of $V_{\rm in}$, V_c, V_{mem}, V_{o1}. The yellow line represents $V_{\rm in}$ which is the input signal of neuron; the pink line represents V_c which is the control signal of trigger module; the blue line represents V_{mem} which indicates the variation of membrane voltage; the red dot line represents the V_{o1} which is the output of trigger module; the gray line represents the V_{env} which determines whether the feedback signal can apply to the two terminals of memristor M.

Its general definition can be written as:

$$I(t) = G(L(t), t)V_M(t) \tag{1}$$

$$\dot{L}(t) = f(V_M(t), t), \tag{2}$$

where $L(t)$ is defined as the tunnel barrier width, $\dot{L}(t)$ is the change rate of $L(t)$, $G(L(t), t)$ is the memristors conductance. The current and applied voltage are $I(t)$ and $V_M(t)$ respectively.

The memristance of this model is defined as

$$R(L_{V_M,t}) = f_0 \frac{e^{2L_{V_M,t}}}{L_{V_M,t}}, \tag{3}$$

where f_0 is a model fitting parameter, $L_{V_M,t}$ is the tunnel barrier width which is related to the applied voltage V_M and time t. Its mathematical formula follows

$$L(V_M, t) = L_0 \cdot \left[1 - \frac{m}{r(V_M, t)}\right], \tag{4}$$

where L_0 is the maximum value that $L(V_M, t)$ can attain, and m is a fitting parameter that determines the boundaries of the barrier width. According to the experimental data of the physical structure of memristive devices, the switching rate of L is small (fast) when the applied voltage is above (below) to the threshold voltage (V_{SET} or V_{REST}). $r(V_M, t)$ reflects this property, and its gradient is defined as

$$\dot{r}(V_M, t) = \begin{cases} a \cdot \frac{V_M + V_{th}}{c + |V_M + V_{th}|}, & \text{if } V_M \in [-V_0, V_{REST}) \\ b \cdot V_M, & \text{if } V_M \in [V_{REST}, V_{SET}] \\ a \cdot \frac{V_M - V_{th}}{c + |V_M - V_{th}|}, & \text{if } V_M \in (V_{SET}, +V_0], \end{cases} \tag{5}$$

where a, b, c are fitting constants which reflect the rate of memristor change, and V_{th} is the threshold voltage of memristor. In this paper, this memristor model is simplified to impose a hard switching behavior by setting b to zero. So the initial states of memristor in every period can be available. In the duration of Δt, V_M is a constant, so the parameter that determines both the device dynamics and the corresponding state, $r(V_M, t)$, can be simplified as

$$r(V_M, t) = \begin{cases} r_0 - \Delta t a \cdot \frac{V_M + V_{th}}{c + |V_M + V_{th}|}, & \text{if } V_M \in [-V_0, V_{REST}) \\ r_0, & \text{if } V_M \in [V_{REST}, V_{SET}] \\ r_0 - \Delta t a \cdot \frac{V_M - V_{th}}{c + |V_M - V_{th}|}, & \text{if } V_M \in (V_{SET}, +V_0], \end{cases} \tag{6}$$

where r_0 is the initial state of the memristor, Δt is the duration during which the over-threshold voltage is applied to the memristor. The current-voltage and memristance characteristics of the utilized memristor are demonstrated in Fig. 4. The threshold voltage of memristor is set to |2| V and the memristance is limited in the range [2 kΩ, 220 kΩ].

B. Trigger Module

The trigger module is based on the principle of leaky integrate-and-fire (LIF) model, which is simple to implement, and particularly attractive for large-scale network simulations [44]. In this paper, we propose a trigger module which utilizes a memristor to substitute the resistor of LIF neuron model, its equivalent circuit schematics for different phases are shown in Fig. 5. To understand the circuit principle, the detailed relation between states of switches S_0, S_1, S_2 and circuit phases are shown in Table I.

The neuron circuit operates in three different phases, integration, firing, and modification, controlled by the trigger module.

TABLE I
CIRCUIT PHASES AND SWITCH STATES

Circuit phases	S_0	S_1	S_2	V_c
Integration	Closed	Open	Open	LOW
Firing	Closed	Open	Open	HIGH
Modification	Open	Closed	Closed	HIGH

When the circuit operates in the integration period, V_c is low, S_0 is closed, S_1 and S_2 are open; when the circuit operates in the firing period, V_c is high, S_0 is closed, S_1 and S_2 are open. When the S_1 and S_2 are closed, S_0 is open, the circuit will operate in period of modification. To illustrate more clearly, V_c controls the states of the CMOS transmission gate which will be abbreviated to TG further. When V_c is low, the TG turns off, which indicates that the leaky path is cut off, and the negative input signal V_{in} flows through the reverse integration circuit structure to increase the membrane voltage V_{mem}. V_{mem} can be written as

$$V_{mem} = -\frac{1}{R_M C_1}\int_o^t V_{\text{in}}(s)ds. \tag{7}$$

When the V_c is high, the TG is turned on, and it induces C_1 to fully discharge through R_1, which will rest V_{mem} to 0. Considering that the pulse generator module is triggered by the signal with falling edge, V_{ref} shown in the schematic is little smaller than the real threshold voltage of neuron, V_{TH}. V_{o1} is the output of the trigger module which represents whether V_{mem} exceeds the V_{ref}. If V_{mem} is below the V_{ref}, the V_{o1} will be set to low (0 V), in contrast, if V_{mem} is beyond the V_{ref}, the V_{o1} will be set to high (8.8 V). In this paper, C_1 is 250 nf, R_1 is 100, V_{ref} is set to 8.8 V and V_{TH} is set to 9 V. The simulation result of V_{mem} and V_{o1} is shown in Fig. 6(b).

In the circuit, the duration of negative and positive parts of V_c are controlled by the V_{mem} and V_{o2} respectively. When the V_{mem} is below the threshold voltage of neuron (V_{TH}), Vc is low (-10 V). As V_{mem} rises gradually and exceeds V_{TH}, V_c will be set to high (10 V). Meanwhile, when V_{mem} exceeds V_{TH}, the pulse generation module will be triggered and generate a pulse. Once the firing event is over, V_c turns to the low state which will induce the circuit operation back to integration. The simulation result of V_c is shown in Fig. 6(a).

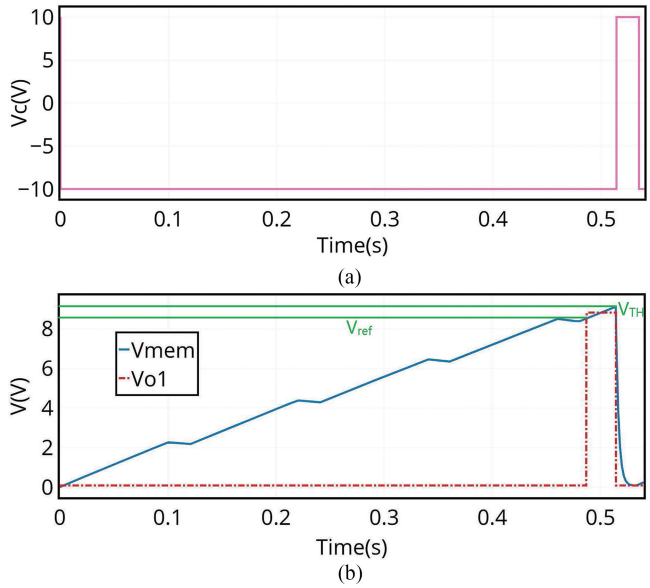

Fig. 6. Simulation result of trigger module. (a) V_c is the control voltage of the trigger module, when V_c is low (-10 V), the circuit stays in the period of integration, when the V_c is high (10 V), the circuit stays in the period of firing. (b) V_{mem} is moving up when the input is negative, once the V_{mem} is equal to the V_{ref}, the V_{o1} will set to high. V_{mem} continues to rise up, when it reaches the threshold voltage of neuron V_{TH}, the circuit will operate in the period of firing.

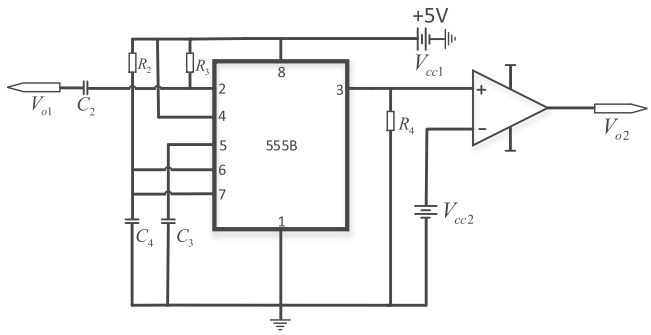

Fig. 7. Schematic diagram of pulse generation module, where R_2 is 20 kΩ, R_3 is 10 kΩ and R_4 is 1 GΩ, C_2 is 1000 pf, C_3 is 0.01 μf, and C_4 is 0.2 μf.

C. The Pulse Generation Module

In our design, we define that the input of neuron is the wide pulse with a low amplitude, and the output of neuron is the narrow pulse with a high amplitude. Considering properties of output pulses, the pulse generation module of the neuron is proposed, which is composed of a 555 timer and a simple comparison circuit (see Fig. 7). The 555 timer is configurated as a monostable flip-flop circuit which has a steady state and a transient state. When the trigger module does not generate a trigger pulse, the circuit remains in the steady state. When the trigger module generates a trigger pulse, the circuit changes from steady state to transient state, and the 555 timer generates a pulse whose width and amplitude are constant. The output pulse width T_W is equal to the duration of the transient state, which can be written as

$$T_W = R_2 C_4 ln\left(\frac{V_{cc}-0}{V_{cc}-2\cdot\frac{V_{cc}}{3}}\right). \tag{8}$$

As for the proposed monostable flip-flop, the amplitude and pulse width of its output will not be affected by the trigger pulse. According to the working principle of 555 timer, C_4 is used to charge and discharge. When the trigger pulse arrives, the power supply V_{cc} charges the capacitor C_4 through R_2, before it rises from 0 V to about 3.33 V, the output of 555 timer stays high, once C_4 charges to 3.33 V, the output of 555 timer is immediately converted to low, then the process of charging and discharging starts again. It is worth to note that the repetition period of the input trigger pulse must be longer than the output pulse width T_W, and the pulse width of the trigger pulse should be less than T_W to ensure that the monostable flip-flop can be

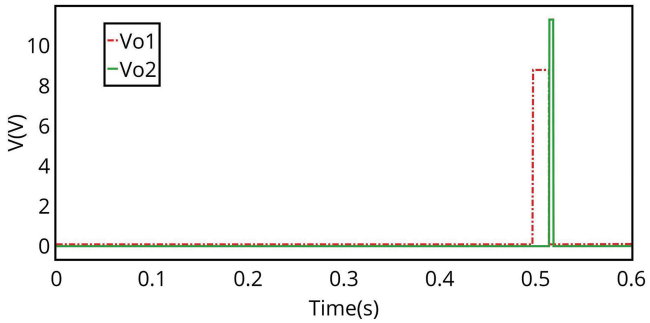

Fig. 8. Simulation result of pulse generation module. The red dashed line represents the input of pulse generation module, and green solid line represents the output pulse V_{o2}.

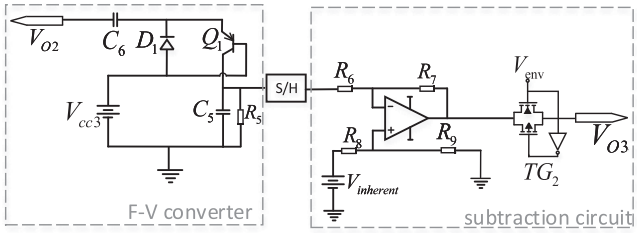

Fig. 9. Schematic diagram of feedback module that consists of frequency to voltage converter, sample and hold circuit, and subtraction circuit. Where C_6 is 0.2 μf, C_5 is 39.6 μf. R_6, R_7, R_8, R_9 are 10 kΩ, 50 kΩ, 10 kΩ and 50 kΩ respectively.

triggered repeatedly. In order to ensure that the output of pulse generation module always has the standard rectangular figure, a simple comparison circuit is designed in the pulse generation module. The simulation results of trigger pulse V_{o1} and the generated pulse V_{o2} are shown in Fig. 8.

D. Feedback Module

Feedback module is the key component of the memristive neuron circuit, and its circuit structure is shown in Fig. 9. The feedback module consists of three parts, which are the frequency to voltage converter, sample and hold circuit and subtraction circuit. The input of the feedback module comes from the output of pulse generation module whose different frequencies can be converted into different output voltages V_{c5} through the f-V converter. Then the converted voltage is applied to the subtraction circuit, where the converted voltage will compare with a fixed voltage $V_{inherent}$ (represents the inherent frequency of neuron). When S_1 and S_2 are set to be closed and S_0 is set to be open, circuit will operate in the period of modification, then the output voltage V_{o3} will be applied to the two terminals of memristor as the feedback and modify its memristance. In addition, the duration of modification is 0.015 s. The work principle of each part of feedback module will be discussed in detail as follows.

1) Frequency-Voltage Converter: A transistor pump frequency discriminator mentioned in [45] is applied for the frequency-voltage converter. The schematic is shown in Fig. 9, where the D_1 becomes the emitter-base diode of a transistor and C_5 is placed in the collector circuit. The frequency-voltage converter depends on the same transfer rate of fixed charge with input signal, which means that the charge transfer rate is directly proportional to the input frequency. To demonstrate more specifically, V_{o2} is the output of pulse generator module. When the V_{o2} is low, the C_6 will charge through D_1, for the diode D_1 turns on under the positive voltage. Because the pulse width of the V_{o2} is far less than the whole cycle of pulse, V_{o2} keeps low for a longer time than that it takes C_6 to fully charge, then the final voltage dropping across C_6 will be $V_{cc3} - V_{D_1}$. Q_1 is not conducted until the V_{o2} goes to high. When the V_{o2} turns to high, V_e will increase to $V_{cc3} - V_{D_1} + V_{o2}$, which is larger than V_b, so Q_1 will be conducted and C_6 will discharge its charge into Q_1 emitter. When Q_1 stays in saturation, the V_{c5} will almost equal to V_e, and the charge stored in C_6 will transfer to C_5, which indicates that V_e will increase. Then the Q_1 can be conducted until V_{eb} reaches the turn-on voltage V_{Q1}. During the duration of discharging C_6, the initial voltage of C_6 is

$$V_{c6,ini} = V_{cc3} - V_{D_1} + V_{o2}, \tag{9}$$

at the end of the discharging, the voltage of C_6 is

$$V_{c6,fin} = V_{cc3} + V_{Q_1}. \tag{10}$$

In the circuit, both of the V_{D_1} and V_{Q_1} are at 0.7 V, according to the relation of charge and voltage, so total charge is quickly stored in C_5

$$Q_{c5} = (V_{c6,ini} - V_{c6,fin}) \cdot C_6, \tag{11}$$

and the voltage of C_5 is

$$V_{c5} = \frac{(V_{c6,ini} - V_{c6,fin}) \cdot C_6}{C_5}. \tag{12}$$

Consequently, C_5 receives the charge Q_{c5} on every cycle and during the cycle discharges into the load R_5. Assuming the duration which V_{o2} stays high is much lower than $C_5 \cdot R_5$, which indicates that almost the whole charge released from C_6 will be stored in C_5 and not lose through R_5. When the voltage increased on the C_5 is the same as that C_5 has released, the output voltage reaches the equilibrium, so the following relationship can be obtained as follows

$$\frac{(V_{c6,ini} - V_{c6,fin}) \cdot C_6}{C_5} = V_{c5} \cdot \exp\left(\frac{-t}{R_5 \cdot C_5}\right). \tag{13}$$

Since the pulse width of the input pulse is much smaller than the pulse period, the turn-off time of Q_1 can be approximated as the whole period of input pulse T. Then the right side of (13) can be extended in series, we can obtain the final relationship between the frequency of input pulse and output voltage V_{c5}, which can be written as

$$V_{c5} = f \cdot C_6 \cdot R_5 \cdot (V_{o2} - V_{D_1} - V_{Q_1}). \tag{14}$$

A special situation is shown in Fig. 10, where the firing frequency equals to the inherent frequency. As for this situation, V_{c5} performs the rising staircase waveform within one second. After one second, the output voltage V_{c5} reaches the equilibrium and is equal to the threshold voltage of memristor V_{th}, 2 V. So the sensibility of neuron membrane will not be changed.

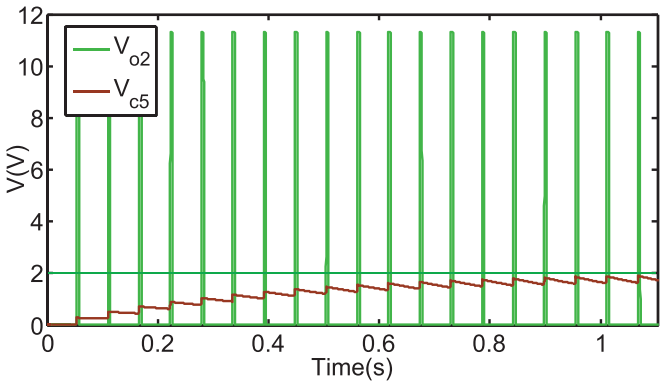

Fig. 10. The simulation result of frequency-voltage converter which the frequency of firing pulse (V_{o2}) is equal to the inherent frequency. The green solid line represents the firing pulse V_{o2}, and the brown solid line represents the voltage V_{c5}, which is converted from the frequency of V_{o2} according to (14).

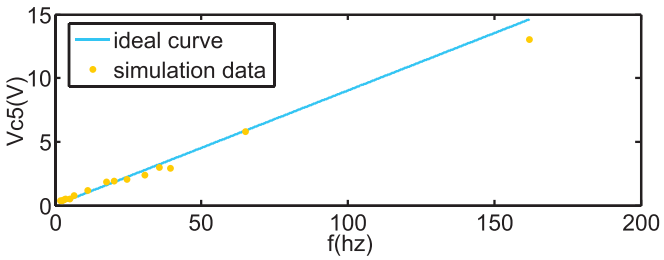

Fig. 11. The relationship of firing frequency and V_{c5}. The cyan line represents the ideal result that reveals the relationship between the firing frequency and output voltage of the converter. The yellow dots represent the simulation data from experimental circuit, whose simulation response is quite linear, as well as the tendency of simulation points and predicted slopes are consistent.

According to (14), the firing frequency of neuron is directly proportional to the output voltage of frequency-voltage converter V_{c5}, and the relation between them is shown in Fig. 11. The simulation results are basically in accordance with the theoretical relation between frequency and voltage. However, there are still errors between the ideal results and experimental results due to the mathematical simplification of (13) and (14) as well as the limitation of simulation accuracy. In order to test the efficacy of the frequency-voltage converter, the normalized mean square error function which was used in [23] is also suitable in this paper.

$$\text{NMSE} = \frac{1}{p}\sum_{i=1}^{p}\left(\frac{V_{ide}^{i} - V_{sim}^{i}}{\delta_i}\right)^2, \tag{15}$$

where V_{ide}^{i}, V_{sim}^{i} and δ_i are theoretical output voltage of f-V converter, measured voltage and the standard error mean of V_{ide}^{i} for a given data point i respectively P is the number of samples. After the simulation of the frequency-voltage converter, NMSE is calculated as 0.1123 which meets the requirement of our design.

2) Sample and Hold Circuit: Before V_{c5} comes to the equilibrium, V_{c5} is the staircase waveform which changes continuously. So V_{c5} should be detected every second when V_{c5} has already reached the equilibrium, then the quantitative relationship between the number of pulse in one second and V_{c5} can be attained. To realize this function, the sample and hold circuit is necessary for feedback module. In this paper, we use the AWBLF398H model configured as the sample and hold circuit, its schematic is shown in Fig. 12.

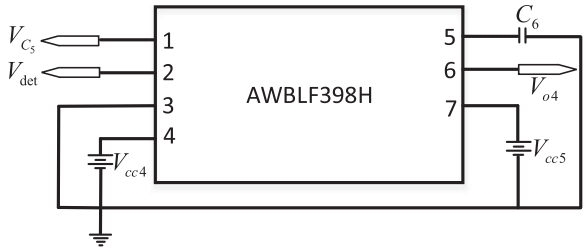

Fig. 12. Schematic diagram of AWBLF398H model, where C_6 is 1.05 μf.

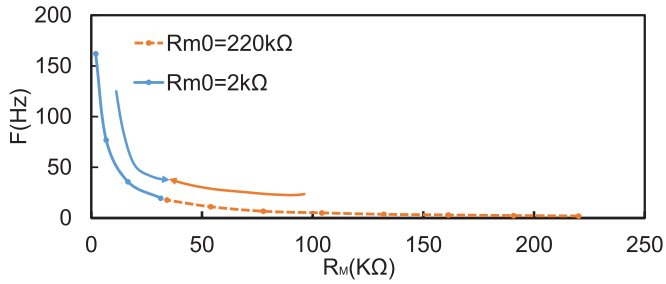

Fig. 13. Relationship between the memristance and firing frequency of the neuron. The blue part shows the negative homeostatic regulation of firing frequency, and the orange part shows the positive homeostatic regulation of firing frequency.

In the model of AWBLF398H, Pin1 receives the input signal which needs to be sampled, Pin2 is the logic pin which determines the detect timing and the duration of holding. In order to ensure that the sampled voltage of V_{c5} has reached the equilibrium, V_{c5} is detected every second and is held until the next detect timing comes. Pin4 and Pin7 are imported positive and negative source respectively, Pin6 outputs the sampled voltage V_{o4}, which equals to V_{c5} in every sample cycle.

3) Subtraction Circuit: Each type of neuron has its inherent firing frequency. If the output frequency of neuron is greater than its inherent firing frequency, the neuron will tune the output frequency within the inherent frequency through homeostatic plasticity and vice versa. In this design, the inherent frequency of the neuron is converted to a voltage $V_{inherent}$ by (14) and subtracts it with the voltage V_{o4} which is sampled and held from V_{c5}. When the S_1 and S_2 are closed, the difference between the two voltages as the feedback will be transmitted to the V_{o3} port of the trigger module, adjusting the memristance. Consequently, the purpose of adaptively controlling the firing frequency is achieved. The subtraction circuit (see Fig. 9) is an amplifier circuit combined with the in-phase input and anti-phase input. By the ideal operational amplification model, as well as the concept of virtual ground and virtual break, the output voltage V_{o3} can be calculated as

$$V_{o3} = \left(1 + \frac{R_7}{R_6}\right)\left(\frac{R_9/R_8}{1 + R_9/R_8}\right)V_{o4} - \left(\frac{R_7}{R_6}\right)V_{inherent}, \tag{16}$$

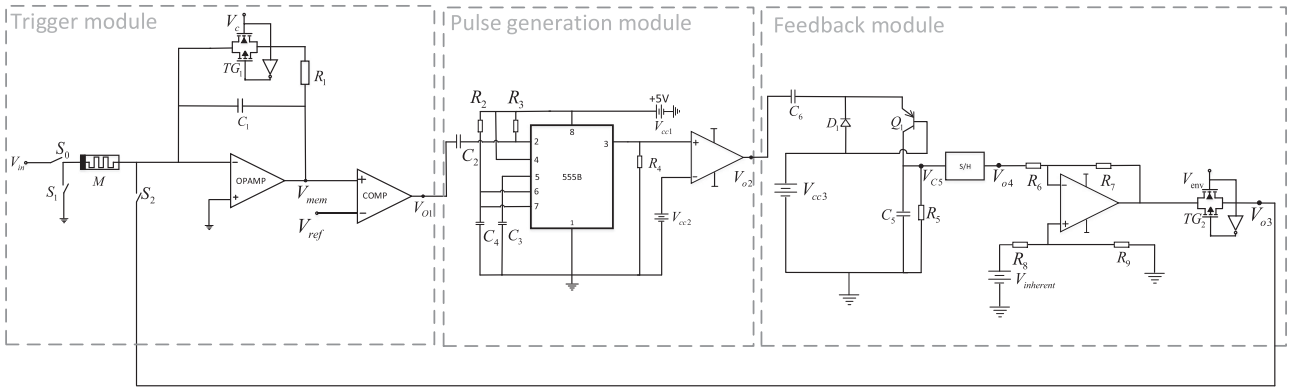

Fig. 14. The overall schematic of neuron circuit. TG_2 is controlled by V_{env} which indicates the external states. If the V_{env} is high, TG_1 will turn on and the neuron circuit can work in preceding three operations. If the V_{env} is low, TG_1 will turn off, which means that S_2 cannot be triggered and V_{o3} cannot be applied to the memristor.

where $V_{inherent}$ is the voltage converted from the inherent frequency of neuron, V_{o4} is the output voltage of the sample and hold circuit, V_{o3} is the output voltage of the feedback module, which is also related to f and t. When $R_7/R_6 = R_9/R_8$, the output voltage V_{o3} of the feedback module can be written as

$$V_{o3} = \frac{R_7}{R_6}\left(V_{inherent} - V_{o4}\right). \tag{17}$$

By substituting (14) into (17), V_{o3} can be written as follows, which is also regarded as the applied voltage V_M in modification period.

$$V_{o3}(f,t) = V_M(f,t) = \begin{cases} \frac{R_7}{R_6}\left[V_{inherent} - f \cdot C_4 \cdot R_5 \cdot (V_{o2} - V_{D_1} - V_{Q_1})\right], \\ \qquad \text{if} \quad t \in [1.1i + \Delta t(i-1), (1.1 + \Delta ti)] \\ 0, \qquad \text{otherwise.} \end{cases} \tag{18}$$

As shown in Fig. 15(b), a complete work period is composed of two parts, one part is the detecting period (t_{det}) and the other is the modifying period (t_{mod}). In this paper, the firing frequency is detected every period, and there is a little interval between detecting timing and modifying timing which can supply enough charging time for C_6 and ensure V_{o4} to reach the sampled voltage. The duration of applying voltage V_{o3} to the memristor is fixed, so the memristance is only related to the amplitude of V_{o3}. According to (18), memristance remains unchanged unless t $\in [1.1i + \Delta t(i-1), (1.1 + \Delta ti))$, in this way, when t $\in [1.1i + \Delta t(i-1), (1.1 + \Delta ti))$, $\dot{r}(V_M)$ can be written as

$$\dot{r}(V_M, t) = \begin{cases} \Delta t \frac{a \cdot (V_M(f) + V_{th})}{c + |V_M(f) + V_{th}|}, & \text{if } f \in (f_1, f_{\max}] \\ 0, & \text{if } f \in [f_2, f_1] \\ \Delta t \frac{a \cdot (V_M(f) - V_{th})}{c + |V_M(f) - V_{th}|}, & \text{if } f \in [f_{\min}, f_2), \end{cases} \tag{19}$$

where, f is a variable which represents the firing rate of neuron, f_1 and f_2 are constants which denote the firing frequencies of neuron when V_{RESET} and V_{SET} are applied to the memristor in the neuron respectively. Based on the definition of the value of memristor mentioned in (3), the memristor value of the ith period can be simplified as

$$R_i(V_M) = f_0 \frac{e^{2L_0\left(1 - \frac{m}{r_0 - (i-1)\cdot\Delta t \cdot \dot{r}(V_M)}\right)}}{L_0\left(1 - \frac{m}{r_0 - (i-1)\cdot\Delta t \cdot \dot{r}(V_M)}\right)}, \tag{20}$$

where i $(i = 1, 2, \ldots, n)$ represents the ith period, r_0 and Δt are constants representing the initial state of memristor and duration of applying V_{o3} to the memristor every period respectively, where Δt is set to 0.015 s. Finally, the relation between the memristance and firing frequency of the neuron can be obtained by substituting (19) into (20). The simulation result is shown in Fig. 13, which is in accordance with the theoretical value. As shown in Fig. 15(a)–(d), if the initial firing frequency is higher than the inherent frequency, the memristance will be increased to regulate the firing frequency, leading it to approach the inherent frequency. If the initial firing frequency is less than the inherent frequency, the memristance will be reduced, then the firing frequency can be stabilized.

IV. Experimental Results

The overall simulation is implemented in the simulation program with integrated circuit emphasis (SPICE). Considering that the biological neuron has its finite range of firing frequency, the acceptable firing frequency of proposed neuron circuit is limited in [1.9 Hz,162 Hz], and its inherent frequency is set to 18 Hz. The overall schematic of neuron circuit is shown in Fig. 14.

A. Two Scenarios of Circuit

In this paper, two different scenarios are considered to verify homeostatic plasticity. In order to test the function of feedback module, V_{env} will stay high to ensure non-zero V_{o3}. Under the first scenario, the initial memristance is 220 kΩ , which can represent a class of initial states that firing frequency is less than the inherent frequency. When the neuron is fired, its firing frequency is 1.9 Hz that is far less than the inherent firing frequency. According to (19) and (20), the rising difference between output firing frequency and the inherent frequency leads to the increase of V_{o3}, which will reduce the intrinsic memristance. Its

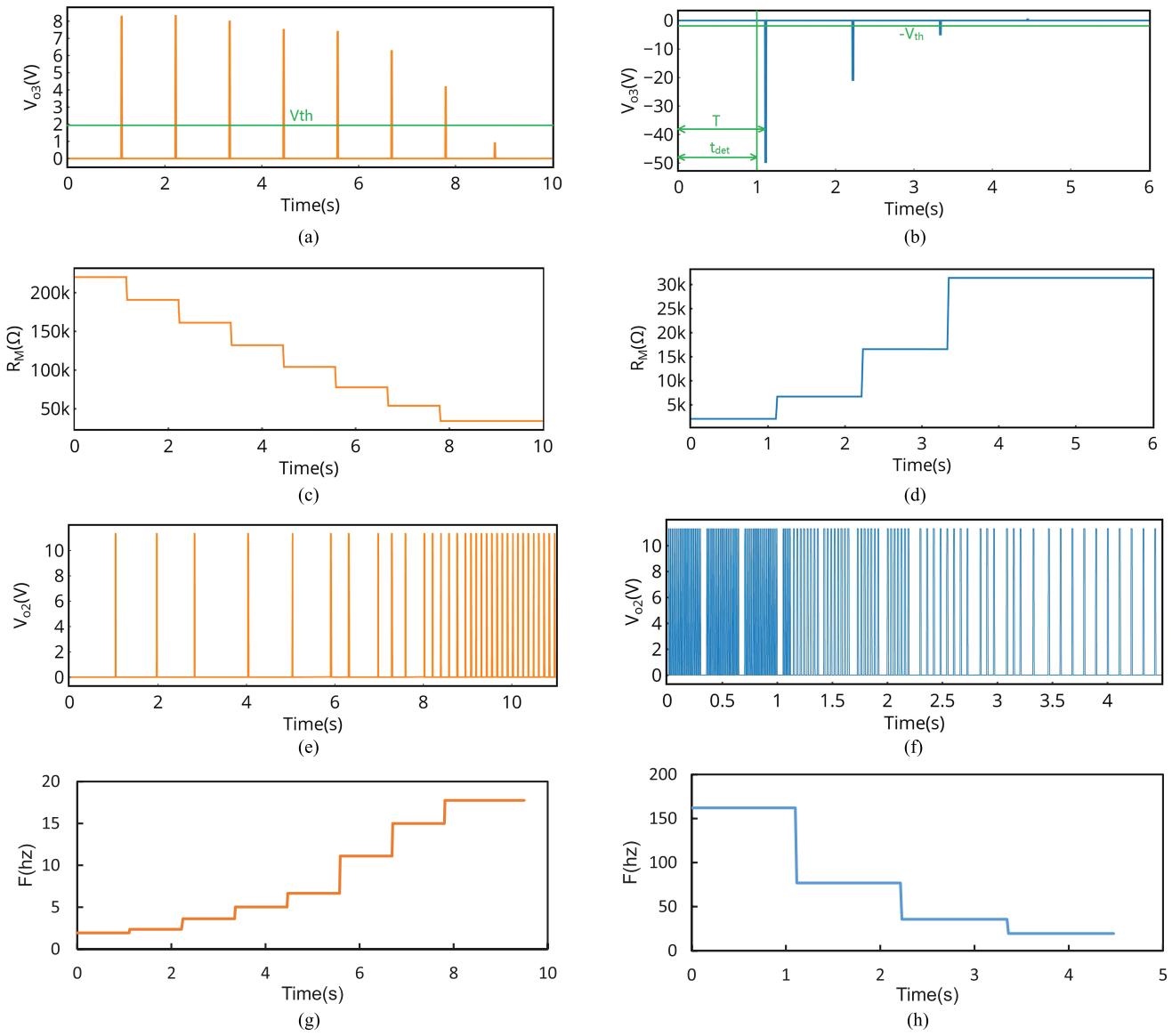

Fig. 15. (a) Simulation result of V_{o3}, the amplitude of V_{o3} is positive under the scenario 1. (b) Simulation result of V_{o3}, the amplitude of V_{o3} is negative under the scenario 2. (c) Under the scenario 1, the memristance of neuron reduces to 34.5 kΩ until firing frequency reaches the inherent frequency. (d) Under the scenario 2, the memristance of neuron increases to 34.5 kΩ until firing frequency reaches the inherent frequency. (e) Simulation result of V_{o2}, under scenario 1. (f) Simulation result of V_{o2}, under scenario 2. (g) and (h) The proposed the neuron successfully emulates the homeostatic regulation, which can regulate the firing frequency to inherent frequency 18 Hz, under scenario 1 shown in (g) and scenario 2 presented in (h).

simulation results are shown in Fig. 15(a). The intrinsic memristance varies from 220 kΩ to 35 kΩ under the different feedback voltages V_{o3}, which is shown in Fig. 15(c). The decrease of intrinsic memristance will consequently contribute to the increment of the firing frequency of neuron, and make it gradually reach the inherent frequency 18 Hz, which indicates that the feedback voltage V_{o3} gradually approaches to the threshold voltage, until V_{o3} is less than or equal to the threshold voltage of memristor V_{th}. The memristance does not reduce anymore and the firing frequency remains stable. During the whole processing of homeostatic regulation under the first scenario, the firing frequency of neuron can be increased from 1.9 Hz to the inherent frequency 18 Hz, the simulation of homeostatic regulation is shown in Fig. 15(e) and (g).

Under the second scenario, the initial memristance is 2 kΩ, which can represent a class of the situations that initial frequency is greater than the inherent firing frequency. When the neuron is fired, the firing frequency reaches the maximum, 162 Hz, which is much larger than the inherent frequency. When the simulation runs in the second scenario, the negative feedback voltage V_{o3} will be applied to the intrinsic memristor and increase its memristance, which indicates that the membrane sensibility of neuron will be weakened, and the firing frequency can be increased. Similar to the first scenario, the difference between the output firing frequency and inherent frequency determines the changing rate of memristance. The simulation result of V_{o3} and memristance variation are shown in Fig. 15(b) and (d) respectively. Due to the regulation of memristance under the

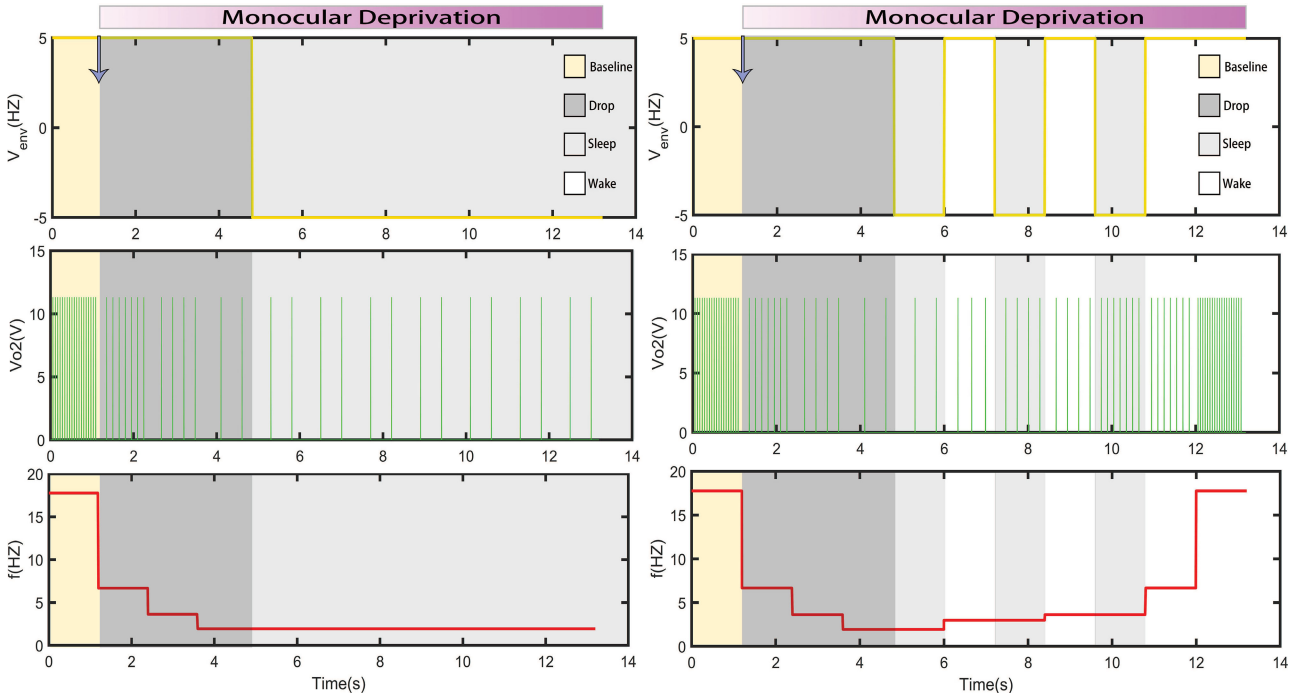

Fig. 16. The simulation results of mimicking the monocular deprivation experiment. The left side represents the results which no waking activity of brain exists in the individual, and the right side represents the results under the waking-condition. The white area represents the period of waking, and the light grey area represents the sleep state. The dark grey area represents the processing of dropping the firing rate, and the yellow area represents that the firing rate stays in the baseline. The upper graph shows the variation of V_{env}, which indicates the wake/sleep states. The mid graph shows the variation of V_{o2}, which is the output of visual cortex neuron. The bottom graph shows the variation of firing rate.

scenario 2, the firing frequency is reduced to inherent frequency, whose simulation result is presented in Fig. 15(f) and (h) respectively. It is worth to note that R_9/R_{10} is set to 5 to prevent the feedback voltage V_{o3} from being trapped in the range of $[-V_{th}, V_{th}]$. If the difference between V_{c5} and $V_{inherent}$ is larger than 0.4 V, the feedback voltage will exceed the threshold voltage of memristor V_{th}, and the intrinsic memristance can be modified. However, if its difference is less than 0.4 V, the memristance will not be changed, which means the firing frequency has already been stable. So the output firing frequency of proposed memristive neuron can be stabilized in 18 Hz with a little fluctuation. According to (14), the fluctuation is ± 3 Hz.

B. Monocular Deprivation Experiment of K. B. Hengen [39]

In order to verify the function of the proposed memristive neuron circuit with homeostatic plasticity, the neuron circuit is applied to simulate the behaviors of the monocular deprivation experiment of K. B. Hengen mentioned in [39]. In the monocular deprivation experiment performed in rodent, firing of visual cortex neuron (V1) is tracked during the induction of homeostatic plasticity. At first, the firing rate of the visual cortex neuron is depressed by the prolonged monocular deprivation, but the firing rate then returns to the inherent rate in spite of the continued monocular deprivation, which indicates that the homeostatic plasticity of neuron can maintain the firing rate around the baseline. The results of the experiment also show that the waking activities of brain can enable the expression of homeostatic plasticity and sleep states can inhibit the expression of homeostatic plasticity.

The proposed memristive neuron circuit is aimed to emulate the firing behaviors of visual cortex neuron in the monocular deprivation experiment. As shown in Fig. 14, V_{env} represents whether the individual is waking. If V_{env} is 5 V, it represents that the individual is waking, however, if V_{env} is -5 V, it represents that the individual is sleeping. Furthermore, due to the limitation of simulation time, we set one day in the experiment performed in rodent as 1.2 seconds in the circuit simulation. Fig. 16 shows the simulation results of the circuit, where the left side and right side show the simulation results of no waking-condition and waking-condition after the monocular deprivation respectively. To emulate the experiment performed in rodent, a similar role of the monocular deprivation structure is carried on the neuron circuit, which is to reduce the amplitude of input voltage of neuron circuit. Therefore, the firing rate can be dropped from 18 Hz to 1.93 Hz during 1.2 s to 4.8 s. The simulations are divided into two parts, which aim to mimic firing behaviors with waking states and without waking states respectively. The left side of Fig. 16 is the result of simulating the firing behaviors without waking states in the individual with monocular deprivation. In order to emulate the sleeping time in the biological experiment, the three sleeping periods are set as 4.8 s to 6 s, 7.2 s to 8.4 s and 9.6 s to 10.8 s respectively. In these three sleeping periods, V_{evn} stays low (-5 V) and the feedback path of the neuron circuit is cut off. As a result, the firing rate of neuron circuit cannot be changed and cannot return to the baseline, which indicates that

TABLE II
DEFINITIONS OF EXPERIMENT TERMS AND CIRCUIT STATES

Experiment Condition	Rodent Experiment	Circuit Simulation
Waking	REM	V_{env} =5V
Sleeping	Non-REM	V_{env} =-5V
Monocular deprivation	Visual Deprivation	V_{in} =-0.1V
Non-monocular deprivation	Without Deprivation	V_{in} =-1.5V
Time	One Day	1.2s

the homeostatic plasticity is inhibited during sleeping period. In the monocular deprivation experiment of K. B. Hengen in [39], eye movement of rodent is considered as the standard to differentiate the wake and sleeping states. In the sleeping conditions, the rodent performs rapid eye movement (REM), while the rodent would perform slow-wave (non-REM) of eye movement if the rodent keeps awake. Specific definitions of neuroscience terms and corresponding circuit states are shown in Table II in the paper.

The simulation results of mimicking firing behaviors with waking states are shown in the right side of Fig. 16. There are also three waking periods in the circuit simulation to mimic the waking time of rodent, which are 6 s to 7.2 s, 8.4 s to 9.6 s and 10.8 s to 13.2 s. During these waking periods, V_{evn} stays high (5V) and the expression of homeostatic plasticity can be induced. In the first waking period, the firing rate of visual cortex neuron is promoted from 1.93 Hz to 2.98 Hz. In the second waking period, the firing rate is increased from 2.98 Hz to 3.63 Hz. Finally, the firing rate returns to the baseline 18 Hz in the last waking period. In a conclusion, the circuit simulation results show that the proposed neuron circuit can realize similar firing behaviors of visual cortex neuron in the monocular deprivation experiment. And the homeostatic plasticity of proposed neuron circuit can be promoted by waking states and inhibited by sleeping states, which is in accordance with the results in [39].

C. Circuit Performance Analysis

There are three modules in the neuron circuit, where the pulse generation module can be substituted according to various requirements of researches. Therefore, the pulse generation module will not be fabricated in neuron chip implementation. There has been a method to fabricate the integrated circuit into a compatible platform mentioned in [46], which is written as

$$AREA_{MOS} = 3(W/l + 1)f^2 \tag{21}$$

$$AREA_{MEM} = 4f^2, \tag{22}$$

where $AREA_{MOS}$ and $AREA_{MEM}$ denote the area of single transistor and memristor respectively. W and l are the parameters of the transistor; f denotes the half-pitch (the half of the minimum distance between two metal wires). Based on the above estimation methods in [47] and [48], the trigger module (one memristor, two CMOS OpAmps, one CMOS transmission gate, one inverter, one capacitor, one resistor and three switches) approximately occupies 191.2 μm^2 in a 0.35 μm CMOS process. As for the feedback module (two capacitors, one transistor, five resistors, one sample and hold circuit, one CMOS transmission gate and one CMOS OpAmp), it approximately occupies 810.2 μm^2 in a 0.35 μm CMOS process. Therefore, the total on-chip area of proposed neuron circuit is 1001.4 μm^2. The area comparison of each module is shown in Table III.

TABLE III
POWER CONSUMPTION AND AREA

Module Function	Trigger	Pulse generation	Feedback
Power Consumption(μJ)	0.383	0.24	2.45
Area (μm^2)	191.2	*	810.2

TABLE IV
COMPARISON OF THE PROPOSED NEURON CIRCUIT AND OTHER NEURON MODELS

Neuron model	Power(μw)	Approximate area(μm^2)
Spiking and bursting [50]	40	2800
Hindmarsh-Rose [51]	163.4	1114
Conductance-based [52]	23.3	1013
Proposed circuit	76.6	1001.4

According to [49], the power consumption of one operation can be calculated by

$$P = \int_0^T V(t) \cdot I(t)dt. \tag{23}$$

Based on (23), the power consumption of each separate module can be calculated by the difference between input power P_{in} and output power P_{out}. In this paper, the highest current is less than 16.73 mA while most of current in the circuit is in picoampere-level because of the high impedance. As a result, the power consumption of each separated module is shown in Table III.

Table IV shows the comparison of the proposed neuron circuit and other neuron models. Compared with other neuron model, the power consumption and circuit area of the proposed neuron are at the average level of these four models. However, the proposed neuron circuit can emulate the homeostatic plasticity of biological neurons efficiently.

All the electronic elements in the circuit simulation are easily accessible. Especially, there has been commercial physical memristor [53], which exhibits similar behaviors with this model such as nonlinearity and threshold switching. In terms of power and area, the on-chip neuron circuit is feasible to implement. In addition, the proposed neuron circuit is tolerable for the external errors such as temperature, parameter variations and input noises. Therefore, there will be huge potential to applying the proposed neuron circuit to the further applications. Similar with the conventional integrate and fire model, the trigger module of proposed neuron circuit exhibits quick response to input stimuli, simple circuit structure. However, distinguishing from the conventional integrate and fire model, the resistor in the conventional integrate and fire model is substituted by a memristor in the proposed neuron circuit. Combined with the operation of feedback module, the memristance can be changed hence the time constant τ of integrate and fire model would be regulated. Furthermore, the amplitude of feedback signal is related to the differences between firing rate and the inherent firing rate of

neuron. As a result, the homeostatic plasticity can be realized by the proposed neuron circuit.

V. Conclusion

The aforementioned sections demonstrate the homeostatic regulation and memristive neuron circuit to emulate the homeostatic plasticity. Compared with other existing neuron circuits, the proposed memristive neuron circuit, which comprises of three modules, the trigger module, pulse generation module and feedback module, completely shows the capacity of realizing the intrinsic homeostatic plasticity of neuron that can adaptively adjust firing frequency within the inherent range. Specially, the memristor is applied to the neuron circuit and its memristance can represent the membrane sensibility of neuron. Then the quantitative relation between the intrinsic memristance and output firing frequency is given. The simulations under the two different scenarios are realized to verify the feasibility of the memristive neuron with homeostatic plasticity. Moreover, the proposed memristor-based neuron circuit is applied to emulate the firing behaviors of visual cortex neuron in the monocular deprivation experiments, and the simulation results show the accordance with biological experiment, which indicates our design has more biomimetic characteristics.

The proposed design could be the groundwork for future circuits that can combine the synaptic homeostatic plasticity to implement the full-function homeostatic plasticity efficiently in terms of area and power. In addition, considering the importance of homeostasis-type rules in neuromorphic computing, future research can utilize memristive synapses with proposed memristive neuron to realize more complex applications such as pattern recognition and extraction of visual features.

References

[1] C. S. Goodman and C. J. Shatz, "Developmental mechanisms that generate precise patterns of neuronal connectivity," *Cell*, vol. 72, no. 1001, pp. 77–98, 1993.

[2] D. W. Munno and N. I. Syed, "Synaptogenesis in the CNS: An odyssey from wiring together to firing together," *J. Physiol.*, vol. 552, no. 1, pp. 1–11, 2003.

[3] M. A. Corner, R. E. Baker, and P. J. Van, "Homeostatically regulated spontaneous neuronal discharges protect developing cerebral cortex networks from becoming hyperactive following prolonged blockade of excitatory synaptic receptors," *Brain Res.*, vol. 1106, no. 1, pp. 40–45, 2006.

[4] C. D. Schuman *et al.*, "A survey of neuromorphic computing and neural networks in hardware," arXiv:1705.06963, 2017.

[5] J. M. Cruz-Albrecht, M. W. Yung, and N. Srinivasa, "Energy-efficient neuron, synapse and STDP integrated circuits," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 3, pp. 246–256, Jun. 2012.

[6] A. Bofillipetit and A. F. Murray, "Synchrony detection and amplification by silicon neurons with STDP synapses," *IEEE Trans. Neural Netw.*, vol. 15, no. 5, pp. 1296–304, Sep. 2004.

[7] J. Schemmel, A. Grubl, K. Meier, and E. Mueller, "Implementing synaptic plasticity in a VLSI spiking neural network model," in *Proc. Int. Joint Conf. Neural Netw.*, 2006, pp. 1–6.

[8] H. K. Riis and P. Hafliger, "Spike based learning with weak multi-level static memory," in *Proc. Int. Symp. Circuits Syst.*, 2004, pp. 393–396.

[9] E. M. Izhikevich, "Simple model of spiking neurons," *IEEE Trans. Neural Netw.*, vol. 14, no. 6, pp. 1569–1572, Nov. 2003.

[10] Y. Theodore and C. Gert, "Analog VLSI biophysical neurons and synapses with programmable membrane channel kinetics," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 139–148, Jun. 2010.

[11] C. S. Thakur, R. Wang, T. J. Hamilton, J. Tapson, and A. van Schaik, "A low power trainable neuromorphic integrated circuit that is tolerant to device mismatch," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 2, pp. 211–221, Feb. 2016.

[12] S. C. Liu and B. A. Minch, "Silicon synaptic adaptation mechanisms for homeostasis and contrast gain control," *IEEE Trans. Neural Netw.*, vol. 13, no. 6, pp. 1497–1503, Nov. 2002.

[13] C. Bartolozzi, O. Nikolayeva, and G. Indiveri, "Implementing homeostatic plasticity in VLSI networks of spiking neurons," in *Proc. Int. Conf. Electron. Circuits Syst.*, 2008, pp. 682–685.

[14] L. O. Chua, "Memristor-the missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, Sep. 1971.

[15] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[16] X. Wang, Y. Chen, H. Xi, H. Li, and D. Dimitrov, "Spintronic memristor through spin-torque-induced magnetization motion," *IEEE Electron. Device Lett.*, vol. 30, no. 3, pp. 294–297, Mar. 2009.

[17] A. C. Torrezan, J. P. Strachan, G. Medeirosribeiro, and R. S. Williams, "Sub-nanosecond switching of a tantalum oxide memristor," *Nanotechnology*, vol. 22, no. 48, 2011, Art. no. 485203.

[18] A. Chanthbouala *et al.*, "A ferroelectric memristor," *Nature Mater*, vol. 11, no. 10, pp. 860–864, 2012.

[19] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," *Nature Nanotechnol.*, vol. 8, no. 1, pp. 13–24, 2013.

[20] M. Prezioso, F. M. Bayat, B. Hoskins, K. Likharev, and D. Strukov, "Self-adaptive spike-time-dependent plasticity of metal-oxide memristors," *Sci. Rep.*, vol. 6, 2016, Art. no. 21331.

[21] Y. Zhang, Z. Zeng, and S. Wen, "Implementation of memristive neural networks with spike-rate-dependent plasticity synapses," in *Proc. Int. Joint Conf. Neural Netw.*, 2014, pp. 2226–2233.

[22] W. Cai, F. Ellinger, and R. Tetzlaff, "Neuronal synapse as a memristor: Modeling pair- and triplet-based STDP rule," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 1, pp. 87–95, Feb. 2015.

[23] M. R. Azghadi, B. Linares-Barranco, D. Abbott, and P. H. W. Leong, "A hybrid CMOS-memristor neuromorphic synapse," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 2, pp. 434–445, Apr. 2017.

[24] X. Liu, Z. Zeng, and S. Wen, "Implementation of memristive neural network with full-function Pavlov associative memory," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1454–1463, Sep. 2016.

[25] M. Hu, Y. Chen, J. J. Yang, Y. Wang, and H. H. Li, "A compact memristor-based dynamic synapse for spiking neural networks," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 36, no. 8, pp. 1353–1366, Aug. 2017.

[26] N. Ge *et al.*, "An efficient analog hamming distance comparator realized with a unipolar memristor array: A showcase of physical computing," *Sci. Rep.*, vol. 7, 2017, Art. no. 40135.

[27] Y. Zhang, X. Wang, and E. G. Friedman, "Memristor-based circuit design for multilayer neural networks," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 2, pp. 677–686, Feb. 2018.

[28] M. Hu, H. Li, Y. Chen, Q. Wu, G. S. Rose, and R. W. Linderman, "Memristor crossbar-based neuromorphic computing system: A case study," *IEEE Trans. Neural Netw. Learn. Syst.*, vol. 25, no. 10, pp. 1864–1878, Oct. 2014.

[29] S. Yu, "Orientation classification by a winner-take-all network with oxide RRAM based synaptic devices," in *Proc. Int. Symp. Circuits Syst.*, 2014, pp. 1058–1061.

[30] I. E. Ebong and P. Mazumder, "CMOS and memristor-based neural network design for position detection," *Proc. IEEE*, vol. 100, no. 6, pp. 2050–2060, Jun. 2012.

[31] C. Yakopcic, M. Z. Alom, and T. M. Taha, "Memristor crossbar deep network implementation based on a convolutional neural network," in *Proc. Int. Joint Conf. Neural Netw.*, 2016, pp. 963–970.

[32] A. Shafiee *et al.*, "ISAAC: A convolutional neural network accelerator with in-situ analog arithmetic in crossbars," in *Proc. Int. Symp. Comput. Archit.*, 2016, pp. 14–26.

[33] G. W. Burr *et al.*, "Neuromorphic computing using non-volatile memory," *Adv. Phys., X*, vol. 2, no. 1, pp. 89–124, 2016.

[34] C. D. Wright, Y. Liu, K. I. Kohary, M. M. Aziz, and R. J. Hicken, "Arithmetic and biologically-inspired computing using phase-change materials," *Adv. Mater.*, vol. 23, no. 30, pp. 3408–3413, 2011.

[35] T. Tuma, A. Pantazi, M. L. Gallo, A. Sebastian, and E. Eleftheriou, "Stochastic phase-change neurons," *Nature Nanotechnol.*, vol. 11, no. 8, pp. 693–699, 2016.

[36] M. Al-Shedivat, R. Naous, G. Cauwenberghs, and K. N. Salama, "Memristors empower spiking neurons with stochasticity," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 5, no. 2, pp. 242–253, Jun. 2015.
[37] D. Querlioz, O. Bichler, and C. Gamrat, "Simulation of a memristor-based spiking neural network immune to device variations," in *Proc. Int. Joint Conf. Neural Netw.*, 2011, pp. 1775–1781.
[38] M. Hansen, F. Zahari, M. Ziegler, and H. Kohlstedt, "Double-barrier memristive devices for unsupervised learning and pattern recognition," *Frontiers Neuroscience*, vol. 11, pp. 2045–2322, 2017.
[39] K. B. Hengen, P. A. Torrado, J. N. Mcgregor, S. D. Van Hooser, and G. G. Turrigiano, "Neuronal firing rate homeostasis is inhibited by sleep and promoted by wake," *Cell*, vol. 165, no. 1, pp. 180–191, 2016.
[40] G. G. Turrigiano and S. B. Nelson, "Hebb and homeostasis in neuronal plasticity," *Current Opinion Neurobiology*, vol. 10, no. 3, pp. 358–364, 2000.
[41] G. G. Turrigiano, "Homeostatic plasticity in neuronal networks: the more things change, the more they stay the same," *Trends Neuroscience*, vol. 22, no. 5, pp. 221–227, 1999.
[42] G. G. Turrigiano and S. B. Nelson, "Homeostatic plasticity in the developing nervous system," *Nature Rev. Neuroscience*, vol. 5, no. 2, pp. 97–108, 2004.
[43] I. Vourkas, A. Batsos, and G. C. Sirakoulis, "Spice modeling of nonlinear memristive behavior," *Int. J. Circuit Theory Appl.*, vol. 43, no. 5, pp. 553–565, 2015.
[44] R. Brette *et al.*, "Simulation of networks of spiking neurons: A review of tools and strategies," *J. Comput. Neuroscience*, vol. 23, no. 3, pp. 349–398, 2007.
[45] T. K. Hemingway, *Electronic Designer's Handbook: A Practical Guide to Transistor Circuit Design*. London, U.K.: Business Publication, 1970.
[46] M. Dong and L. Zhong, "Nanowire crossbar logic and standard cell-based integration," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 8, pp. 997–1007, Aug. 2009.
[47] I. Vourkas and G. C. Sirakoulis, "A novel design and modeling paradigm for memristor-based crossbar circuits," *IEEE Trans. Nanotechnol.*, vol. 11, no. 6, pp. 1151–1159, Nov. 2012.
[48] L. Xia *et al.*, "MNSIM: Simulation platform for memristor-based neuromorphic computing system," in *Proc. Des., Automat. Test Eur. Conf. Exhib.*, 2017, pp. 469–474.
[49] C. Wu, T. W. Kim, H. Y. Choi, D. B. Strukov, and J. J. Yang, "Flexible three-dimensional artificial synapse networks with correlated learning and trainable memory capability," *Nature Commun.*, vol. 8, no. 1, 2017, Art. no. 752.
[50] J. H. Wijekoon and P. Dudek, "Compact silicon neuron circuit with spiking and bursting behaviour," *Neural Netw.*, vol. 21, no. 2/3, pp. 524–534, 2008.
[51] Y. J. Lee, J. Lee, Y. B. Kim, and J. Ayers, "Low power real time electronic neuron VLSI design using subthreshold technique," in *Proc. Int. Symp. Circuits Syst.*, 2004, pp. 744–747.
[52] P. Livi and G. Indiveri, "A current-mode conductance-based silicon neuron for address-event neuromorphic systems," in *Proc. Int. Symp. Circuits Syst.*, 2009, pp. 2898–2901.
[53] "Bio inspired technologies," 2015. [Online]. Available: http://www.bioinspired.net/documents.html. Accessed on: Sep. 20, 2017.

Xinming Shi received the B.S. degree from the College of Electrical Engineering, Wuhan University of Technology, Wuhan, China, in 2016. She is currently working toward the M.S. degree at the School of Automation, Huazhong University of Science and Technology, Wuhan, China. Her research focuses on memristor-based artificial neural network circuits.

Zhigang Zeng received the Ph.D. degree in systems analysis and integration from the Huazhong University of Science and Technology, Wuhan, China, in 2003. He is currently a Professor with the School of Automation, Huazhong University of Science and Technology, and also with the Key Laboratory of Image Processing and Intelligent Control of the Education Ministry of China, Wuhan, China. He has authored/coauthored more than 100 international journal papers. His current research interests include theory of functional differential equations and differential equations with discontinuous right-hand sides, and their applications to dynamics of neural networks, memristive systems, and control systems. He has been a member of the Editorial Board of Cognitive Computation (since 2010), the Editorial Board of Neural Networks (since 2012), and the Editorial Board of Applied Soft Computing (since 2013). He has been an Associate Editor for the IEEE TRANSACTIONS ON CYBERNETICS (since 2014), and the IEEE TRANSACTIONS ON FUZZY SYSTEMS (since 2016). From 2010 to 2011, he was an Associate Editor for the IEEE TRANSACTIONS ON NEURAL NETWORKS.

Le Yang received the M.S. degree from the College of Engineering, Huazhong Agricultural University, Wuhan, China, in 2014. He is currently working toward the D.S. degree at the School of Automation, Huazhong University of Science and Technology, Wuhan, China. His research focuses on memristor-based artificial neural networks.

Yi Huang received the B.S. degree from the School of Automation, Huazhong University of Science and Technology, Wuhan, China, in 2016. He is currently working toward the M.S. degree at the School of Automation, Huazhong University of Science and Technology, Wuhan, China. His research focuses on memristor-based artificial neural network circuits.